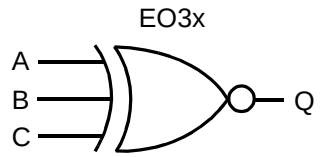
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

EO3x is a family of 3-input gates which perform the logical exclusive OR (XOR) function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H

HDL Syntax

Verilog ..... EO3x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: EO3x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads				
	EO31	EO32	EO33	EO34	EO36
A	2.1	2.1	2.1	2.1	2.1
B	2.1	2.1	2.1	2.1	2.1
C	2.1	3.4	3.2	3.2	3.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
EO31	5.0	TBD	10.6
EO32	8.0	TBD	15.2
EO33	8.0	TBD	16.9
EO34	10.0	TBD	19.7
EO36	10.0	TBD	22.4

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

EO31	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.76 0.62	0.81 0.69	0.97 0.86	1.12 1.01	1.23 1.10
EO32	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.85 0.74	0.92 0.81	1.02 0.92	1.13 1.04	1.21 1.13
EO33	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.80 1.00	0.93 1.14	1.03 1.25	1.12 1.35	1.22 1.46
EO34	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.88 1.02	0.97 1.19	1.07 1.30	1.17 1.39	1.27 1.47
EO36	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.96 1.07	1.07 1.21	1.16 1.33	1.24 1.43	1.33 1.54

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Logic Schematic