Section I. Stratix Device Family Data Sheet

This section provides designers with the data sheet specifications for Stratix devices. They contain feature definitions of the internal architecture, configuration and JTAG boundary-scan testing information, DC operating conditions, AC timing parameters, a reference to power consumption, and ordering information for Stratix devices.

This section contains the following chapters:

- Chapter 1. Introduction
- Chapter 2. Stratix Architecture
- Chapter 3. Configuration & Testing
- Chapter 4. DC & Switching Characteristics
- Chapter 5. Reference & Ordering Information

Revision History

The table below shows the revision history for Chapter 1 through Chapter 5.

Chapter	Date/Version	Changes Made
1	September 2004, v3.1	Updated Table 1–6 on page 1–5.
	April 2004, v3.0	Main section page numbers changed on first page. Changed PCI-X to PCI-X 1.0 in “Features” on page 1–2. Global change from SignalTap to SignalTap II. The DSP blocks in “Features” on page 1–2 provide dedicated implementation of multipliers that are now “faster than 300 MHz.”
	January 2004, v2.2	Updated -5 speed grade device information in Table 1-6.
	October 2003, v2.1	Add -8 speed grade device information.
	July 2003, v2.0	Format changes throughout chapter.

Chapter	Date/Version	Changes Made
2	September 2004, v3.1	● Updated fast regional clock networks description on page 2–71. ● Deleted the word preliminary from the “specification for the maximum time to relock is 100 µs” on page 2–88. ● Added information about differential SSTL and HSTL outputs in “External Clock Outputs” on page 2–90. ● Updated notes in Figure 2–55 on page 2–91. ● Added information about *m* counter to “Clock Multiplication & Division” on page 2–99. ● Updated Note 1 in Table 2–58 on page 2–99. ● Updated description of “Clock Multiplication & Division” on page 2–86. ● Updated Table 2–22 on page 2–100. ● Added references to AN 349 and AN 329 to “External RAM Interfacing” on page 2–113. ● Table 2–25 on page 2–114: updated the table, updated Notes 3 and 4. Notes 4, 5, and 6, are now Notes 5, 6, and 7, respectively. ● Updated Table 2–26 on page 2–115. ● Added information about PCI Compliance to page 2–118. ● Table 2–32 on page 2–124: updated the table and deleted Note 1. ● Updated reference to device pin-outs now being available on the web on page 2–128. ● Added Notes 4 and 5 to Table 2–36 on page 2–128. ● Updated Note 3 in Table 2–37 on page 2–129. ● Updated Note 5 in Table 2–41 on page 2–134.
	April 2004, v3.0	● Added note 3 to rows 11 and 12 in Table 2–18. ● Deleted “Stratix and Stratix GX Device PLL Availability” table. ● Added I/O standards row in Table 2–28 that support max and min strength. ● Row `clk [1,3,8,10]` was removed from Table 2–30. ● Added checkmarks in Enhanced column for LVPECL, 3.3-V PCML, LVDS, and HyperTransport technology rows in Table 2–32. ● Removed the Left and Right I/O Banks row in Table 2–34. ● Changed `RCLK` values in Figures 2–50 and 2–51. ● External RAM Interfacing section replaced.
	November 2003, v2.2	● Added 672-pin BGA package information in Table 2–37. ● Removed support for series and parallel on-chip termination. ● Termination Technology renamed differential on-chip termination. ● Updated the number of channels per PLL in Tables 2-38 through 2-42. ● Updated Figures 2–65 and 2–67.
	October 2003, v2.1	● Updated DDR I information. ● Updated Table 2–22. ● Added Tables 2–25, 2–29, 2–30, and 2–72. ● Updated Figures 2–59, 2–65, and 2–67. ● Updated the Lock Detect section.

Chapter	Date/Version	Changes Made
2	July 2003, v2.0	- Added reference on page 2-73 to Figures 2-50 and 2-51 for `RCLK` connections. - Updated ranges for EPLL post-scale and pre-scale dividers on page 2-85. - Updated PLL Reconfiguration frequency from 25 to 22 MHz on page 2-87. - New requirement to assert are set signal each PLL when it has to re-acquire lock on either a new clock after loss of lock (page 2-96). - Updated max input frequency for `CLK[1,3,8,10]` from 462 to 500, Table 2-24. - Renamed impedance matching to series termination throughout. - Updated naming convention for DQS pins on page 2-112 to match pin tables. - Added DDR SDRAM Performance Specification on page 2-117. - Added external reference resistor values for terminator technology (page 2-136). - Added Terminator Technology Specification on pages 2-137 and 2-138. - Updated Tables 2-45 to 2-49 to reflect PLL cross-bank support for high speed differential channels at full speed. - Wire bond package performance specification for “high” speed channels was increased to 624 Mbps from 462 Mbps throughout chapter.
3	September 2004, v1.1	- Added new section, “Stratix Automated Single Event Upset (SEU) Detection” on page 3–12. - Updated description of “Custom-Built Circuitry” on page 3–13.
	April 2003, v1.0	- No new changes in *Stratix Device Handbook* v2.0.
4	September 2004, v3.1	- Updated Note 3 in Table 4–8 on page 4–4. - Updated Table 4–10 on page 4–6. - Updated Table 4–20 on page 4–11 through Table 4–23 on page 4–12. Added rows $V_{IL(AC)}$ and $V_{IH(AC)}$ to each table. - Updated Table 4–26 on page 4–13 through Table 4–29 on page 4–14. - Updated Table 4–31 on page 4–15. - Updated description of “External Timing Parameters” on page 4–32. - Updated Table 4–36 on page 4–19. - Added signals t_{OUTCO}, T_{XZ}, and T_{ZX} to Figure 4–4 on page 4–32. - Added rows $t_{M512CLKENSU}$ and $t_{M512CLKENH}$ to Table 4–40 on page 4–23. - Added rows $t_{M4CLKENSU}$ and $t_{M4CLKENH}$ to Table 4–41 on page 4–23. - Updated Note 2 in Table 4–54 on page 4–34. - Added rows $t_{MRAMCLKENSU}$ and $t_{MRAMCLKENH}$ to Table 4–42 on page 4–24. - Updated Table 4–46 on page 4–28. - Updated Table 4–47 on page 4–28.

Chapter	Date/Version	Changes Made
4		● Table 4–48 on page 4–29: added rows $t_{M512CLKSENSU}$ and $t_{M512CLKENH}$, and updated symbol names. ● Updated power-up current (ICCINT) required to power a Stratix device on page 4–16. ● Updated Table 4–37 on page 4–21 through Table 4–43 on page 4–26. ● Table 4–49 on page 4–30: added rows $t_{M4KCLKENSU}$, $t_{M4KCLKENH}$, $t_{M4KBESU}$, and $t_{M4KBEH,}$ deleted rows $t_{M4KRADDRASU}$ and $t_{M4KRADDRH}$, and updated symbol names. ● Table 4–50 on page 4–30: added rows $t_{MRAMCLKENSU}$, $t_{MRAMCLKENH}$, $t_{MRAMBESU}$, and $t_{MRAMBEH}$, deleted rows $t_{MRAMADDRASU}$ and $t_{MRAMRADDRH}$, and updated symbol names. ● Table 4–52 on page 4–33: updated table, deleted “Conditions” column, and added rows t_{XZ} and t_{ZX}. ● Table 4–52 on page 4–33: updated table, deleted “Conditions” column, and added rows t_{XZ} and t_{ZX}. ● Table 4–53 on page 4–33: updated table and added rows t_{XZPLL} and t_{ZXPLL}. ● Updated Note 2 in Table 4–53 on page 4–33. ● Table 4–54 on page 4–34: updated table, deleted “Conditions” column, and added rows t_{XZPLL} and t_{ZXPLL}. ● Updated Note 2 in Table 4–54 on page 4–34. ● Deleted Note 2 from Table 4–55 on page 4–35 through Table 4–66 on page 4–40. ● Updated Table 4–55 on page 4–35 through Table 4–96 on page 4–55. Added rows T_{XZ}, T_{ZX}, T_{XZPLL}, and $T_{ZXPLL.}$ ● Added Note 4 to Table 4–101 on page 4–61. ● Deleted Note 1 from Table 4–67 on page 4–41 through Table 4–84 on page 4–49. ● Added new section “I/O Timing Measurement Methodology” on page 4–59. ● Deleted Note 1 from Table 4–67 on page 4–41 through Table 4–84 on page 4–49. ● Deleted Note 2 from Table 4–85 on page 4–50 through Table 4–96 on page 4–55. ● Added Note 4 to Table 4–101 on page 4–61. ● Table 4–102 on page 4–63: updated table and added Note 4. ● Updated description of “External I/O Delay Parameters” on page 4–65. ● Added Note 1 to Table 4–109 on page 4–74 and Table 4–110 on page 4–75. ● Updated Table 4–103 on page 4–65 through Table 4–110 on page 4–75. ● Deleted Note 2 from Table 4–103 on page 4–65 through Table 4–106 on page 4–69. ● Added new paragraph about output adder delays on page 4–66. ● Updated Table 4–110 on page 4–75. ● Added Note 1 to Table 4–111 through Table 4–113 on page 4–77.

Chapter	Date/Version	Changes Made
4		● Updated Table 4–123 on page 4–87 through Table 4–126 on page 4–94. ● Updated Note 3 in Table 4–123 on page 4–87. ● Table 4–125 on page 4–90: moved to correct order in chapter, and updated table. ● Updated Table 4–126 on page 4–94. ● Updated Table 4–127 on page 4–96. ● Updated Table 4–128 on page 4–97.
	April 2004, v3.0	● Table 4–129 on page 4–98: updated table and added Note 10. ● Updated Table 4–130 and Table 4–131 on page 4–100. ● Updated Table 4–110 on page 4–75. ● Updated Table 4–123 on page 4–87. ● Updated Table 4–124 on page 4–89. through Table 4–126 on page 4–94. ● Added Note 10 to Table 4–129 on page 4–98. ● Moved Table 4–127 on page 4–96 to correct order in the chapter. ● Updated Table 4–130 on page 4–100 through Table 4–131 on page 4–100. ● Deleted t_{XZ} and t_{ZX} from Figure 4–4. ● Waveform was added to Figure 4–6. ● The vin and maximum duty cycle values in Note 3 of Table 4–8 were moved to a new Table 4–9. ● Changes were made to values in SSTL-3 class I and II rows in Table 4–17. ● Note 1 was added to Table 4–34. ● Added t_{SU_R} and t_{SU_C} rows in Table 4–38. ● Changed Table 4–55 title from "EP1S10 Column Pin Fast Regional Clock External I/O Timing Parameters" to "EP1S10 External I/O Timing on Column Pins Using Fast Regional Clock Networks." ● Changed values in Tables 4–46, 4–48 to 4–51, 4–128, and 4–130. ● Added t_{ARESET} row in Tables 4–127 to 4–131. ● Deleted -5 Speed Grade column in Tables 4–117 to 4–119 and 4–122 to 4–123. ● Fixed differential waveform in Figure 4–1. ● Added "Definition of I/O Skew" section. ● Added t_{SU} and t_{CO_C} rows and made changes to values in t_{PRE} and t_{CLKHL} rows in Table 4–46. ● Values changed in the t_{SU} and t_{H} rows in Table 4–47. ● Values changed in the $t_{M4KCLKHL}$ row in Table 4–49. ● Values changed in the $t_{MRAMCLKHL}$ row in Table 4–50. ● Added Table 4–51 to "Internal Timing Parameters" section. ● The timing information is preliminary in Tables 4–55 through 4–96. ● Table 4–111 was separated into 3 tables: Tables 4–111 to 4–113.
	November 2003, v2.2	● Updated Tables 4–127 through 4–129.

Chapter	Date/Version	Changes Made
4	October 2003, v2.1	● Added -8 speed grade information. ● Updated performance information in Table 4–36. ● Updated timing information in Tables 4–55 through 4–96. ● Updated delay information in Tables 4–103 through 4–108. ● Updated programmable delay information in Tables 4–100 and 4–103.
	July 2003, v2.0	● Updated clock rates in Tables 4–114 through 4–123. ● Updated speed grade information in the introduction on page 4-1. ● Corrected figures 4-1 & 4-2 and Table 4-9 to reflect how VID and VOD are specified. ● Added note 6 to Table 4-32. ● Updated Stratix Performance Table 4-35. ● Updated EP1S60 and EP1S80 timing parameters in Tables 4-82 to 4-93. The Stratix timing models are final for all devices. ● Updated Stratix IOE programmable delay chains in Tables 4-100 to 4-101. ● Added single-ended I/O standard output pin delay adders for loading in Table 4-102. ● Added spec for FPLL[10..7]CLK pins in Tables 4-104 and 4-107. ● Updated high-speed I/O specification for J=2 in Tables 4-114 and 4-115. ● Updated EPLL specification and fast PLL specification in Tables 4-116 to 4-120.
5	September 2004, v2.1	● Updated reference to device pin-outs on page 5–1 to indicate that device pin-outs are no longer included in this manual and are now available on the Altera web site.
	April 2003, v1.0	● No new changes in Stratix Device Handbook v2.0.

Chapter 1. Introduction

S51001-3.1

Introduction

The Stratix® family of FPGAs is based on a 1.5-V, 0.13-µm, all-layer copper SRAM process, with densities of up to 79,040 logic elements (LEs) and up to 7.5 Mbits of RAM. Stratix devices offer up to 22 digital signal processing (DSP) blocks with up to 176 (9-bit × 9-bit) embedded multipliers, optimized for DSP applications that enable efficient implementation of high-performance filters and multipliers. Stratix devices support various I/O standards and also offer a complete clock management solution with its hierarchical clock structure with up to 420-MHz performance and up to 12 phase-locked loops (PLLs).

The following shows the main sections in the Stratix Device Family Data Sheet:

Features

The Stratix family offers the following features:

- 10,570 to 79,040 LEs; see Table 1–1
- Up to 7,427,520 RAM bits (928,440 bytes) available without reducing logic resources
- TriMatrix™ memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers
- High-speed DSP blocks provide dedicated implementation of multipliers (faster than 300 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
- Up to 16 global clocks with 22 clocking resources per device region
- Up to 12 PLLs (four enhanced PLLs and eight fast PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting
- Support for numerous single-ended and differential I/O standards
- High-speed differential I/O support on up to 116 channels with up to 80 channels optimized for 840 megabits per second (Mbps)
- Support for high-speed networking and communications bus standards including RapidIO, UTOPIA IV, CSIX, HyperTransport™ technology, 10G Ethernet XSBI, SPI-4 Phase 2 (POS-PHY Level 4), and SFI-4
- Differential on-chip termination support for LVDS
- Support for high-speed external memory, including zero bus turnaround (ZBT) SRAM, quad data rate (QDR and QDRII) SRAM, double data rate (DDR) SDRAM, DDR fast cycle RAM (FCRAM), and single data rate (SDR) SDRAM
- Support for 66-MHz PCI (64 and 32 bit) in -6 and faster speed-grade devices, support for 33-MHz PCI (64 and 32 bit) in -8 and faster speed-grade devices
- Support for 133-MHz PCI-X 1.0 in -5 speed-grade devices
- Support for 100-MHz PCI-X 1.0 in -6 and faster speed-grade devices
- Support for 66-MHz PCI-X 1.0 in -7 speed-grade devices
- Support for multiple intellectual property megafunctions from Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
- Support for remote configuration updates

Table 1–1. Stratix Device Features — EP1S10, EP1S20, EP1S25, EP1S30

Feature	EP1S10	EP1S20	EP1S25	EP1S30
LEs	10,570	18,460	25,660	32,470
M512 RAM blocks (32 × 18 bits)	94	194	224	295
M4K RAM blocks (128 × 36 bits)	60	82	138	171
M-RAM blocks (4K × 144 bits)	1	2	2	4
Total RAM bits	920,448	1,669,248	1,944,576	3,317,184
DSP blocks	6	10	10	12
Embedded multipliers *(1)*	48	80	80	96
PLLs	6	6	6	10
Maximum user I/O pins	426	586	706	726

Table 1–2. Stratix Device Features — EP1S40, EP1S60, EP1S80

Feature	EP1S40	EP1S60	EP1S80
LEs	41,250	57,120	79,040
M512 RAM blocks (32 × 18 bits)	384	574	767
M4K RAM blocks (128 × 36 bits)	183	292	364
M-RAM blocks (4K × 144 bits)	4	6	9
Total RAM bits	3,423,744	5,215,104	7,427,520
DSP blocks	14	18	22
Embedded multipliers *(1)*	112	144	176
PLLs	12	12	12
Maximum user I/O pins	822	1,022	1,238

Note to Tables 1–1 and 1–2:

(1) This parameter lists the total number of 9 × 9-bit multipliers for each device. For the total number of 18 × 18-bit multipliers per device, divide the total number of 9 × 9-bit multipliers by 2. For the total number of 36 × 36-bit multipliers per device, divide the total number of 9 × 9-bit multipliers by 8.

Stratix devices are available in space-saving FineLine BGA™ and ball-grid array (BGA) packages (see Tables 1–3 through 1–5). All Stratix devices support vertical migration within the same package (e.g., the designer can migrate between the EP1S10, EP1S20, and EP1S25 devices in the 672-pin BGA package). Vertical migration means that designers can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, the designer must cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migrational. The Quartus® II software can automatically cross reference and place all pins except differential pins for migration when given a device migration list. The designer must use the pin-outs for each device to verify the differential placement migration. A future version of the Quartus II software will support differential pin migration.

Table 1–3. Stratix Package Options & I/O Pin Counts

Device	672-Pin BGA	956-Pin BGA	484-Pin FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP1S10	345		335	345	426		
EP1S20	426		361	426	586		
EP1S25	473			473	597	706	
EP1S30		683			597	726	
EP1S40		683			615	773	822
EP1S60		683				773	1,022
EP1S80		683				773	1,203

Note to Table 1–3:

(1) All I/O pin counts include 20 dedicated clock input pins (`clk[15..0]p`, `clk0n`, `clk2n`, `clk9n`, and `clk11n`) that can be used for data inputs.

Table 1–4. Stratix BGA Package Sizes

Dimension	672 Pin	956 Pin
Pitch (mm)	1.27	1.27
Area (mm^2)	1,225	1,600
Length × width (mm × mm)	35 × 35	40 × 40

Table 1–5. Stratix FineLine BGA Package Sizes

Dimension	484 Pin	672 Pin	780 Pin	1,020 Pin	1,508 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm^2)	529	729	841	1,089	1,600
Length × width (mm × mm)	23 × 23	27 × 27	29 × 29	33 × 33	40 × 40

Stratix devices are available in up to four speed grades, -5, -6, -7, and -8, with -5 being the fastest. Table 1–6 shows Stratix device speed-grade offerings.

Table 1–6. Stratix Device Speed Grades

Device	672-Pin BGA	956-Pin BGA	484-Pin FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP1S10	-6, -7		-5, -6, -7	-6, -7	-5, -6, -7		
EP1S20	-6, -7		-5, -6, -7	-6, -7	-5, -6, -7		
EP1S25	-6, -7			-6, -7, -8	-5, -6, -7	-5, -6, -7	
EP1S30		-5, -6, -7			-5, -6, -7, -8	-5, -6, -7	
EP1S40		-5, -6, -7			-5, -6, -7, -8	-5, -6, -7	-5, -6, -7
EP1S60		-6, -7				-5, -6, -7	-6, -7
EP1S80		-6, -7				-5, -6, -7	-5, -6, -7

Chapter 2. Stratix Architecture

S51002-3.1

Functional Description

Stratix® devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provide signal interconnects between logic array blocks (LABs), memory block structures, and DSP blocks.

The logic array consists of LABs, with 10 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 318 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 291 MHz. These blocks are grouped into columns across the device in between certain LABs.

M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 269 MHz. Several M-RAM blocks are located individually or in pairs within the device’s logic array.

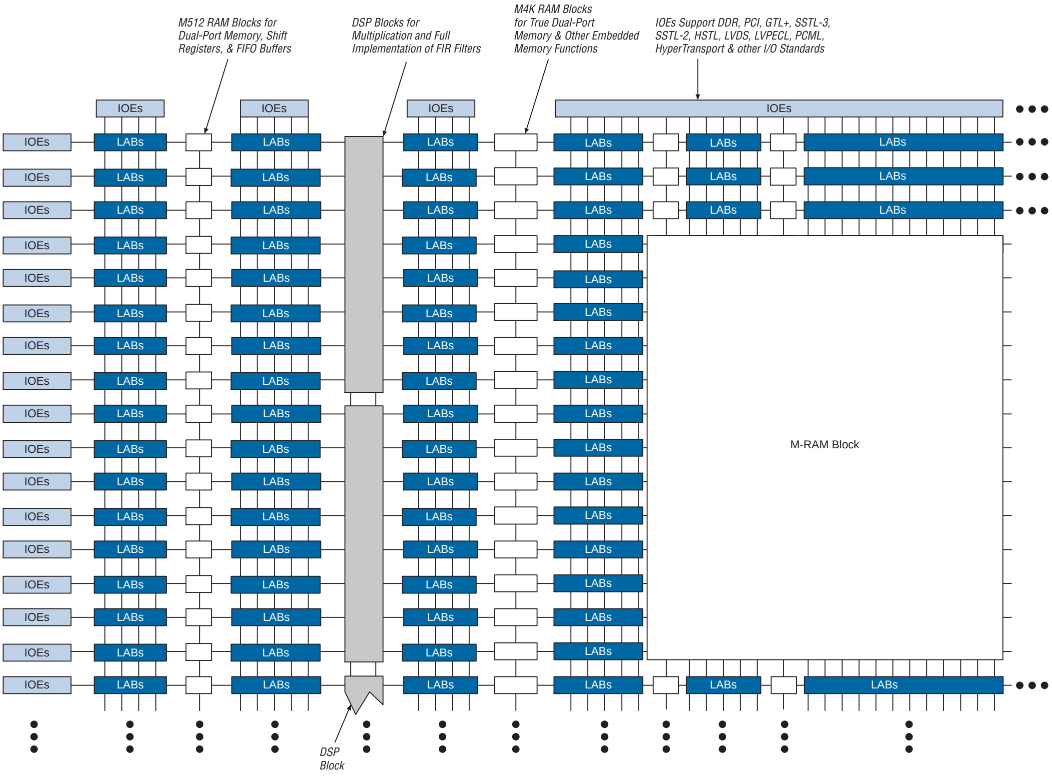
Digital signal processing (DSP) blocks can implement up to either eight full-precision 9 ° 9-bit multipliers, four full-precision 18 ° 18-bit multipliers, or one full-precision 36 ° 36-bit multiplier with add or subtract features. These blocks also contain 18-bit input shift registers for digital signal processing applications, including FIR and infinite impulse response (IIR) filters. DSP blocks are grouped into two columns in each device.

Each Stratix device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR SDRAM, FCRAM, ZBT, and QDR SRAM devices.

High-speed serial interface channels support transfers at up to 840 Mbps using LVDS, LVPECL, 3.3-V PCML, or HyperTransport technology I/O standards.

Figure 2–1 shows an overview of the Stratix device.

Figure 2–1. Stratix Block Diagram



The number of M512 RAM, M4K RAM, and DSP blocks varies by device along with row and column numbers and M-RAM blocks. Table 2–1 lists the resources available in Stratix devices.

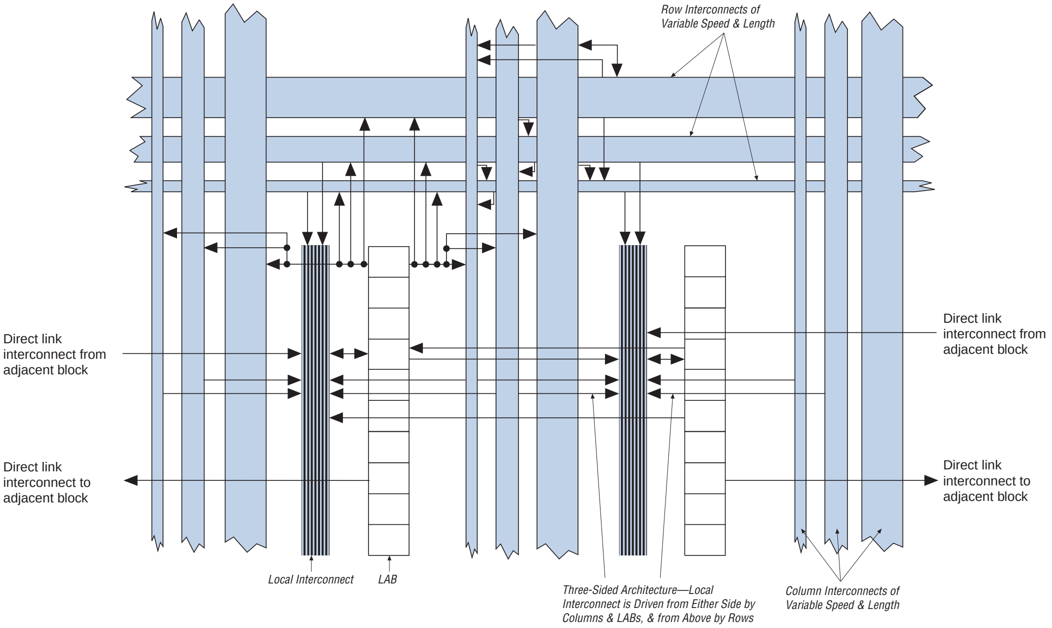
Table 2–1. Stratix Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP1S10	4 / 94	2 / 60	1	2 / 6	40	30
EP1S20	6 / 194	2 / 82	2	2 / 10	52	41
EP1S25	6 / 224	3 / 138	2	2 / 10	62	46
EP1S30	7 / 295	3 / 171	4	2 / 12	67	57
EP1S40	8 / 384	3 / 183	4	2 / 14	77	61
EP1S60	10 / 574	4 / 292	6	2 / 18	90	73
EP1S80	11 / 767	4 / 364	9	2 / 22	101	91

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, local interconnect, LUT chain, and register chain connection lines. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within an LAB. The Quartus® II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–2 shows the Stratix LAB.

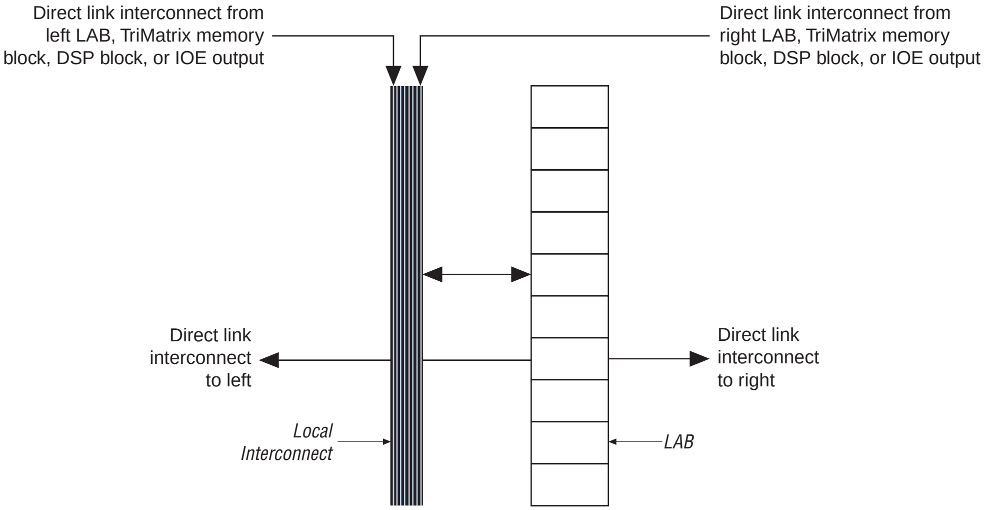
Figure 2–2. Stratix LAB Structure



LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, or DSP blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and direct link interconnects. Figure 2–3 shows the direct link connection.

Figure 2–3. Direct Link Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, synchronous load, and add/subtract control signals. This gives a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

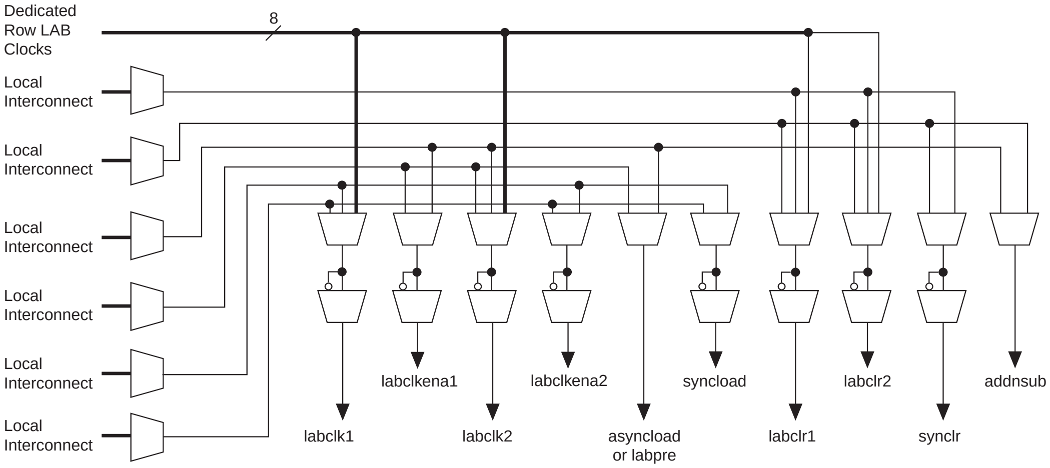
Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal will also use `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. De-asserting the clock enable signal will turn off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. The asynchronous load acts as a preset when the asynchronous load data input is tied high.

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as DSP correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB row clocks [7..0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–4 shows the LAB control signal generation circuit.

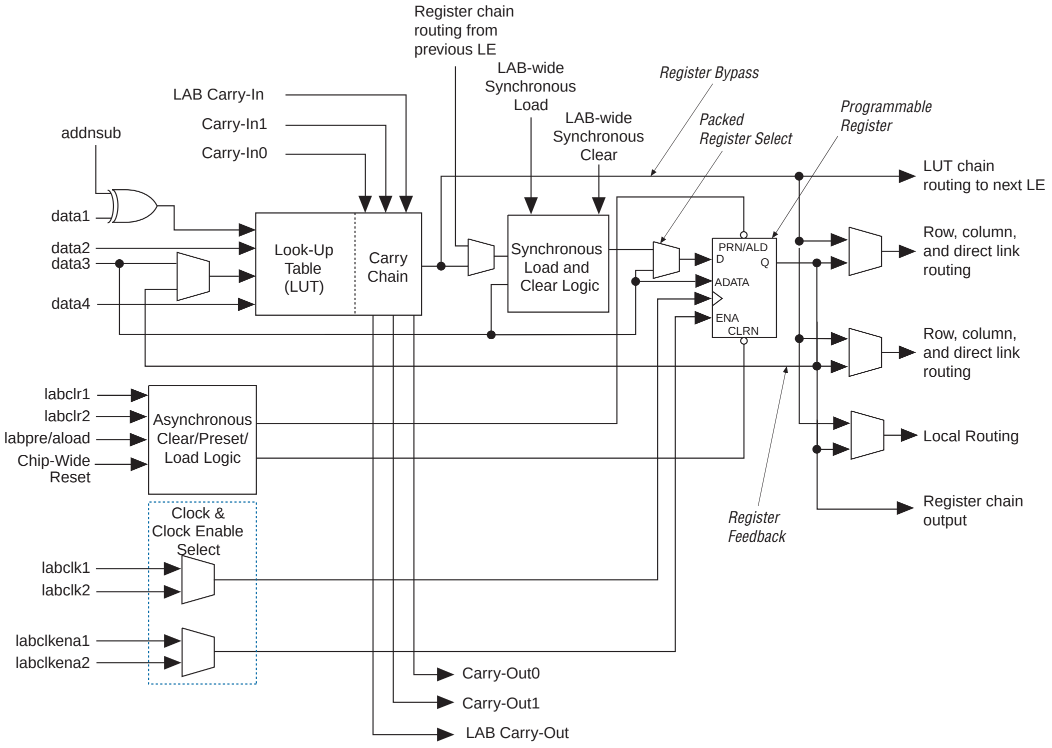
Figure 2–4. LAB-Wide Control Signals



Logic Elements

The smallest unit of logic in the Stratix architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry select capability. A single LE also supports dynamic single bit addition or subtraction mode selectable by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and direct link interconnects. See Figure 2–5.

Figure 2–5. Stratix LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the `data3` input of the LE. For combinatorial functions, the register is bypassed and the output of the LUT drives directly to the outputs of the LE.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and direct link routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the LUT for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

LUT Chain & Register Chain

In addition to the three general routing outputs, the LEs within an LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinatorial function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. See "MultiTrack Interconnect" on page 2–14 for more information on LUT chain and register chain connections.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either A + B or A – B. The LUT computes addition, and subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in = 1 to add one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The Stratix LE can operate in one of the following modes:

- Normal mode
- Dynamic arithmetic mode

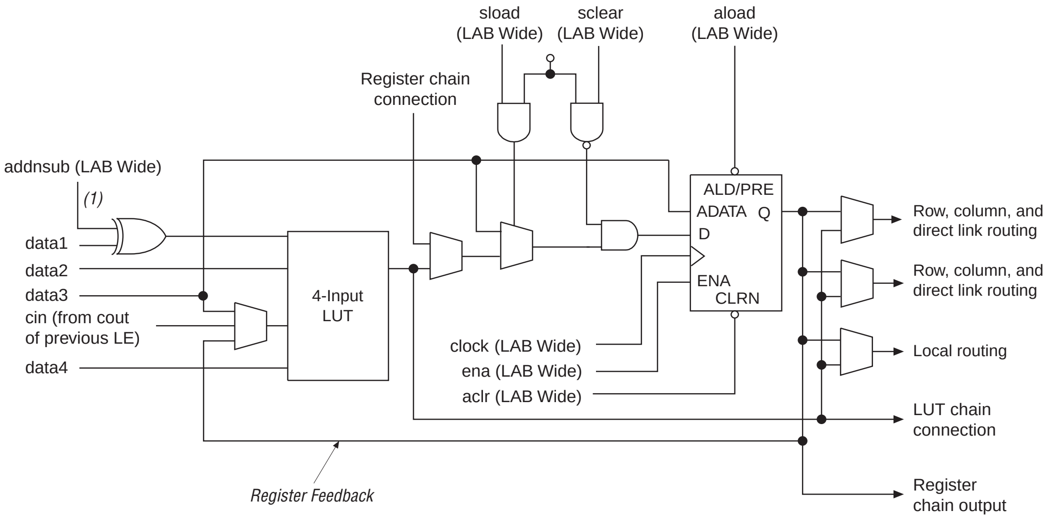
Each mode uses LE resources differently. In each mode, eight available inputs to the LE—the four data inputs from the LAB local interconnect; `carry-in0` and `carry-in1` from the previous LE; the LAB carry-in from the previous carry-chain LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The `addnsub` control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinatorial functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2–6). The Quartus II Compiler automatically selects the carry-in or the `data3` signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinatorial output directly to the next LE in the LAB. Asynchronous load data for the register comes from the `data3` input of the LE. LEs in normal mode support packed registers.

Figure 2–6. LE in Normal Mode



Note to Figure 2–6:

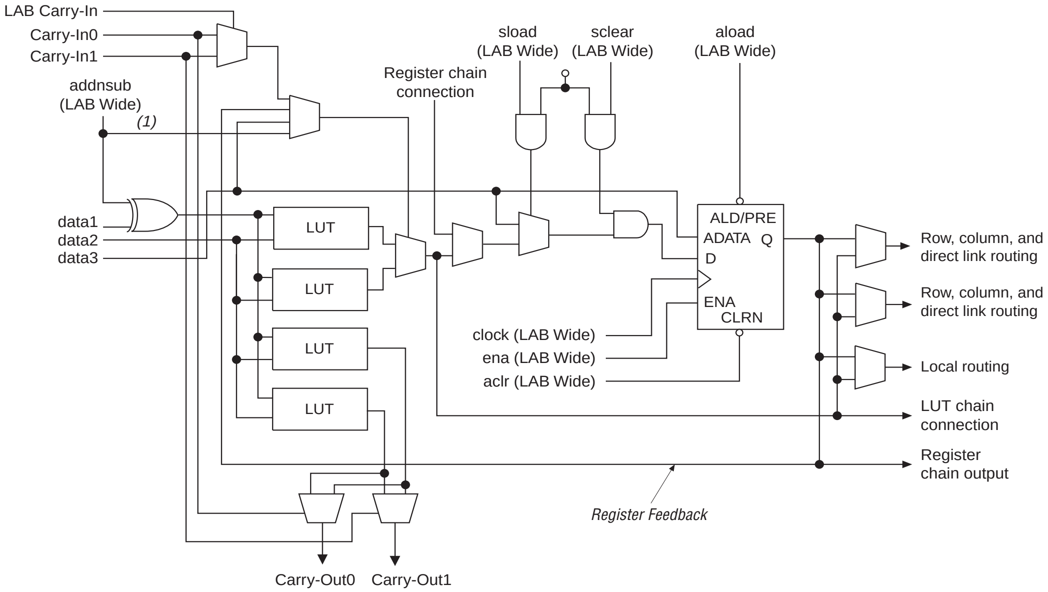
(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

Dynamic Arithmetic Mode

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry select circuitry. As shown in Figure 2–7, the LAB carry-in signal selects either the `carry-in0` or `carry-in1` chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinatorial or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums: `data1` + `data2` + `carry-in0` or `data1` + `data2` + `carry-in1`. The other two LUTs use the `data1` and `data2` signals to generate two possible carry-out signals—one for a carry of 1 and the other for a carry of 0. The `carry-in0` signal acts as the carry select for the `carry-out0` output and `carry-in1` acts as the carry select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The `addnsub` LAB-wide signal controls whether the LE acts as an adder or subtractor.

Figure 2–7. LE in Dynamic Arithmetic Mode



Note to Figure 2–7:

(1) The `addnsub` signal is tied to the carry input for the first LE of a carry chain only.

Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 1 and carry-in of 0 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

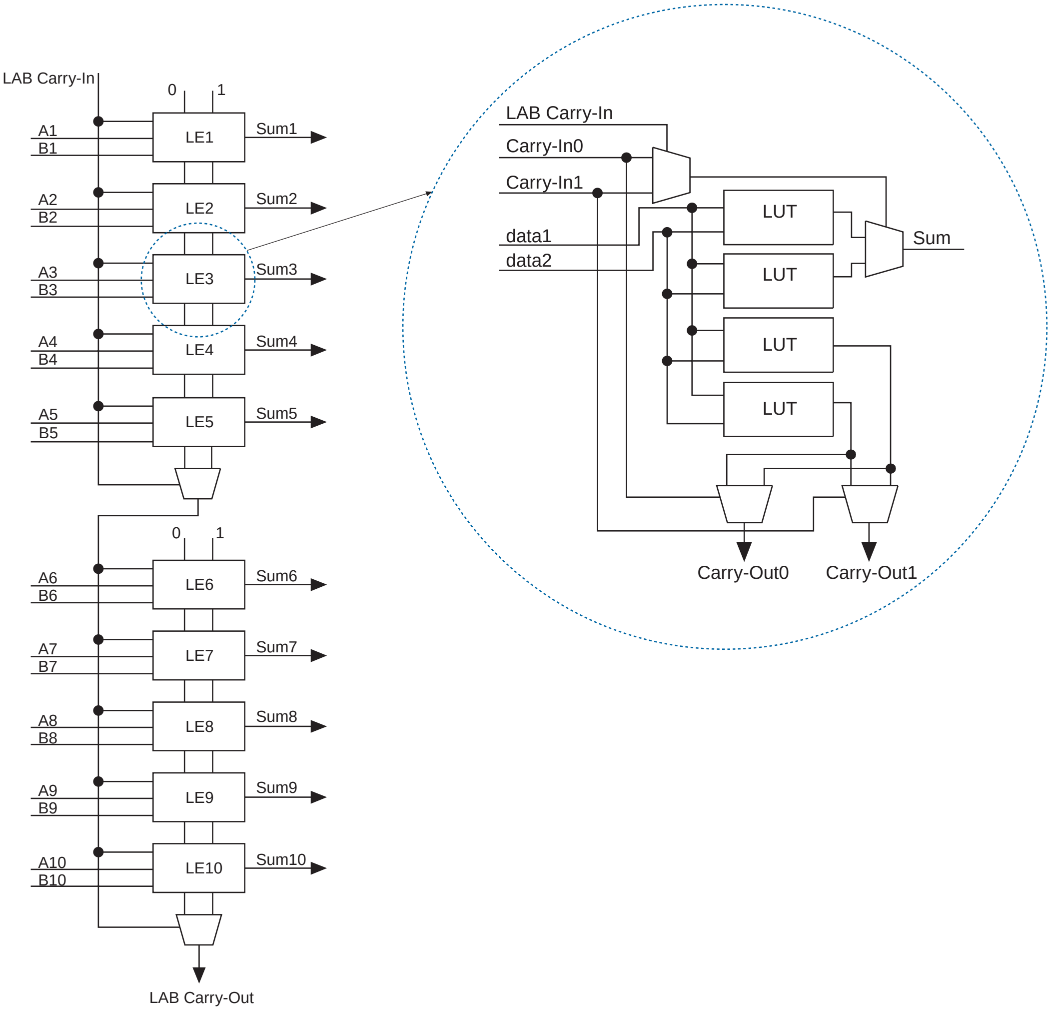
The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delay between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the Stratix architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 2–8 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, `carry-in0` or `carry-in1`, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.

The Quartus II Compiler automatically creates carry chain logic during design processing, or the designer can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II Compiler creates carry chains longer than 10 LEs by linking LABs together automatically. For enhanced fitting, a long carry chain runs vertically allowing fast horizontal connections to TriMatrix memory and DSP blocks. A carry chain can continue as far as a full column.

Figure 2–8. Carry Select Chain



Clear & Preset Logic Control

LAB-wide signals control the logic for the register′s clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. The direct asynchronous preset does not require a NOT-gate push-back technique. Stratix devices support simultaneous preset/

asynchronous load, and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, Stratix devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals.

MultiTrack Interconnect

In the Stratix architecture, connections between LEs, TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement within the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

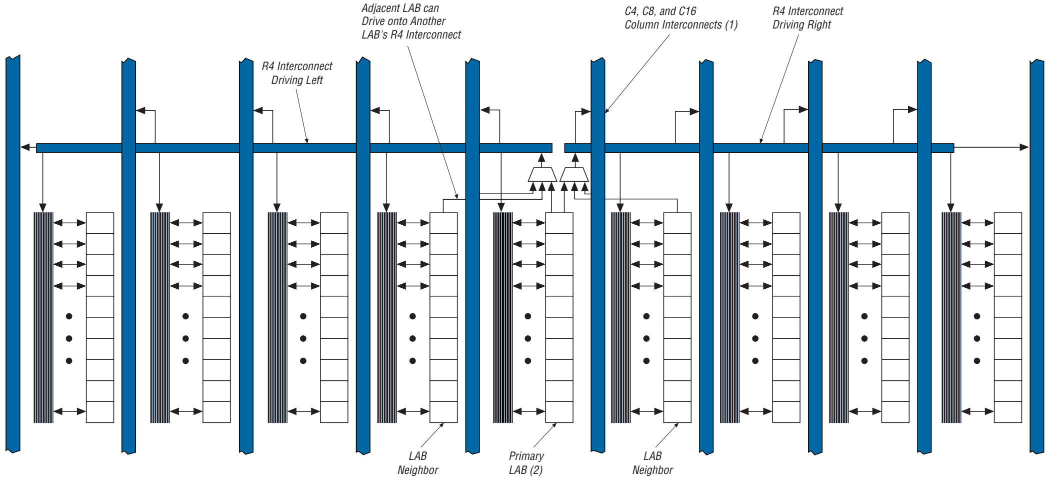
The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory within the same row. These row resources include:

- Direct link interconnects between LABs and adjacent blocks.
- R4 interconnects traversing four blocks to the right or left.
- R8 interconnects traversing eight blocks to the right or left.
- R24 row interconnects for high-speed access across the length of the device.

The direct link interconnect allows an LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors and then back into itself. Only one side of a M-RAM block interfaces with direct link and row interconnects. This provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs, three LABs and one M512 RAM block, two LABs and one M4K RAM block, or two LABs and one DSP block to the right or left of a source LAB. These resources are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–9 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by DSP blocks and RAM blocks and horizontal IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 and C16 interconnects for connections from one row to another. Additionally, R4 interconnects can drive R24 interconnects.

Figure 2–9. R4 Interconnect Connections



Notes to Figure 2–9:

(1) C4 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

The R8 interconnects span eight LABs, M512 or M4K RAM blocks, or DSP blocks to the right or left from a source LAB. These resources are used for fast row connections in an eight-LAB region. Every LAB has its own set of R8 interconnects to drive either left or right. R8 interconnect connections between LABs in a row are similar to the R4 connections shown in Figure 2–9, with the exception that they connect to eight LABs to the right or left, not four. Like R4 interconnects, R8 interconnects can drive and be driven by all types of architecture blocks. R8 interconnects can drive other R8 interconnects to extend their range as well as C8 interconnects for row-to-row connections. One R8 interconnect is faster than two R4 interconnects connected together.

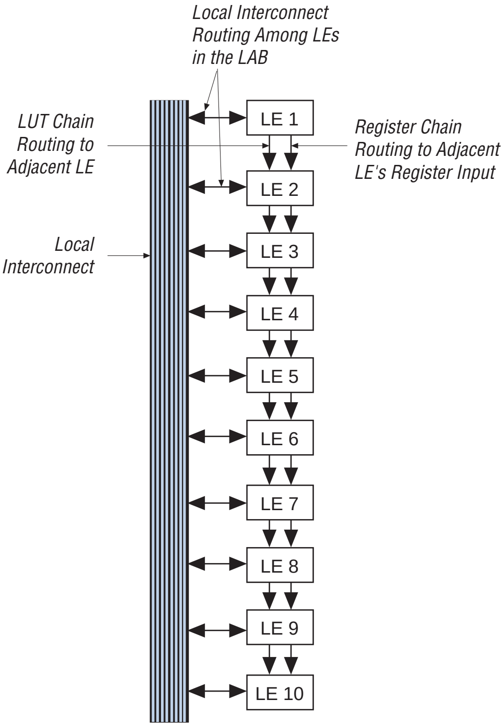
R24 row interconnects span 24 LABs and provide the fastest resource for long row connections between LABs, TriMatrix memory, DSP blocks, and IOEs. The R24 row interconnects can cross M-RAM blocks. R24 row interconnects drive to other row or column interconnects at every fourth LAB and do not drive directly to LAB local interconnects. R24 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R24 interconnects can drive R24, R4, C16, and C4 interconnects.

The column interconnect operates similarly to the row interconnect and vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs, TriMatrix memory and DSP blocks, and horizontal IOEs. These column resources include:

- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four blocks in up and down direction
- C8 interconnects traversing a distance of eight blocks in up and down direction
- C16 column interconnects for high-speed vertical routing through the device

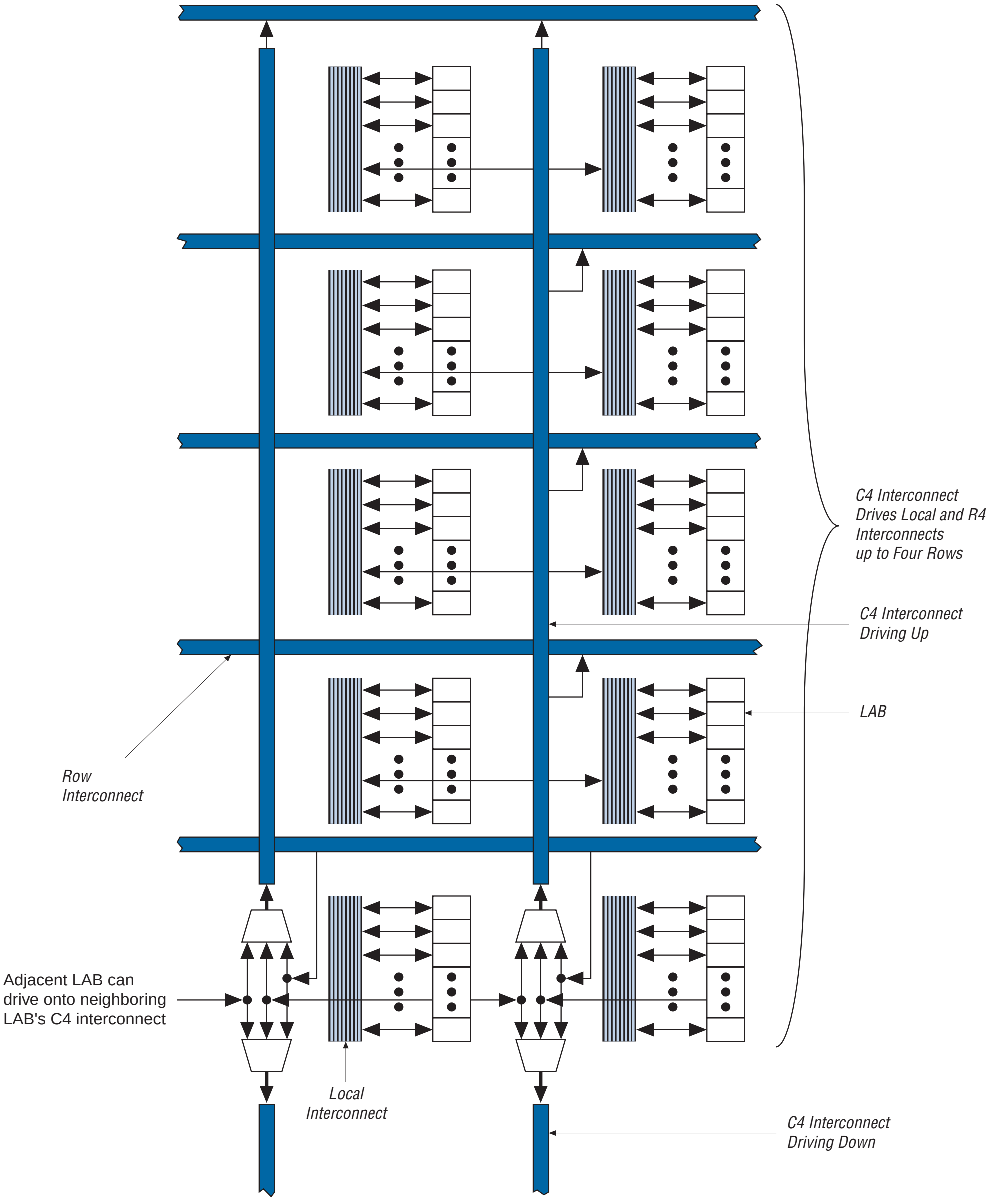
Stratix devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinatorial output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–10 shows the LUT chain and register chain interconnects.

Figure 2–10. LUT Chain & Register Chain Interconnects



The C4 interconnects span four LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–11 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and vertical IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2–11. C4 Interconnect Connections *Note (1)*



Note to Figure 2–11:

(1) Each C4 interconnect can drive either up or down four rows.

C8 interconnects span eight LABs, M512, or M4K blocks up or down from a source LAB. Every LAB has its own set of C8 interconnects to drive either up or down. C8 interconnect connections between the LABs in a column are similar to the C4 connections shown in Figure 2–11 with the exception that they connect to eight LABs above and below. The C8 interconnects can drive and be driven by all types of architecture blocks similar to C4 interconnects. C8 interconnects can drive each other to extend their range as well as R8 interconnects for column-to-column connections. C8 interconnects are faster than two C4 interconnects.

C16 column interconnects span a length of 16 LABs and provide the fastest resource for long column connections between LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C16 interconnects can cross M-RAM blocks and also drive to row and column interconnects at every fourth LAB. C16 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly.

All embedded blocks communicate with the logic array similar to LAB-to-LAB interfaces. Each block (i.e., TriMatrix memory and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB. All blocks are fed by the row LAB clocks, `labclk[7..0]`.

Table 2–2 shows the Stratix device's routing scheme.

Table 2–2. Stratix Device Routing Scheme

Source	Destination																
	LUT Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R8 Interconnect	R24 Interconnect	C4 Interconnect	C8 Interconnect	C16 Interconnect	LE	M512 RAM Block	M4K RAM Block	M-RAM Block	DSP Blocks	Column IOE	Row IOE
LUT Chain											✓						
Register Chain											✓						
Local Interconnect											✓	✓	✓	✓	✓	✓	✓
Direct Link Interconnect			✓														
R4 Interconnect			✓		✓		✓	✓		✓							
R8 Interconnect			✓			✓			✓								
R24 Interconnect					✓		✓	✓		✓							
C4 Interconnect			✓		✓			✓									
C8 Interconnect			✓			✓			✓								
C16 Interconnect					✓		✓	✓		✓							
LE	✓	✓	✓	✓	✓	✓		✓	✓								
M512 RAM Block			✓	✓	✓	✓		✓	✓								
M4K RAM Block			✓	✓	✓	✓		✓	✓								
M-RAM Block								✓	✓								
DSP Blocks			✓	✓	✓	✓		✓	✓								
Column IOE				✓				✓	✓	✓							
Row IOE				✓		✓	✓	✓	✓	✓							

TriMatrix Memory

TriMatrix memory consists of three types of RAM blocks: M512, M4K, and M-RAM blocks. Although these memory blocks are different, they can all implement various types of memory with or without parity, including true dual-port, simple dual-port, and single-port RAM, ROM, and FIFO buffers. Table 2–3 shows the size and features of the different RAM blocks.

Table 2–3. TriMatrix Memory Features (Part 1 of 2)

Memory Feature	M512 RAM Block (32 ° 18 Bits)	M4K RAM Block (128 ° 36 Bits)	M-RAM Block (4K ° 144 Bits)
Maximum performance	*(1)*	*(1)*	*(1)*
True dual-port memory		✓	✓
Simple dual-port memory	✓	✓	✓
Single-port memory	✓	✓	✓
Shift register	✓	✓	
ROM	✓	✓	*(2)*
FIFO buffer	✓	✓	✓
Byte enable		✓	✓
Parity bits	✓	✓	✓
Mixed clock mode	✓	✓	✓
Memory initialization	✓	✓	
Simple dual-port memory mixed width support	✓	✓	✓
True dual-port memory mixed width support		✓	✓
Power-up conditions	Outputs cleared	Outputs cleared	Outputs unknown
Register clears	Input and output registers	Input and output registers	Output registers
Mixed-port read-during-write	Unknown output/old data	Unknown output/old data	Unknown output

Table 2–3. TriMatrix Memory Features (Part 2 of 2)

Memory Feature	M512 RAM Block (32 ° 18 Bits)	M4K RAM Block (128 ° 36 Bits)	M-RAM Block (4K ° 144 Bits)
Configurations	512 × 1 256 × 2 128 × 4 64 × 8 64 × 9 32 × 16 32 × 18	4K × 1 2K × 2 1K × 4 512 × 8 512 × 9 256 × 16 256 × 18 128 × 32 128 × 36	64K × 8 64K × 9 32K × 16 32K × 18 16K × 32 16K × 36 8K × 64 8K × 72 4K × 128 4K × 144

Notes to Table 2–3:

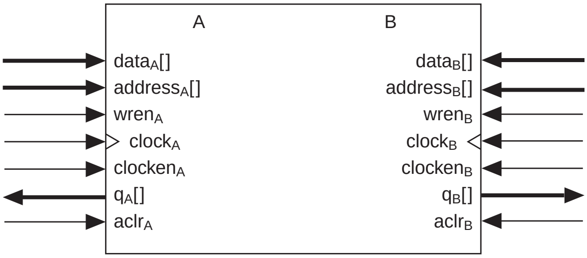
(1) See Table 4–36 for maximum performance information.

(2) The M-RAM block does not support memory initializations. However, the M-RAM block can emulate a ROM function using a dual-port RAM bock. The Stratix device must write to the dual-port memory once and then disable the write-enable ports afterwards.

Memory Modes

TriMatrix memory blocks include input registers that synchronize writes and output registers to pipeline designs and improve system performance. M4K and M-RAM memory blocks offer a true dual-port mode to support any combination of two-port operations: two reads, two writes, or one read and one write at two different clock frequencies. Figure 2–12 shows true dual-port memory.

Figure 2–12. True Dual-Port Memory Configuration

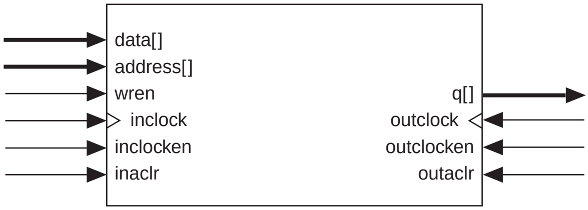


In addition to true dual-port memory, the memory blocks support simple dual-port and single-port RAM. Simple dual-port memory supports a simultaneous read and write and can either read old data before the write occurs or just read the don’t care bits. Single-port memory supports nonsimultaneous reads and writes, but the `q[]` port will output the data once it has been written to the memory (if the outputs are not registered) or after the next rising edge of the clock (if the outputs are registered). For more information, see Chapter 2, TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices of the *Stratix Device Handbook, Volume 2*. Figure 2–13 shows these different RAM memory port configurations for TriMatrix memory.

Figure 2–13. Simple Dual-Port & Single-Port Memory Configurations

Simple Dual-Port Memory

Single-Port Memory *(1)*



Note to Figure 2–13:

(1) Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The memory blocks also enable mixed-width data ports for reading and writing to the RAM ports in dual-port RAM configuration. For example, the memory block can be written in °1 mode at port A and read out in °16 mode from port B.

TriMatrix memory architecture can implement pipelined RAM by registering both the input and output signals to the RAM block. All TriMatrix memory block inputs are registered providing synchronous write cycles. In synchronous operation, the memory block generates its own self-timed strobe write enable (`WREN`) signal derived from the global or regional clock. In contrast, a circuit using asynchronous RAM must generate the RAM `WREN` signal while ensuring its data and address signals meet setup and hold time specifications relative to the `WREN` signal. The output registers can be bypassed. Flow-through reading is possible in the simple dual-port mode of M512 and M4K RAM blocks by clocking the read enable and read address registers on the negative clock edge and bypassing the output registers.

Two single-port memory blocks can be implemented in a single M4K block as long as each of the two independent block sizes is equal to or less than half of the M4K block size.

The Quartus II software automatically implements larger memory by combining multiple TriMatrix memory blocks. For example, two 256 ° 16-bit RAM blocks can be combined to form a 256 ° 32-bit RAM block. Memory performance does not degrade for memory blocks using the maximum number of words available in one memory block. Logical memory blocks using less than the maximum number of words use physical blocks in parallel, eliminating any external control logic that would increase delays. To create a larger high-speed memory block, the Quartus II software automatically combines memory blocks with LE control logic.

Parity Bit Support

The memory blocks support a parity bit for each byte. The parity bit, along with internal LE logic, can implement parity checking for error detection to ensure data integrity. Designers can also use parity-size data words to store user-specified control bits. In the M4K and M-RAM blocks, byte enables are also available for data input masking during write operations.

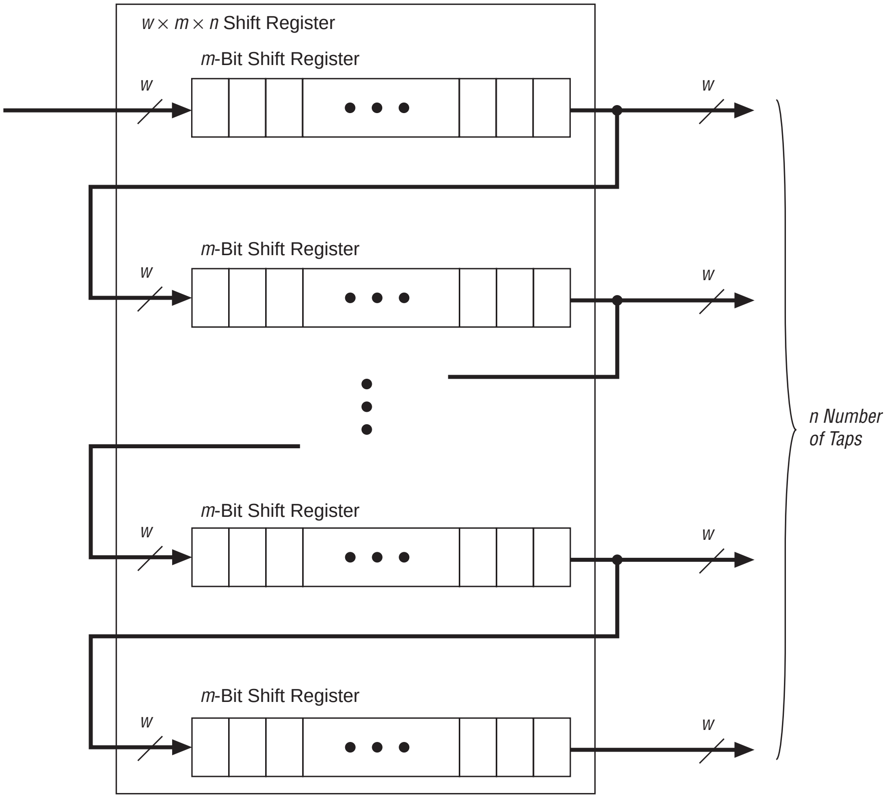
Shift Register Support

The designer can configure embedded memory blocks to implement shift registers for DSP applications such as pseudo-random number generators, multi-channel filtering, auto-correlation, and cross-correlation functions. These and other DSP applications require local data storage, traditionally implemented with standard flip-flops, which can quickly consume many logic cells and routing resources for large shift registers. A more efficient alternative is to use embedded memory as a shift register block, which saves logic cell and routing resources and provides a more efficient implementation with the dedicated circuitry.

The size of a w ° m ° n shift register is determined by the input data width (w), the length of the taps (m), and the number of taps (n). The size of a w ° m ° n shift register must be less than or equal to the maximum number of memory bits in the respective block: 576 bits for the M512 RAM block and 4,608 bits for the M4K RAM block. The total number of shift register outputs (number of taps n ° width w) must be less than the maximum data width of the RAM block (18 for M512 blocks, 36 for M4K blocks). To create larger shift registers, the memory blocks are cascaded together.

Data is written into each address location at the falling edge of the clock and read from the address at the rising edge of the clock. The shift register mode logic automatically controls the positive and negative edge clocking to shift the data in one clock cycle. Figure 2–14 shows the TriMatrix memory block in the shift register mode.

Figure 2–14. Shift Register Memory Configuration



Memory Block Size

TriMatrix memory provides three different memory sizes for efficient application support. The large number of M512 blocks are ideal for designs with many shallow first-in first-out (FIFO) buffers. M4K blocks provide additional resources for channelized functions that do not require large amounts of storage. The M-RAM blocks provide a large single block of RAM ideal for data packet storage. The different-sized blocks allow Stratix devices to efficiently support variable-sized memory in designs.

The Quartus II software automatically partitions the user-defined memory into the embedded memory blocks using the most efficient size combinations. The designer can also manually assign the memory to a specific block size or a mixture of block sizes.

M512 RAM Block

The M512 RAM block is a simple dual-port memory block and is useful for implementing small FIFO buffers, DSP, and clock domain transfer applications. Each block contains 576 RAM bits (including parity bits). M512 RAM blocks can be configured in the following modes:

- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, the designer can use an initialization file to pre-load the memory contents.

The memory address depths and output widths can be configured as 512 × 1, 256 × 2, 128 × 4, 64 × 8 (64 × 9 bits with parity), and 32 × 16 (32 × 18 bits with parity). Mixed-width configurations are also possible, allowing different read and write widths. Table 2–4 summarizes the possible M512 RAM block configurations.

Table 2–4. M512 RAM Block Configurations (Simple Dual-Port RAM) (Part 1 of 2)

Read Port	Write Port						
	512 × 1	256 × 2	128 × 4	64 × 8	32 × 16	64 × 9	32 × 18
512 × 1	✓	✓	✓	✓	✓		
256 × 2	✓	✓	✓	✓	✓		
128 × 4	✓	✓	✓		✓		
64 × 8	✓	✓		✓			
32 × 16	✓	✓	✓		✓		

Table 2–4. M512 RAM Block Configurations (Simple Dual-Port RAM) (Part 2 of 2)

Read Port	Write Port						
	512 ° 1	256 ° 2	128 ° 4	64 ° 8	32 ° 16	64 ° 9	32 ° 18
64 ° 9						✓	
32 ° 18							✓

When the M512 RAM block is configured as a shift register block, a shift register of size up to 576 bits is possible.

The M512 RAM block can also be configured to support serializer and deserializer applications. By using the mixed-width support in combination with DDR I/O standards, the block can function as a SERDES to support low-speed serial I/O standards using global or regional clocks. See "I/O Structure" on page 2–102 for details on dedicated SERDES in Stratix devices.

M512 RAM blocks can have different clocks on its inputs and outputs. The `wren`, `datain`, and write address registers are all clocked together from one of the two clocks feeding the block. The read address, `rden`, and output registers can be clocked by either of the two clocks driving the block. This allows the RAM block to operate in read/write or input/output clock modes. Only the output register can be bypassed. The eight `labclk` signals or local interconnect can drive the `inclock`, `outclock`, `wren`, `rden`, `inclr`, and `outclr` signals. Because of the advanced interconnect between the LAB and M512 RAM blocks, LEs can also control the `wren` and `rden` signals and the RAM clock, clock enable, and asynchronous clear signals. Figure 2–15 shows the M512 RAM block control signal generation logic.

The RAM blocks within Stratix devices have local interconnects to allow LEs and interconnects to drive into RAM blocks. The M512 RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. The M512 RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. Up to 10 direct link input connections to the M512 RAM block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M512 RAM outputs can also connect to left and right LABs through 10 direct link interconnects. The M512 RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 2–16 shows the M512 RAM block to logic array interface.

Figure 2–15. M512 RAM Block Control Signals

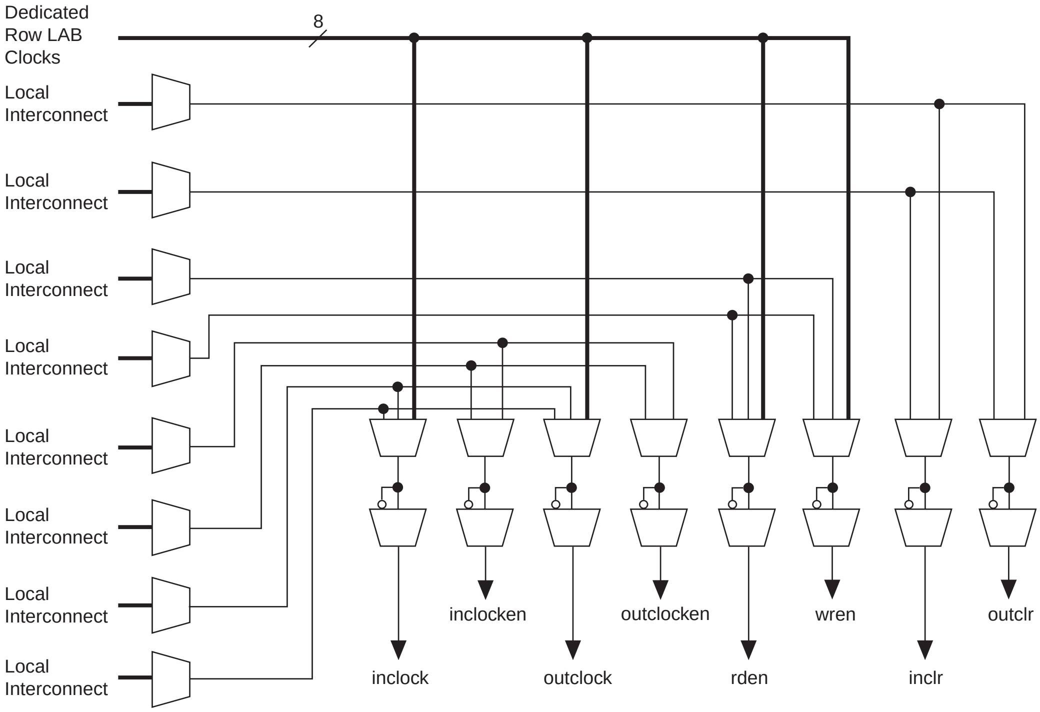
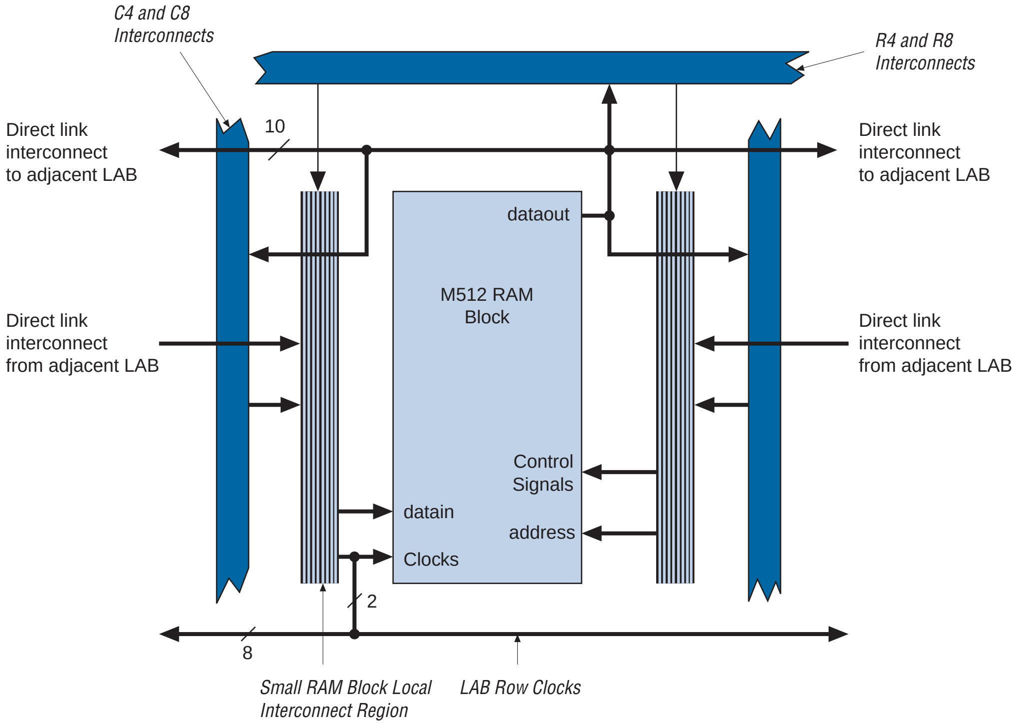


Figure 2–16. M512 RAM Block LAB Row Interface



M4K RAM Blocks

The M4K RAM block includes support for true dual-port RAM. The M4K RAM block is used to implement buffers for a wide variety of applications such as storing processor code, implementing lookup schemes, and implementing larger memory applications. Each block contains 4,608 RAM bits (including parity bits). M4K RAM blocks can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO
- ROM
- Shift register

When configured as RAM or ROM, the designer can use an initialization file to pre-load the memory contents.

The memory address depths and output widths can be configured as 4,096 ° 1, 2,048 ° 2, 1,024 ° 4, 512 ° 8 (or 512 ° 9 bits), 256 ° 16 (or 256 ° 18 bits), and 128 ° 32 (or 128 ° 36 bits). The 128 ° 32- or 36-bit configuration is not available in the true dual-port mode. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–5 and 2–6 summarize the possible M4K RAM block configurations.

Table 2–5. M4K RAM Block Configurations (Simple Dual-Port)

Read Port	Write Port								
	4K ° 1	**2K ° 2**	**1K ° 4**	**512 ° 8**	**256 ° 16**	**128 ° 32**	**512 ° 9**	**256 ° 18**	**128 ° 36**
4K ° 1	✓	✓	✓	✓	✓	✓			
2K ° 2	✓	✓	✓	✓	✓	✓			
1K ° 4	✓	✓	✓	✓	✓	✓			
512 ° 8	✓	✓	✓	✓	✓	✓			
256 ° 16	✓	✓	✓	✓	✓	✓			
128 ° 32	✓	✓	✓	✓	✓	✓			
512 ° 9							✓	✓	✓
256 ° 18							✓	✓	✓
128 ° 36							✓	✓	✓

Table 2–6. M4K RAM Block Configurations (True Dual-Port)

Port A	Port B						
	4K ° 1	**2K ° 2**	**1K ° 4**	**512 ° 8**	**256 ° 16**	**512 ° 9**	**256 ° 18**
4K ° 1	✓	✓	✓	✓	✓		
2K ° 2	✓	✓	✓	✓	✓		
1K ° 4	✓	✓	✓	✓	✓		
512 ° 8	✓	✓	✓	✓	✓		
256 ° 16	✓	✓	✓	✓	✓		
512 ° 9						✓	✓
256 ° 18						✓	✓

When the M4K RAM block is configured as a shift register block, the designer can create a shift register up to 4,608 bits (w ° m ° n).

M4K RAM blocks support byte writes when the write port has a data width of 16, 18, 32, or 36 bits. The byte enables allow the input data to be masked so the device can write to specific bytes. The unwritten bytes retain the previous written value. Table 2–7 summarizes the byte selection.

Table 2–7. Byte Enable for M4K Blocks *Notes (1), (2)*

byteena[3..0]	datain °18	datain °36
[0] = 1	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]
[2] = 1	–	[26..18]
[3] = 1	–	[35..27]

Notes to Table 2–7:
(1) Any combination of byte enables is possible.
(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16 and ×32 modes.

The M4K RAM blocks allow for different clocks on their inputs and outputs. Either of the two clocks feeding the block can clock M4K RAM block registers (`renwe`, address, byte enable, `datain`, and output registers). Only the output register can be bypassed. The eight `labclk` signals or local interconnects can drive the control signals for the A and B ports of the M4K RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, `clr_b`, `clocken_a`, and `clocken_b` signals, as shown in Figure 2–17.

The R4, R8, C4, C8, and direct link interconnects from adjacent LABs drive the M4K RAM block local interconnect. The M4K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 10 direct link input connections to the M4K RAM Block are possible from the left adjacent LABs and another 10 possible from the right adjacent LAB. M4K RAM block outputs can also connect to left and right LABs through 10 direct link interconnects each. Figure 2–18 shows the M4K RAM block to logic array interface.

Figure 2–17. M4K RAM Block Control Signals

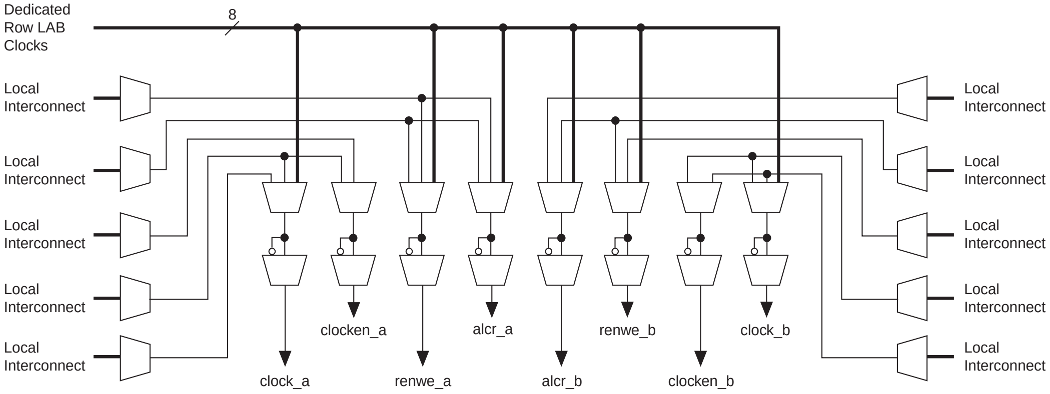
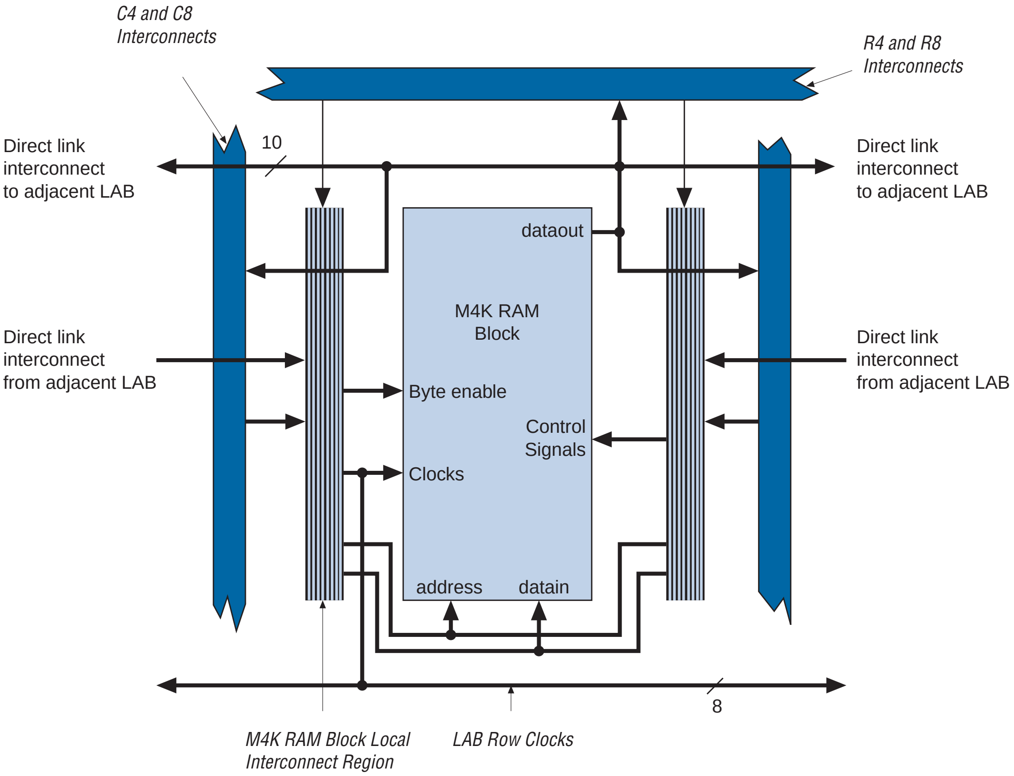


Figure 2–18. M4K RAM Block LAB Row Interface



M-RAM Block

The largest TriMatrix memory block, the M-RAM block, is useful for applications where a large volume of data must be stored on-chip. Each block contains 589,824 RAM bits (including parity bits). The M-RAM block can be configured in the following modes:

- True dual-port RAM
- Simple dual-port RAM
- Single-port RAM
- FIFO RAM

The designer cannot use an initialization file to initialize the contents of a M-RAM block. All M-RAM block contents power up to an undefined value. Only synchronous operation is supported in the M-RAM block, so all inputs are registered. Output registers can be bypassed. The memory address and output width can be configured as 64K ° 8 (or 64K ° 9 bits), 32K ° 16 (or 32K ° 18 bits), 16K ° 32 (or 16K ° 36 bits), 8K ° 64 (or 8K ° 72 bits), and 4K ° 128 (or 4K ° 144 bits). The 4K ° 128 configuration is unavailable in true dual-port mode because there are a total of 144 data output drivers in the block. Mixed-width configurations are also possible, allowing different read and write widths. Tables 2–8 and 2–9 summarizes the possible M-RAM block configurations:

Table 2–8. M-RAM Block Configurations (Simple Dual-Port)

Read Port	**Write Port**				
	64K ° 9	**32K ° 18**	**16K ° 36**	**8K ° 72**	**4K ° 144**
64K ° 9	✓	✓	✓	✓	
32K ° 18	✓	✓	✓	✓	
16K ° 36	✓	✓	✓	✓	
8K ° 72	✓	✓	✓	✓	
4K ° 144					✓

Table 2–9. M-RAM Block Configurations (True Dual-Port)

Port A	Port B			
	64K ° 9	32K ° 18	16K ° 36	8K ° 72
64K ° 9	✓	✓	✓	✓
32K ° 18	✓	✓	✓	✓
16K ° 36	✓	✓	✓	✓
8K ° 72	✓	✓	✓	✓

The read and write operation of the memory is controlled by the `WREN` signal, which sets the ports into either read or write modes. There is no separate read enable (`RE`) signal.

Writing into RAM is controlled by both the `WREN` and byte enable (`byteena`) signals for each port. The default value for the `byteena` signal is high, in which case writing is controlled only by the `WREN` signal. The byte enables are available for the °18, °36, and °72 modes. In the °144 simple dual-port mode, the two sets of `byteena` signals (`byteena_a` and `byteena_b`) are combined to form the necessary 16 byte enables. Tables 2–10 and 2–11 summarize the byte selection.

Table 2–10. Byte Enable for M-RAM Blocks Notes (1), (2)

byteena[3..0]	datain °18	datain °36	datain °72
[0] = 1	[8..0]	[8..0]	[8..0]
[1] = 1	[17..9]	[17..9]	[17..9]
[2] = 1	–	[26..18]	[26..18]
[3] = 1	–	[35..27]	[35..27]
[4] = 1	–	–	[44..36]
[5] = 1	–	–	[53..45]
[6] = 1	–	–	[62..54]
[7] = 1	–	–	[71..63]

Table 2–11. M-RAM Combined Byte Selection for °144 Mode Notes (1), (2)

byteena[15..0]	datain °144
[0] = 1	[8..0]
[1] = 1	[17..9]
[2] = 1	[26..18]
[3] = 1	[35..27]
[4] = 1	[44..36]
[5] = 1	[53..45]
[6] = 1	[62..54]
[7] = 1	[71..63]
[8] = 1	[80..72]
[9] = 1	[89..81]
[10] = 1	[98..90]
[11] = 1	[107..99]
[12] = 1	[116..108]
[13] = 1	[125..117]
[14] = 1	[134..126]
[15] = 1	[143..135]

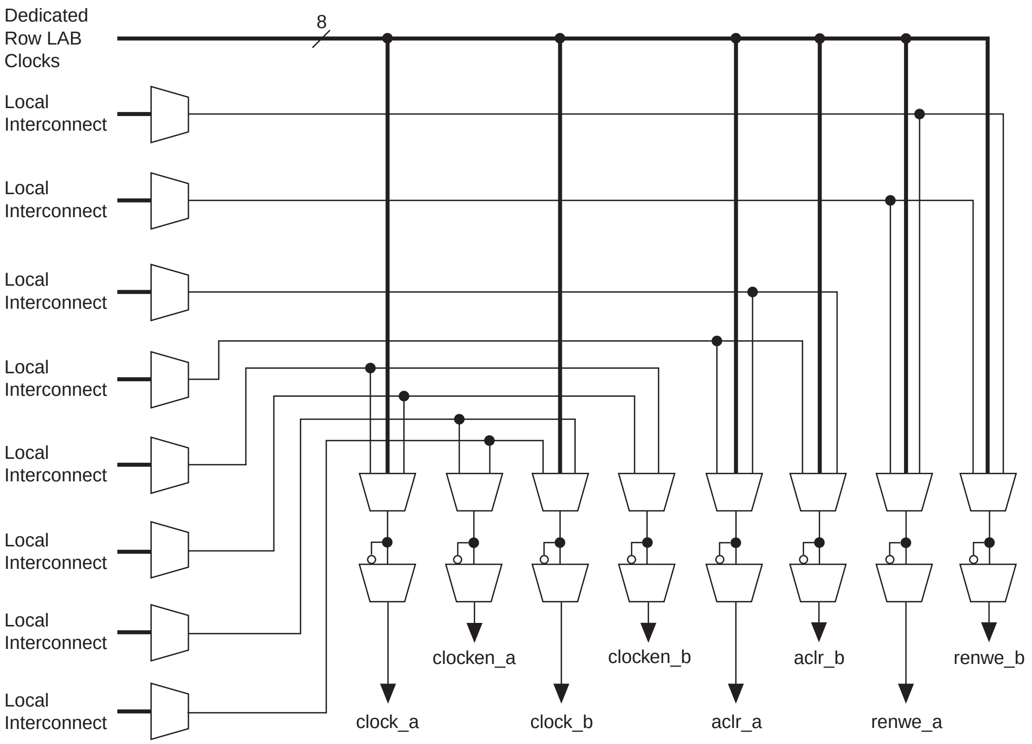
Notes to Tables 2–10 and 2–11:

(1) Any combination of byte enables is possible.

(2) Byte enables can be used in the same manner with 8-bit words, i.e., in ×16, ×32, ×64, and ×128 modes.

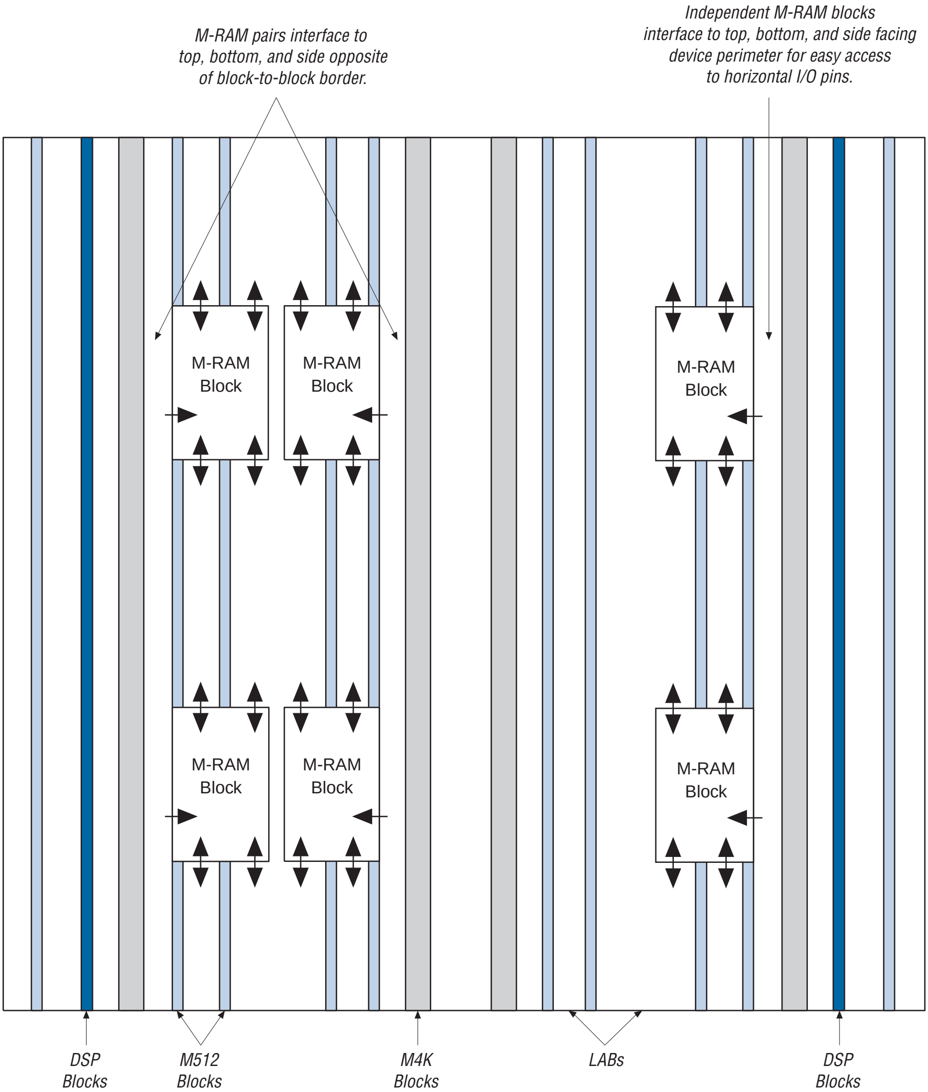
Similar to all RAM blocks, M-RAM blocks can have different clocks on their inputs and outputs. All input registers—`renwe`, `datain`, address, and byte enable registers—are clocked together from either of the two clocks feeding the block. The output register can be bypassed. The eight `labclk` signals or local interconnect can drive the control signals for the A and B ports of the M-RAM block. LEs can also control the `clock_a`, `clock_b`, `renwe_a`, `renwe_b`, `clr_a`, clr_b, `clocken_a`, and `clocken_b` signals as shown in Figure 2–19.

Figure 2–19. M-RAM Block Control Signals



One of the M-RAM block's horizontal sides drive the address and control signal (clock, renwe, byteena, etc.) inputs. Typically, the horizontal side closest to the device perimeter contains the interfaces. The one exception is when two M-RAM blocks are paired next to each other. In this case, the side of the M-RAM block opposite the common side of the two blocks contains the input interface. The top and bottom sides of any M-RAM block contain data input and output interfaces to the logic array. The top side has 72 data inputs and 72 data outputs for port B, and the bottom side has another 72 data inputs and 72 data outputs for port A. Figure 2–20 shows an example floorplan for the EP1S60 device and the location of the M-RAM interfaces.

Figure 2–20. EP1S60 Device with M-RAM Interface Locations Note (1)

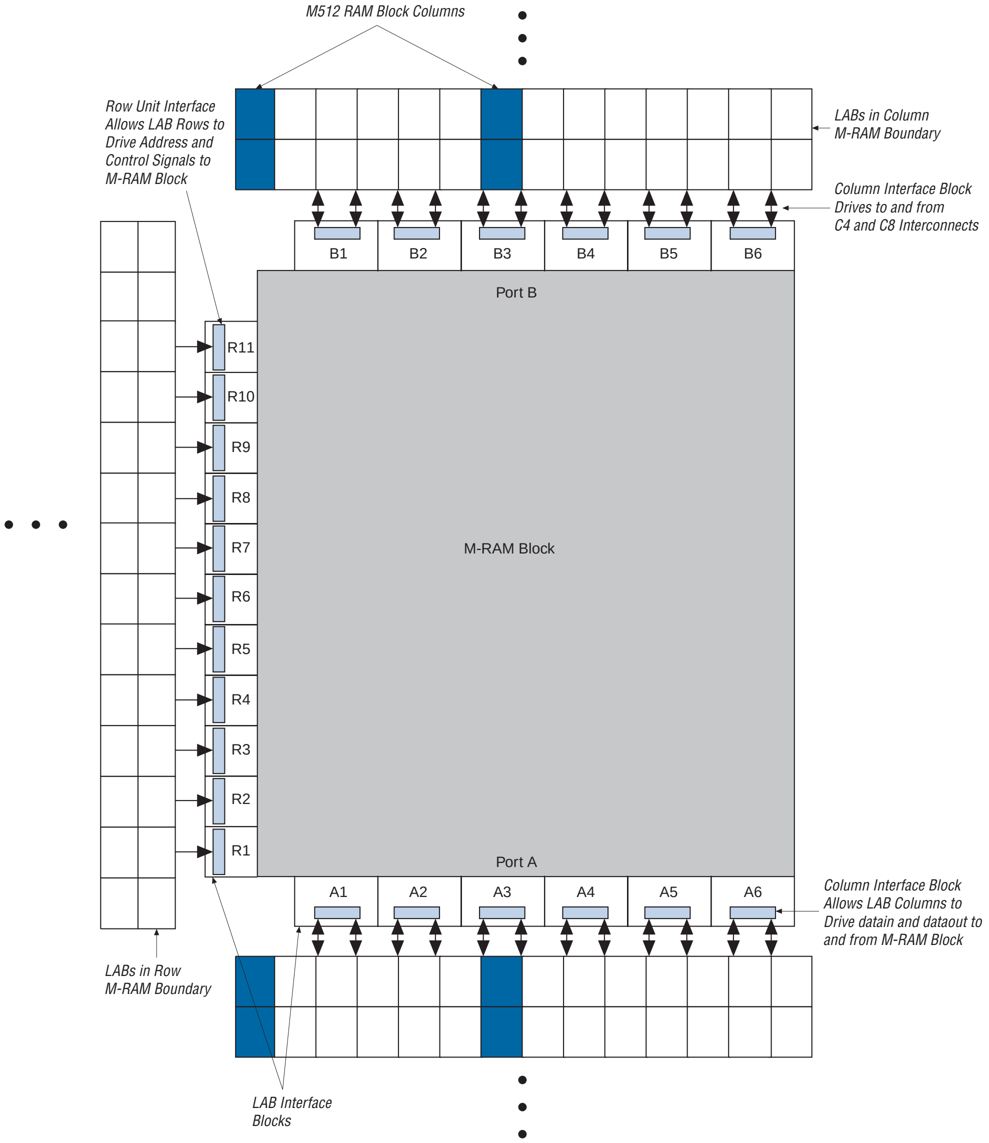


Note to Figure 2–20:

(1) Device shown is an EP1S60 device. The number and position of M-RAM blocks varies in other devices.

The M-RAM block local interconnect is driven by the R4, R8, C4, C8, and direct link interconnects from adjacent LABs. For independent M-RAM blocks, up to 10 direct link address and control signal input connections to the M-RAM block are possible from the left adjacent LABs for M-RAM blocks facing to the left, and another 10 possible from the right adjacent LABs for M-RAM blocks facing to the right. For column interfacing, every M-RAM column unit connects to the right and left column lines, allowing each M-RAM column unit to communicate directly with three columns of LABs. Figures 2–21 through 2–23 show the interface between the M-RAM block and the logic array.

***Figure 2–21. Left-Facing M-RAM to Interconnect Interface** Notes (1), (2)*



Notes to Figure 2–21:

(1) Only R24 and C16 interconnects cross the M-RAM block boundaries.

(2) The right-facing M-RAM block has interface blocks on the right side, but none on the left. B1 to B6 and A1 to A6 orientation is clipped across the vertical axis for right-facing M-RAM blocks.

Figure 2–22. M-RAM Row Unit Interface to Interconnect

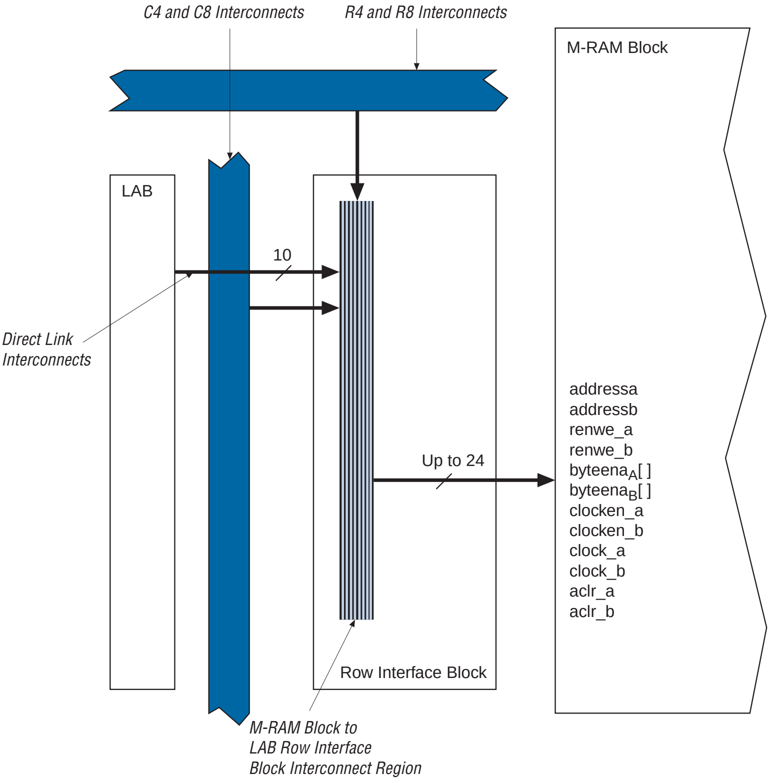


Figure 2–23. M-RAM Column Unit Interface to Interconnect

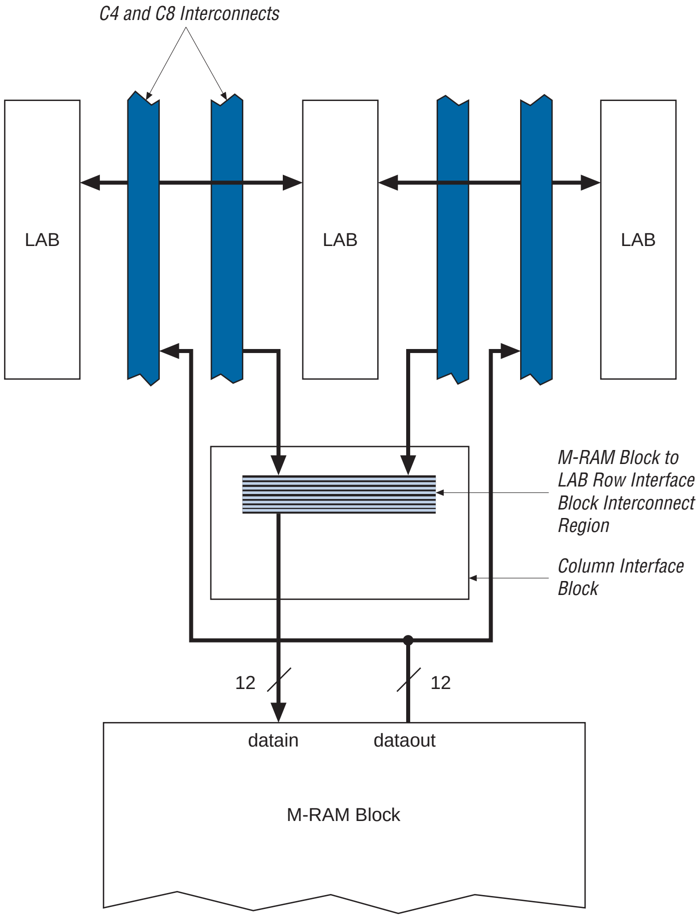


Table 2–12 shows the input and output data signal connections for the column units (B1 to B6 and A1 to A6). It also shows the address and control signal input connections to the row units (R1 to R11).

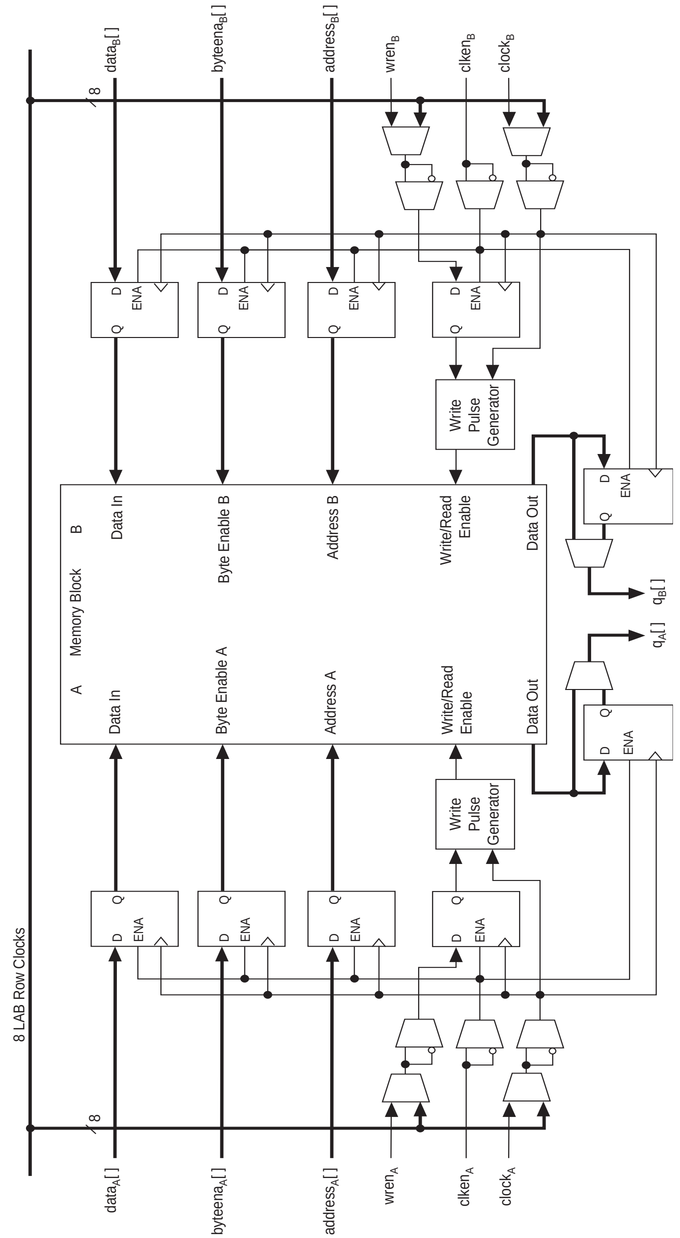
Table 2–12. M-RAM Row & Column Interface Unit Signals

Unit Interface Block	Input SIgnals	Output Signals
R1	addressa[7..0]	
R2	addressa[15..8]	
R3	byte_enable_a[7..0] renwe_a	
R4	-	
R5	-	
R6	clock_a clocken_a clock_b clocken_b	
R7	-	
R8	-	
R9	byte_enable_b[7..0] renwe_b	
R10	addressb[15..8]	
R11	addressb[7..0]	
B1	datain_b[71..60]	dataout_b[71..60]
B2	datain_b[59..48]	dataout_b[59..48]
B3	datain_b[47..36]	dataout_b[47..36]
B4	datain_b[35..24]	dataout_b[35..24]
B5	datain_b[23..12]	dataout_b[23..12]
B6	datain_b[11..0]	dataout_b[11..0]
A1	datain_a[71..60]	dataout_a[71..60]
A2	datain_a[59..48]	dataout_a[59..48]
A3	datain_a[47..36]	dataout_a[47..36]
A4	datain_a[35..24]	dataout_a[35..24]
A5	datain_a[23..12]	dataout_a[23..12]
A6	datain_a[11..0]	dataout_a[11..0]

Independent Clock Mode

The memory blocks implement independent clock mode for true dual-port memory. In this mode, a separate clock is available for each port (ports A and B). Clock A controls all registers on the port A side, while clock B controls all registers on the port B side. Each port, A and B, also supports independent clock enables and asynchronous clear signals for port A and B registers. Figure 2–24 shows a TriMatrix memory block in independent clock mode.

Figure 2–24. Independent Clock Mode *Note (1)*



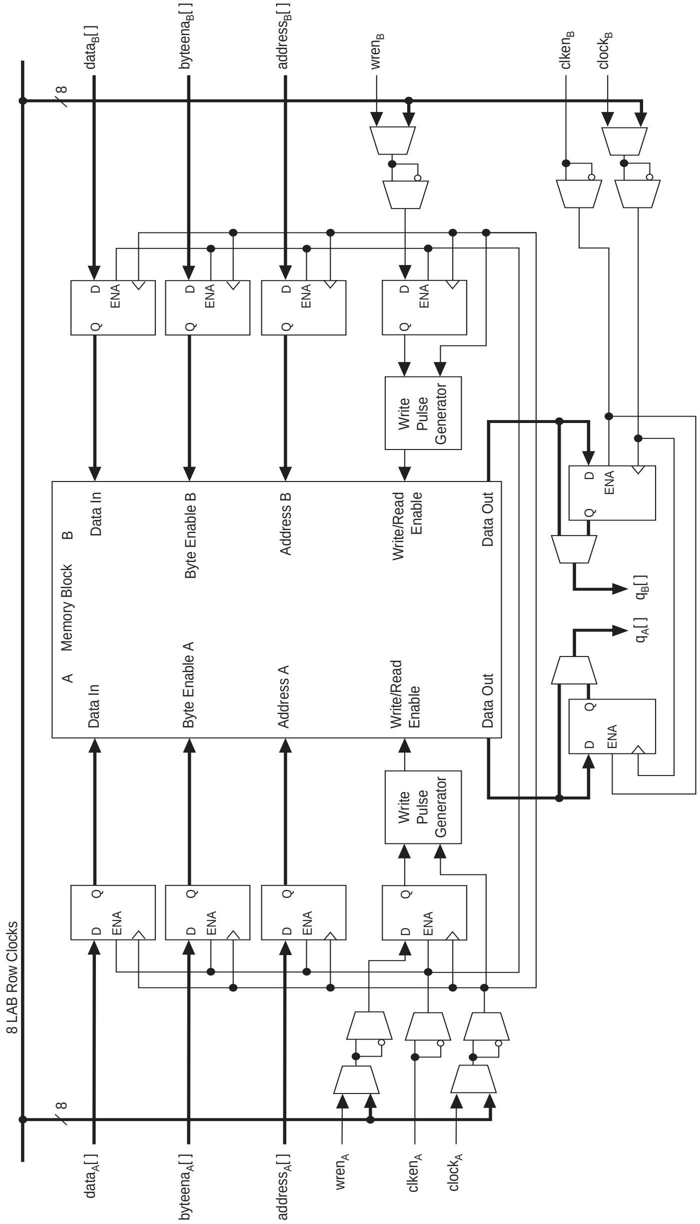
Note to Figure 2–24:

(1) All registers shown have asynchronous clear ports.

Input/Output Clock Mode

Input/output clock mode can be implemented for both the true and simple dual-port memory modes. On each of the two ports, A or B, one clock controls all registers for inputs into the memory block: data input, `wren`, and address. The other clock controls the block's data output registers. Each memory block port, A or B, also supports independent clock enables and asynchronous clear signals for input and output registers. Figures 2–25 and 2–26 show the memory block in input/output clock mode.

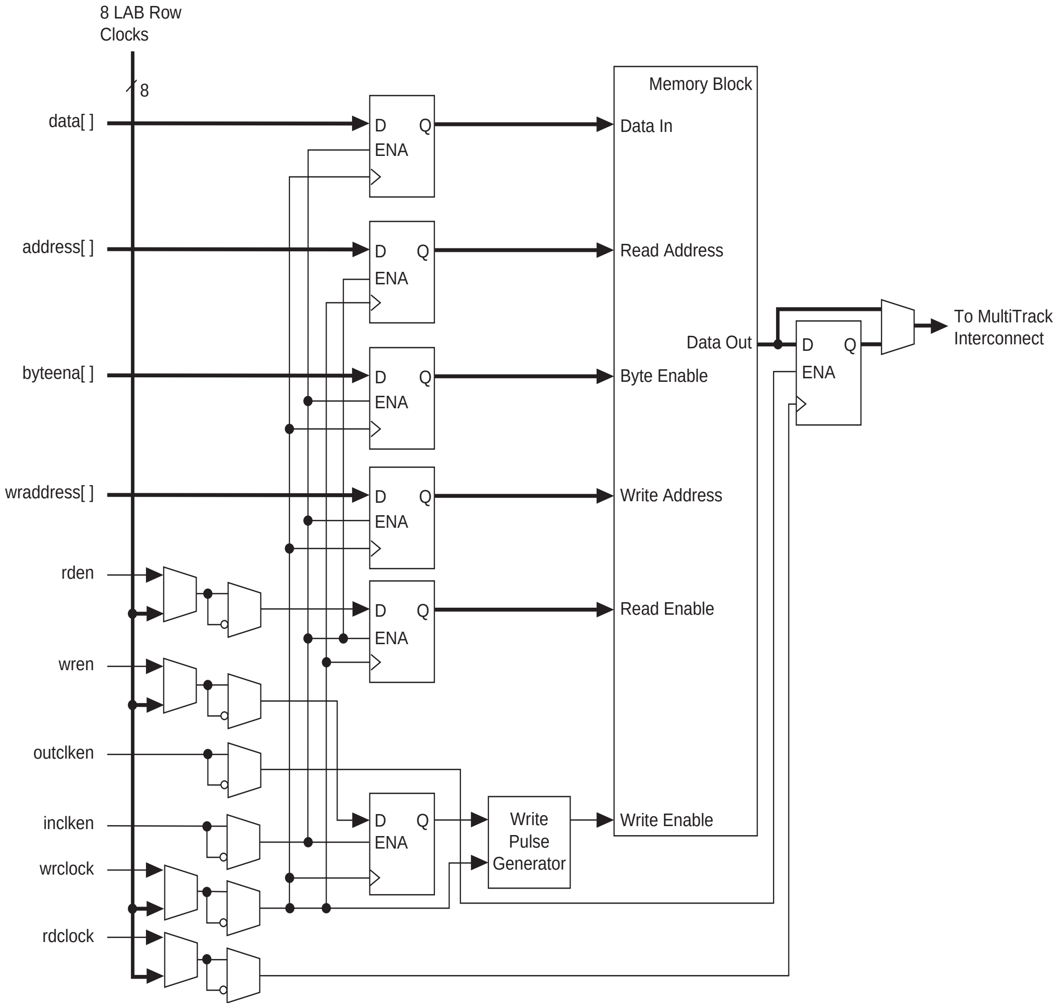
Figure 2–25. Input/Output Clock Mode in True Dual-Port Mode Note (1)



Note to Figure 2–25:

(1) All registers shown have asynchronous clear ports.

Figure 2–26. Input/Output Clock Mode in Simple Dual-Port Mode Note (1)



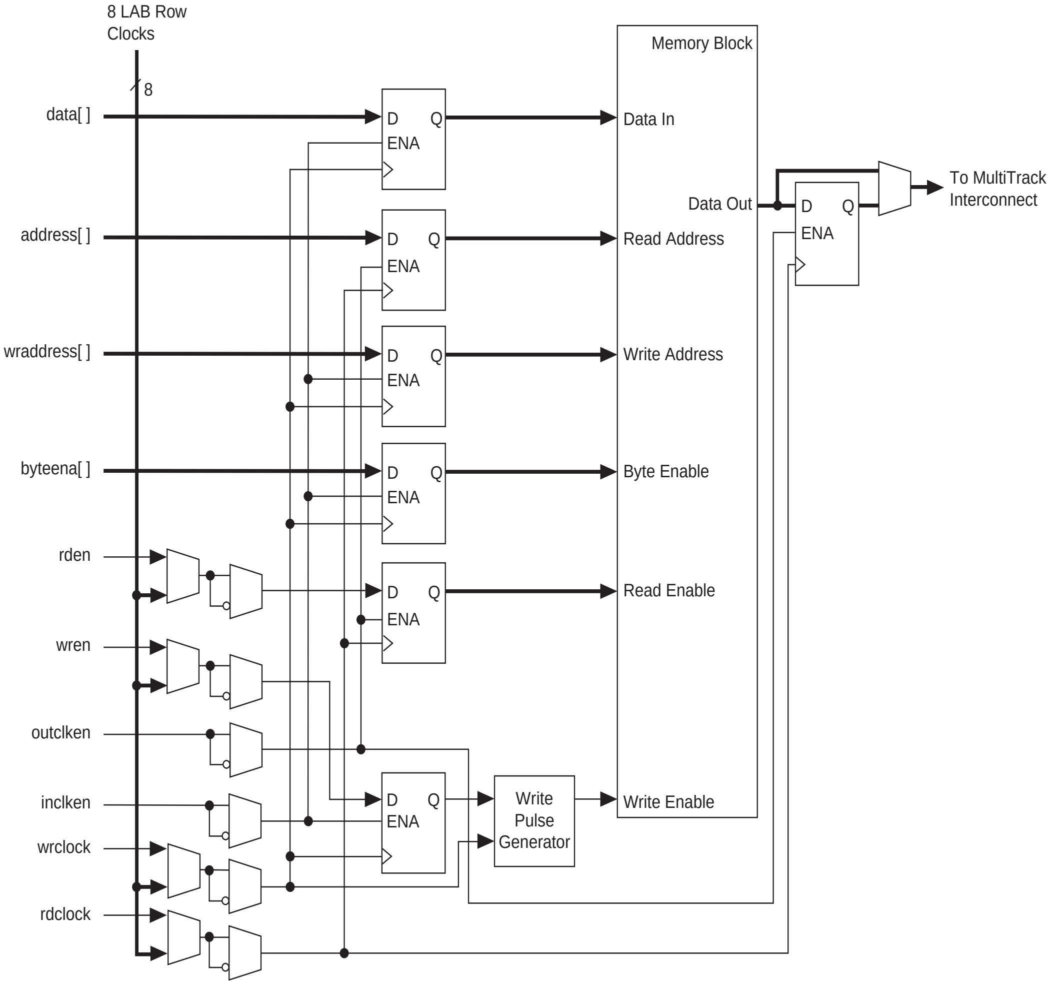
Note to Figure 2–26:

(1) All registers shown except the `rden` register have asynchronous clear ports.

Read/Write Clock Mode

The memory blocks implement read/write clock mode for simple dual-port memory. The designer can use up to two clocks in this mode. The write clock controls the block's data inputs, `wraddress`, and `wren`. The read clock controls the data output, `rdaddress`, and `rden`. The memory blocks support independent clock enables for each clock and asynchronous clear signals for the read- and write-side registers. Figure 2–27 shows a memory block in read/write clock mode.

Figure 2–27. Read/Write Clock Mode in Simple Dual-Port Mode Note (1)



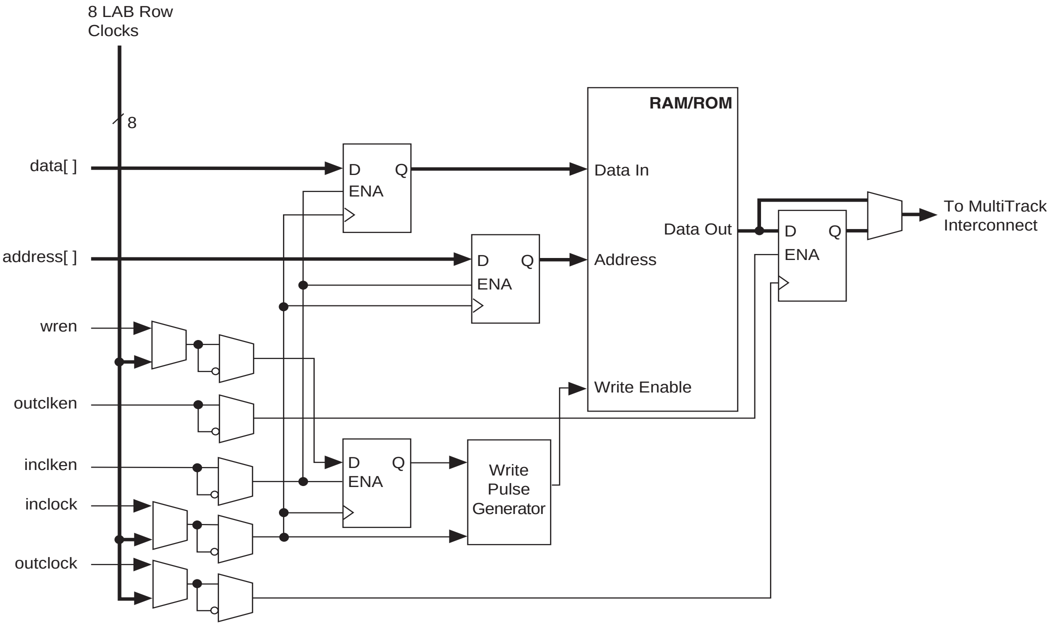
Note to Figure 2–27:

(1) All registers shown except the `rden` register have asynchronous clear ports.

Single-Port Mode

The memory blocks also support single-port mode, used when simultaneous reads and writes are not required. See Figure 2–28. A single block in a memory block can support up to two single-port mode RAM blocks in the M4K RAM blocks if each RAM block is less than or equal to 2K bits in size.

Figure 2–28. Single-Port Mode



Digital Signal Processing Block

The most commonly used DSP functions are finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, direct cosine transform (DCT) functions, and correlators. All of these blocks have the same fundamental building block: the multiplier. Additionally, some applications need specialized operations such as multiply-add and multiply-accumulate operations. Stratix devices provide DSP blocks to meet the arithmetic requirements of these functions.

Each Stratix device has two columns of DSP blocks to efficiently implement DSP functions faster than LE-based implementations. Larger Stratix devices have more DSP blocks per column (see Table 2–13). Each DSP block can be configured to support up to:

- Eight 9 ° 9-bit multipliers
- Four 18 ° 18-bit multipliers
- One 36 ° 36-bit multiplier

As indicated, the Stratix DSP block can support one 36 ° 36-bit multiplier in a single DSP block. This is true for any matched sign multiplications (either unsigned by unsigned or signed by signed), but the capabilities for dynamic and mixed sign multiplications are handled differently. The following list provides the largest functions that can fit into a single DSP block.

- 36 ° 36-bit unsigned by unsigned multiplication
- 36 ° 36-bit signed by signed multiplication
- 35 ° 36-bit unsigned by signed multiplication
- 36 ° 35-bit signed by unsigned multiplication
- 36 ° 35-bit signed by dynamic sign multiplication
- 35 ° 36-bit dynamic sign by signed multiplication
- 35 ° 36-bit unsigned by dynamic sign multiplication
- 36 ° 35-bit dynamic sign by unsigned multiplication
- 35 ° 35-bit dynamic sign multiplication when the sign controls for each operand are different
- 36 ° 36-bit dynamic sign multiplication when the same sign control is used for both operands

This list only shows functions that can fit into a single DSP block. Multiple DSP blocks can support larger multiplication functions.

Figure 2–29 shows one of the columns with surrounding LAB rows.

Figure 2–29. DSP Blocks Arranged in Columns

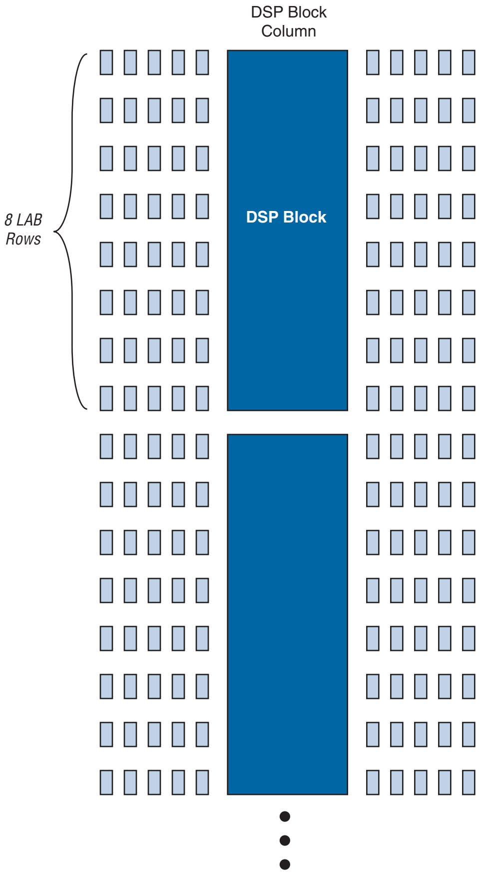


Table 2–13 shows the number of DSP blocks in each Stratix device.

***Table 2–13. DSP Blocks in Stratix Devices** Notes (1), (2)*

Device	DSP Blocks	Total 9 ° 9 Multipliers	Total 18 ° 18 Multipliers	Total 36 ° 36 Multipliers
EP1S10	6	48	24	6
EP1S20	10	80	40	10
EP1S25	10	80	40	10
EP1S30	12	96	48	12
EP1S40	14	112	56	14
EP1S60	18	144	72	18
EP1S80	22	176	88	22

Notes to Table 2–13:

(1) Each device has either the number of 9 × 9-, 18 × 18-, or 36 × 36-bit multipliers shown. The total number of multipliers for each device is not the sum of all the multipliers.

(2) The number of supported multiply functions shown is based on signed/signed or unsigned/unsigned implementations.

DSP block multipliers can optionally feed an adder/subtractor or accumulator within the block depending on the configuration. This makes routing to LEs easier, saves LE routing resources, and increases performance, because all connections and blocks are within the DSP block. Additionally, the DSP block input registers can efficiently implement shift registers for FIR filter applications.

Figure 2–30 shows the top-level diagram of the DSP block configured for 18 ° 18-bit multiplier mode. Figure 2–31 shows the 9 ° 9-bit multiplier configuration of the DSP block.

Figure 2–30. DSP Block Diagram for 18 ° 18-Bit Configuration

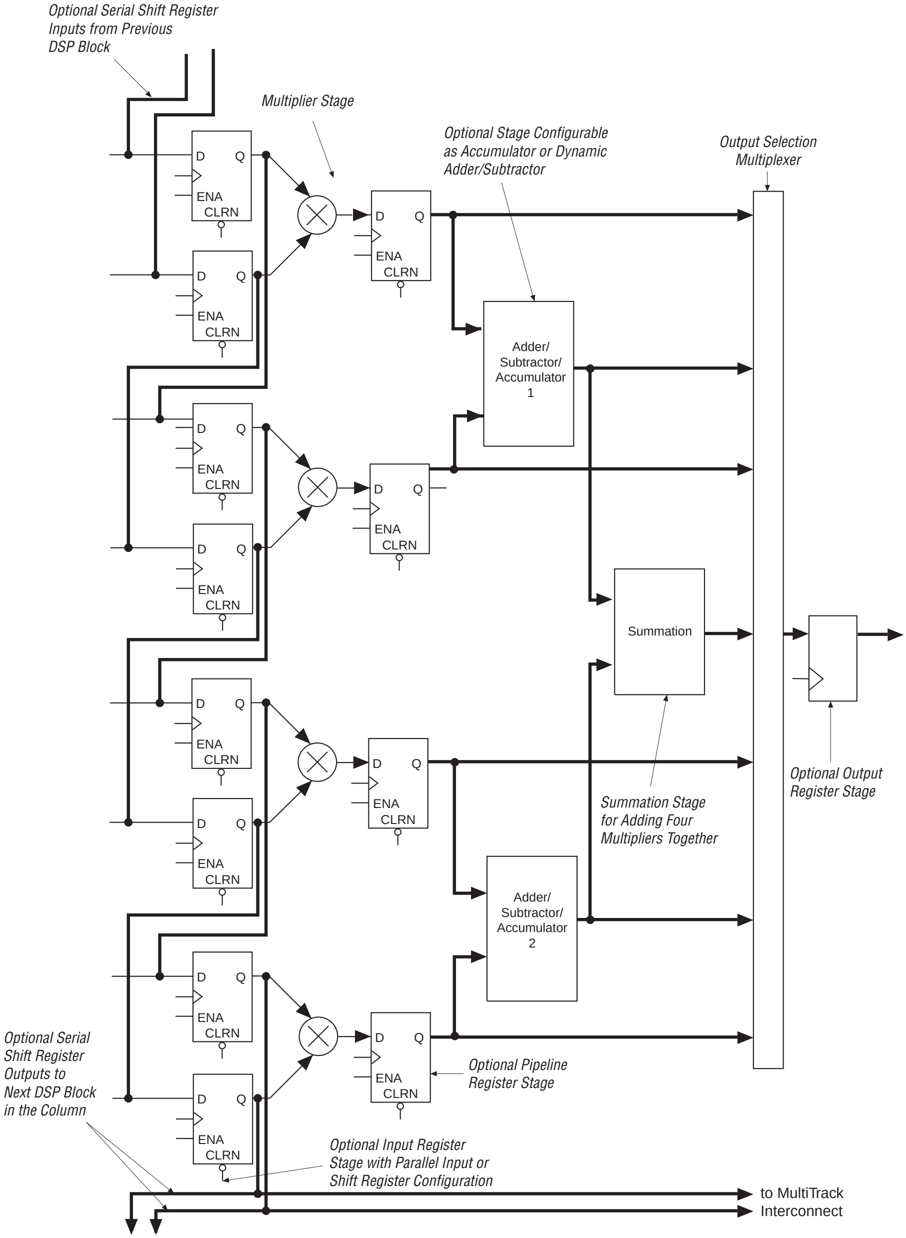
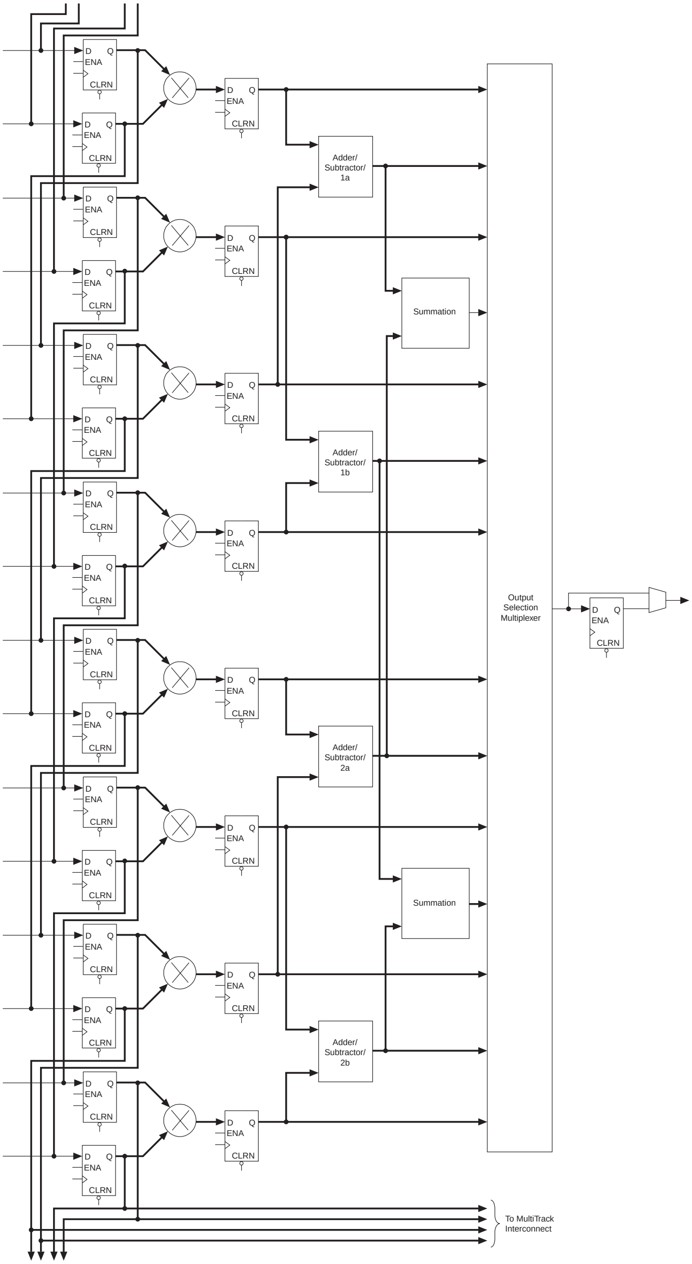


Figure 2–31. DSP Block Diagram for 9 ° 9-Bit Configuration



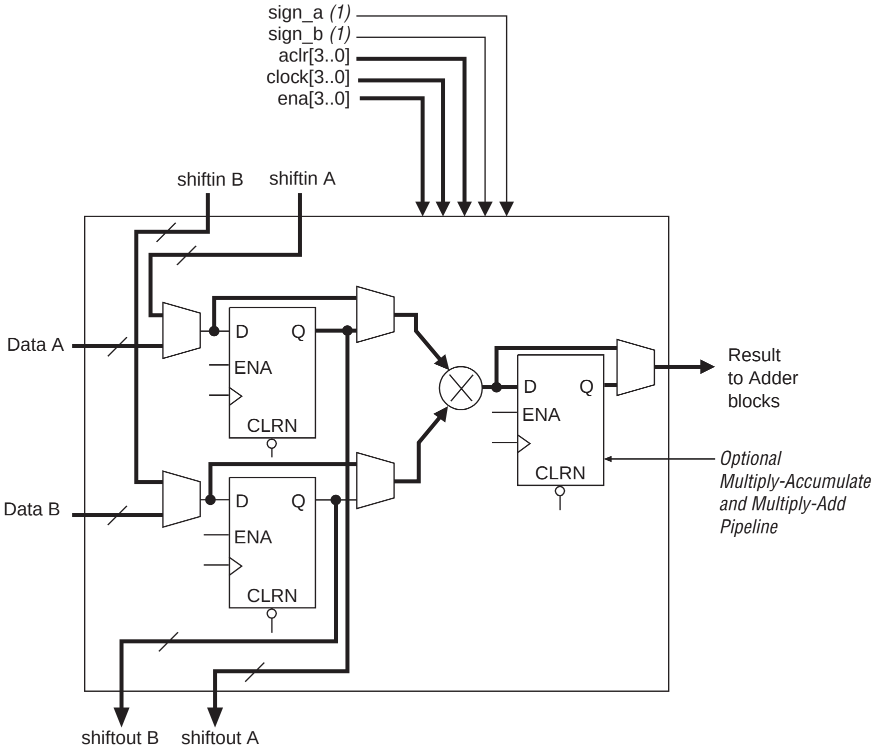
The DSP block consists of the following elements:

- Multiplier block
- Adder/output block

Multiplier Block

The DSP block multiplier block consists of the input registers, a multiplier, and pipeline register for pipelining multiply-accumulate and multiply-add/subtract functions as shown in Figure 2–32.

Figure 2–32. Multiplier Sub-Block within Stratix DSP Block



Note to Figure 2–32:

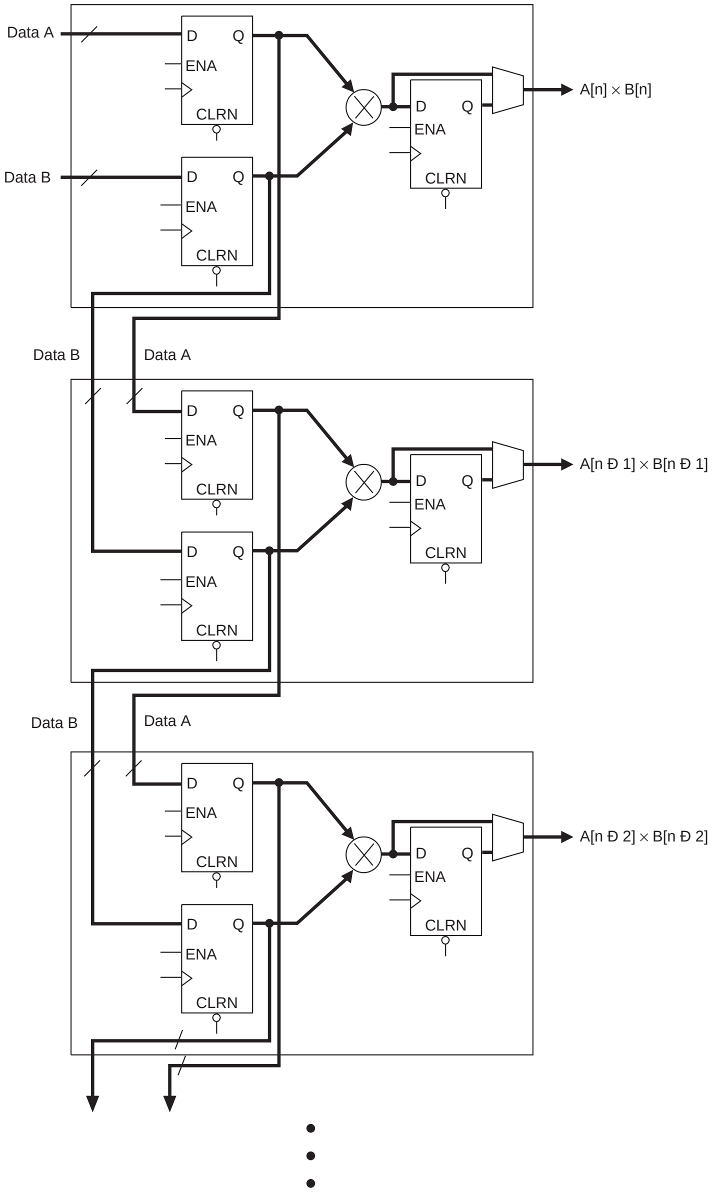
(1) These signals can be unregistered or registered once to match data path pipelines if required.

Input Registers

A bank of optional input registers is located at the input of each multiplier and multiplicand inputs to the multiplier. When these registers are configured for parallel data inputs, they are driven by regular routing resources. Designers can use a clock signal, asynchronous clear signal, and a clock enable signal to independently control each set of A and B inputs for each multiplier in the DSP block. Designers select these control signals from a set of four different `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]` signals that drive the entire DSP block.

Designers can also configure the input registers for a shift register application. In this case, the input registers feed the multiplier and drive two dedicated shift output lines: `shiftoutA` and `shiftoutB`. The shift outputs of one multiplier block directly feed the adjacent multiplier block in the same DSP block (or the next DSP block) as shown in Figure 2–33, to form a shift register chain. This chain can terminate in any block, i.e., designers can create any length of shift register chain up to 224 registers. The designer can use the input shift registers for FIR filter applications. One set of shift inputs can provide data for a filter, and the other are coefficients that are optionally loaded in serial or parallel. When implementing 9 ° 9- and 18 ° 18-bit multipliers, the designer does not need to implement external shift registers in LAB LEs. The designer implements all the filter circuitry within the DSP block and its routing resources, saving LE and general routing resources for general logic. External registers are needed for shift register inputs when using 36 ° 36-bit multipliers.

Figure 2–33. Multiplier Sub-Blocks Using Input Shift Register Connections *Note (1)*



Note to Figure 2–33:

(1) Either Data A or Data B input can be set to a parallel input for constant coefficient multiplication.

Table 2–14 shows the summary of input register modes for the DSP block.

Table 2–14. Input Register Modes

Register Input Mode	9 ° 9	18 ° 18	36 ° 36
Parallel input	✓	✓	✓
Shift register input	✓	✓	

Multiplier

The multiplier supports 9 ° 9-, 18 ° 18-, or 36 ° 36-bit multiplication. Each DSP block supports eight possible 9 ° 9-bit or smaller multipliers. There are four multiplier blocks available for multipliers larger than 9 ° 9 bits but smaller than 18 ° 18 bits. There is one multiplier block available for multipliers larger than 18 ° 18 bits but smaller than or equal to 36 ° 36 bits. The ability to have several small multipliers is useful in applications such as video processing. Large multipliers greater than 18 ° 18 bits are useful for applications such as the mantissa multiplication of a single-precision floating-point number.

The multiplier operands can be signed or unsigned numbers, where the result is signed if either input is signed as shown in Table 2–15. The `sign_a` and `sign_b` signals provide dynamic control of each operand's representation: a logic 1 indicates the operand is a signed number, a logic 0 indicates the operand is an unsigned number. These sign signals affect all multipliers and adders within a single DSP block and designers can register them to match the data path pipeline. The multipliers are full precision (i.e., 18 bits for the 18-bit multiply, 36-bits for the 36-bit multiply, etc.) regardless of whether `sign_a` or `sign_b` set the operands as signed or unsigned numbers.

Table 2–15. Multiplier Signed Representation

Data A	Data B	Result
Unsigned	Unsigned	Unsigned
Unsigned	Signed	Signed
Signed	Unsigned	Signed
Signed	Signed	Signed

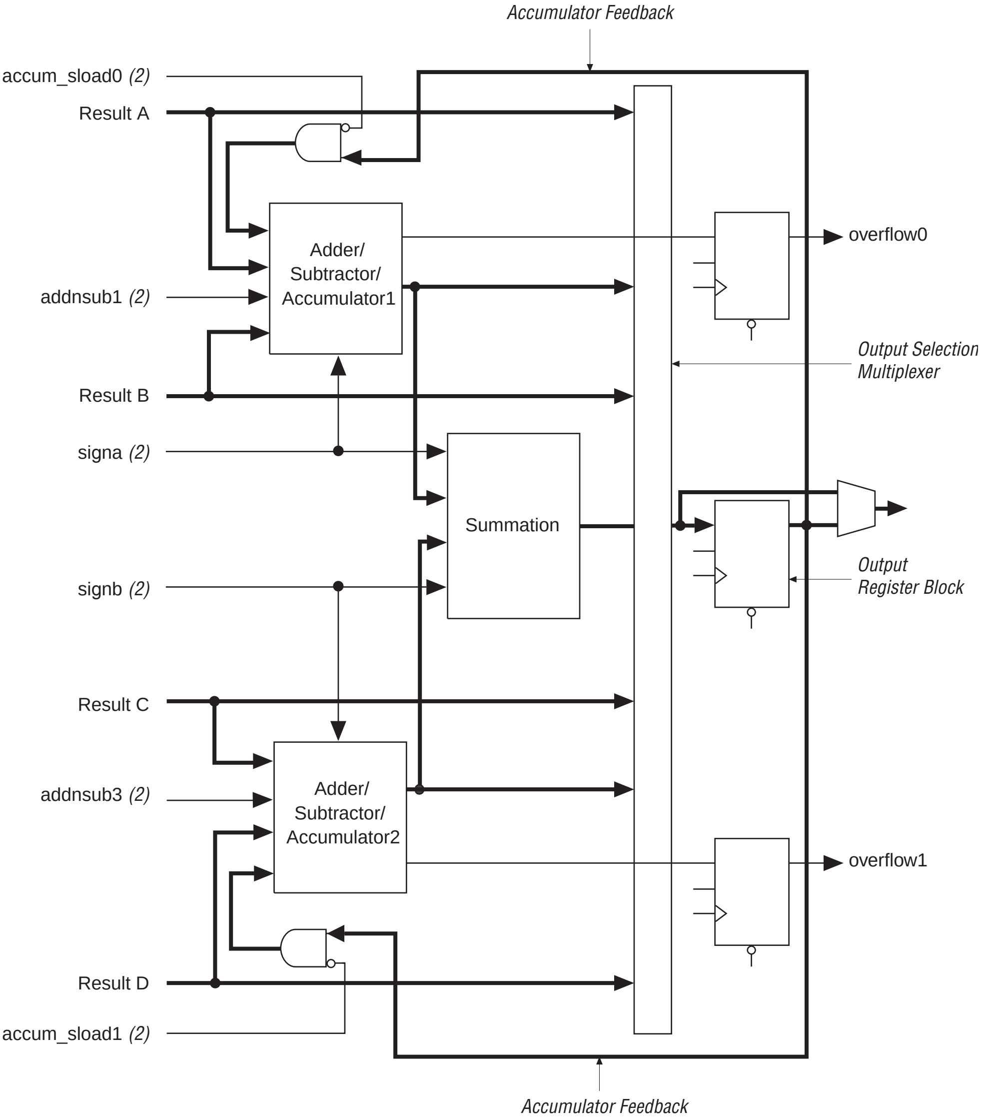
Pipeline/Post Multiply Register

The output of 9 ° 9- or 18 ° 18-bit multipliers can optionally feed a register to pipeline multiply-accumulate and multiply-add/subtract functions. For 36 ° 36-bit multipliers, this register will pipeline the multiplier function.

Adder/Output Blocks

The result of the multiplier sub-blocks are sent to the adder/output block which consist of an adder/subtractor/accumulator unit, summation unit, output select multiplexer, and output registers. The results are used to configure the adder/output block as a pure output, accumulator, a simple two-multiplier adder, four-multiplier adder, or final stage of the 36-bit multiplier. The designer can configure the adder/output block to use output registers in any mode, and must use output registers for the accumulator. The system cannot use adder/output blocks independently of the multiplier. Figure 2–34 shows the adder and output stages.

Figure 2–34. Adder/Output Blocks Note (1)



Notes to Figure 2–34:

(1) Adder/output block shown in Figure 2–34 is in 18 × 18-bit mode. In 9 × 9-bit mode, there are four adder/subtractor blocks and two summation blocks.

(2) These signals are either not registered, registered once, or registered twice to match the data path pipeline.

Adder/Subtractor/Accumulator

The adder/subtractor/accumulator is the first level of the adder/output block and can be used as an accumulator or as an adder/subtractor.

Adder/Subtractor

Each adder/subtractor/accumulator block can perform addition or subtraction using the `addnsub` independent control signal for each first-level adder in 18 ° 18-bit mode. There are two `addnsub[1..0]` signals available in a DSP block for any configuration. For 9 ° 9-bit mode, one `addnsub[1..0]` signal controls the top two one-level adders and another `addnsub[1..0]` signal controls the bottom two one-level adders. A high `addnsub` signal indicates addition, and a low signal indicates subtraction. The `addnsub` control signal can be unregistered or registered once or twice when feeding the adder blocks to match data path pipelines.

The `signa` and `signb` signals serve the same function as the multiplier block `signa` and `signb` signals. The only difference is that these signals can be registered up to two times. These signals are tied to the same `signa` and `signb` signals from the multiplier and must be connected to the same clocks and control signals.

Accumulator

When configured for accumulation, the adder/output block output feeds back to the accumulator as shown in Figure 2–34. The `accum_sload[1..0]` signal synchronously loads the multiplier result to the accumulator output. This signal can be unregistered or registered once or twice. Additionally, the `overflow` signal indicates the accumulator has overflowed or underflowed in accumulation mode. This signal is always registered and must be externally latched in LEs if the design requires a latched `overflow` signal.

Summation

The output of the adder/subtractor/accumulator block feeds to an optional summation block. This block sums the outputs of the DSP block multipliers. In 9 ° 9-bit mode, there are two summation blocks providing the sums of two sets of four 9 ° 9-bit multipliers. In 18 ° 18-bit mode, there is one summation providing the sum of one set of four 18 ° 18-bit multipliers.

Output Selection Multiplexer

The outputs from the various elements of the adder/output block are routed through an output selection multiplexer. Based on the DSP block operational mode and user settings, the multiplexer selects whether the output from the multiplier, the adder/subtractor/accumulator, or summation block feeds to the output.

Output Registers

Optional output registers for the DSP block outputs are controlled by four sets of control signals: `clock[3..0]`, `aclr[3..0]`, and `ena[3..0]`. Output registers can be used in any mode.

Modes of Operation

The adder, subtractor, and accumulate functions of a DSP block have four modes of operation:

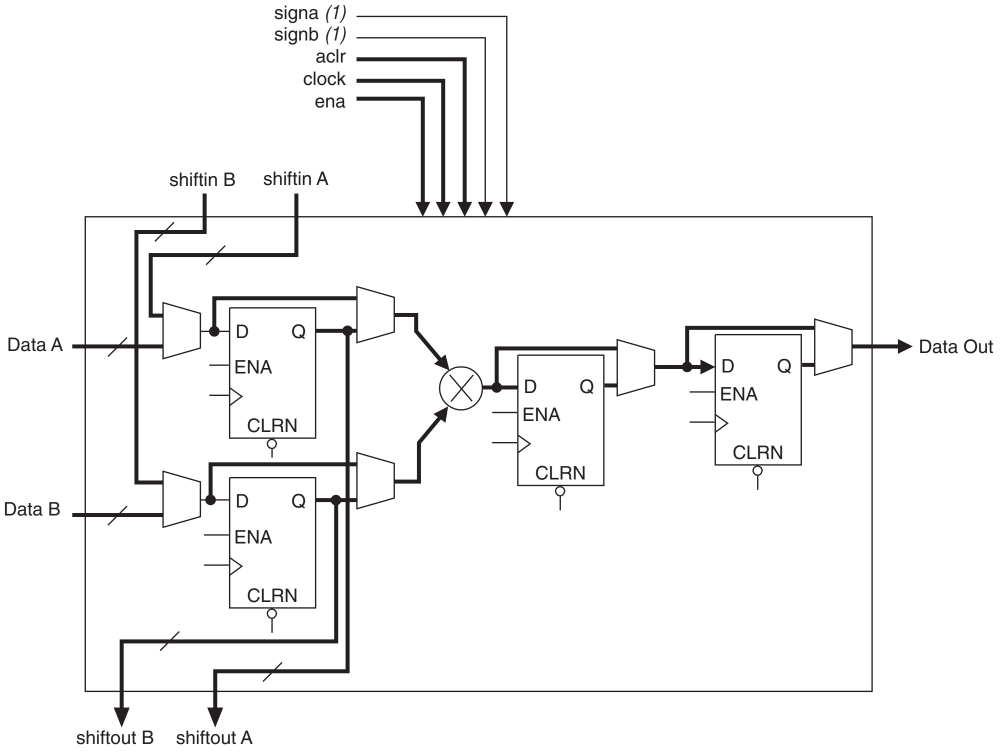
- Simple multiplier
- Multiply-accumulator
- Two-multipliers adder
- Four-multipliers adder

☞ Each DSP block can only support one mode. Mixed modes in the same DSP block is not supported.

Simple Multiplier Mode

In simple multiplier mode, the DSP block drives the multiplier sub-block result directly to the output with or without an output register. Up to four 18 ° 18-bit multipliers or eight 9 ° 9-bit multipliers can drive their results directly out of one DSP block. See Figure 2–35.

Figure 2–35. Simple Multiplier Mode

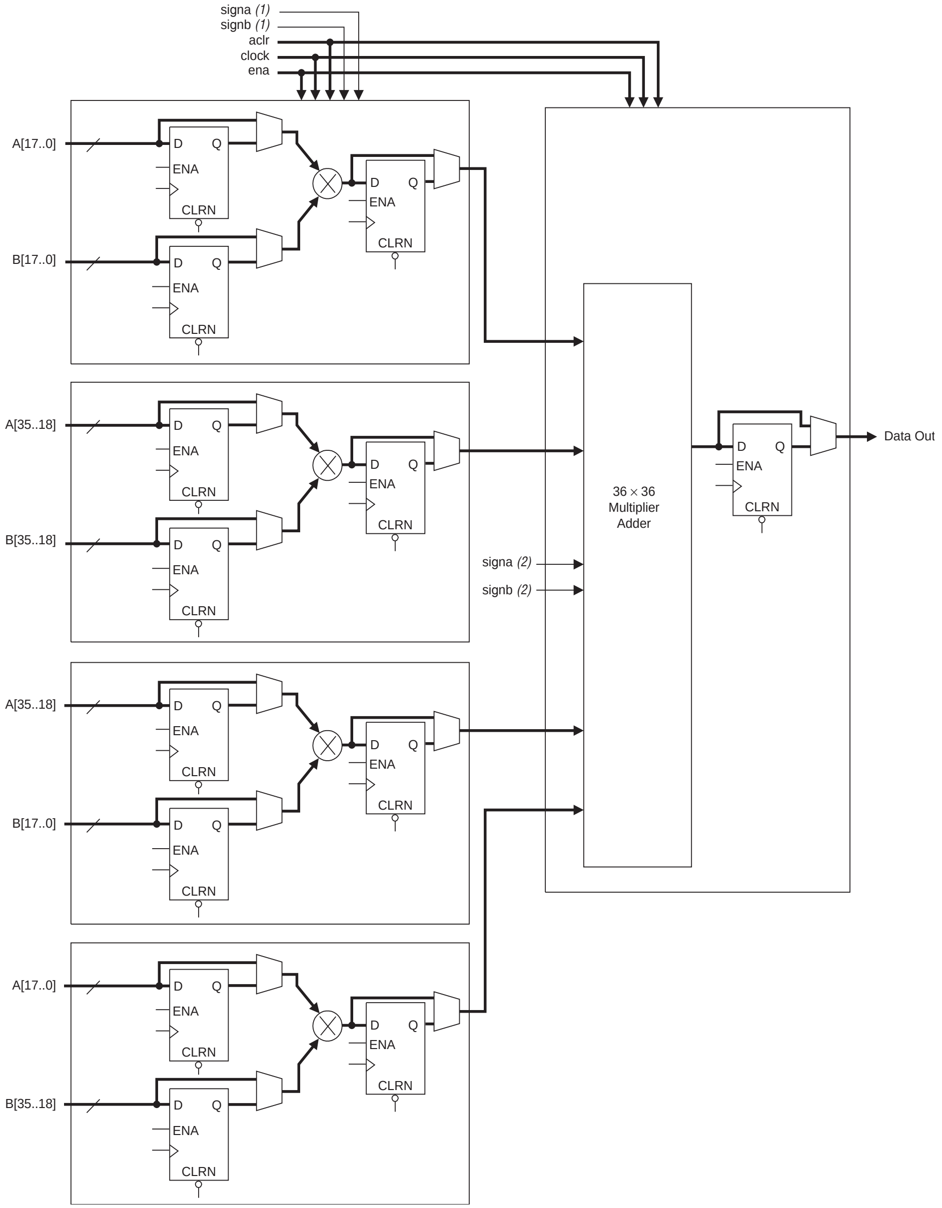


Note to Figure 2–35:

(1) These signals are not registered or registered once to match the data path pipeline.

DSP blocks can also implement one 36 ° 36-bit multiplier in multiplier mode. DSP blocks use four 18 ° 18-bit multipliers combined with dedicated adder and internal shift circuitry to achieve 36-bit multiplication. The input shift register feature is not available for the 36 ° 36-bit multiplier. In 36 ° 36-bit mode, the device can use the register that is normally a multiplier-result-output register as a pipeline stage for the 36 ° 36-bit multiplier. Figure 2–36 shows the 36 ° 36-bit multiply mode.

Figure 2–36. 36 ° 36 Multiply Mode



Notes to Figure 2–36:

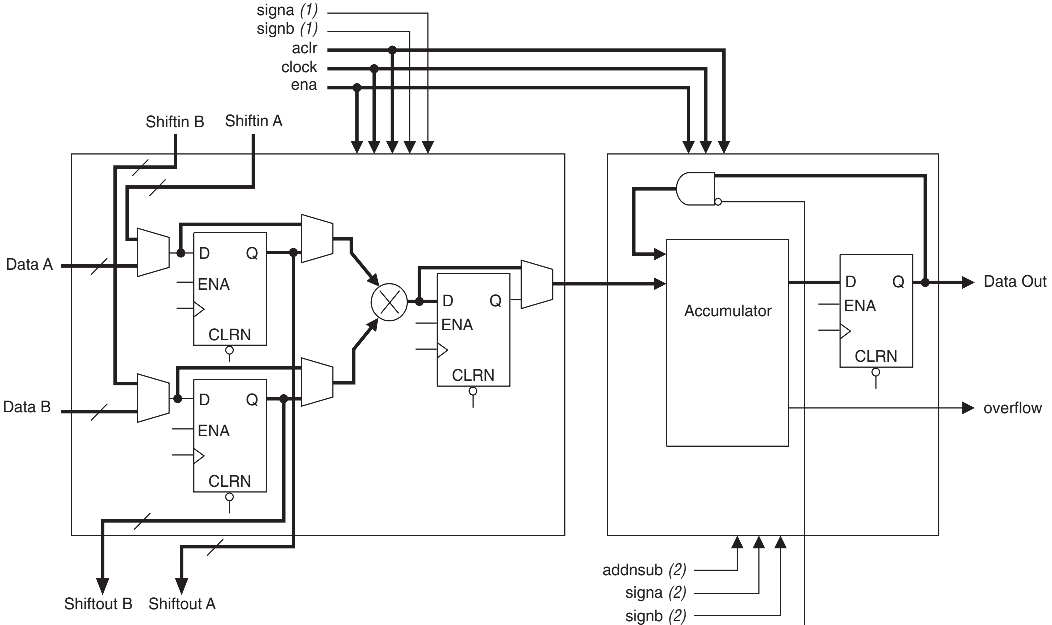
(1) These signals are not registered or registered once to match the pipeline.

(2) These signals are not registered, registered once, or registered twice for latency to match the pipeline.

Multiply-Accumulator Mode

In multiply-accumulator mode (see Figure 2–37), the DSP block drives multiplied results to the adder/subtractor/accumulator block configured as an accumulator. A designer can implement one or two multiply-accumulators up to 18 ° 18 bits in one DSP block. The first and third multiplier sub-blocks are unused in this mode, since only one multiplier can feed one of two accumulators. The multiply-accumulator output can be up to 52 bits—a maximum of a 36-bit result with 16 bits of accumulation. The `accum_sload` and `overflow` signals are only available in this mode. The `addnsub` signal can set the accumulator for decimation and the `overflow` signal will indicate underflow condition.

Figure 2–37. Multiply-Accumulate Mode



Notes to Figure 2–37:

(1) These signals are not registered or registered once to match the data path pipeline.

(2) These signals are not registered, registered once, or registered twice for latency to match the data path pipeline.

Two-Multipliers Adder Mode

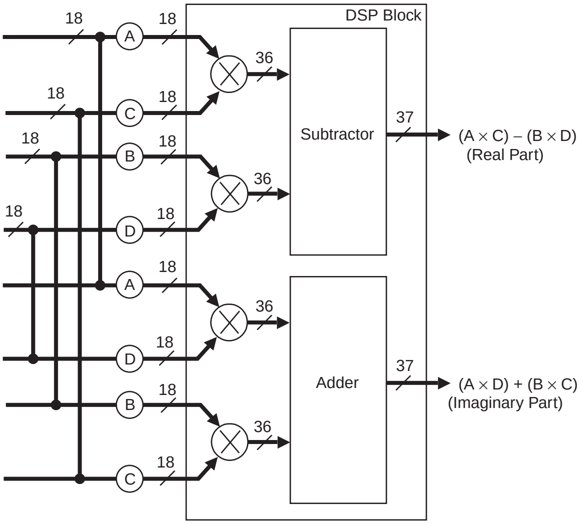
The two-multipliers adder mode uses the adder/subtractor/accumulator block to add or subtract the outputs of the multiplier block, which is useful for applications such as FFT functions and complex FIR filters. A single DSP block can implement two sums or differences from two 18 ° 18-bit multipliers each or four sums or differences from two 9 ° 9-bit multipliers each.

Designers can use the two-multipliers adder mode for complex multiplications, which are written as:

(a + jb) ° (c + jd) = [(a ° c) – (b ° d)] + j ° [(a ° d) + (b ° c)]

The two-multipliers adder mode allows a single DSP block to calculate the real part [(a ° c) – (b ° d)] using one subtractor and the imaginary part [(a ° d) + (b ° c)] using one adder, for data widths up to 18 bits. Two complex multiplications are possible for data widths up to 9 bits using four adder/subtractor/accumulator blocks. Figure 2–38 shows an 18-bit two-multipliers adder.

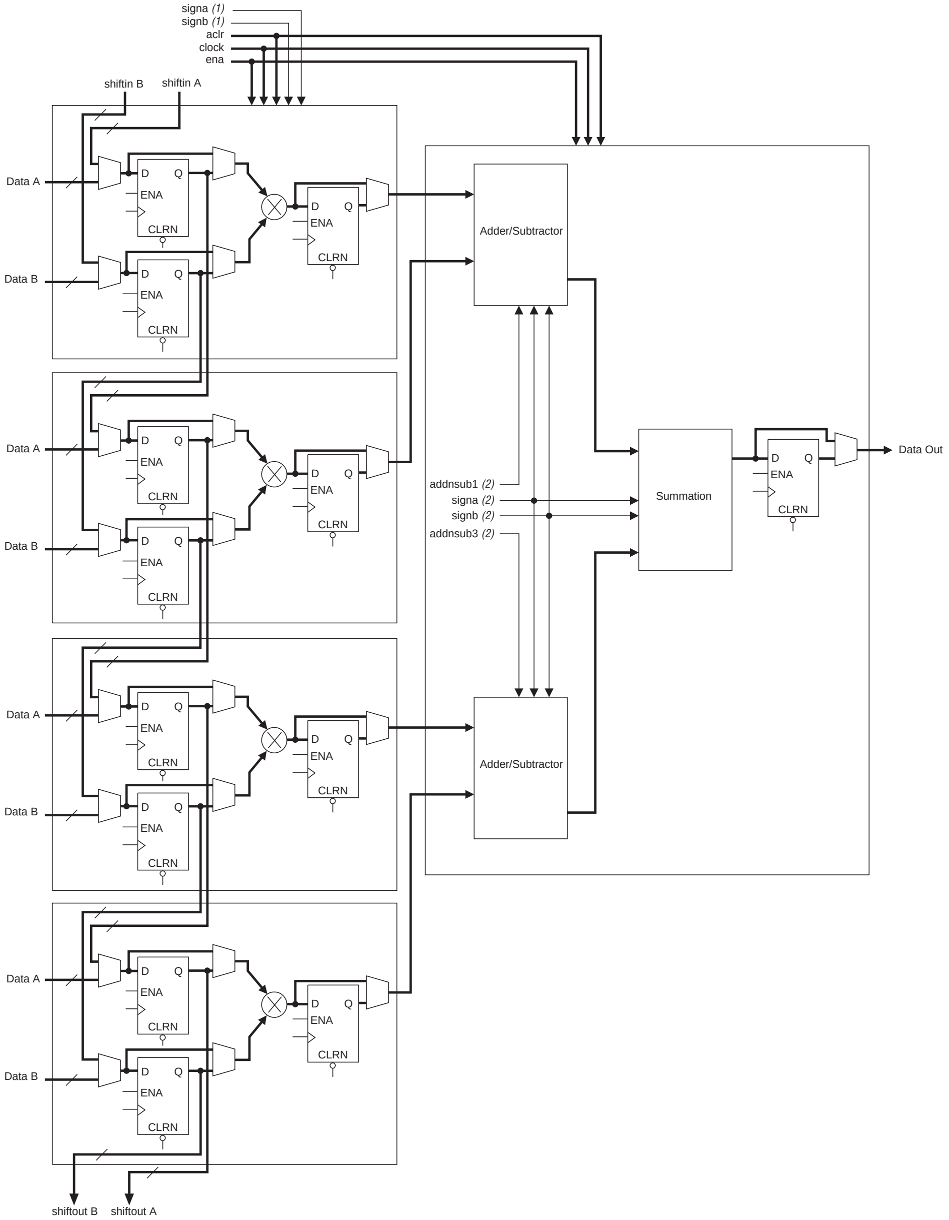
Figure 2–38. Two-Multipliers Adder Mode Implementing Complex Multiply



Four-Multipliers Adder Mode

In the four-multipliers adder mode, the DSP block adds the results of two first -stage adder/subtractor blocks. One sum of four 18 ° 18-bit multipliers or two different sums of two sets of four 9 ° 9-bit multipliers can be implemented in a single DSP block. The product width for each multiplier must be the same size. The four-multipliers adder mode is useful for FIR filter applications. Figure 2–39 shows the four multipliers adder mode.

Figure 2–39. Four-Multipliers Adder Mode



Notes to Figure 2–39:

(1) These signals are not registered or registered once to match the data path pipeline.

(2) These signals are not registered, registered once, or registered twice for latency to match the data path pipeline.

For FIR filters, the DSP block combines the four-multipliers adder mode with the shift register inputs. One set of shift inputs contains the filter data, while the other holds the coefficients loaded in serial or parallel. The input shift register eliminates the need for shift registers external to the DSP block (i.e., implemented in LEs). This architecture simplifies filter design since the DSP block implements all of the filter circuitry.

One DSP block can implement an entire 18-bit FIR filter with up to four taps. For FIR filters larger than four taps, DSP blocks can be cascaded with additional adder stages implemented in LEs.

Table 2–16 shows the different number of multipliers possible in each DSP block mode according to size. These modes allow the DSP blocks to implement numerous applications for DSP including FFTs, complex FIR, FIR, and 2D FIR filters, equalizers, IIR, correlators, matrix multiplication and many other functions.

Table 2–16. Multiplier Size & Configurations per DSP block

DSP Block Mode	9 ° 9	18 ° 18	36 ° 36 *(1)*
Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier with one product output
Multiply-accumulator	Two multiply and accumulate (52 bits)	Two multiply and accumulate (52 bits)	–
Two-multipliers adder	Four sums of two multiplier products each	Two sums of two multiplier products each	–
Four-multipliers adder	Two sums of four multiplier products each	One sum of four multiplier products each	–

Note to Table 2–16:

(1) The number of supported multiply functions shown is based on signed/signed or unsigned/unsigned implementations.

DSP Block Interface

Stratix device DSP block outputs can cascade down within the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. The designer can cascade DSP blocks for 9 ° 9- or 18 ° 18-bit FIR filters larger than four taps, with additional adder stages implemented in LEs. If the DSP block is configured as 36 ° 36 bits, the adder, subtractor, or accumulator stages are implemented in LEs. Each DSP block can route the shift register chain out of the block to cascade two full columns of DSP blocks.

The DSP block is divided into eight block units that interface with eight LAB rows on the left and right. Each block unit can be considered half of an 18 ° 18-bit multiplier sub-block with 18 inputs and 18 outputs. A local interconnect region is associated with each DSP block. Like an LAB, this interconnect region can be fed with 10 direct link interconnects from the LAB to the left or right of the DSP block in the same row. All row and column routing resources can access the DSP block's local interconnect region. The outputs also work similarly to LAB outputs as well. Nine outputs from the DSP block can drive to the left LAB through direct link interconnects and nine can drive to the right LAB though direct link interconnects. All 18 outputs can drive to all types of row and column routing. Outputs can drive right- or left-column routing. Figures 2–40 and 2–41 show the DSP block interfaces to LAB rows.

Figure 2–40. DSP Block Interconnect Interface

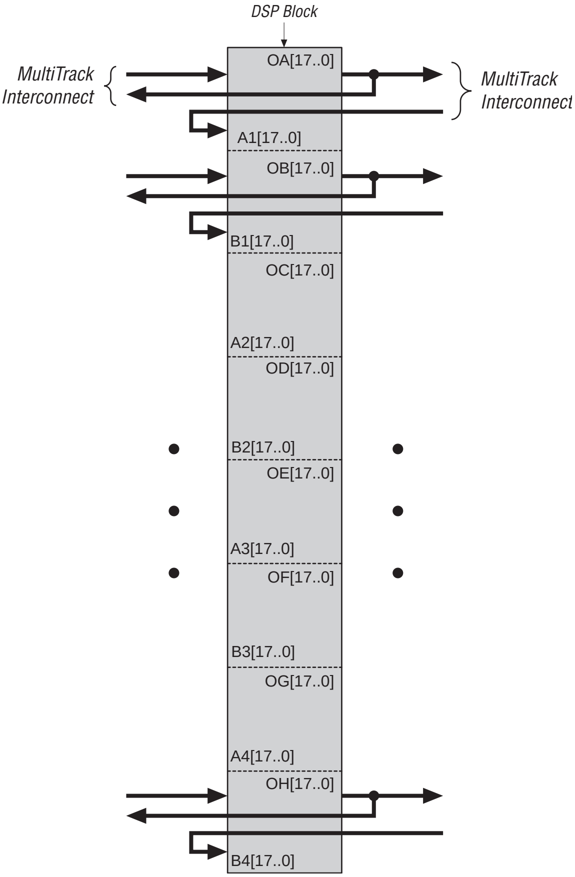
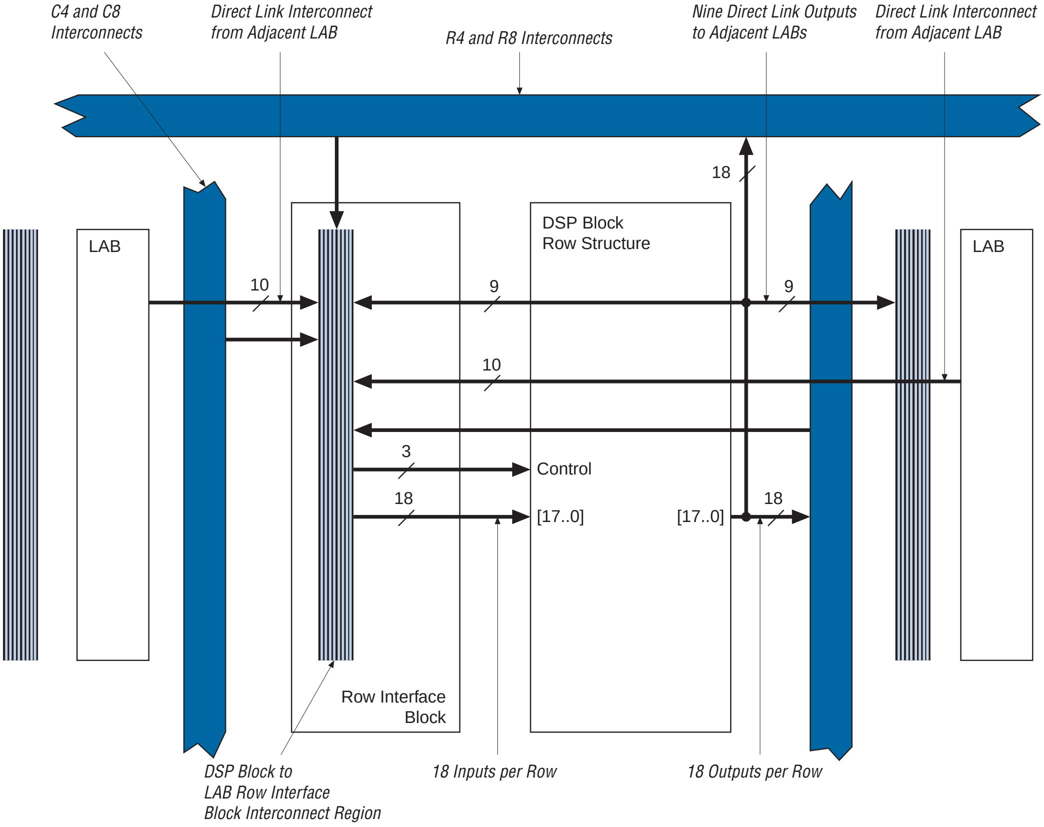


Figure 2–41. DSP Block Interface to Interconnect



A bus of 18 control signals feeds the entire DSP block. These signals include `clock[0..3]` clocks, `aclr[0..3]` asynchronous clears, `ena[1..4]` clock enables, `signa`, `signb` signed/unsigned control signals, `addnsub1` and `addnsub3` addition and subtraction control signals, and `accum_sload[0..1]` accumulator synchronous loads. The clock signals are routed from LAB row clocks and are generated from specific LAB rows at the DSP block interface. The LAB row source for control signals, data inputs, and outputs is shown in Table 2–17.

Table 2–17. DSP Block Signal Sources & Destinations

LAB Row at Interface	Control Signals Generated	Data Inputs	Data Outputs
1	`signa`	`A1[17..0]`	`OA[17..0]`
2	`aclr0` `accum_sload0`	`B1[17..0]`	`OB[17..0]`

3	`addnsub1`
	`clock0`
	`ena0`
		`A2[17..0]`	`OC[17..0]`

4	`aclr1`
	`clock1`
	`ena1`
		`B2[17..0]`	`OD[17..0]`

5	`aclr2`
	`clock2`
	`ena2`
		`A3[17..0]`	`OE[17..0]`

6	`sign_b`
	`clock3`
	`ena3`
		`B3[17..0]`	`OF[17..0]`

7	`clear3` `accum_sload1`	`A4[17..0]`	`OG[17..0]`
8	`addnsub3`	`B4[17..0]`	`OH[17..0]`

PLLs & Clock Networks

Stratix devices provide a hierarchical clock structure and multiple PLLs with advanced features. The large number of clocking resources in combination with the clock synthesis precision provided by enhanced and fast PLLs provides a complete clock management solution.

Global & Hierarchical Clocking

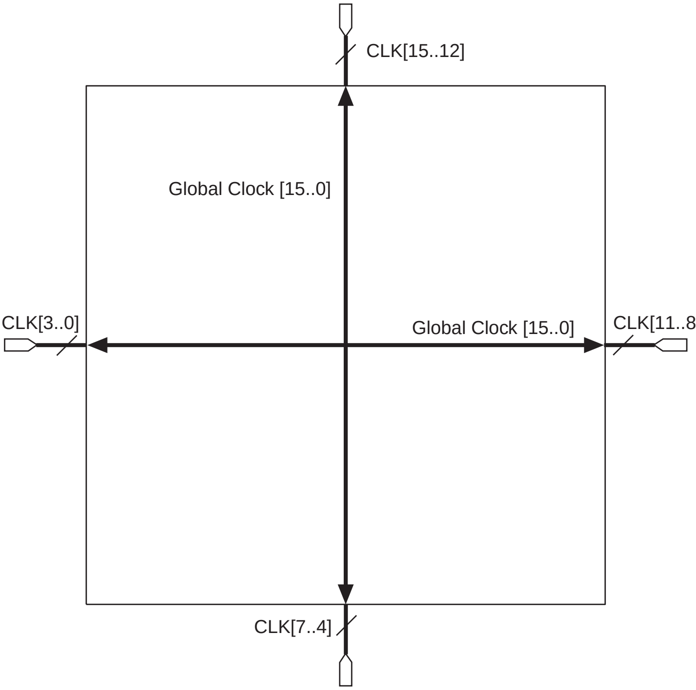
Stratix devices provide 16 dedicated global clock networks, 16 regional clock networks (four per device quadrant), and 8 dedicated fast regional clock networks (for EP1S10, EP1S20, and EP1S25 devices), and 16 dedicated fast regional clock networks (for EP1S30 EP1S40, and EP1S60, and EP1S80 devices). These clocks are organized into a hierarchical clock structure that allows for up to 22 clocks per device region with low skew and delay. This hierarchical clocking scheme provides up to 48 unique clock domains within Stratix devices.

There are 16 dedicated clock pins (`CLK[15..0]`) to drive either the global or regional clock networks. Four clock pins drive each side of the device, as shown in Figure 2–42. Enhanced and fast PLL outputs can also drive the global and regional clock networks.

Global Clock Network

These clocks drive throughout the entire device, feeding all device quadrants. The global clock networks can be used as clock sources for all resources within the device—IOEs, LEs, DSP blocks, and all memory blocks. These resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed from the external pin. The global clock networks can also be driven by internal logic for internally generated global clocks and asynchronous clears, clock enables, or other control signals with large fanout. Figure 2–42 shows the 16 dedicated `CLK` pins driving global clock networks.

Figure 2–42. Global Clocking Note (1)



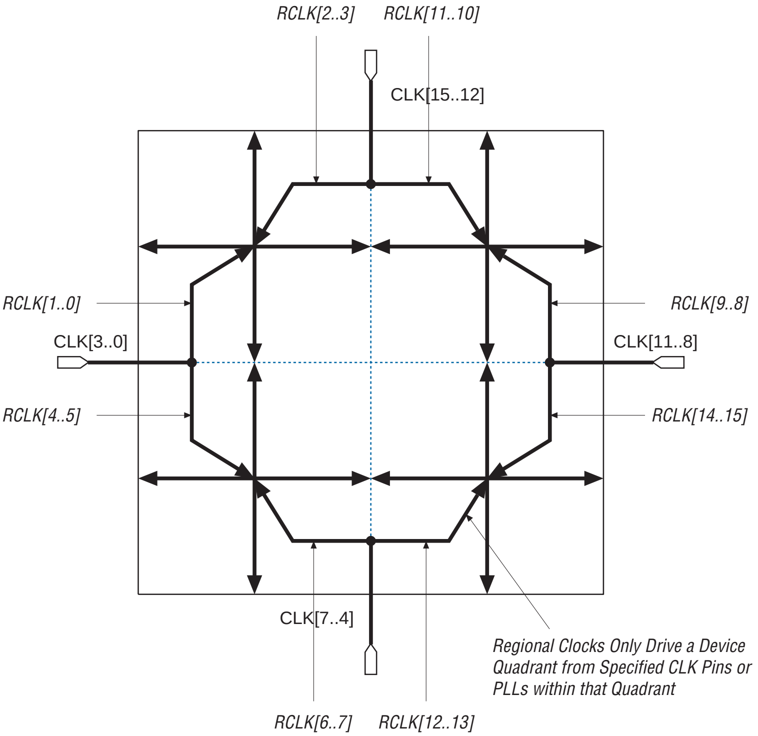
Note to Figure 2–42:

(1) The corner fast PLLs can also be driven through the global or regional clock networks. The global or regional clock input to the fast PLL can be driven by an output from another PLL, a pin-driven global or regional clock, or internally-generated global signals.

Regional Clock Network

There are four regional clock networks within each quadrant of the Stratix device that are driven by the same dedicated `CLK[15..0]` input pins or from PLL outputs. From a top view of the silicon, `RCLK[0..3]` are in the top left quadrant, `RCLK[8..11]` are in the top right quadrant, `RCLK[4..7]` are in the bottom left quadrant, and `RCLK[12..15]` are in the bottom right quadrant. The regional clock networks only pertain to the quadrant they drive into. The regional clock networks provide the lowest clock delay and skew for logic contained within a single quadrant. `RCLK` cannot be driven by internal logic. The `CLK` clock pins symmetrically drive the `RCLK` networks within a particular quadrant, as shown in Figure 2–43. See Figures 2–50 and 2–51 for `RCLK` connections from PLLs and `CLK` pins.

Figure 2–43. Regional Clocks

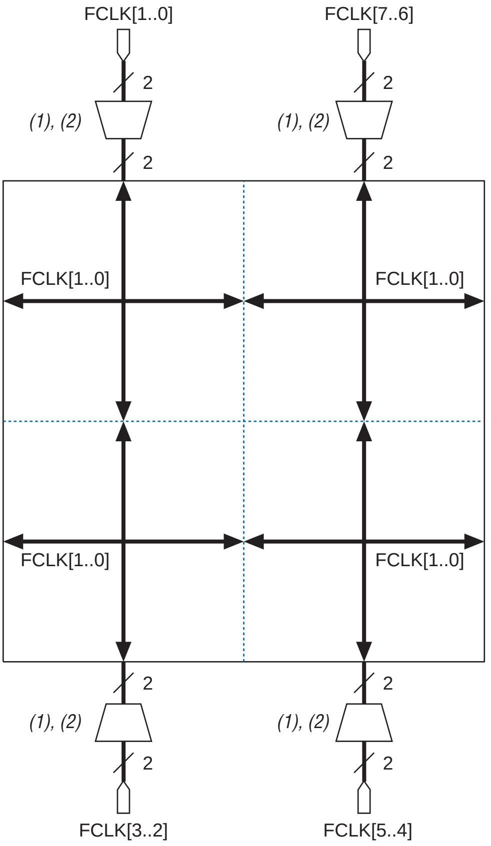


Regional Clocks Only Drive a Device Quadrant from Specified CLK Pins or PLLs within that Quadrant

Fast Regional Clock Network

In EP1S25, EP1S20, and EP1S10 devices, there are two fast regional clock networks, `FCLK[1..0]`, within each quadrant, fed by input pins that can connect to fast regional clock networks (see Figure 2–44). In EP1S30 and larger devices, there are two fast regional clock networks within each half-quadrant (see Figure 2–45). Dual-purpose `FCLK` pins drive the fast clock networks. All devices have eight `FCLK` pins to drive fast regional clock networks. Any I/O pin can drive a clock or control signal onto any fast regional clock network with the addition of a delay. This signal is driven via the I/O interconnect. The fast regional clock networks can also be driven from internal logic elements.

Figure 2–44. EP1S25, EP1S20 & EP1S10 Device Fast Clock Pin Connections to Fast Regional Clocks

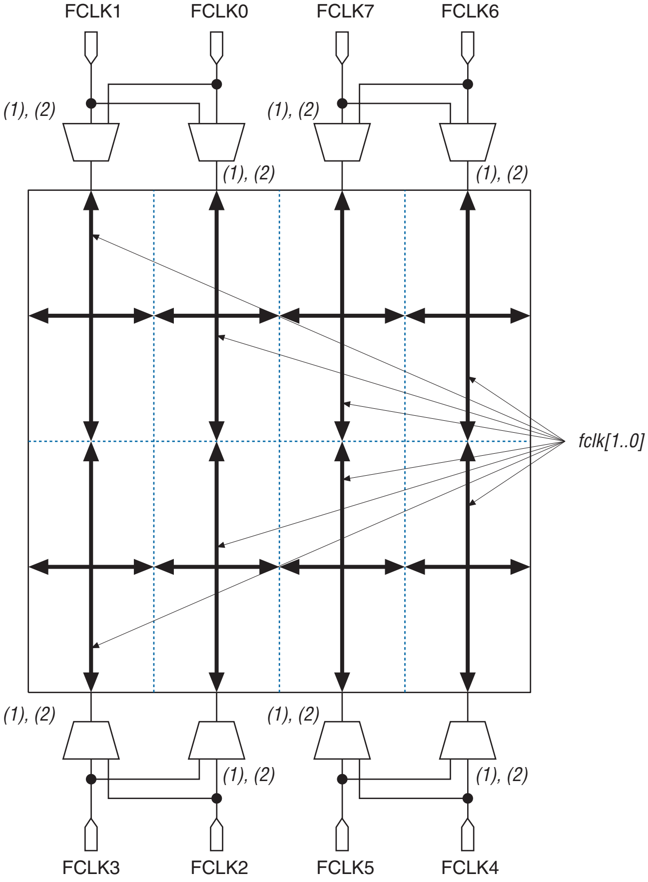


Notes to Figure 2–44:

(1) This is a set of two multiplexers.

(2) In addition to the `FCLK` pin inputs, there is also an input from the I/O interconnect.

Figure 2–45. EP1S30 Device Fast Regional Clock Pin Connections to Fast Regional Clocks

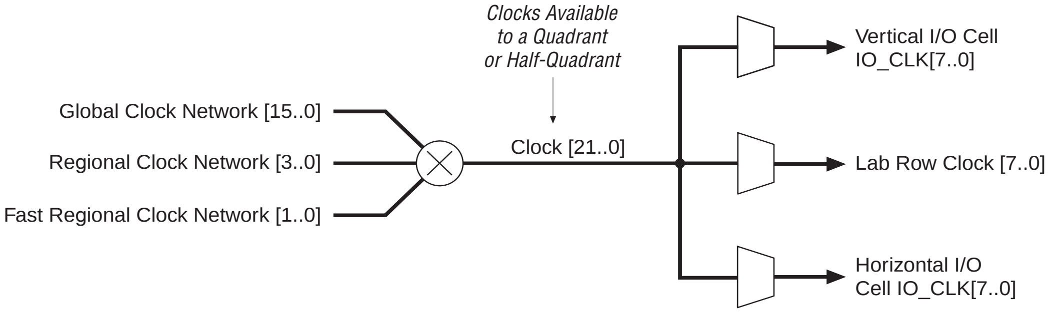


Notes to Figure 2–45:
(1) This is a set of two multiplexers.
(2) In addition to the `FCLK` pin inputs, there is also an input from the I/O interconnect.

Combined Resources

Within each region, there are 22 distinct dedicated clocking resources consisting of 16 global clock lines, four regional clock lines, and two fast regional clock lines. Multiplexers are used with these clocks to form eight bit busses to drive LAB row clocks, column IOE clocks, or row IOE clocks. Another multiplexer is used at the LAB level to select two of the eight row clocks to feed the LE registers within the LAB. See Figure 2–46.

Figure 2–46. Regional Clock Bus



IOE clocks have horizontal and vertical block regions that are clocked by eight I/O clock signals chosen from the 22 quadrant or half-quadrant clock resources. Figures 2–47 and 2–48 show the quadrant and half-quadrant relationship to the I/O clock regions, respectively. The vertical regions (column pins) have less clock delay than the horizontal regions (row pins).

Figure 2–47. EP1S10, EP1S20 & EP1S25 Device I/O Clock Groups

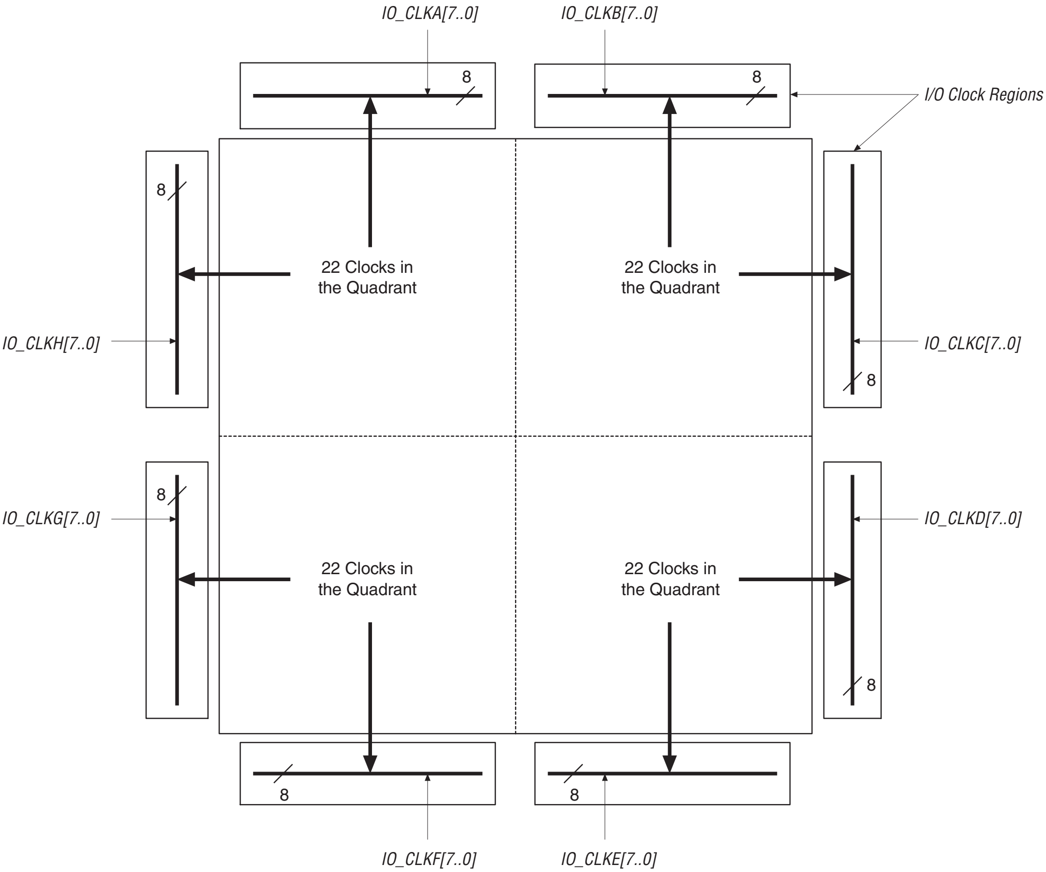
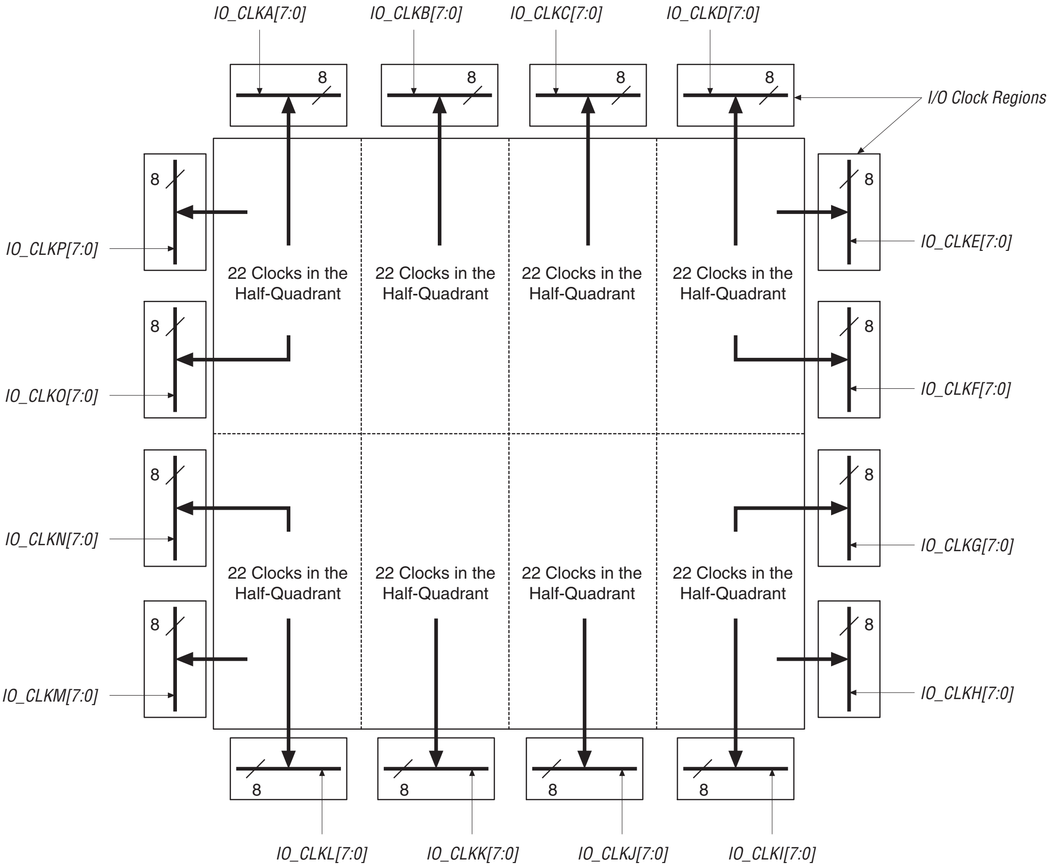


Figure 2–48. EP1S30, EP1S40, EP1S60, EP1S80 Device I/O Clock Groups



Designers can use the Quartus II software to control whether a clock input pin is either global, regional, or fast regional. The Quartus II software automatically selects the clocking resources if not specified.

Enhanced & Fast PLLs

Stratix devices provide robust clock management and synthesis using up to four enhanced PLLs and eight fast PLLs. These PLLs increase performance and provide advanced clock interfacing and clock-frequency synthesis. With features such as clock switchover, spread spectrum clocking, programmable bandwidth, phase and delay control, and PLL reconfiguration, the Stratix device's enhanced PLLs provide designers with complete control of their clocks and system timing. The fast PLLs provide general purpose clocking with multiplication and phase shifting as well as high-speed outputs for high-speed differential I/O support. Enhanced and fast PLLs work together with the Stratix high-speed I/O and advanced clock architecture to provide significant improvements in system performance and bandwidth.

The Quartus II software enables the PLLs and their features without requiring any external devices. Table 2–18 shows the PLLs available for each Stratix device.

Table 2–18. Stratix Device PLL Availability

Device	Fast PLLs								Enhanced PLLs			
	1	2	3	4	7	8	9	10	5 *(1)*	6 *(1)*	11 *(2)*	12 *(2)*
EP1S10	✓	✓	✓	✓					✓	✓		
EP1S20	✓	✓	✓	✓					✓	✓		
EP1S25	✓	✓	✓	✓					✓	✓		
EP1S30	✓	✓	✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	✓		
EP1S40	✓	✓	✓	✓	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓ *(3)*	✓	✓	✓ *(3)*	✓ *(3)*
EP1S60	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
EP1S80	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes to Table 2–18:

(1) PLLs 5 and 6 each have eight single-ended outputs or four differential outputs.

(2) PLLs 11 and 12 each have one single-ended output.

(3) EP1S30 and EP1S40 devices do not support these PLLs in the 780-pin FineLine BGA® package.

Table 2–19 shows the enhanced PLL and fast PLL features in Stratix devices.

Table 2–19. Stratix PLL Features

Feature	Enhanced PLL	Fast PLL
Clock multiplication and division	$m/(n \times \text{post-scale counter})$ *(1)*	$m/(\text{post-scale counter})$ *(2)*
Phase shift	Down to 156.25-ps increments *(3)*, *(4)*	Down to 125-ps increments *(3)*, *(4)*
Delay shift	250-ps increments for ±3 ns	
Clock switchover	✓	
PLL reconfiguration	✓	
Programmable bandwidth	✓	
Spread spectrum clocking	✓	
Programmable duty cycle	✓	✓
Number of internal clock outputs	6	3 *(5)*
Number of external clock outputs	Four differential/eight singled-ended or one single-ended *(6)*	*(7)*
Number of feedback clock inputs	2 *(8)*	

Notes to Table 2–19:

(1) For enhanced PLLs, m, n, range from 1 to 512 and post-scale counters g, l, e range from 1 to 1024 with 50% duty cycle. With a non-50% duty cycle the post-scale counters g, l, e range from 1 to 512.

(2) For fast PLLs, m and post-scale counters range from 1 to 32.

(3) The smallest phase shift is determined by the voltage controlled oscillator (VCO) period divided by 8.

(4) For degree increments, Stratix devices can shift all output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the frequency and divide parameters.

(5) PLLs 7, 8, 9, and 10 have two output ports per PLL. PLLs 1, 2, 3, and 4 have three output ports per PLL.

(6) Every Stratix device has two enhanced PLLs (PLLs 5 and 6) with either eight single-ended outputs or four differential outputs each. Two additional enhanced PLLs (PLLs 11 and 12) in EP1S80, EP1S60, and EP1S40 devices each have one single-ended output. Devices in the 780 pin FineLine BGA packages do not support PLLs 11 and 12.

(7) Fast PLLs can drive to any I/O pin as an external clock. For high-speed differential I/O pins, the device uses a data channel to generate `txclkout`.

(8) Every Stratix device has two enhanced PLLs with one single-ended or differential external feedback input per PLL.

Figure 2–49 shows a top-level diagram of the Stratix device and PLL floorplan.

Figure 2–49. PLL Locations

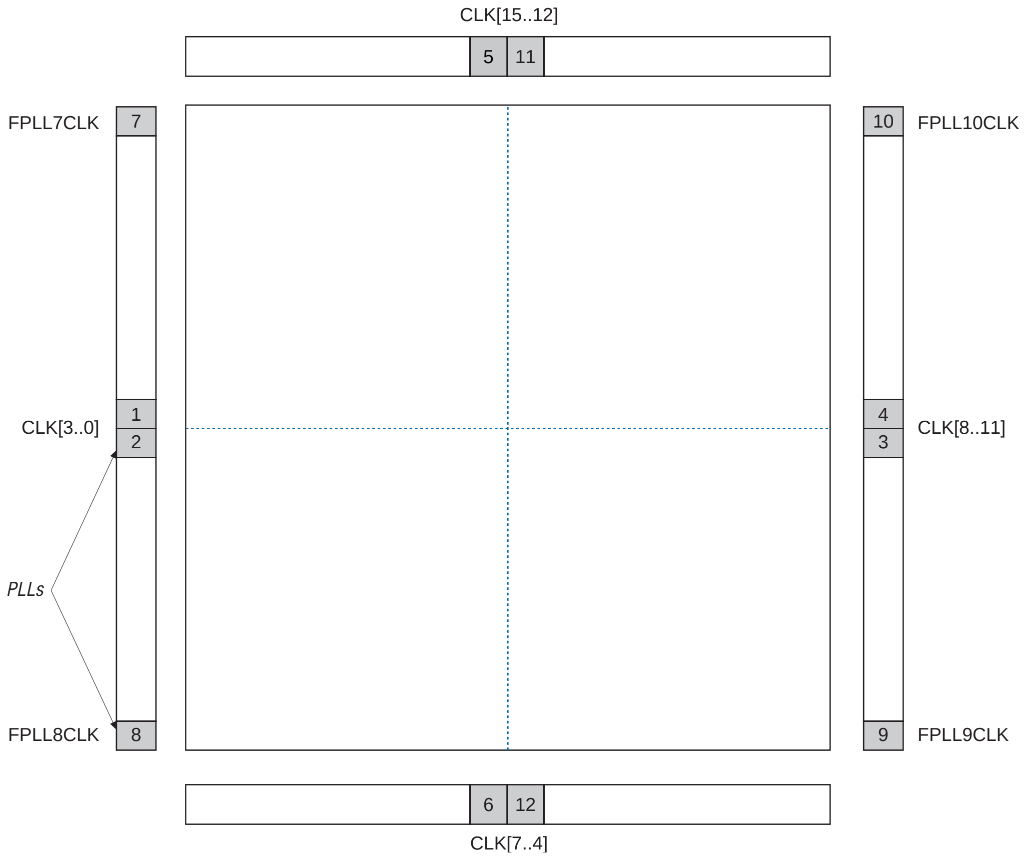
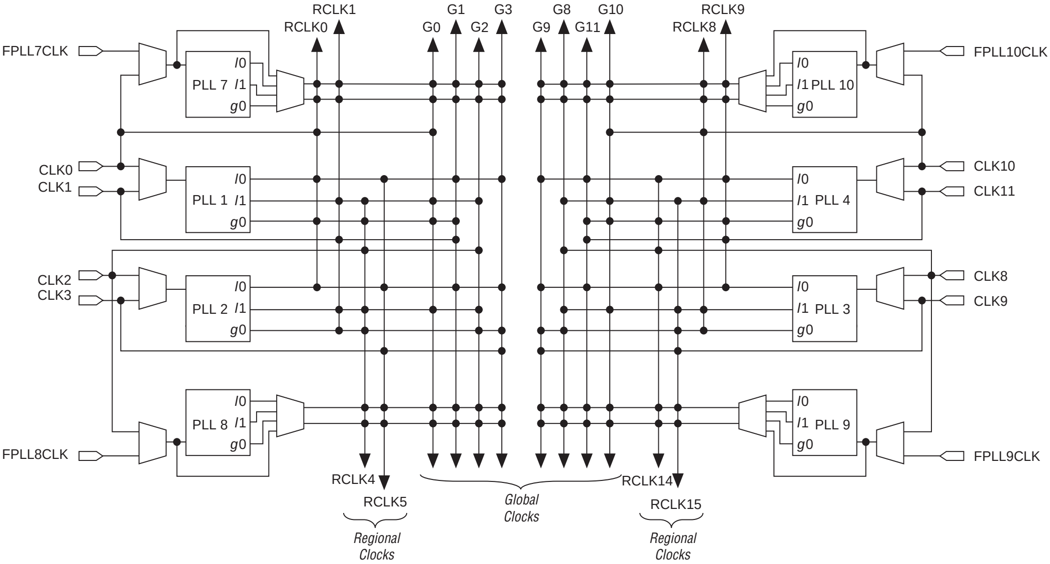


Figure 2–50 shows the global and regional clocking from the PLL outputs and the CLK pins.

Figure 2–50. Global & Regional Clock Connections from Side Pins & Fast PLL Outputs Note (1), (2)



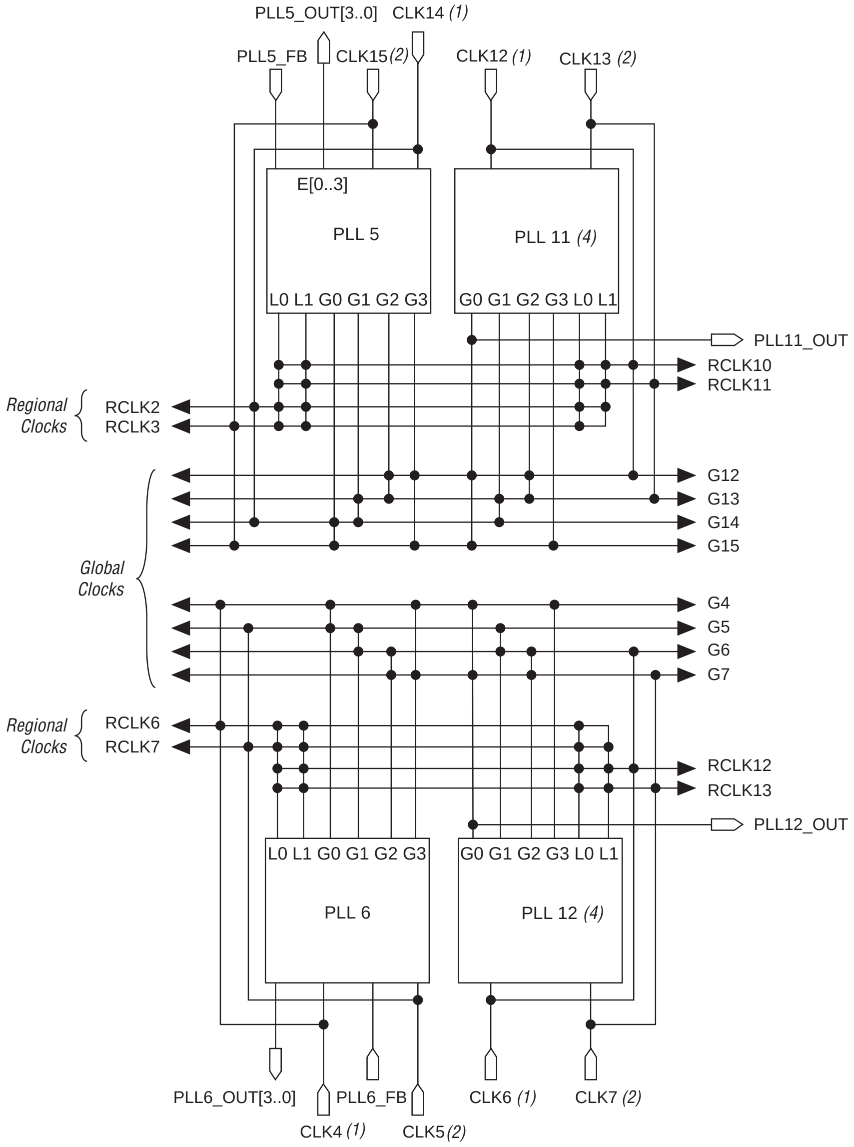
Notes to Figure 2–50:

(1) PLLs 1 to 4 and 7 to 10 are fast PLLs. PLLs 5, 6, 11, and 12 are enhanced PLLs.

(2) The global or regional clocks in a fast PLL's quadrant can drive the fast PLL input. A pin or other PLL must drive the global or regional source. The source cannot be driven by internally generated logic before driving the fast PLL.

Figure 2–51 shows the global and regional clocking from enhanced PLL outputs and top `CLK` pins.

Figure 2–51. Global & Regional Clock Connections from Top Clock Pins & Enhanced PLL Outputs Note (1)



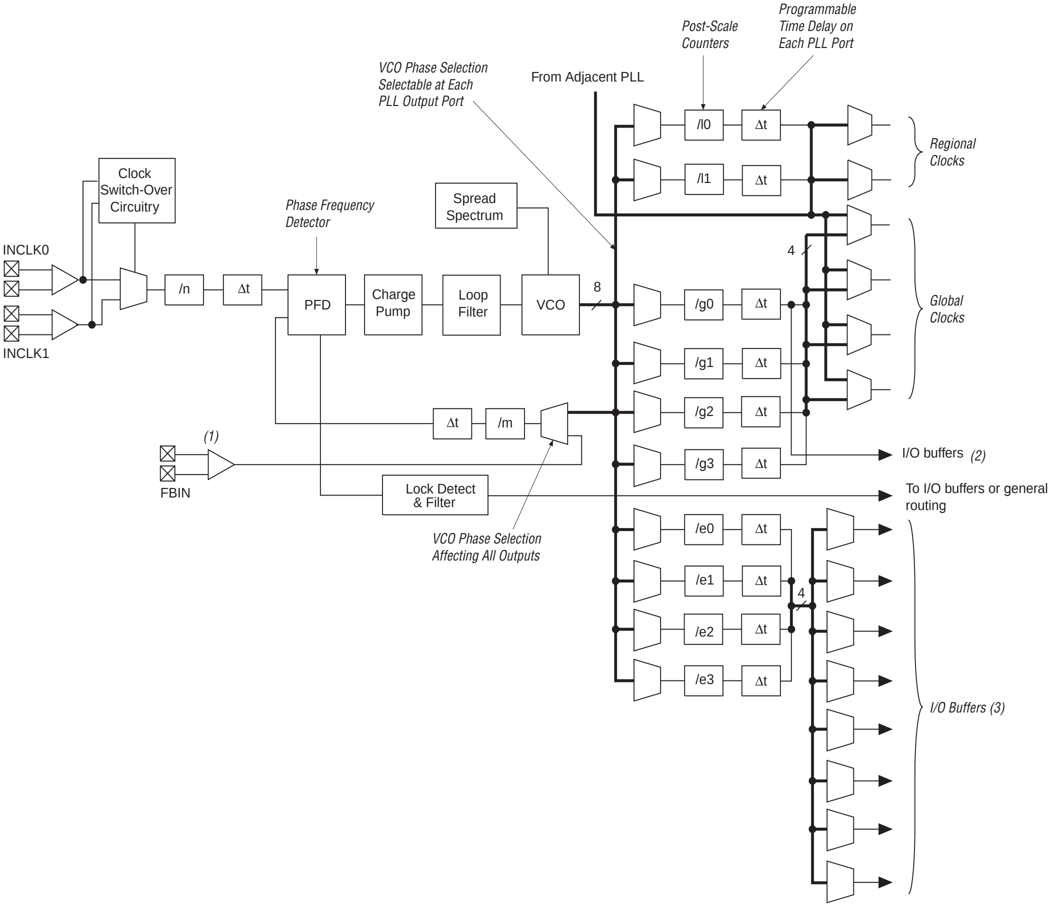
Notes to Figure 2–51:

(1) PLLs 1 to 4 and 7 to 10 are fast PLLs. PLLs 5, 6, 11, and 12 are enhanced PLLs.
(2) `CLK4`, `CLK6`, `CLK12`, and `CLK14` feed the corresponding PLL's `inclk0` port.
(3) `CLK5`, `CLK7`, `CLK13`, and `CLK15` feed the corresponding PLL's `inclk1` port.
(4) The EP1S40 device in the 780-pin FineLine BGA package does not support PLLs 11 and 12.

Enhanced PLLs

Stratix devices contain up to four enhanced PLLs with advanced clock management features. Figure 2–52 shows a diagram of the enhanced PLL.

Figure 2–52. Stratix Enhanced PLL



Notes to Figure 2–52:

(1) External feedback is available in PLLs 5 and 6.
(2) This single-ended external output is available from the *g*0 counter for PLLs 11 and 12.
(3) These four counters and external outputs are available in PLLs 5 and 6.
(4) This connection is only available on EP1S40 and larger Stratix devices. For example, PLLs 5 and 11 are adjacent and PLLs 6 and 12 are adjacent. The EP1S40 device in the 780-pin FineLine BGA package does not support PLLs 11 and 12.

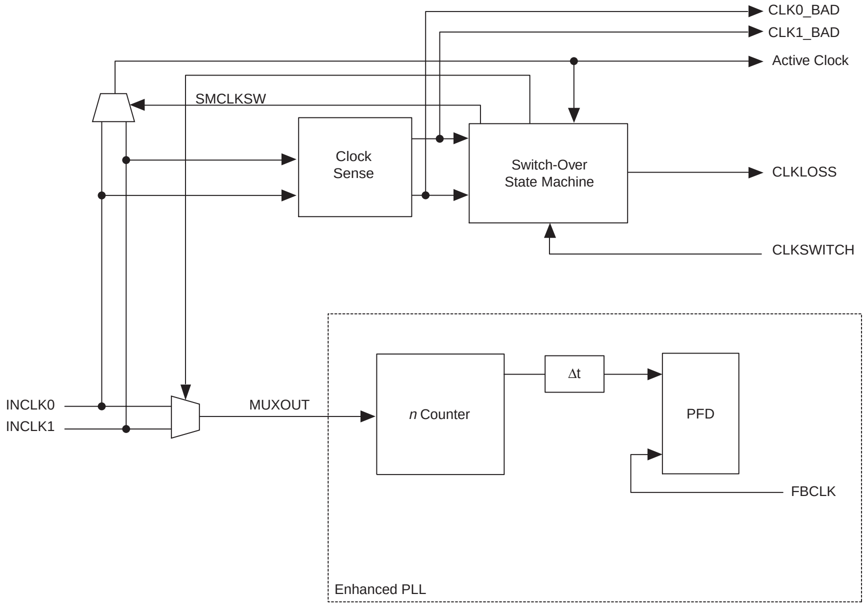
Clock Multiplication & Division

Each Stratix device enhanced PLL provides clock synthesis for PLL output ports using $m/(n \circ \text{post-scale counter})$ scaling factors. The input clock is divided by a pre-scale divider, n, and is then multiplied by the m feedback factor. The control loop drives the VCO to match $f_{IN} \circ (m/n)$. Each output port has a unique post-scale counter that divides down the high-frequency VCO. For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets its frequency specifications. Then, the post-scale dividers scale down the output frequency for each output port. For example, if output frequencies required from one PLL are 33 and 66 MHz, set the VCO to 330 MHz (the least common multiple in the VCO's range). There is one pre-scale counter, n, and one multiply counter, m, per PLL, with a range of 1 to 512 on each. There are two post-scale counters (l) for regional clock output ports, four counters (g) for global clock output ports, and up to four counters (e) for external clock outputs, all ranging from 1 to 1024 with a 50% duty cycle setting. The post-scale counters range from 1 to 512 with any non-50% duty cycle setting. The Quartus II software automatically chooses the appropriate scaling factors according to the input frequency, multiplication, and division values entered.

Clock Switchover

To effectively develop high-reliability network systems, clocking schemes must support multiple clocks to provide redundancy. For this reason, Stratix device enhanced PLLs support a flexible clock switchover capability. Figure 2–53 shows a block diagram of the switchover circuit.The switchover circuit is configurable, so the designer can define how to implement it. Clock-sense circuitry automatically switches from the primary to secondary clock for PLL reference when the primary clock signal is not present.

Figure 2–53. Clock Switchover Circuitry



There are two possible ways to use the clock switch-over feature.

- Designers can use automatic switch-over circuitry for switching between inputs of the same frequency. For example, in applications that require a redundant clock with the same frequency as the primary clock, the switchover state machine generates a signal that controls the multiplexer select input on the bottom of Figure 2–53. In this case, the secondary clock becomes the reference clock for the PLL.
- Designers can use the `clkswitch` input for user- or system-controlled switch conditions. This is possible for same-frequency switchover or to switch between inputs of different frequencies. For example, if `inclk0` is 66 MHz and `inclk1` is 100 MHz, the designer must control the switchover because the automatic clock-sense circuitry cannot monitor primary and secondary clock frequencies with a frequency difference of more than ±20%. This feature is useful when clock sources can originate from multiple cards on the backplane, requiring a system-controlled switchover between frequencies of operation. The designer can use `clkswitch` together with the lock signal to trigger the switch from a clock that is running but becomes unstable and cannot be locked onto.

During switch over, the PLL VCO continues to run and will either slow down or speed up, generating frequency drift on the PLL outputs. The clock switchover transitions without any glitches. After the switch, there is a finite resynchronization period to lock onto new clock as the VCO ramps up. The exact amount of time it takes for the PLL to relock relates to the PLL configuration and may be adjusted by using the programmable bandwidth feature of the PLL. The specification for the maximum time to relock is 100 µs.

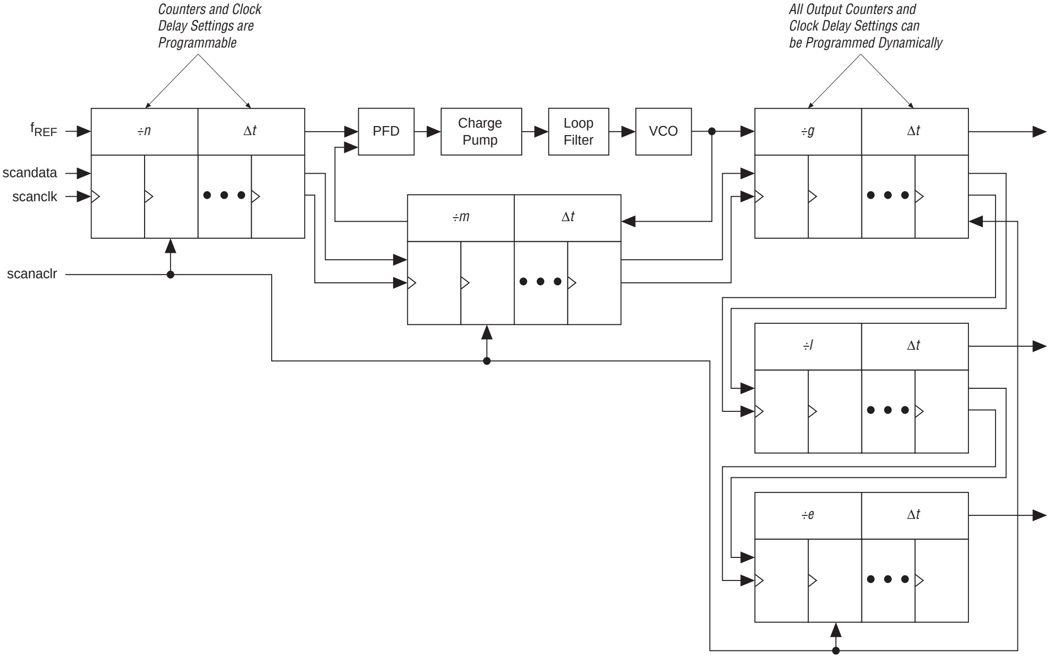
For more information on clock switchover, see *AN 313, Implementing Clock Switchover in Stratix & Stratix GX Devices*.

PLL Reconfiguration

The PLL reconfiguration feature enables system logic to change Stratix device enhanced PLL counters and delay elements without reloading a Programmer Object File (**.pof**). This provides considerable flexibility for frequency synthesis, allowing real-time PLL frequency and output clock delay variation. The designer can sweep the PLL output frequencies and clock delay in prototype environments. The PLL reconfiguration feature can also dynamically or intelligently control system clock speeds or t_{CO} delays in end systems.

Clock delay elements at each PLL output port implement variable delay. Figure 2–54 shows a diagram of the overall dynamic PLL control feature for the counters and the clock delay elements. The configuration time is less than 20 µs for the enhanced PLL using a input shift clock rate of 22 MHz. The charge pump, loop filter components, and phase shifting using VCO phase taps cannot be dynamically adjusted.

Figure 2–54. Dynamically Programmable Counters & Delays in Stratix Device Enhanced PLLs



PLL reconfiguration data is shifted into serial registers from the logic array or external devices. The PLL input shift data uses a reference input shift clock. Once the last bit of the serial chain is clocked in, the register chain is synchronously loaded into the PLL configuration bits. The shift circuitry also provides an asynchronous clear for the serial registers.

For more information on PLL reconfiguration, see *AN 282. Implementing PLL Reconfiguration in Stratix and Stratix GX Devices.*

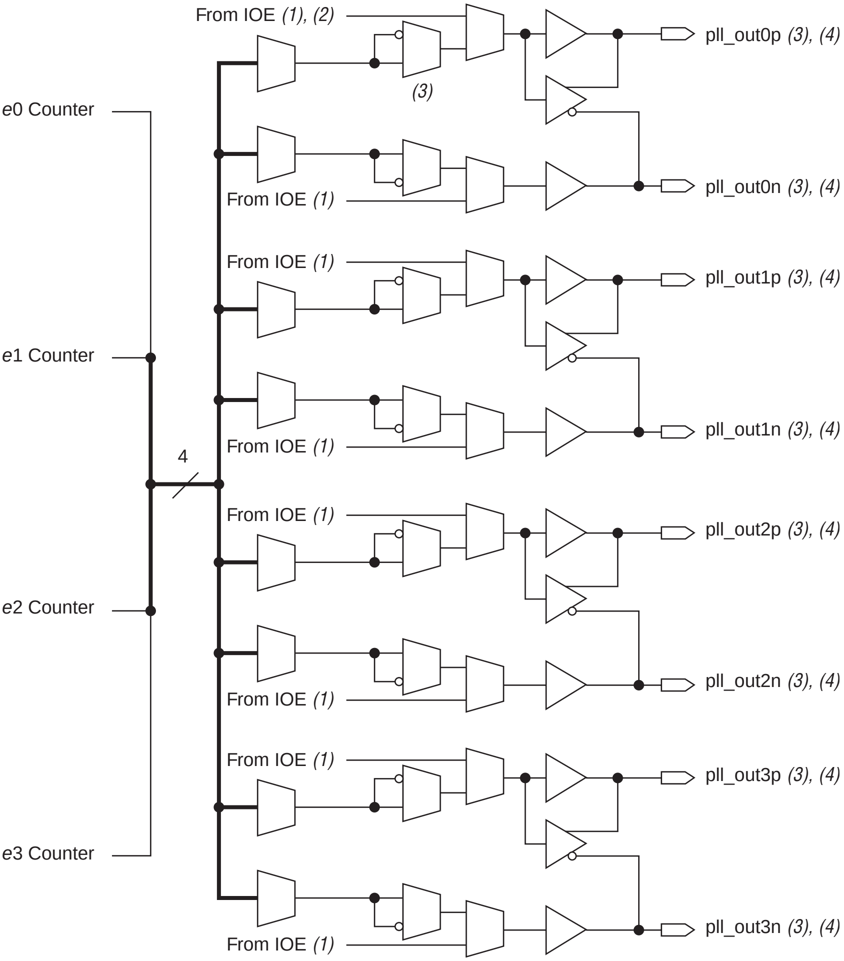
Programmable Bandwidth

The designer has advanced control of the PLL bandwidth using the programmable control of the PLL loop characteristics, including loop filter and charge pump. The PLL's bandwidth is a measure of its ability to track the input clock and jitter. A high-bandwidth PLL can quickly lock onto a reference clock and react to any changes in the clock. It also will allow a wide band of input jitter spectrum to pass to the output. A low-bandwidth PLL will take longer to lock, but it will attenuate all high-frequency jitter components. The Quartus II software can adjust PLL characteristics to achieve the desired bandwidth. The programmable bandwidth is tuned by varying the charge pump current, loop filter resistor value, high frequency capacitor value, and *m* counter value. Designers can manually adjust these values if desired. Bandwidth is programmable from 200 kHz to 1.5 MHz.

External Clock Outputs

Enhanced PLLs 5 and 6 each support up to eight single-ended clock outputs (or four differential pairs). Differential SSTL and HSTL outputs are implemented using 2 single-ended output buffers which are programmed to have opposite polarity. In Quartus II software, simply assign the appropriate differential I/O standard and the software will implement the inversion. See Figure 2–55.

Figure 2–55. External Clock Outputs for PLLs 5 & 6



Notes to Figure 2–55:

(1) The design can use each external clock output pin as a general-purpose output pin from the logic array. These pins are multiplexed with IOE outputs.

(2) Two single-ended outputs are possible per output counter—either two outputs of the same frequency and phase or one shifted 180°.

(3) EP1S10, EP1S20, and EP1S25 devices in 672-pin BGA and 484- and 672-pin FineLine BGA packages only have two pairs of external clocks (i.e., `pll_out0p`, `pll_out0n`, `pll_out1p`, and `pll_out1n`).

(4) Differential SSTL and HSTL outputs are implemented using two single-ended output buffers, which are programmed to have opposite polarity.

Any of the four external output counters can drive the single-ended or differential clock outputs for PLLs 5 and 6. This means one counter or frequency can drive all output pins available from PLL 5 or PLL 6. Each pair of output pins (four pins total) has dedicated `VCC` and `GND` pins to reduce the output clock's overall jitter by providing improved isolation from switching I/O pins.

For PLLs 5 and 6, each pin of a single-ended output pair can either be in phase or 180° out of phase. The clock output pin pairs support the same I/O standards as standard output pins (in the top and bottom banks) as well as LVDS, LVPECL, 3.3-V PCML, HyperTransport technology, differential HSTL, and differential SSTL. Table 2–20 shows which I/O standards the enhanced PLL clock pins support. When in single-ended or differential mode, the two outputs operate off the same power supply. Both outputs use the same standards in single-ended mode to maintain performance. Designers can also use the external clock output pins as user output pins if external enhanced PLL clocking is not needed.

Table 2–20. I/O Standards Supported for Enhanced PLL Pins (Part 1 of 2)

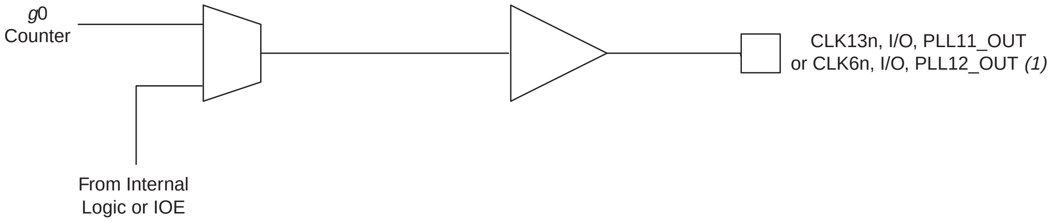
I/O Standard	Input			Output
	INCLK	FBIN	PLLENABLE	EXTCLK
LVTTL	✓	✓	✓	✓
LVCMOS	✓	✓	✓	✓
2.5 V	✓	✓		✓
1.8 V	✓	✓		✓
1.5 V	✓	✓		✓
3.3-V PCI	✓	✓		✓
3.3-V PCI-X 1.0	✓	✓		✓
LVPECL	✓	✓		✓
3.3-V PCML	✓	✓		✓
LVDS	✓	✓		✓
HyperTransport technology	✓	✓		✓
Differential HSTL	✓			✓
Differential SSTL				✓
3.3-V GTL	✓	✓		✓
3.3-V GTL+	✓	✓		✓
1.5-V HSTL class I	✓	✓		✓

Table 2–20. I/O Standards Supported for Enhanced PLL Pins (Part 2 of 2)

I/O Standard	Input			Output
	INCLK	FBIN	PLLENABLE	EXTCLK
1.5-V HSTL class II	✓	✓		✓
1.8-V HSTL class I	✓	✓		✓
1.8-V HSTL class II	✓	✓		✓
SSTL-18 class I	✓	✓		✓
SSTL-18 class II	✓	✓		✓
SSTL-2 class I	✓	✓		✓
SSTL-2 class II	✓	✓		✓
SSTL-3 class I	✓	✓		✓
SSTL-3 class II	✓	✓		✓
AGP (1× and 2×)	✓	✓		✓
CTT	✓	✓		✓

Enhanced PLLs 11 and 12 support one single-ended output each (see Figure 2–56). These outputs do not have their own `VCC` and `GND` signals. Therefore, to minimize jitter, do not place switching I/O pins next to this output pin.

Figure 2–56. External Clock Outputs for Enhanced PLLs 11 & 12



Note to Figure 2–56:

(1) For PLL 11, this pin is `CLK13n`; for PLL 12 this pin is `CLK7n`.

Stratix devices can drive any enhanced PLL driven through the global clock or regional clock network to any general I/O pin as an external output clock. The jitter on the output clock is not guaranteed for these cases.

Clock Feedback

The following four feedback modes in Stratix device enhanced PLLs allow multiplication and/or phase and delay shifting:

- Zero delay buffer: The external clock output pin is phase-aligned with the clock input pin for zero delay. Altera recommends using the same I/O standard on the input clock and the output clocks for optimum performance.

- External feedback: The external feedback input pin, `FBIN`, is phase-aligned with the clock input, `CLK`, pin. Aligning these clocks allows the designer to remove clock delay and skew between devices. This mode is only possible for PLLs 5 and 6. PLLs 5 and 6 each support feedback for one of the dedicated external outputs, either one single-ended or one differential pair. In this mode, one *e* counter feeds back to the PLL `FBIN` input, becoming part of the feedback loop. Altera recommends using the same I/O standard on the input clock, the `FBIN` pin, and the output clocks for optimum performance.

- Normal mode: If an internal clock is used in this mode, it is phase-aligned to the input clock pin. The external clock output pin will have a phase delay relative to the clock input pin if connected in this mode. The designer defines which internal clock output from the PLL should be phase-aligned to the internal clock pin.

- No compensation: In this mode, the PLL will not compensate for any clock networks or external clock outputs.

Phase & Delay Shifting

Stratix device enhanced PLLs provide advanced programmable phase and clock delay shifting. These parameters are set in the Quartus II software.

Phase Delay

The Quartus II software automatically sets the phase taps and counter settings according to the phase shift entry. The designer enters a desired phase shift and the Quartus II software automatically sets the closest setting achievable. This type of phase shift is not reconfigurable during system operation. For phase shifting, enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. Designers can select phase-shifting values in time units with a resolution of 156.25 to 416.66 ps. This resolution is a function of frequency input and the multiplication and division factors (i.e., it is a function of the VCO period), with the finest step being equal to an eighth (°0.125) of the VCO period. Each clock output counter can choose a different phase of the VCO period from up to eight taps for individual fine step selection. Also, each clock output counter can use a unique initial count setting to achieve individual coarse shift selection in steps of one VCO period. The combination of coarse and fine shifts allows phase shifting for the entire input clock period.

The equation to determine the precision of the phase shifting in degrees is: 45° ÷ post-scale counter value. Therefore, the maximum step size is 45°, and smaller steps are possible depending on the multiplication and division ratio necessary on the output counter port.

This type of phase shift provides the highest precision since it is the least sensitive to process, supply, and temperature variation.

Clock Delay

In addition to the phase shift feature, the ability to fine tune the Δt clock delay provides advanced time delay shift control on each of the four PLL outputs. There are time delays for each post-scale counter (*e*, *g*, or *l*) from the PLL, the *n* counter, and *m* counter. Each of these can shift in 250-ps increments for a range of 3.0 ns. The *m* delay shifts all outputs earlier in time, while *n* delay shifts all outputs later in time. Individual delays on post-scale counters (*e*, *g*, and *l*) provide positive delay for each output. Table 2–21 shows the combined delay for each output for normal or zero delay buffer mode where Δt_e, Δt_g, or Δt_l is unique for each PLL output.

The t_{OUTPUT} for a single output can range from –3 ns to +6 ns. The total delay shift difference between any two PLL outputs, however, must be less than ±3 ns. For example, shifts on two outputs of –1 and +2 ns is allowed, but not –1 and +2.5 ns because these shifts would result in a difference of 3.5 ns. If the design uses external feedback, the Δt_e delay will remove delay from outputs, represented by a negative sign (see Table 2–21). This effect occurs because the Δt_e delay is then part of the feedback loop.

Table 2–21. Output Clock Delay for Enhanced PLLs

Normal or Zero Delay Buffer Mode	External Feedback Mode
$\Delta t_{eOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_e$	$\Delta t_{eOUTPUT} = \Delta t_n - \Delta t_m - \Delta t_e$ *(1)*
$\Delta t_{gOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_g$	$\Delta t_{gOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_g$
$\Delta t_{lOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_l$	$\Delta t_{lOUTPUT} = \Delta t_n - \Delta t_m + \Delta t_l$

Note to Table 2–21:

(1) Δt_e removes delay from outputs in external feedback mode.

The variation due to process, voltage, and temperature is about ±15% on the delay settings. PLL reconfiguration can control the clock delay shift elements, but not the VCO phase shift multiplexers, during system operation.

Spread-Spectrum Clocking

Stratix device enhanced PLLs use spread-spectrum technology to reduce electromagnetic interference generation from a system by distributing the energy over a broader frequency range. The enhanced PLL typically provides 0.5% down spread modulation using a triangular profile. The modulation frequency is programmable. Enabling spread-spectrum for a PLL affects all of its outputs.

Lock Detect

The lock output indicates that there is a stable clock output signal in phase with the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. A designer may need to gate the lock signal for use as a system control. The lock signal from the locked port can drive the logic array or an output pin.

Whenever the PLL loses lock e.g., `inclk` jitter, clock switchover, PLL reconfiguration, power supply noise, etc.), the PLL must be reset with the `areset` signal to guarantee correct phase relationship between the PLL output clocks. If the phase relationship between the input clock versus output clock, and between different output clocks from the PLL is not important in the design, then the PLL need not be reset.

See the *Stratix FPGA Errata Sheet* for more information on implementing the gated lock signal in a design.

Programmable Duty Cycle

The programmable duty cycle allows enhanced PLLs to generate clock outputs with a variable duty cycle. This feature is supported on each enhanced PLL post-scale counter (*g*0..*g*3, *l*0..*l*3, *e*0..*e*3). The duty cycle setting is achieved by a low and high time count setting for the post-scale dividers. The Quartus II software uses the frequency input and the required multiply or divide rate to determine the duty cycle choices.

Advanced Clear & Enable Control

There are several control signals for clearing and enabling PLLs and their outputs. The designer can use these signals to control PLL resynchronization and gate PLL output clocks for low-power applications.

The `pllenable` pin is a dedicated pin that enables/disables PLLs. When the `pllenable` pin is low, the clock output ports are driven by `GND` and all the PLLs go out of lock. When the `pllenable` pin goes high again, the PLLs relock and resynchronize to the input clocks. The designer can choose which PLLs are controlled by the `pllenable` signal by connecting the `pllenable` input port of the `altpll` megafunction to the common `pllenable` input pin.

The `areset` signals are reset/resynchronization inputs for each PLL. The `areset` signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL output clocks. Users should include the `areset` signal in designs if any of the following conditions are true:

- PLL Reconfiguration or Clock switchover enables in the design.
- Phase relationships between output clocks need to be maintained after a loss of lock condition

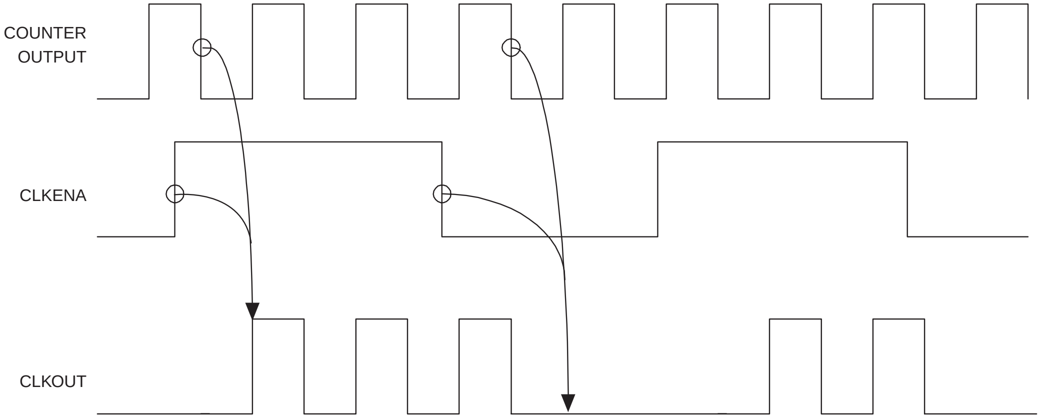
The device input pins or logic elements (LEs) can drive these input signals. When driven high, the PLL counters will reset, clearing the PLL output and placing the PLL out of lock. The VCO will set back to its nominal setting (~700 MHz). When driven low again, the PLL will resynchronize to its input as it relocks. If the target VCO frequency is below this nominal frequency, then the output frequency will start at a higher value than desired as the PLL locks. If the system cannot tolerate this, the `clkena` signal can disable the output clocks until the PLL locks.

The `pfdena` signals control the phase frequency detector (PFD) output with a programmable gate. If the designer disables the PFD, the VCO will operate at its last set value of control voltage and frequency with some long-term drift to a lower frequency. The system will continue running when the PLL goes out of lock or the input clock is disabled. By maintaining the last locked frequency, the system has time to store its current settings before shutting down. Designers can either use their own control signal or a `clkloss` status signal to trigger `pfdena`.

The `clkena` signals control the enhanced PLL regional and global outputs. Each regional and global output port has its own `clkena` signal. The `clkena` signals synchronously disable or enable the clock at the PLL output port by gating the outputs of the *g* and *l* counters. The `clkena` signals are registered on the falling edge of the counter output clock to enable or disable the clock without glitches. Figure 2–57 shows the waveform example for a PLL clock port enable. The PLL can remain locked independent of the `clkena` signals since the loop-related counters are not affected. This feature is useful for applications that require a low power or sleep mode. Upon re-enabling, the PLL does not need a resynchronization or relock period. The `clkena` signal can also disable clock outputs if the system is not tolerant to frequency overshoot during resynchronization.

The `extclkena` signals work in the same way as the `clkena` signals, but they control the external clock output counters (*e*0, *e*1, *e*2, and *e*3). Upon re-enabling, the PLL does not need a resynchronization or relock period unless the PLL is using external feedback mode. In order to lock in external feedback mode, the external output must drive the board trace back to the `FBIN` pin.

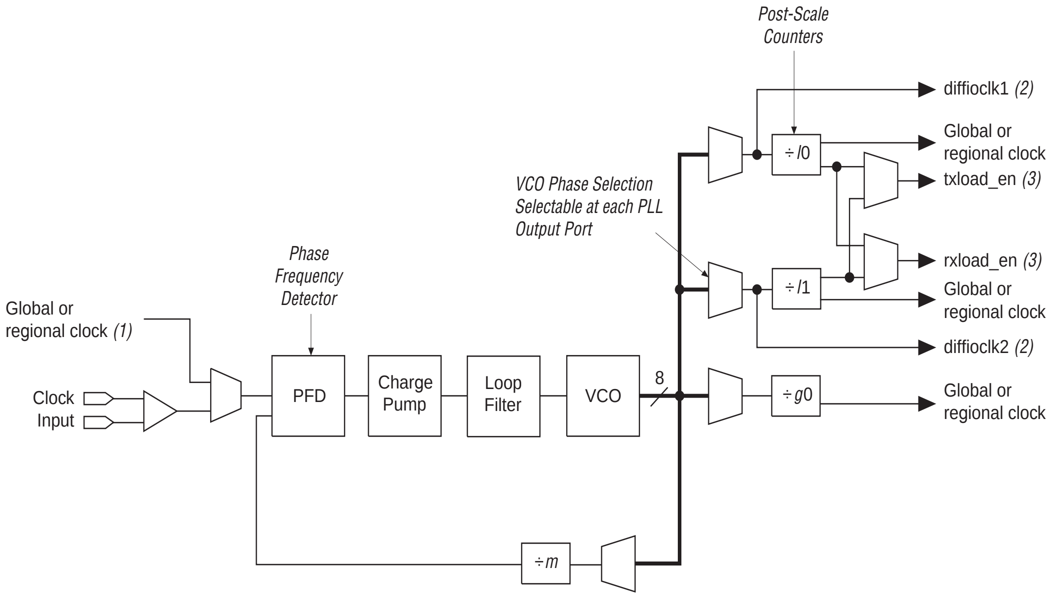
Figure 2–57. extclkena Signals



Fast PLLs

Stratix devices contain up to eight fast PLLs with high-speed serial interfacing ability, along with general-purpose features. Figure 2–58 shows a diagram of the fast PLL.

Figure 2–58. Stratix Device Fast PLL



Notes to Figure 2–58:

(1) The global or regional clock input can be driven by an output from another PLL or any dedicated CLK or FCLK pin. It cannot be driven by internally-generated global signals.

(2) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

(3) This signal is a high-speed differential I/O support SERDES control signal.

Clock Multiplication & Division

Stratix device fast PLLs provide clock synthesis for PLL output ports using *m*/(post scaler) scaling factors. The input clock is multiplied by the *m* feedback factor. Each output port has a unique post scale counter to divide down the high-frequency VCO. There is one multiply divider, *m*, per fast PLL with a range of 1 to 32. There are two post scale L dividers for regional and/or LVDS interface clocks, and *g*0 counter for global clock output port; all range from 1 to 32.

In the case of a high-speed differential interface, the designer can set the output counter to 1 to allow the high-speed VCO frequency to drive the SERDES. When used for clocking the SERDES, the *m* counter can range from 1 to 30. The VCO frequency is equal to f_{IN}×m, where VCO frequency must be between 300 and 1000 MHz.

External Clock Inputs

Each fast PLL supports single-ended or differential inputs for source synchronous transmitters or for general-purpose use. Source-synchronous receivers support differential clock inputs. The fast PLL inputs are fed by `CLK[0..3]`, `CLK[8..11]`, and `FPLL[7..10]CLK` pins, as shown in Figure 2–50 on page 2–83.

Table 2–22 shows the I/O standards supported by fast PLL input pins.

Table 2–22. Fast PLL Port I/O Standards (Part 1 of 2)

I/O Standard	Input	
	INCLK	PLLENABLE
LVTTL	✓	✓
LVCMOS	✓	✓
2.5 V	✓	
1.8 V	✓	
1.5 V	✓	
3.3-V PCI		
3.3-V PCI-X 1.0		
LVPECL	✓	
3.3-V PCML	✓	
LVDS	✓	
HyperTransport technology	✓	
Differential HSTL	✓	
Differential SSTL		
3.3-V GTL		
3.3-V GTL+	✓	
1.5-V HSTL class I	✓	
1.5-V HSTL class II		
1.8-V HSTL class I	✓	
1.8-V HSTL class II		
SSTL-18 class I	✓	
SSTL-18 class II		
SSTL-2 class I	✓	

Table 2–22. Fast PLL Port I/O Standards (Part 2 of 2)

I/O Standard	Input	
	INCLK	PLLENABLE
SSTL-2 class II	✓	
SSTL-3 class I	✓	
SSTL-3 class II	✓	
AGP (1× and 2×)		
CTT	✓	

Table 2–23 shows the performance on each of the fast PLL clock inputs when using LVDS, LVPECL, 3.3-V PCML, or HyperTransport technology.

Table 2–23. LVDS Performance on Fast PLL Input

Fast PLL Clock Input	Maximum Input Frequency (MHz)
CLK0, CLK2, CLK9, CLK11, FPLL7CLK, FPLL8CLK, FPLL9CLK, FPLL10CLK	717 *(1)*
CLK1, CLK3, CLK8, CLK10	500

Note to Table 2–23:

(1) See "Maximum Input & Output Clock Rates" on page 4–78.

External Clock Outputs

Each fast PLL supports differential or single-ended outputs for source-synchronous transmitters or for general-purpose external clocks. There are no dedicated external clock output pins. Any I/O pin can be driven by the fast PLL global or regional outputs as an external output pin. The I/O standards supported by any particular bank determines what standards are possible for an external clock output driven by the fast PLL in that bank.

Phase Shifting

Stratix device fast PLLs have advanced clock shift capability that enables programmable phase shifts. Designers can enter a phase shift (in degrees or time units) for each PLL clock output port or for all outputs together in one shift. Designers can perform phase shifting in time units with a resolution range of 125 to 416.66 ps. This resolution is a function of the VCO period, with the finest step being equal to an eighth (°0.125) of the VCO period.

Control Signals

The fast PLL has the same `lock` output, `pllenable` input, and `areset` input control signals as the enhanced PLL.

If the input clock stops and causes the PLL to lose lock, then the PLL must be reset for correct phase shift operation.

For more information on high-speed differential I/O support, see "High-Speed Differential I/O Support" on page 2–128.

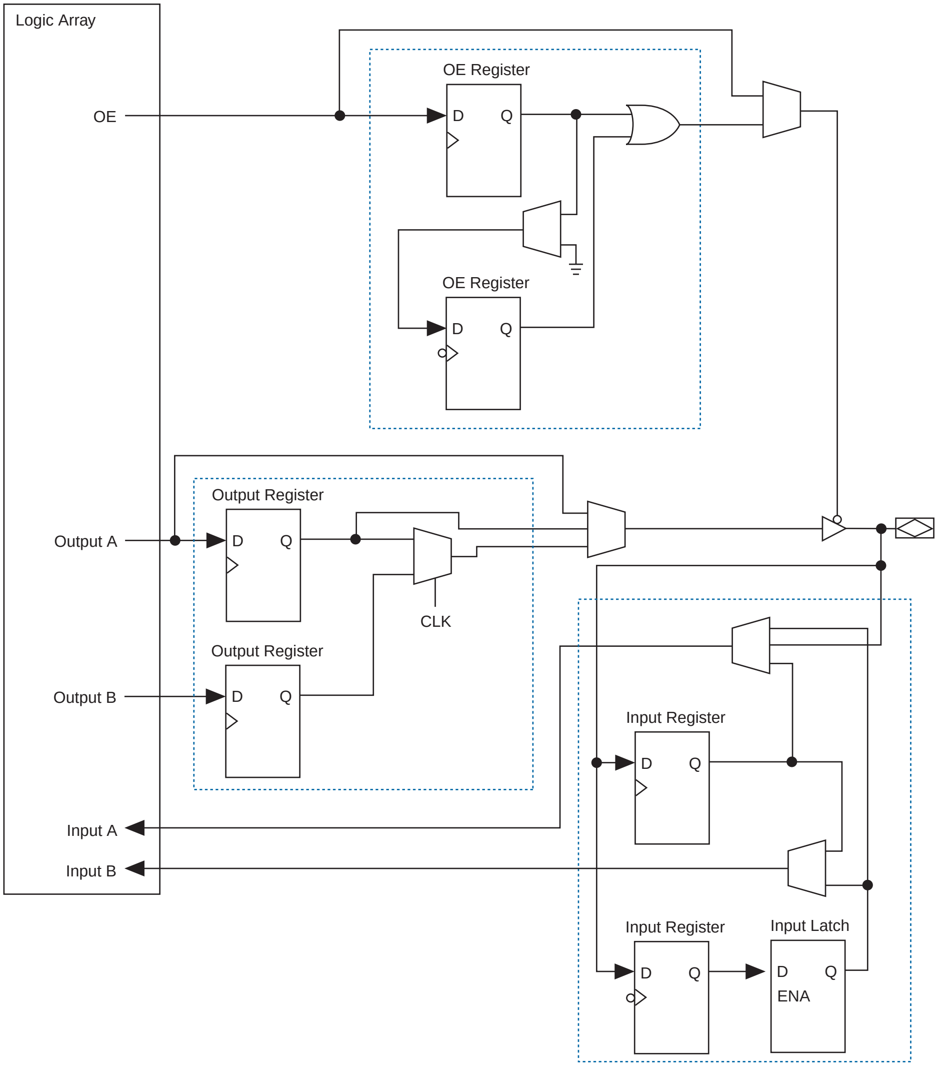
I/O Structure

IOEs provide many features, including:

- Dedicated differential and single-ended I/O buffers
- 3.3-V, 64-bit, 66-MHz PCI compliance
- 3.3-V, 64-bit, 133-MHz PCI-X 1.0 compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Differential on-chip termination for LVDS I/O standard
- Programmable pull-up during configuration
- Output drive strength control
- Slew-rate control
- Tri-state buffers
- Bus-hold circuitry
- Programmable pull-up resistors
- Programmable input and output delays
- Open-drain outputs
- DQ and DQS I/O pins
- Double-data rate (DDR) Registers

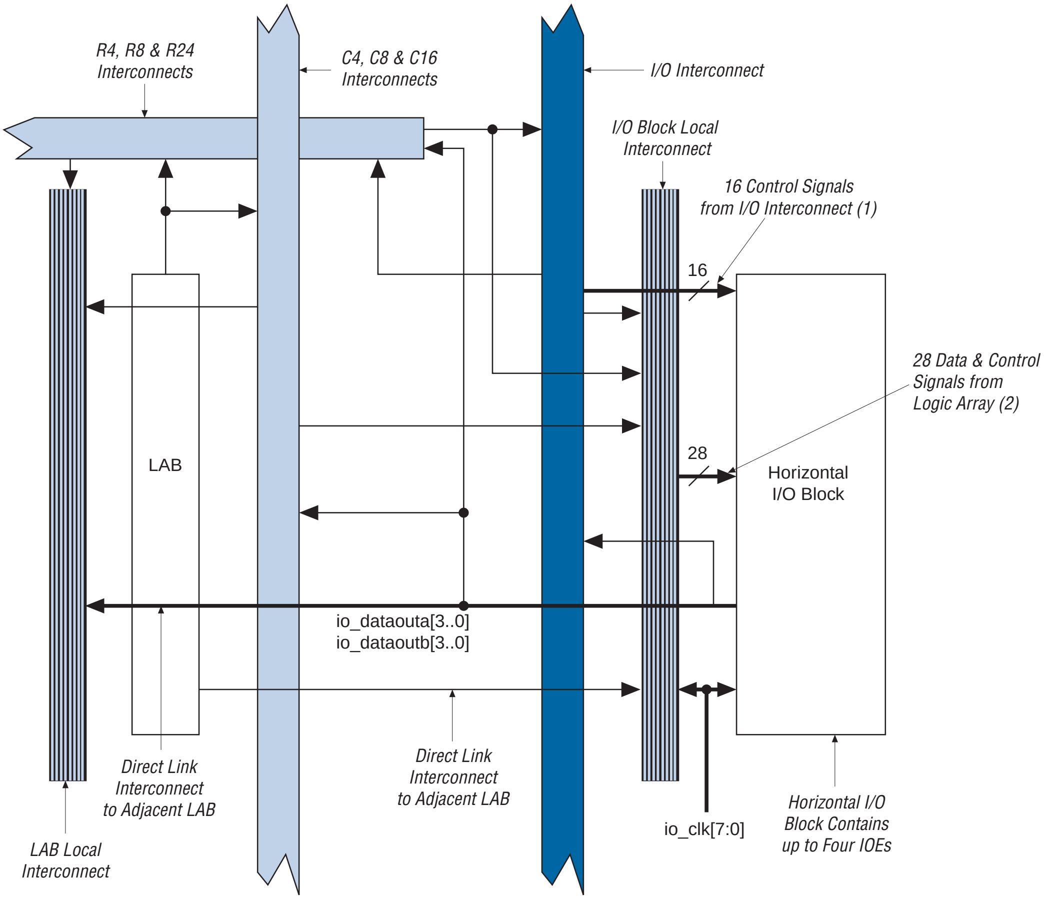
The IOE in Stratix devices contains a bidirectional I/O buffer, six registers, and a latch for a complete embedded bidirectional single data rate or DDR transfer. Figure 2–59 shows the Stratix IOE structure. The IOE contains two input registers (plus a latch), two output registers, and two output enable registers. The design can use both input registers and the latch to capture DDR input and both output registers to drive DDR outputs. Additionally, the design can use the output enable (OE) register for fast clock-to-output enable timing. The negative edge-clocked OE register is used for DDR SDRAM interfacing. The Quartus II software automatically duplicates a single OE register that controls multiple output or bidirectional pins.

Figure 2–59. Stratix IOE Structure



The IOEs are located in I/O blocks around the periphery of the Stratix device. There are up to four IOEs per row I/O block and six IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 2–60 shows how a row I/O block connects to the logic array. Figure 2–61 shows how a column I/O block connects to the logic array.

Figure 2–60. Row I/O Block Connection to the Interconnect

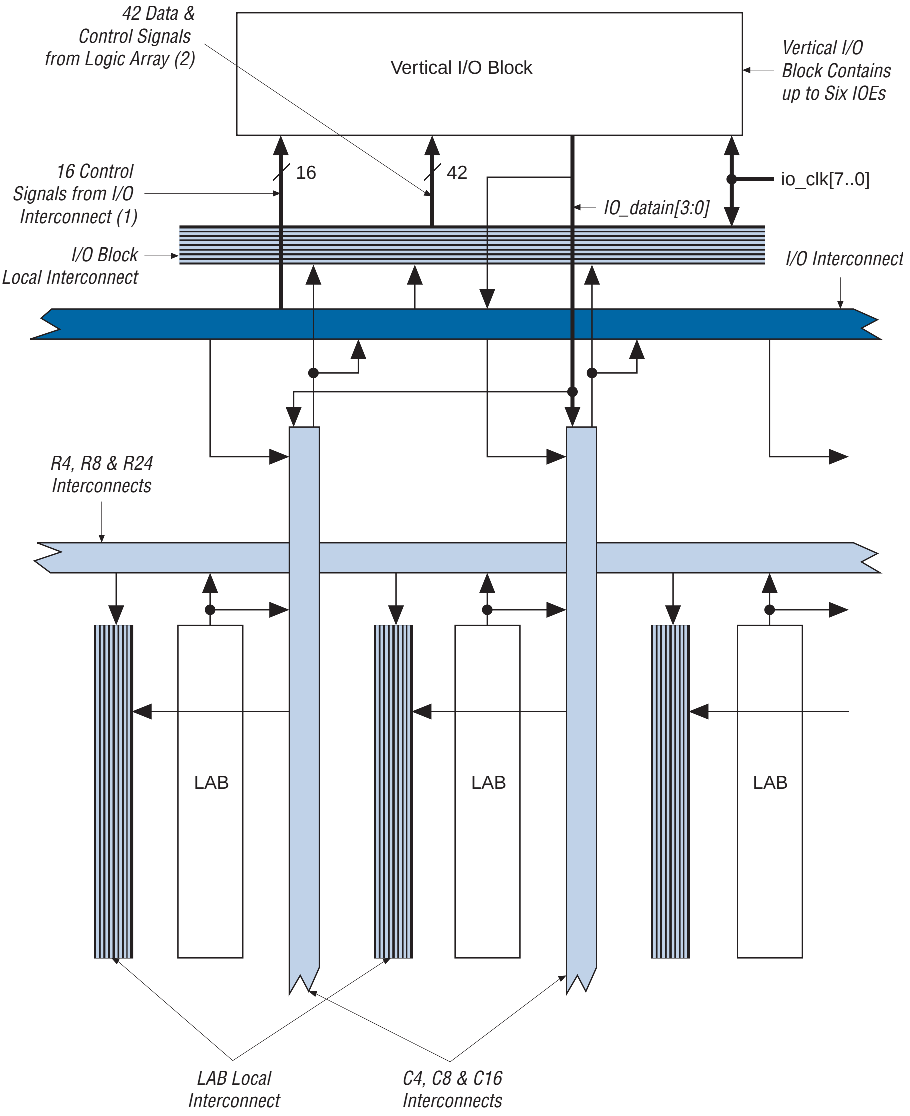


Notes to Figure 2–60:

(1) The 16 control signals are composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_clk[3..0]`, and four clear signals `io_bclr[3..0]`.

(2) The 28 data and control signals consist of eight data out lines: four lines each for DDR applications `io_dataouta[3..0]` and `io_dataoutb[3..0]`, four output enables `io_coe[3..0]`, four input clock enables `io_cce_in[3..0]`, four output clock enables `io_cce_out[3..0]`, four clocks `io_cclk[3..0]`, and four clear signals `io_cclr[3..0]`.

Figure 2–61. Column I/O Block Connection to the Interconnect



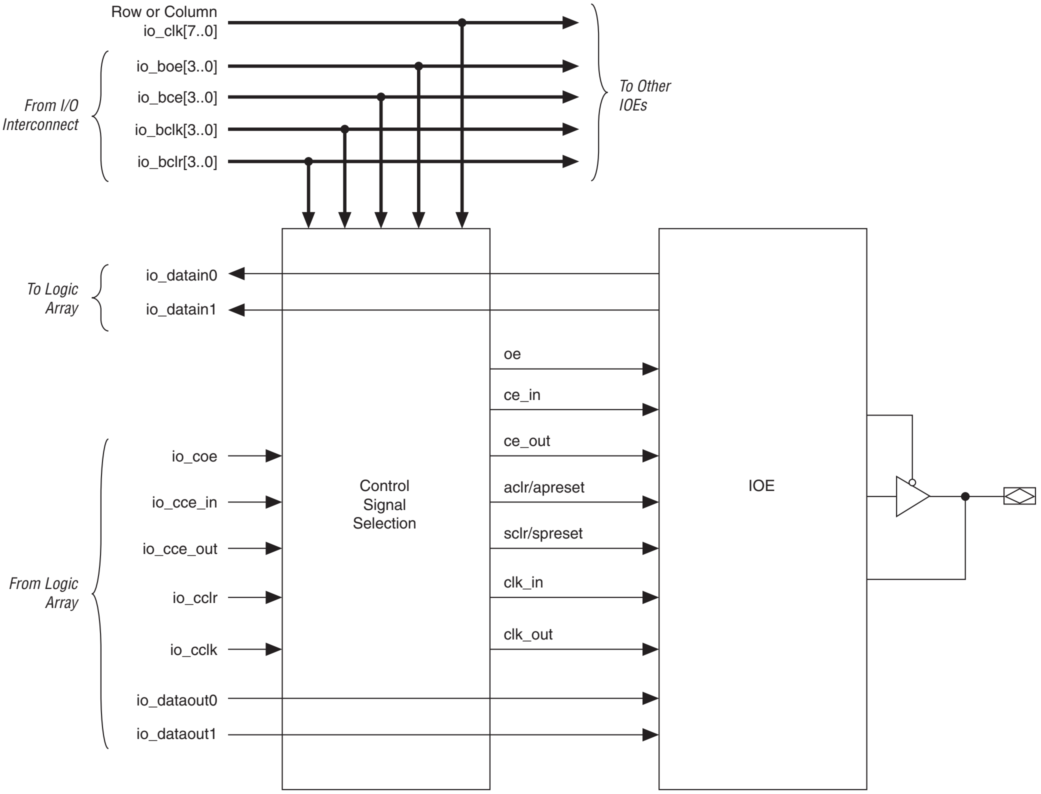
Notes to Figure 2–61:

(1) The 16 control signals are composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`.

(2) The 42 data and control signals consist of 12 data out lines; six lines each for DDR applications `io_dataouta[5..0]` and `io_dataoutb[5..0]`, six output enables `io_coe[5..0]`, six input clock enables `io_cce_in[5..0]`, six output clock enables `io_cce_out[5..0]`, six clocks `io_cclk[5..0]`, and six clear signals `io_cclr[5..0]`.

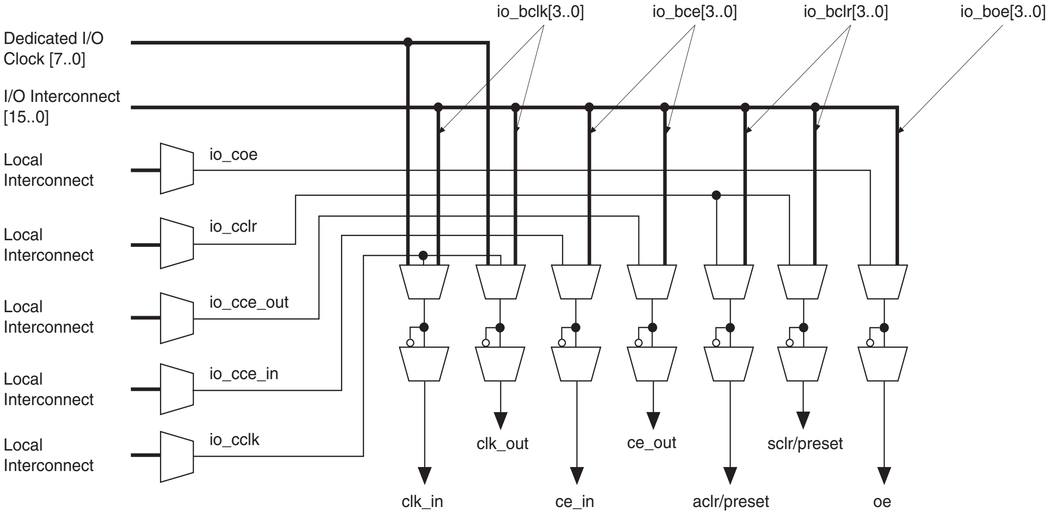
Stratix devices have an I/O interconnect similar to the R4 and C4 interconnect to drive high-fanout signals to and from the I/O blocks. There are 16 signals that drive into the I/O blocks composed of four output enables `io_boe[3..0]`, four clock enables `io_bce[3..0]`, four clocks `io_bclk[3..0]`, and four clear signals `io_bclr[3..0]`. The pin's `datain` signals can drive the IO interconnect, which in turn drives the logic array or other I/O blocks. In addition, the control and data signals can be driven from the logic array, providing a slower but more flexible routing resource. The row or column IOE clocks, `io_clk[7..0]`, provide a dedicated routing resource for low-skew, high-speed clocks. I/O clocks are generated from regional, global, or fast regional clocks (see "PLLs & Clock Networks" on page 2–71). Figure 2–62 illustrates the signal paths through the I/O block.

Figure 2–62. Signal Path through the I/O Block



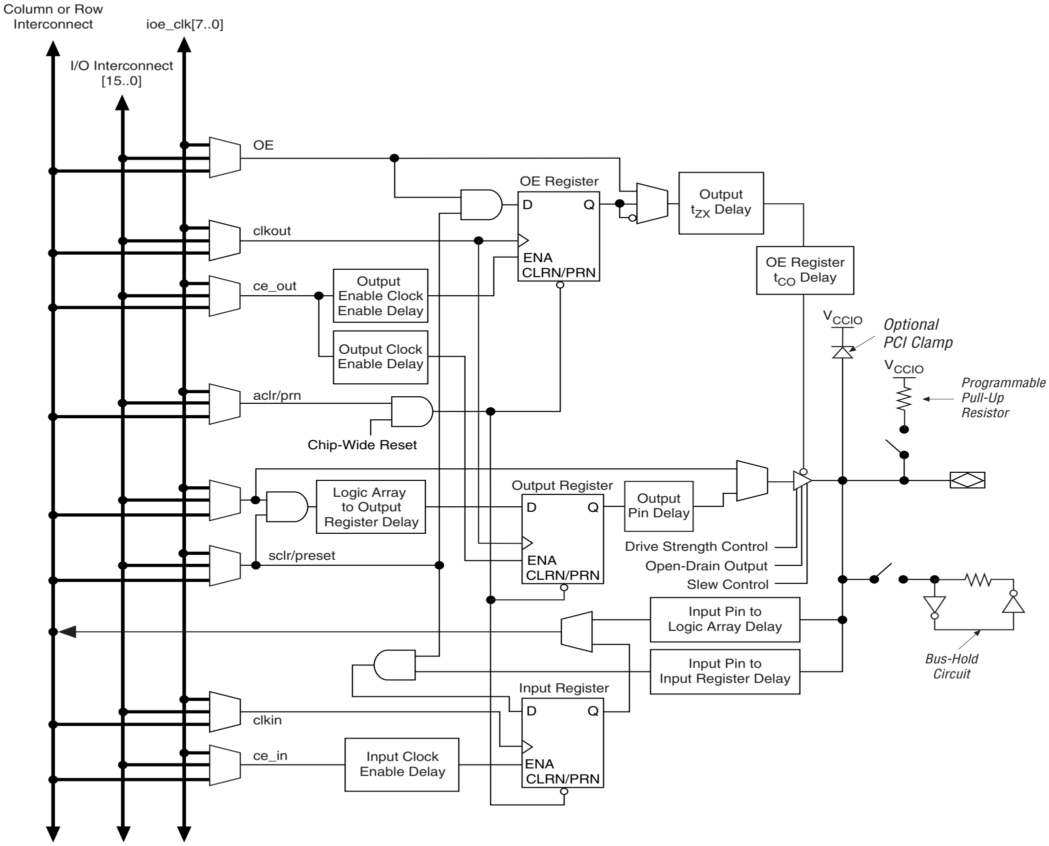
Each IOE contains its own control signal selection for the following control signals: `oe`, `ce_in`, `ce_out`, `aclr/preset`, `sclr/preset`, `clk_in`, and `clk_out`. Figure 2–63 illustrates the control signal selection.

Figure 2–63. Control Signal Selection per IOE



In normal bidirectional operation, the input register can be used for input data requiring fast setup times. The input register can have its own clock input and clock enable separate from the OE and output registers. The output register can be used for data requiring fast clock-to-output performance. The OE register can be used for fast clock-to-output enable timing. The OE and output register share the same clock source and the same clock enable source from local interconnect in the associated LAB, dedicated I/O clocks, and the column and row interconnects. Figure 2–64 shows the IOE in bidirectional configuration.

Figure 2–64. Stratix IOE in Bidirectional I/O Configuration Note (1)



Note to Figure 2–64:

(1) All input signals to the IOE can be inverted at the IOE.

The Stratix device IOE includes programmable delays that can be activated to ensure zero hold times, input IOE register-to-logic array register transfers, or logic array-to-output IOE register transfers.

A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay. Programmable delays exist for decreasing input-pin-to-logic-array and IOE input register delays. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output and/or output enable registers. A programmable delay exists to increase the t_{ZX} delay to the output pin, which is required for ZBT interfaces. Table 2–24 shows the programmable delays for Stratix devices.

Table 2–24. Stratix Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin to logic array delay	Decrease input delay to internal cells
Input pin to input register delay	Decrease input delay to input register
Output pin delay	Increase delay to output pin
Output enable register t_{CO} delay	Increase delay to output enable pin
Output t_{ZX} delay	Increase t_{ZX} delay to output pin
Output clock enable delay	Increase output clock enable delay
Input clock enable delay	Increase input clock enable delay
Logic array to output register delay	Decrease input delay to output register
Output enable clock enable delay	Increase output enable clock enable delay

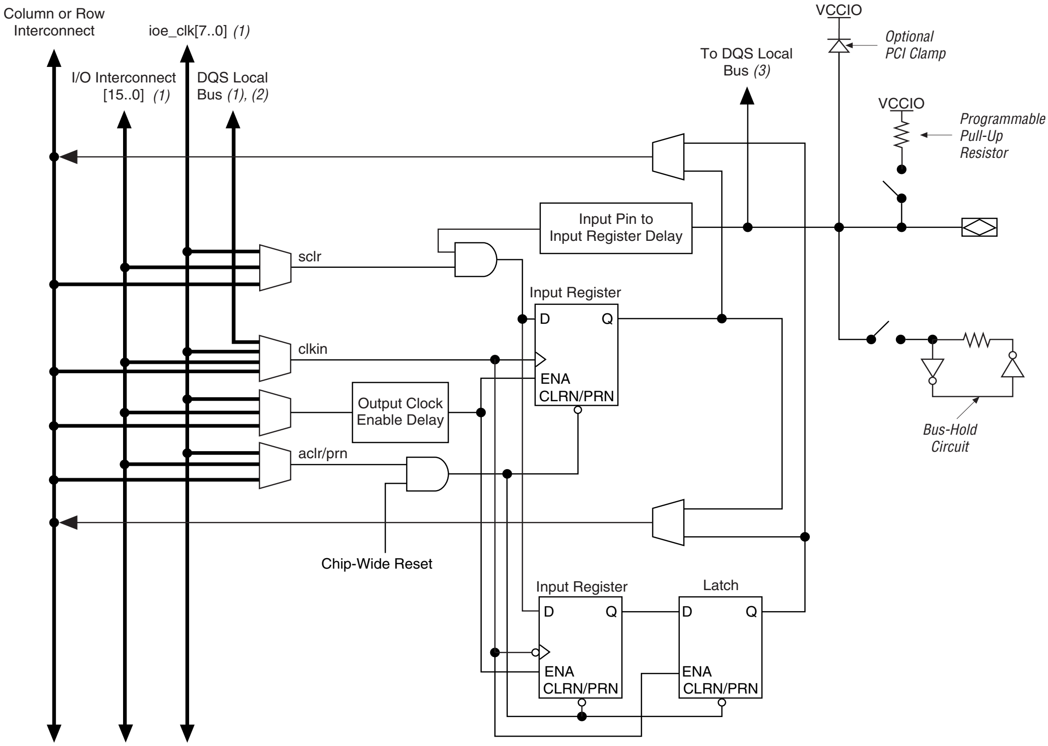
The IOE registers in Stratix devices share the same source for clear or preset. The designer can program preset or clear for each individual IOE. The designer can also program the registers to power up high or low after configuration is complete. If programmed to power up low, an asynchronous clear can control the registers. If programmed to power up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of another device's active-low input upon power-up. If one register in an IOE uses a preset or clear signal then all registers in the IOE must use that same signal if they require preset or clear. Additionally a synchronous reset signal is available to the designer for the IOE registers.

Double-Data Rate I/O Pins

Stratix devices have six registers in the IOE, which support DDR interfacing by clocking data on both positive and negative clock edges. The IOEs in Stratix devices support DDR inputs, DDR outputs, and bidirectional DDR modes.

When using the IOE for DDR inputs, the two input registers clock double rate input data on alternating edges. An input latch is also used within the IOE for DDR input acquisition. The latch holds the data that is present during the clock high times. This allows both bits of data to be synchronous with the same clock edge (either rising or falling). Figure 2–65 shows an IOE configured for DDR input. Figure 2–66 shows the DDR input timing diagram.

Figure 2–65. Stratix IOE in DDR Input I/O Configuration Note (1)



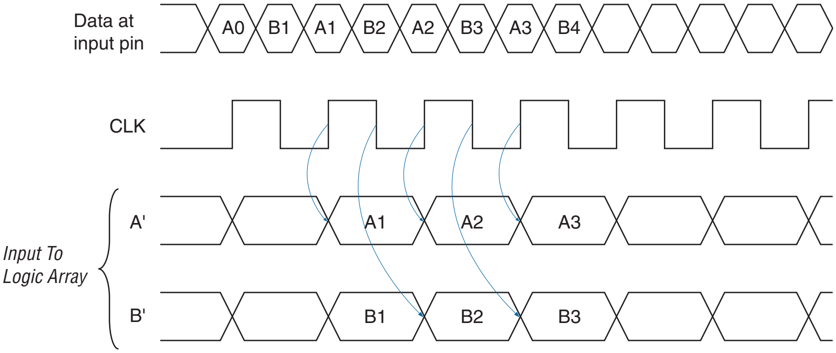
Notes to Figure 2–65:

(1) All input signals to the IOE can be inverted at the IOE.

(2) This signal connection is only allowed on dedicated DQ function pins.

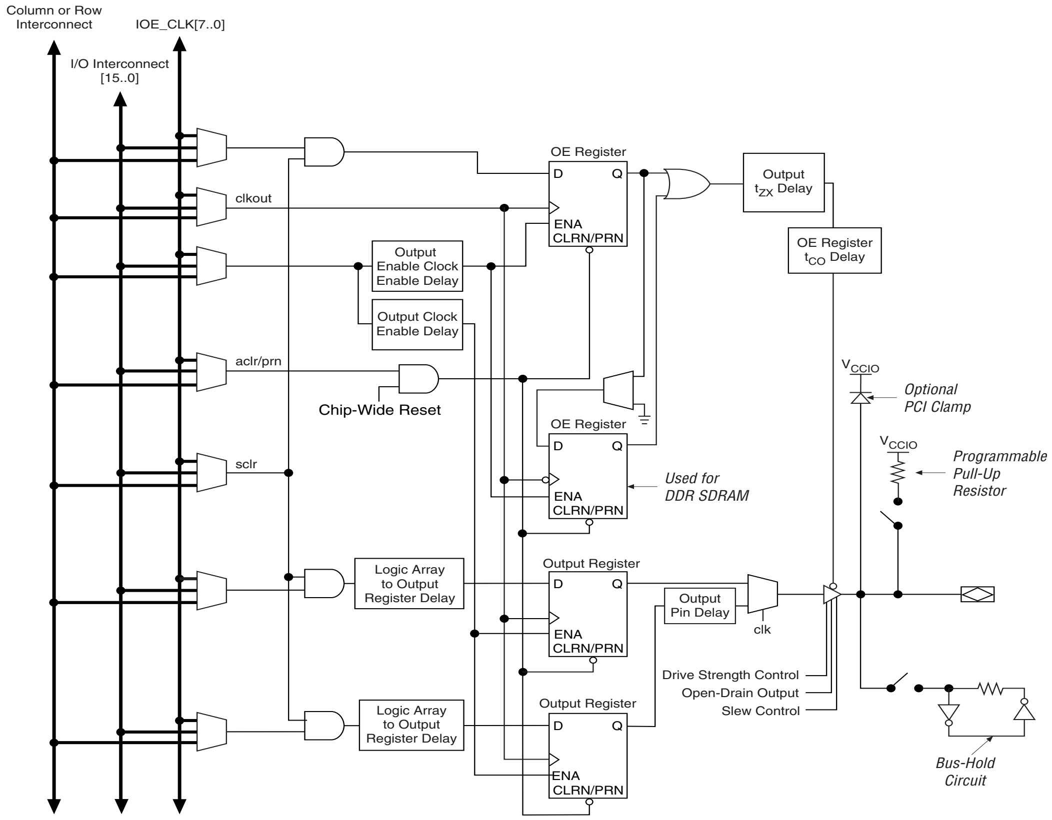
(3) This signal is for dedicated DQS function pins only.

Figure 2–66. Input Timing Diagram in DDR Mode



When using the IOE for DDR outputs, the two output registers are configured to clock two data paths from LEs on rising clock edges. These output registers are multiplexed by the clock to drive the output pin at a °2 rate. One output register clocks the first bit out on the clock high time, while the other output register clocks the second bit out on the clock low time. Figure 2–67 shows the IOE configured for DDR output. Figure 2–68 shows the DDR output timing diagram.

Figure 2–67. Stratix IOE in DDR Output I/O Configuration Notes (1), (2)

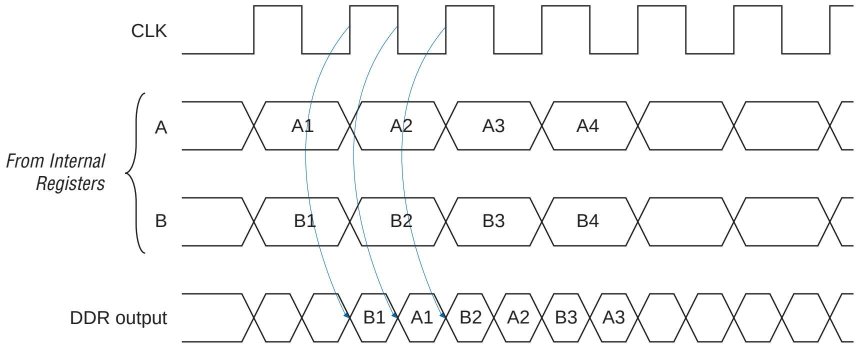


Notes to Figure 2–67:

(1) All input signals to the IOE can be inverted at the IOE.

(2) The tristate is by default active high. It can, however, be designed to be active low.

Figure 2–68. Output Timing Diagram in DDR Mode



The Stratix IOE operates in bidirectional DDR mode by combining the DDR input and DDR output configurations. Stratix device I/O pins transfer data on a DDR bidirectional bus to support DDR SDRAM. The negative-edge-clocked OE register holds the OE signal inactive until the falling edge of the clock. This is done to meet DDR SDRAM timing requirements.

External RAM Interfacing

Stratix devices support DDR SDRAM at up to 200 MHz (400-Mbps data rate) through dedicated phase-shift circuitry, QDR and QDRII SRAM interfaces up to 167 MHz, and ZBT SRAM interfaces up to 200 MHz. Stratix devices also provide preliminary support for reduced latency DRAM II (RLDRAM II) at rates up to 200 MHz through the dedicated phase-shift circuitry.

☞ In addition to the required signals for external memory interfacing, Stratix devices offer the optional clock enable signal. By default the Quartus II software sets the clock enable signal high, which tells the output register to update with new values. The output registers hold their own values if the design sets the clock enable signal low. See Figure 2–64.

To find out more about the DDR SDRAM specification, see the JEDEC web site (**www.jedec.org**). For information on memory controller megafunctions for Stratix devices, see the Altera web site (**www.altera.com**). See *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices* for more information on DDR SDRAM interface in Stratix. Also see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices* and *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

Tables 2–25 and 2–26 show the performance specification for DDR SDRAM, RLDRAM II, QDR SRAM, QDRII SRAM, and ZBT SRAM interfaces in EP1S10 through EP1S40 devices and in EP1S60 and EP1S80 devices. The DDR SDRAM and QDR SRAM numbers in Table 2–25 have been verified with hardware characterization with third-party DDR SDRAM and QDR SRAM devices over temperature and voltage extremes.

Table 2–25. External RAM Support in EP1S10 through EP1S40 Devices

DDR Memory Type	I/O Standard	Maximum Clock Rate (MHz)						
		-5 Speed Grade	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade	
		Flip-Chip	Flip-Chip	Wire-Bond	Flip-Chip	Wire-Bond	Flip-Chip	Wire-Bond
DDR SDRAM *(1)*, *(2)*	SSTL-2	200	167	133	133	100	100	100
DDR SDRAM - side banks *(2)*, *(3)*, *(4)*	SSTL-2	150	133	110	133	100	100	100
RLDRAM II *(4)*	1.8-V HSTL	200	*(5)*	*(5)*	*(5)*	*(5)*	*(5)*	*(5)*
QDR SRAM *(6)*	1.5-V HSTL	167	167	133	133	100	100	100
QDRII SRAM *(6)*	1.5-V HSTL	200	167	133	133	100	100	100
ZBT SRAM *(7)*	LVTTL	200	200	200	167	167	133	133

Notes to Table 2–25:

(1) These maximum clock rates apply if the Stratix device uses DQS phase-shift circuitry to interface with DDR SDRAM. DQS phase-shift circuitry is only available in the top and bottom I/O banks (I/O banks 3, 4, 7, and 8).

(2) For more information on DDR SDRAM, see *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices.*

(3) DDR SDRAM is supported on the Stratix device side I/O banks (I/O banks 1, 2, 5, and 6) without dedicated DQS phase-shift circuitry. The read DQS signal is ignored in this mode.

(4) These performance specifications are preliminary.

(5) This device does not support RLDRAM II.

(6) For more information on QDR or QDRII SRAM, see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

(7) For more information on ZBT SRAM, see *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

Table 2–26. External RAM Support in EP1S60 & EP1S80 Devices

DDR Memory Type	I/O Standard	Maximum Clock Rate (MHz)		
		-5 Speed Grade	-6 Speed Grade	-7 Speed Grade
DDR SDRAM *(1)*, *(2)*	SSTL-2	167	167	133
DDR SDRAM - side banks *(2)*, *(3)*	SSTL-2	150	133	133
QDR SRAM *(4)*	1.5-V HSTL	133	133	133
QDRII SRAM *(4)*	1.5-V HSTL	167	167	133
ZBT SRAM *(5)*	LVTTL	200	200	167

Notes to Table 2–26:

(1) These maximum clock rates apply if the Stratix device uses DQS phase-shift circuitry to interface with DDR SDRAM. DQS phase-shift circuitry is only available in the top and bottom I/O banks (I/O banks 3, 4, 7, and 8).

(2) For more information on DDR SDRAM, see *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices.*

(3) DDR SDRAM is supported on the Stratix device side I/O banks (I/O banks 1, 2, 5, and 6) without dedicated DQS phase-shift circuitry. The read DQS signal is ignored in this mode. Numbers are preliminary.

(4) For more information on QDR or QDRII SRAM, see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

(5) For more information on ZBT SRAM, see *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

In addition to six I/O registers and one input latch in the IOE for interfacing to these high-speed memory interfaces, Stratix devices also have dedicated circuitry for interfacing with DDR SDRAM. In every Stratix device, the I/O banks at the top (I/O banks 3 and 4) and bottom (I/O banks 7 and 8) of the device support DDR SDRAM up to 200 MHz. These pins support DQS signals with DQ bus modes of ×8, ×16, or ×32.

Table 2–27 shows the number of DQ and DQS buses that are supported per device.

Table 2–27. DQS & DQ Bus Mode Support (Part 1 of 2) Note (1)

Device	Package	Number of ×8 Groups	Number of ×16 Groups	Number of ×32 Groups
EP1S10	672-pin BGA 672-pin FineLine BGA	12 *(2)*	0	0
	484-pin FineLine BGA 780-pin FineLine BGA	16 *(3)*	0	4
EP1S20	484-pin FineLne BGA	18*(4)*	7 *(5)*	4
	672-pin BGA 672-pin FineLine BGA	16*(3)*	7 *(5)*	4
	780-pin FineLine BGA	20	7 *(5)*	4

Table 2–27. DQS & DQ Bus Mode Support (Part 2 of 2) Note (1)

Device	Package	Number of ×8 Groups	Number of ×16 Groups	Number of ×32 Groups
EP1S25	672-pin BGA 672-pin FineLine BGA	16 *(3)*	8	4
	780-pin FineLine BGA 1,020-pin FineLine BGA	20	8	4
EP1S30	956-pin BGA 780-pin FineLine BGA 1,020-pin FineLine BGA	20	8	4
EP1S40	956-pin BGA 1,020-pin FineLine BGA 1,508-pin FineLine BGA	20	8	4
EP1S60	956-pin BGA 1,020-pin FineLine BGA 1,508-pin FineLine BGA	20	8	4
EP1S80	956-pin BGA 1,508-pin FineLine BGA 1,923-pin FineLine BGA	20	8	4

Notes to Table 2–27:

(1) See the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter in the *Stratix Device Handbook, Volume 2* for V_{REF} guidelines.

(2) These packages have six groups in I/O banks 3 and 4 and six groups in I/O banks 7 and 8.

(3) These packages have eight groups in I/O banks 3 and 4 and eight groups in I/O banks 7 and 8.

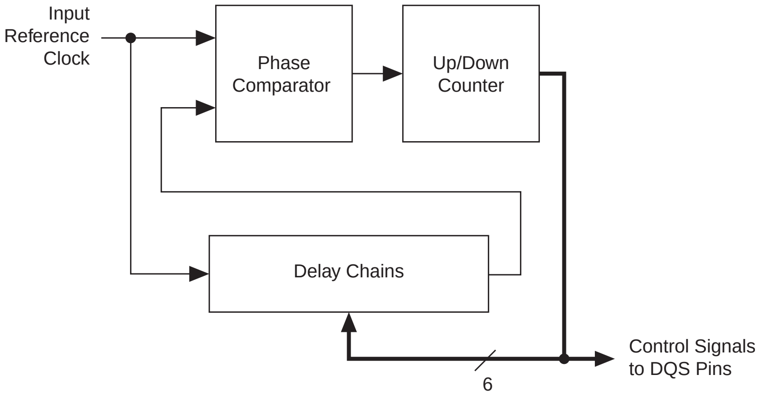
(4) This package has nine groups in I/O banks 3 and 4 and nine groups in I/O banks 7 and 8.

(5) These packages have three groups in I/O banks 3 and 4 and four groups in I/O banks 7 and 8.

A compensated delay element on each DQS pin automatically aligns input DQS synchronization signals with the data window of their corresponding DQ data signals. The DQS signals drive a local DQS bus in the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and is used to clock DQ input registers with the DQS signal.

Two separate single phase-shifting reference circuits are located on the top and bottom of the Stratix device. Each circuit is driven by a system reference clock through the `CLK` pins that is the same frequency as the DQS signal. Clock pins `CLK[15..12]p` feed the phase-shift circuitry on the top of the device and clock pins `CLK[7..4]p` feed the phase-shift circuitry on the bottom of the device. The phase-shifting reference circuit on the top of the device controls the compensated delay elements for all 10 DQS pins located at the top of the device. The phase-shifting reference circuit on the bottom of the device controls the compensated delay elements for all 10 DQS pins located on the bottom of the device. All 10 delay elements (DQS signals) on either the top or bottom of the device shift by the same degree amount. For example, all 10 DQS pins on the top of the device can be shifted by 90° and all 10 DQS pins on the bottom of the device can be shifted by 72°. The reference circuits require a maximum of 256 system reference clock cycles to set the correct phase on the DQS delay elements. Figure 2–69 illustrates the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 2–69. Simplified Diagram of the DQS Phase-Shift Circuitry



See the *External Memory Interfaces* chapter in the *Stratix Device Handbook, Volume 2* for more information on external memory interfaces.

Programmable Drive Strength

The output buffer for each Stratix device I/O pin has a programmable drive strength control for certain I/O standards. The LVTTL and LVCMOS standard has several levels of drive strength that the user can control. SSTL-3 class I and II, SSTL-2 class I and II, HSTL class I and II, and 3.3-V GTL+ support a minimum setting, the lowest drive strength that guarantees the I_{OH}/I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

Table 2–28 shows the possible settings for the I/O standards with drive strength control.

Table 2–28. Programmable Drive Strength

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA)
3.3-V LVTTL	24 *(1)*, 16, 12, 8, 4
3.3-V LVCMOS	24 *(2)*, 12 *(1)*, 8, 4, 2
2.5-V LVTTL/LVCMOS	16 *(1)*, 12, 8, 2
1.8-V LVTTL/LVCMOS	12 *(1)*, 8, 2
1.5-V LVCMOS	8 *(1)*, 4, 2
GTL/GTL+ 1.5-V HSTL class I and II 1.8-V HSTL Class I and II SSTL-3 class I and II SSTL-2 class I and II SSTL-18 class I and II	Support max and min strength

Notes to Table 2–28:

(1) This is the Quartus II software default current setting.

(2) I/O banks 1, 2, 5, and 6 do not support this setting.

Quartus II software version 4.2 and later will report current strength as “PCI Compliant” for 3.3-V PCI, 3.3-V PCI-X 1.0, and Compact PCI I/O standards.

Stratix devices support series on-chip termination (OCT) using programmable drive strength. For more information, contact your Altera Support Representative.

Open-Drain Output

Stratix devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write-enable signals) that can be asserted by any of several devices.

Slew-Rate Control

The output buffer for each Stratix device I/O pin has a programmable output slew-rate control that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Each

I/O pin has an individual slew-rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

Bus Hold

Each Stratix device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not needed to hold a signal level when the bus is tri-stated.

Table 2–29 shows bus hold support for different pin types.

Table 2–29. Bus Hold Support

Pin Type	Bus Hold
I/O pins	✓
`CLK[15..0]`	
`CLK[0,1,2,3,8,9,10,11]`	
`FCLK`	✓
`FPLL[7..10]CLK`	

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the programmable pull-up option cannot be used. Disable the bus-hold feature when using open-drain outputs with the GTL+ I/O standard or when the I/O pin has been configured for differential signals.

The bus-hold circuitry uses a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ to weakly pull the signal level to the last-driven state. Table 4–32 on page 4–15 gives the specific sustaining current driven through this resistor and overdrive current used to identify the next-driven input level. This information is provided for each V_{CCIO} voltage level.

The bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each Stratix device I/O pin provides an optional programmable pull-up resistor during user mode. If this feature is enabled for an I/O pin, the pull-up resistor (typically 25 kΩ) weakly holds the output to the V_{CCIO} level of the output pin's bank. Table 2–30 shows which pin types support the weak pull-up resistor feature.

Table 2–30. Programmable Weak Pull-Up Resistor Support

Pin Type	Programmable Weak Pull-Up Resistor
I/O pins	✓
`CLK[15..0]`	
`FCLK`	✓
`FPLL[7..10]CLK`	
Configuration pins	
JTAG pins	✓ *(1)*

Note to Table 2–30:

(1) TDO pins do not support programmable weak pull-up resistors.

Advanced I/O Standard Support

Stratix device IOEs support the following I/O standards:

- LVTTL
- LVCMOS
- 1.5 V
- 1.8 V
- 2.5 V
- 3.3-V PCI
- 3.3-V PCI-X 1.0
- 3.3-V AGP (1° and 2°)
- LVDS
- LVPECL
- 3.3-V PCML
- HyperTransport
- Differential HSTL (on input/output clocks only)
- Differential SSTL (on output column clock pins only)
- GTL/GTL+
- 1.5-V HSTL class I and II

- 1.8-V HSTL Class I and II
- SSTL-3 class I and II
- SSTL-2 class I and II
- SSTL-18 class I and II
- CTT

Table 2–31 describes the I/O standards supported by Stratix devices.

Table 2–31. Stratix Supported I/O Standards

I/O Standard	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
1.5 V	Single-ended	N/A	1.5	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
3.3-V PCI-X 1.0	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
LVPECL	Differential	N/A	3.3	N/A
3.3-V PCML	Differential	N/A	3.3	N/A
HyperTransport	Differential	N/A	2.5	N/A
Differential HSTL *(1)*	Differential	0.75	1.5	0.75
Differential SSTL *(2)*	Differential	1.25	2.5	1.25
GTL	Voltage-referenced	0.8	N/A	1.20
GTL+	Voltage-referenced	1.0	N/A	1.5
1.5-V HSTL class I and II	Voltage-referenced	0.75	1.5	0.75
1.8-V HSTL class I and II	Voltage-referenced	0.9	1.8	0.9
SSTL-18 class I and II	Voltage-referenced	0.90	1.8	0.90
SSTL-2 class I and II	Voltage-referenced	1.25	2.5	1.25
SSTL-3 class I and II	Voltage-referenced	1.5	3.3	1.5
AGP (1× and 2°)	Voltage-referenced	1.32	3.3	N/A
CTT	Voltage-referenced	1.5	3.3	1.5

Notes to Table 2–31:

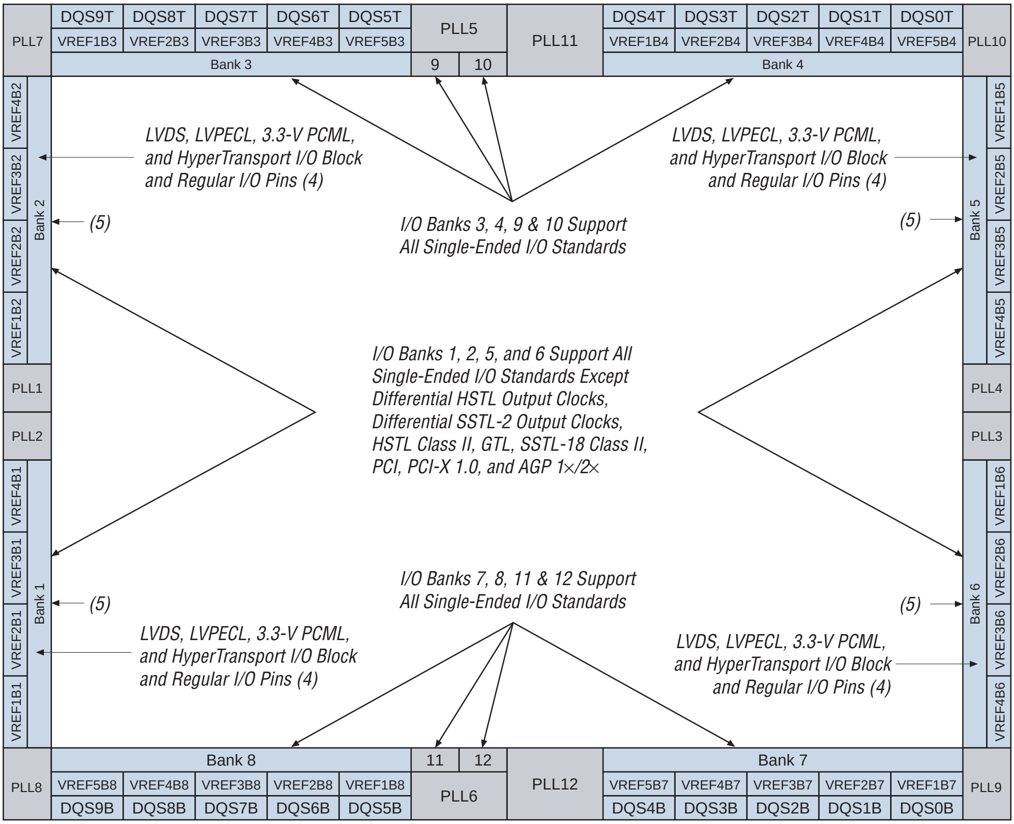
(1) This I/O standard is only available on input and output clock pins.

(2) This I/O standard is only available on output column clock pins.

For more information on I/O standards supported by Stratix devices, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix Device Handbook, Volume 2*.

Stratix devices contain eight I/O banks in addition to the four enhanced PLL external clock out banks, as shown in Figure 2–70. The four I/O banks on the right and left of the device contain circuitry to support high-speed differential I/O for LVDS, LVPECL, 3.3-V PCML, and HyperTransport inputs and outputs. These banks support all I/O standards listed in Table 2–31 except PCI I/O pins or PCI-X 1.0, GTL, SSTL-18 Class II, and HSTL Class II outputs. The top and bottom I/O banks support all single-ended I/O standards. Additionally, Stratix devices support four enhanced PLL external clock output banks, allowing clock output capabilities such as differential support for SSTL and HSTL. Table 2–32 shows I/O standard support for each I/O bank.

***Figure 2–70. Stratix I/O Banks** Notes (1), (2), (3)*



Notes to Figure 2–70:

(1) Figure 2–70 is a top view of the silicon die. This will correspond to a top-down view for non-flip-chip packages, but will be a reverse view for flip-chip packages.

(2) Figure 2–70 is a graphic representation only. See the device pin-outs on the web (**www.altera.com**) and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) If the high-speed differential I/O pins are not used for high-speed differential signaling, they can support all of the I/O standards except HSTL class I and II, GTL, SSTL-18 Class II, PCI, PCI-X 1.0, and AGP 1×/2×.

(5) For guidelines for placing single-ended I/O pads next to differential I/O pads, see the *Selectable I/O Standards in Stratix and Stratix GX Devices* chapter in the *Stratix Device Handbook, Volume 2*.

Table 2–32 shows I/O standard support for each I/O bank.

Table 2–32. I/O Support by Bank (Part 1 of 2)

I/O Standard	Top & Bottom Banks (3, 4, 7 & 8)	Left & Right Banks (1, 2, 5 & 6)	Enhanced PLL External Clock Output Banks (9, 10, 11 & 12)
LVTTL	✓	✓	✓
LVCMOS	✓	✓	✓
2.5 V	✓	✓	✓
1.8 V	✓	✓	✓
1.5 V	✓	✓	✓
3.3-V PCI	✓		✓
3.3-V PCI-X 1.0	✓		✓
LVPECL		✓	✓
3.3-V PCML		✓	✓
LVDS		✓	✓
HyperTransport technology		✓	✓
Differential HSTL (clock inputs)	✓	✓	
Differential HSTL (clock outputs)			✓
Differential SSTL (clock outputs)			✓
3.3-V GTL	✓		✓
3.3-V GTL+	✓	✓	✓
1.5-V HSTL class I	✓	✓	✓
1.5-V HSTL class II	✓		✓
1.8-V HSTL class I	✓	✓	✓
1.8-V HSTL class II	✓		✓
SSTL-18 class I	✓	✓	✓
SSTL-18 class II	✓		✓
SSTL-2 class I	✓	✓	✓
SSTL-2 class II	✓	✓	✓
SSTL-3 class I	✓	✓	✓

Table 2–32. I/O Support by Bank (Part 2 of 2)

I/O Standard	Top & Bottom Banks (3, 4, 7 & 8)	Left & Right Banks (1, 2, 5 & 6)	Enhanced PLL External Clock Output Banks (9, 10, 11 & 12)
SSTL-3 class II	✓	✓	✓
AGP (1× and 2×)	✓		✓
CTT	✓	✓	✓

Each I/O bank has its own `VCCIO` pins. A single device can support 1.5-, 1.8-, 2.5-, and 3.3-V interfaces; each bank can support a different standard independently. Each bank also has dedicated `VREF` pins to support any one of the voltage-referenced standards (such as SSTL-3) independently.

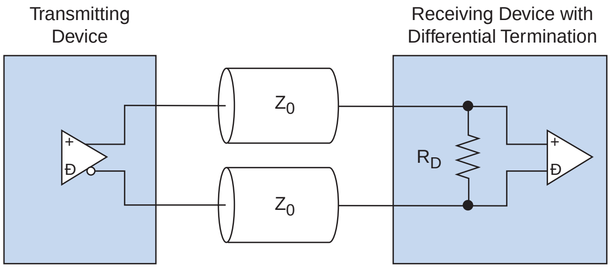
Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. Each bank can support one voltage-referenced I/O standard. For example, when V_{CCIO} is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

Differential On-Chip Termination

Stratix devices provide differential on-chip termination (LVDS I/O standard) to reduce reflections and maintain signal integrity. Differential on-chip termination simplifies board design by minimizing the number of external termination resistors required. Termination can be placed inside the package, eliminating small stubs that can still lead to reflections. The internal termination is designed using transistors in the linear region of operation.

Stratix devices support internal differential termination with a nominal resistance value of 137.5 Ω for LVDS input receiver buffers. LVPECL signals require an external termination resistor. Figure 2–71 shows the device with differential termination.

Figure 2–71. LVDS Input Differential On-Chip Termination



I/O banks on the left and right side of the device support LVDS receiver (far-end) differential termination.

Table 2–33 shows the Stratix device differential termination support.

Table 2–33. Differential Termination Supported by I/O Banks

Differential Termination Support	I/O Standard Support	Top & Bottom Banks (3, 4, 7 & 8)	Left & Right Banks (1, 2, 5 & 6)
Differential termination *(1)*, *(2)*	LVDS		✓

Notes to Table 2–33:

(1) Clock pin `CLK0`, `CLK2`, `CLK9`, `CLK11`, and pins `FPLL[7..10]CLK` do not support differential termination.

(2) Differential termination is only supported for LVDS because of a 3.3-V V_{CCIO}.

Table 2–34 shows the termination support for different pin types.

Table 2–34. Differential Termination Support Across Pin Types

Pin Type	R_D
Top and bottom I/O banks (3, 4, 7, and 8)	
`DIFFIO_RX[]`	✓
`CLK[0,2,9,11],CLK[4-7],CLK[12-15]`	
`CLK[1,3,8,10]`	✓
`FCLK`	
`FPLL[7..10]CLK`	

The differential on-chip resistance at the receiver input buffer is 118 Ω ±20 %.

However, there is additional resistance present between the device ball and the input of the receiver buffer, as shown in Figure 2–72. This resistance is because of package trace resistance (which can be calculated as the resistance from the package ball to the pad) and the parasitic layout metal routing resistance (which is shown between the pad and the intersection of the on-chip termination and input buffer).

Figure 2–72. Differential Resistance of LVDS Differential Pin Pair (R_D)

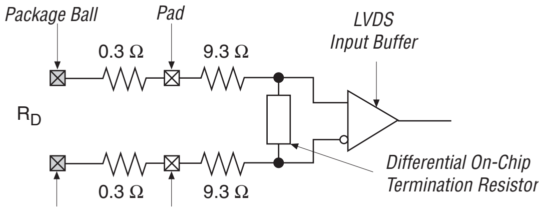


Table 2–35 defines the specification for internal termination resistance for commercial devices.

Table 2–35. Differential On-Chip Termination

Symbol	Description	Conditions	Resistance			Unit
			Min	Typ	Max	
R_D *(2)*	Internal differential termination for LVDS	Commercial *(1)*, *(3)*	110	135	165	W
		Industrial *(2)*, *(3)*	100	135	170	W

Notes to Table 2–35:

(1) Data measured over minimum conditions (T_j = 0 C, V_{CCIO} +5%) and maximum conditions (T_j = 85 C, V_{CCIO} = –5%).

(2) Data measured over minimum conditions (T_j = –40 C, V_{CCIO} +5%) and maximum conditions (T_j = 100 C, V_{CCIO} = –5%).

(3) LVDS data rate is supported for 840 Mbps using internal differential termination.

MultiVolt I/O Interface

The Stratix architecture supports the MultiVolt I/O interface feature, which allows Stratix devices in all packages to interface with systems of different supply voltages.

The Stratix `VCCINT` pins must always be connected to a 1.5-V power supply. With a 1.5-V V_{CCINT} level, input pins are 1.5-V, 1.8-V, 2.5-V, and 3.3-V tolerant. The `VCCIO` pins can be connected to either a 1.5-V, 1.8-V, 2.5-V, or 3.3-V power supply, depending on the output requirements.

The output levels are compatible with systems of the same voltage as the power supply (i.e., when `VCCIO` pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When `VCCIO` pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 2–36 summarizes Stratix MultiVolt I/O support.

Table 2–36. Stratix MultiVolt I/O Support Note (1)

V_{CCIO} (V)	Input Signal (5)					Output Signal (6)				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓ (2)	✓ (2)		✓				
1.8	✓ (2)	✓	✓ (2)	✓ (2)		✓ (3)	✓			
2.5			✓	✓		✓ (3)	✓ (3)	✓		
3.3			✓ (2)	✓	✓ (4)	✓ (3)	✓ (3)	✓ (3)	✓	✓

Notes to Table 2–36:

(1) To drive inputs higher than V_{CCIO} but less than 4.1 V, disable the PCI clamping diode. However, to drive 5.0-V inputs to the device, enable the PCI clamping diode to prevent V_I from rising above 4.0 V.

(2) The input pin current may be slightly higher than the typical value.

(3) Although V_{CCIO} specifies the voltage necessary for the Stratix device to drive out, a receiving device powered at a different level can still interface with the Stratix device if it has inputs that tolerate the V_{CCIO} value.

(4) Stratix devices can be 5.0-V tolerant with the use of an external resistor and the internal PCI clamp diode.

(5) This is the external signal that is driving the Stratix device.

(6) This represents the system voltage that Stratix supports when a VCCIO pin is connected to a specific voltage level. For example, when VCCIO is 3.3 V and if the I/O standard is LVTTL/LVCMOS, the output high of the signal coming out from Stratix is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

High-Speed Differential I/O Support

Stratix devices contain dedicated circuitry for supporting differential standards at speeds up to 840 Mbps. The following differential I/O standards are supported in the Stratix device: LVDS, LVPECL, HyperTransport, and 3.3-V PCML.

There are four dedicated high-speed PLLs in the EP1S10 to EP1S25 devices and eight dedicated high-speed PLLs in the EP1S30 to EP1S80 devices to multiply reference clocks and drive high-speed differential SERDES channels.

See the Stratix device pin-outs at **www.altera.com** for additional high speed DIFFIO pin information for Stratix devices.

Table 2–37 shows the number of channels that each fast PLL can clock in EP1S10, EP1S20, and EP1S25 devices. Tables 2–38 through Table 2–41 show this information for EP1S30, EP1S40, EP1S60, and EP1S80 devices.

Table 2–37. EP1S10, EP1S20 & EP1S25 Device Differential Channels (Part 1 of 2) Note (1)

Device	Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs			
					PLL 1	PLL 2	PLL 3	PLL 4
EP1S10	484-pin FineLine BGA	Transmitter *(2)*	20	840 *(4)*	5	5	5	5
				840 *(3)*	10	10	10	10
		Receiver	20	840 *(4)*	5	5	5	5
				840 *(3)*	10	10	10	10
	672-pin FineLine BGA 672-pin BGA	Transmitter *(2)*	36	624 *(4)*	9	9	9	9
				624 *(3)*	18	18	18	18
		Receiver	36	624 *(4)*	9	9	9	9
				624 *(3)*	18	18	18	18
	780-pin FineLine BGA	Transmitter *(2)*	44	840 *(4)*	11	11	11	11
				840 *(3)*	22	22	22	22
		Receiver	44	840 *(4)*	11	11	11	11
				840 *(3)*	22	22	22	22
EP1S20	484-pin FineLine BGA	Transmitter *(2)*	24	840 *(4)*	6	6	6	6
				840 *(3)*	12	12	12	12
		Receiver	20	840 *(4)*	5	5	5	5
				840 *(3)*	10	10	10	10
	672-pin FineLine BGA 672-pin BGA	Transmitter *(2)*	48	624 *(4)*	12	12	12	12
				624 *(3)*	24	24	24	24
		Receiver	50	624 *(4)*	13	12	12	13
				624 *(3)*	25	25	25	25
	780-pin FineLine BGA	Transmitter *(2)*	66	840 *(4)*	17	16	16	17
				840 *(3)*	33	33	33	33
		Receiver	66	840 *(4)*	17	16	16	17
				840 *(3)*	33	33	33	33

Table 2–37. EP1S10, EP1S20 & EP1S25 Device Differential Channels (Part 2 of 2) Note (1)

Device	Package	Transmitter/ Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs			
					PLL 1	PLL 2	PLL 3	PLL 4
EP1S25	672-pin FineLine BGA 672-pin BGA	Transmitter *(2)*	56	624 *(4)*	14	14	14	14
				624 *(3)*	28	28	28	28
		Receiver	58	624 *(4)*	14	15	15	14
				624 *(3)*	29	29	29	29
	780-pin FineLine BGA	Transmitter *(2)*	70	840 *(4)*	18	17	17	18
				840 *(3)*	35	35	35	35
		Receiver	66	840 *(4)*	17	16	16	17
				840 *(3)*	33	33	33	33
	1,020-pin FineLine BGA	Transmitter *(2)*	78	840 *(4)*	19	20	20	19
				840 *(3)*	39	39	39	39
		Receiver	78	840 *(4)*	19	20	20	19
				840 *(3)*	39	39	39	39

Notes to Table 2–37:

(1) The first row for each transmitter or receiver reports the number of channels driven directly by the PLL. The second row below it shows the maximum channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 484-pin FineLine BGA EP1S10 device, PLL 1 can drive a maximum of five channels at 840 Mbps or a maximum of 10 channels at 840 Mbps. The Quartus II software may also merge receiver and transmitter PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

(2) The number of channels listed includes the transmitter clock output (`tx_outclock`) channel. If the design requires a DDR clock, it can use an extra data channel.

(3) These channels span across two I/O banks per side of the device. When a center PLL clocks channels in the opposite bank on the same side of the device it is called cross-bank PLL support. Both center PLLs can clock cross-bank channels simultaneously if, for example, PLL_1 is clocking all RX channels and PLL_2 is clocking all TX channels. You cannot have two adjacent PLLs simultaneously clocking cross-bank RX channels or two adjacent PLLs simultaneously clocking TX channels. Cross-bank allows for all receiver channels on one side of the device to be clocked on one clock while all transmitter channels on the device are clocked on the other center PLL. Crossbank PLLs are supported at full-speed, 840 Mbps. For wire-bond devices, the full-speed is 624 Mbps.

(4) These values show the channels available for each PLL without crossing another bank.

When you span two I/O banks using cross-bank support, you can route only two loadenable signals total between the PLLs. When you enable `rx_data_align`, you use both `rxloadena` and `txloadena` of a PLL. That leaves no `loadena` for the second PLL.

The only way you can use the `rx_data_align` is if one of the following is true:

- The RX PLL is only clocking RX channels (no resources for TX)
- If all channels can fit in one I/O bank

Table 2–38. EP1S30 Differential Channels *Note (1)*

Package	Transmitter /Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs *(2), (3)*			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
780-pin FineLine BGA	Transmitter *(4)*	70	840	18	17	17	18	*(6)*	*(6)*	*(6)*	*(6)*
			840 *(5)*	35	35	35	35	*(6)*	*(6)*	*(6)*	*(6)*
	Receiver	66	840	17	16	16	17	*(6)*	*(6)*	*(6)*	*(6)*
			840 *(5)*	33	33	33	33	*(6)*	*(6)*	*(6)*	*(6)*
956-pin BGA	Transmitter *(4)*	80	840	19	20	20	19	20	20	20	20
			840 *(5)*	39	39	39	39	20	20	20	20
	Receiver	80	840	20	20	20	20	19	20	20	19
			840 *(5)*	40	40	40	40	19	20	20	19
1,020-pin FineLine BGA	Transmitter *(4)*	80 (2) *(7)*	840	19 (1)	20	20	19 (1)	20	20	20	20
			840 *(5)*,*(8)*	39 (1)	39 (1)	39 (1)	39 (1)	20	20	20	20
	Receiver	80 (2) *(7)*	840	20	20	20	20	19 (1)	20	20	19 (1)
			840 *(5)*,*(8)*	40	40	40	40	19 (1)	20	20	19 (1)

Table 2–39. EP1S40 Differential Channels (Part 1 of 2) *Note (1)*

Package	Transmitter /Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs *(2), (3)*			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
780-pin FineLine BGA	Transmitter *(4)*	68	840	18	16	16	18	*(6)*	*(6)*	*(6)*	*(6)*
			840 *(5)*	34	34	34	34	*(6)*	*(6)*	*(6)*	*(6)*
	Receiver	66	840	17	16	16	17	*(6)*	*(6)*	*(6)*	*(6)*
			840 *(5)*	33	33	33	33	*(6)*	*(6)*	*(6)*	*(6)*
956-pin BGA	Transmitter *(4)*	80	840	18	17	17	18	20	20	20	20
			840 *(5)*	35	35	35	35	20	20	20	20
	Receiver	80	840	20	20	20	20	18	17	17	18
			840 *(5)*	40	40	40	40	18	17	17	18

Table 2–39. EP1S40 Differential Channels (Part 2 of 2) *Note (1)*

Package	**Transmitter /Receiver**	**Total Channels**	**Maximum Speed (Mbps)**	**Center Fast PLLs**				**Corner Fast PLLs** *(2), (3)*			
				PLL1	**PLL2**	**PLL3**	**PLL4**	**PLL7**	**PLL8**	**PLL9**	**PLL10**
1,020-pin FineLine BGA	Transmitter *(4)*	80 (10) *(7)*	840	18 (2)	17 (3)	17 (3)	18 (2)	20	20	20	20
			840 *(5)*, *(8)*	35 (5)	35 (5)	35 (5)	35 (5)	20	20	20	20
	Receiver	80 (10) *(7)*	840	20	20	20	20	18 (2)	17 (3)	17 (3)	18 (2)
			840 *(5)*, *(8)*	40	40	40	40	18 (2)	17 (3)	17 (3)	18 (2)
1,508-pin FineLine BGA	Transmitter *(4)*	80 (10) *(7)*	840	18 (2)	17 (3)	17 (3)	18 (2)	20	20	20	20
			840 *(5)*, *(8)*	35 (5)	35 (5)	35 (5)	35 (5)	20	20	20	20
	Receiver	80 (10) *(7)*	840	20	20	20	20	18 (2)	17 (3)	17 (3)	18 (2)
			840 *(5)*, *(8)*	40	40	40	40	18 (2)	17 (3)	17 (3)	18 (2)

Table 2–40. EP1S60 Differential Channels (Part 1 of 2) *Note (1)*

Package	**Transmitter /Receiver**	**Total Channels**	**Maximum Speed (Mbps)**	**Center Fast PLLs**				**Corner Fast PLLs** *(2), (3)*			
				PLL1	**PLL2**	**PLL3**	**PLL4**	**PLL7**	**PLL8**	**PLL9**	**PLL10**
956-pin BGA	Transmitter *(4)*	80	840	12	10	10	12	20	20	20	20
			840 *(5)*, *(8)*	22	22	22	22	20	20	20	20
	Receiver	80	840	20	20	20	20	12	10	10	12
			840 *(5)*, *(8)*	40	40	40	40	12	10	10	12
1,020-pin FineLine BGA	Transmitter *(4)*	80 (12) *(7)*	840	12 (2)	10 (4)	10 (4)	12 (2)	20	20	20	20
			840 *(5)*, *(8)*	22 (6)	22 (6)	22 (6)	22 (6)	20	20	20	20
	Receiver	80 (10) *(7)*	840	20	20	20	20	12 (8)	10 (10)	10 (10)	12 (8)
			840 *(5)*, *(8)*	40	40	40	40	12 (8)	10 (10)	10 (10)	12 (8)

Package	Transmitter /Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs (2), (3)			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
1,508-pin FineLine BGA	Transmitter *(4)*	80 (36) *(7)*	840	12 (8)	10 (10)	10 (10)	12 (8)	20	20	20	20
			840 *(5)*,*(8)*	22 (18)	22 (18)	22 (18)	22 (18)	20	20	20	20
	Receiver	80 (36) *(7)*	840	20	20	20	20	12 (8)	10 (10)	10 (10)	12 (8)
			840 *(5)*,*(8)*	40	40	40	40	12 (8)	10 (10)	10 (10)	12 (8)

Table 2–40. EP1S60 Differential Channels (Part 2 of 2) Note (1)

Table 2–41. EP1S80 Differential Channels (Part 1 of 2) *Note (1)*

Package	Transmitter /Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs *(2), (3)*			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10
956-pin BGA	Transmitter *(4)*	80 (40) *(7)*	840	10	10	10	10	20	20	20	20
			840 *(5)*,*(8)*	20	20	20	20	20	20	20	20
	Receiver	80	840	20	20	20	20	10	10	10	10
			840 *(5)*,*(8)*	40	40	40	40	10	10	10	10
1,020-pin FineLine BGA	Transmitter *(4)*	92 (12) *(7)*	840	10 (2)	10 (4)	10 (4)	10 (2)	20	20	20	20
			840 *(5)*,*(8)*	20 (6)	20 (6)	20 (6)	20 (6)	20	20	20	20
	Receiver	90 (10) *(7)*	840	20	20	20	20	10 (2)	10 (3)	10 (3)	10 (2)
			840 *(5)*,*(8)*	40	40	40	40	10 (2)	10 (3)	10 (3)	10 (2)
1,508-pin FineLine BGA	Transmitter *(4)*	80 (72) *(7)*	840	10 (10)	10 (10)	10 (10)	10 (10)	20 (8)	20 (8)	20 (8)	20 (8)
			840 *(5)*,*(8)*	20 (20)	20 (20)	20 (20)	20 (20)	20 (8)	20 (8)	20 (8)	20 (8)
	Receiver	80 (56) *(7)*	840	20	20	20	20	10 (14)	10 (14)	10 (14)	10 (14)
			840 *(5)*,*(8)*	40	40	40	40	10 (14)	10 (14)	10 (14)	10 (14)

Table 2–41. EP1S80 Differential Channels (Part 2 of 2) *Note (1)*

Package	Transmitter /Receiver	Total Channels	Maximum Speed (Mbps)	Center Fast PLLs				Corner Fast PLLs (2), (3)			
				PLL1	PLL2	PLL3	PLL4	PLL7	PLL8	PLL9	PLL10

Notes to Tables 2–38 through 2–41:

(1) The first row for each transmitter or receiver reports the number of channels driven directly by the PLL. The second row below it shows the maximum channels a PLL can drive if cross bank channels are used from the adjacent center PLL. For example, in the 780-pin FineLine BGA EP1S30 device, PLL 1 can drive a maximum of 18 transmitter channels at 840 Mbps or a maximum of 35 transmitter channels at 840 Mbps. The Quartus II software may also merge transmitter and receiver PLLs when a receiver is driving a transmitter. In this case, one fast PLL can drive both the maximum numbers of receiver and transmitter channels.

(2) Some of the channels accessible by the center fast PLL and the channels accessible by the corner fast PLL overlap. Therefore, the total number of channels is not the addition of the number of channels accessible by PLLs 1, 2, 3, and 4 with the number of channels accessible by PLLs 7, 8, 9, and 10. For more information on which channels overlap, see the Stratix device pin-outs at **www.altera.com**.

(3) The corner fast PLLs in this device support a data rate of 840 Mbps for channels labeled “high” speed in the device pin-outs at **www.altera.com**.

(4) The numbers of channels listed include the transmitter clock output (`tx_outclock`) channel. An extra data channel can be used if a DDR clock is needed.

(5) These channels span across two I/O banks per side of the device. When a center PLL clocks channels in the opposite bank on the same side of the device it is called cross-bank PLL support. Both center PLLs can clock cross-bank channels simultaneously if say PLL_1 is clocking all RX channels and PLL_2 is clocking all TX channels. You cannot have two adjacent PLLs simultaneously clocking cross-bank RX channels or two adjacent PLLs simultaneously clocking TX channels. Cross-bank allows for all receiver channels on one side of the device to be clocked on one clock while all transmitter channels on the device are clocked on the other center PLL. Crossbank PLLs are supported at full-speed, 840 Mbps. For wire-bond devices, the full-speed is 624 Mbps.

(6) PLLs 7, 8, 9, and 10 are not available in this device.

(7) The number in parentheses is the number of slow-speed channels, guaranteed to operate at up to 462 Mbps. These channels are independent of the high-speed differential channels. For the location of these channels, see the device pin-outs at **www.altera.com**.

(8) See the Stratix device pin-outs at **www.altera.com**. Channels marked “high” speed are 840 MBps and “low” speed channels are 462 MBps.

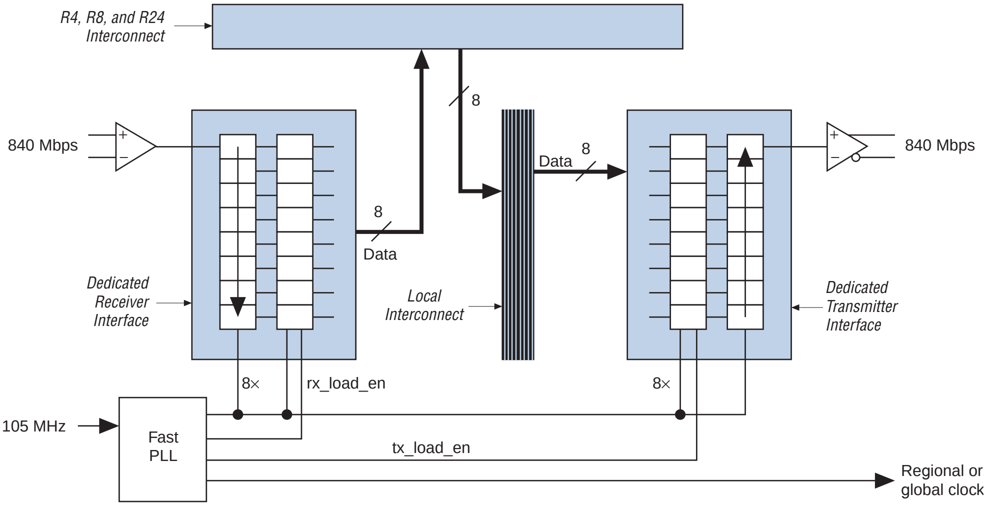
The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications:

- UTOPIA IV
- SPI-4 Phase 2 (POS-PHY Level 4)
- SFI-4
- 10G Ethernet XSBI
- RapidIO
- HyperTransport

Dedicated Circuitry

Stratix devices support source-synchronous interfacing with LVDS, LVPECL, 3.3-V PCML, or HyperTransport signaling at up to 840 Mbps. Stratix devices can transmit or receive serial channels along with a low-speed or high-speed clock. The receiving device PLL multiplies the clock by a integer factor W (W = 1 through 32). For example, a HyperTransport application where the data rate is 800 Mbps and the clock rate is 400 MHz would require that W be set to 2. The SERDES factor J determines the parallel data width to deserialize from receivers or to serialize for transmitters. The SERDES factor J can be set to 4, 7, 8, or 10 and does not have to equal the PLL clock-multiplication W value. For a J factor of 1, the Stratix device bypasses the SERDES block. For a J factor of 2, the Stratix device bypasses the SERDES block, and the DDR input and output registers are used in the IOE. See Figure 2–73.

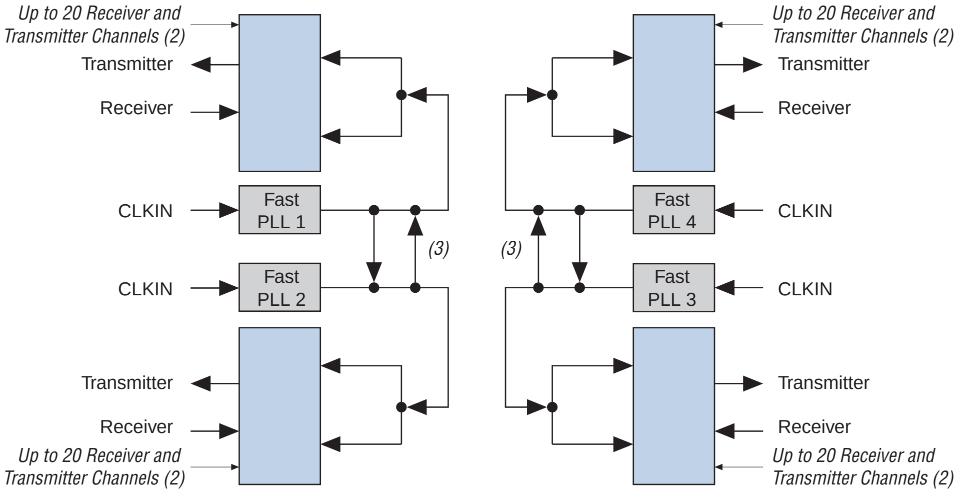
Figure 2–73. High-Speed Differential I/O Receiver / Transmitter Interface Example



An external pin or global or regional clock can drive the fast PLLs, which can output up to three clocks: two multiplied high-speed differential I/O clocks to drive the SERDES block and/or external pin, and a low-speed clock to drive the logic array.

The Quartus II MegaWizard Plug-In Manager only allows the implementation of up to 20 receiver or 20 transmitter channels for each fast PLL. These channels operate at up to 840 Mbps. The receiver and transmitter channels are interleaved such that each I/O bank on the left and right side of the device has one receiver channel and one transmitter channel per LAB row. Figure 2–74 shows the fast PLL and channel layout in EP1S10, EP1S20, and EP1S25 devices. Figure 2–75 shows the fast PLL and channel layout in the EP1S30 to EP1S80 devices.

Figure 2–74. Fast PLL & Channel Layout in the EP1S10, EP1S20 or EP1S25 Devices Note (1)



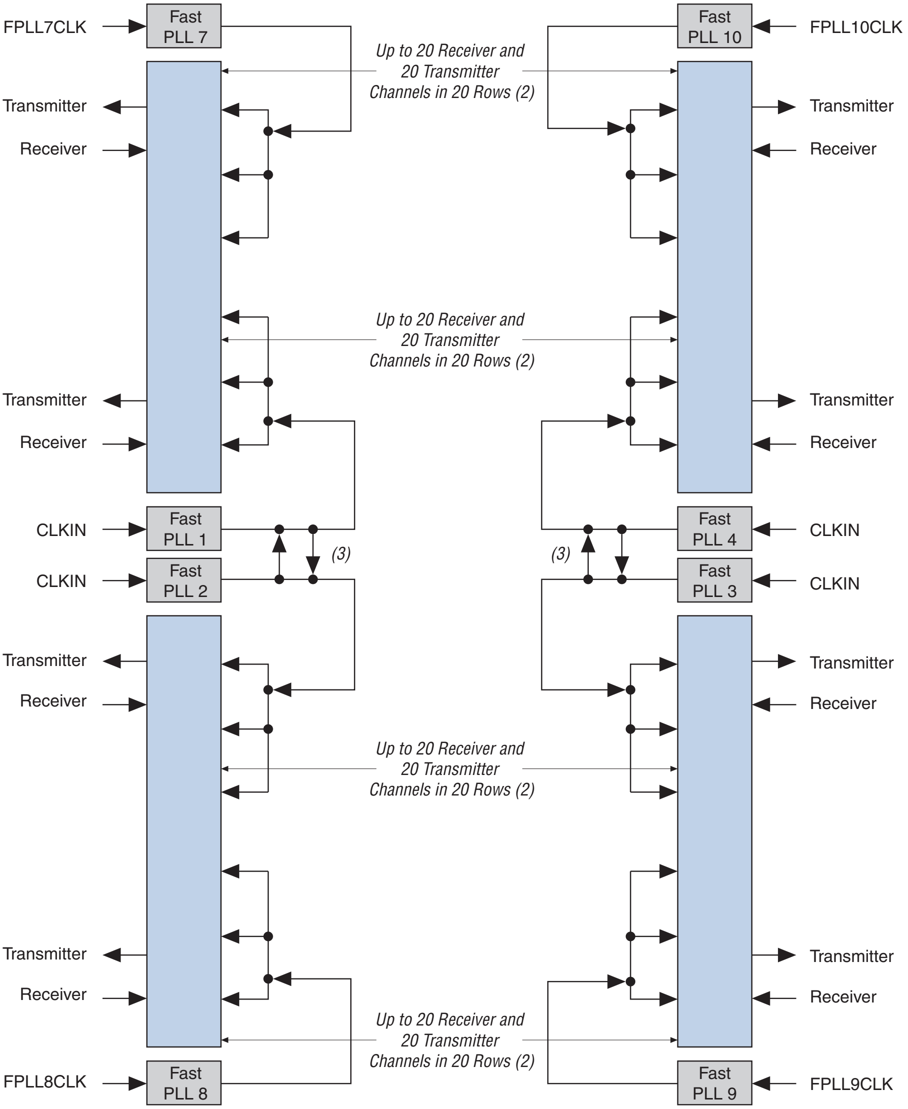
Notes to Figure 2–74:

(1) Wire-bond packages support up to 624 Mbps.

(2) See Table 2–41 for the number of channels each device supports.

(3) There is a multiplexer here to select the PLL clock source. If a PLL uses this multiplexer to clock channels outside of its bank quadrant, those clocked channels support up to 840 Mbps for “high” speed channels and 462 Mbps for “low” speed channels, as labeled in the device pin-outs at **www.altera.com**.

Figure 2–75. Fast PLL & Channel Layout in the EP1S30 to EP1S80 Devices Note (1)



Notes to Figure 2–75:

(1) Wire-bond packages support up to 624 Mbps.

(2) See Table 2–38 through 2–41 for the number of channels each device supports.

(3) There is a multiplexer here to select the PLL clock source. If a PLL uses this multiplexer to clock channels outside of its bank quadrant, those clocked channels support up to 840 Mbps for “high” speed channels and 462 Mbps for “low” speed channels as labeled in the device pin-outs at **www.altera.com**.

The transmitter external clock output is transmitted on a data channel. The `txclk` pin for each bank is located in between data transmitter pins. For °1 clocks (e.g., 622 Mbps, 622 MHz), the high-speed PLL clock bypasses the SERDES to drive the output pins. For half-rate clocks (e.g., 622 Mbps, 311 MHz) or any other even-numbered factor such as 1/4, 1/7, 1/8, or 1/10, the SERDES automatically generates the clock in the Quartus II software.

For systems that require more than four or eight high-speed differential I/O clock domains, a SERDES bypass implementation is possible using IOEs.

Byte Alignment

For high-speed source synchronous interfaces such as POS-PHY 4, XSBI, RapidIO, and HyperTransport technology, the source synchronous clock rate is not a byte- or SERDES-rate multiple of the data rate. Byte alignment is necessary for these protocols since the source synchronous clock does not provide a byte or word boundary since the clock is one half the data rate, not one eighth. The Stratix device's high-speed differential I/O circuitry provides dedicated data realignment circuitry for user-controlled byte boundary shifting. This simplifies designs while saving LE resources. An input signal to each fast PLL can stall deserializer parallel data outputs by one bit period. The designer can use an LE-based state machine to signal the shift of receiver byte boundaries until a specified pattern is detected to indicate byte alignment.

Power Sequencing & Hot Socketing

Because Stratix devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the `VCCIO` and `VCCINT` power supplies may be powered in any order.

Signals can be driven into Stratix devices before and during power up without damaging the device. In addition, Stratix devices do not drive out during power up. Once operating conditions are reached and the device is configured, Stratix devices operate as specified by the user. For more information, see *Hot Socketing* in the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter in the *Stratix Device Handbook, Volume 2*.

Chapter 3. Configuration & Testing

S51003-1.1

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All Stratix® devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1a-1990 specification. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Stratix devices can also use the JTAG port for configuration together with either the Quartus II software or hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**).

Stratix devices support IOE I/O standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode through the `CONFIG_IO` instruction. Designers can use this ability for JTAG testing before configuration when some of the Stratix pins drive or receive from other devices on the board using voltage-referenced standards. Since the Stratix device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming those I/O standards via JTAG allows designers to fully test I/O connection to other devices.

The enhanced PLL reconfiguration bits are part of the JTAG chain before configuration and after power-up. After device configuration, the PLL reconfiguration bits are not part of the JTAG chain.

The JTAG pins support 1.5-V/1.8-V or 2.5-V/3.3-V I/O standards. The `TDO` pin voltage is determined by the V_{CCIO} of the bank where it resides. The `VCCSEL` pin selects whether the JTAG inputs are 1.5-V, 1.8-V, 2.5-V, or 3.3-V compatible.

Stratix devices also use the JTAG port to monitor the logic operation of the device with the SignalTap II embedded logic analyzer. Stratix devices support the JTAG instructions shown in Table 3–1.

Table 3–1. Stratix JTAG Instructions

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST *(1)*	00 0000 0000	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE to be serially shifted out of `TDO`.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between `TDI` and `TDO`, allowing the IDCODE to be serially shifted out of `TDO`.
`HIGHZ` *(1)*	00 0000 1011	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
`CLAMP` *(1)*	00 0000 1010	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring an Stratix device via the JTAG port with a MasterBlaster™, ByteBlasterMV™, or ByteBlaster™ II download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor or JRunner.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the `nCONFIG` pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, after, or during configuration. Stops configuration if executed during configuration. Once issued, the `CONFIG_IO` instruction will hold `nSTATUS` low to reset the configuration device. `nSTATUS` is held low until the device is reconfigured.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

Note to Table 3–1:

(1) Bus hold and weak pull-up resistor features override the high-impedance state of `HIGHZ`, `CLAMP`, and `EXTEST`.

The Stratix device instruction register length is 10 bits and the USERCODE register length is 32 bits. Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for Stratix devices.

Table 3–2. Stratix Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EP1S10	1,317
EP1S20	1,797
EP1S25	2,157
EP1S30	2,253
EP1S40	2,529
EP1S60	3,129
EP1S80	3,777

Table 3–3. 32-Bit Stratix Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP1S10	0000	0010 0000 0000 0001	000 0110 1110	1
EP1S20	0000	0010 0000 0000 0010	000 0110 1110	1
EP1S25	0000	0010 0000 0000 0011	000 0110 1110	1
EP1S30	0000	0010 0000 0000 0100	000 0110 1110	1
EP1S40	0000	0010 0000 0000 0101	000 0110 1110	1
EP1S60	0000	0010 0000 0000 0110	000 0110 1110	1
EP1S80	0000	0010 0000 0000 0111	000 0110 1110	1

Notes to Tables 3–2 and 3–3:

(1) The most significant bit (MSB) is on the left.

(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 3–1 shows the timing requirements for the JTAG signals.

Figure 3–1. Stratix JTAG Waveforms

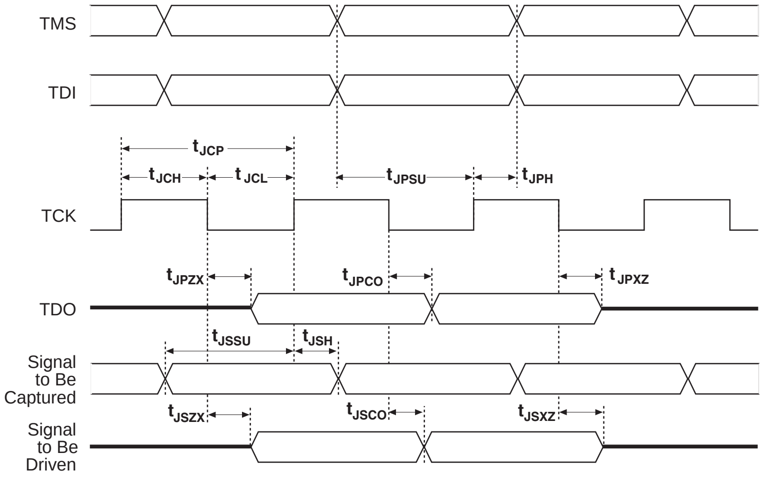


Table 3–4 shows the JTAG timing parameters and values for Stratix devices.

Table 3–4. Stratix JTAG Timing Parameters & Values

Symbol	Parameter	Min	Max	Unit
t_{JCP}	`TCK` clock period	100		ns
t_{JCH}	`TCK` clock high time	50		ns
t_{JCL}	`TCK` clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		35	ns
t_{JSZX}	Update register high impedance to valid output		35	ns
t_{JSXZ}	Update register valid output to high impedance		35	ns

For more information on JTAG, see the following documents:

- *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
- *Jam Programming & Test Language Specification*

SignalTap II Embedded Logic Analyzer

Stratix devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. A designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

Configuration

The logic, circuitry, and interconnects in the Stratix architecture are configured with CMOS SRAM elements. Stratix devices are reconfigurable and are 100% tested prior to shipment. As a result, the designer does not have to generate test vectors for fault coverage purposes, and can instead focus on simulation and design verification. In addition, the designer does not need to manage inventories of different ASIC designs. Stratix devices can be configured on the board for the specific functionality required.

Stratix devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable configuration devices that configure Stratix devices via a serial data stream. Stratix devices can be configured in under 100 ms using 8-bit parallel data at 100 MHz. The Stratix device's optimized interface allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Stratix devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy. After a Stratix device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

Operating Modes

The Stratix architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. Designers can perform in-field upgrades by distributing new configuration files either within the system or remotely.

`PORSEL` is a dedicated input pin used to select POR delay times of 2 ms or 100 ms during power-up. When the `PORSEL` pin is connected to ground, the POR time is 100 ms; when the `PORSEL` pin is connected to V_{CC}, the POR time is 2 ms.

The `nIO_PULLUP` pin enables a built-in weak pull-up resistor to pull all user I/O pins to V_{CCIO} before and during device configuration. If `nIO_PULLUP` is connected to V_{CC} during configuration, the weak pull-ups on all user I/O pins are disabled. If connected to ground, the pull-ups are enabled during configuration. The `nIO_PULLUP` pin can be pulled to 1.5, 1.8, 2.5, or 3.3 V for a logic level high.

`VCCSEL` is a dedicated input that is used to choose whether all dedicated configuration and JTAG input pins can accept 1.5 V/1.8 V or 2.5 V/3.3 V during configuration. A logic low sets 3.3 V/2.5 V, and a logic high sets 1.8 V/1.5 V. `VCCSEL` affects the following pins: `TDI`, `TMS`, `TCK`, `TRST`, `MSEL0`, `MSEL1`, `MSEL2`, `nCONFIG`, `nCE`, `DCLK`, `PLL_ENA`, `CONF_DONE`, `nSTATUS`. The `VCCSEL` pin can be pulled to 1.5, 1.8, 2.5, or 3.3 V for a logic level high.

The V_{CCSEL} signal does not control any of the dual-purpose pins, including the dual-purpose configuration pins. During configuration, the output buffers of dual-purpose pins will drive out a 1.5-V TTL compatible signal while the input buffers will receive 3.3-V TTL. After configuration, the dual-purpose pins inherit the I/O standards specified in the design.

The VCCSEL signal does not control the dual-purpose configuration pins such as the `DATA[7..0]` and PPA pins (`nWS`, `nRS`, `CS`, `nCS`, and `RDYnBSY`). During configuration, these dual-purpose pins will drive out voltage levels corresponding to the V_{CCIO} supply voltage that powers the I/O bank containing the pin. After configuration, the dual-purpose pins use I/O standards specified in the user design.

`TDO` and `nCEO` drive out at the same voltages as the V_{CCIO} supply that powers the I/O bank containing the pin. Users must select the V_{CCIO} supply for bank containing `TDO` accordingly. For example, when using the ByteBlasterMV cable, the V_{CCIO} for the bank containing `TDO` must be powered up at 3.3 V.

Configuring Stratix FPGAs with JRunner

JRunner is a software driver that configures Altera FPGAs, including Stratix FPGAs, through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (**.rbf**) format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms. For more information on the JRunner software driver, see the JRunner Software Driver: An Embedded Solution to the JTAG Configuration White Paper and the source files on the Altera web site (**www.altera.com**).

Configuration Schemes

Designers can load the configuration data for a Stratix device with one of five configuration schemes (see Table 3–5), chosen on the basis of the target application. Designers can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix device. A configuration device can automatically configure a Stratix device at system power-up.

Multiple Stratix devices can be configured in any of five configuration schemes by connecting the configuration enable (`nCE`) and configuration enable output (`nCEO`) pins on each device.

Table 3–5. Data Sources for Configuration

Configuration Scheme	Data Source
Configuration device	Enhanced or EPC2 configuration device
Passive serial (PS)	MasterBlaster, ByteBlasterMV, or ByteBlaster II download cable or serial data source
Passive parallel asynchronous (PPA)	Parallel data source
Fast passive parallel	Parallel data source
JTAG	MasterBlaster, ByteBlasterMV, or ByteBlaster II download cable, a microprocessor with a Jam or JBC file, or JRunner

Partial Reconfiguration

The enhanced PLLs within the Stratix device family support partial reconfiguration of their multiply, divide, and time delay settings without reconfiguring the entire device. Designers can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL. See "Enhanced PLLs" on page 2–85 for more information on Stratix PLLs.

Remote Update Configuration Modes

Stratix devices also support remote configuration using an Altera enhanced configuration device (e.g., EPC16, EPC8, and EPC4 devices) with page mode selection. Factory configuration data is stored in the default page of the configuration device. This is the default configuration which contains the design required to control remote updates and handle or recover from errors. The designer writes the factory configuration once into the flash memory or configuration device. Remote update data can update any of the remaining pages of the configuration device. If there is an error or corruption in a remote update configuration, the configuration device reverts back to the factory configuration information.

There are two remote configuration modes: remote and local configuration. Designers can use the remote update configuration mode for all three configuration modes: serial, parallel synchronous, and parallel asynchronous. Configuration devices (e.g., EPC16 devices) only support serial and parallel synchronous modes. Asynchronous parallel mode allows remote updates when an intelligent host is used to configure the Stratix device. This host must support page mode settings similar to an EPC16 device.

Remote Update Mode

When the Stratix device is first powered up in remote update programming mode, it loads the configuration located at page address "`000`." The factory configuration should always be located at page address "`000`," and should never be remotely updated. The factory configuration contains the required logic to perform the following operations:

- Determine the page address/load location for the next application's configuration data
- Recover from a previous configuration error
- Receive new configuration data and write it into the configuration device

The factory configuration is the default and takes control if an error occurs while loading the application configuration.

While in the factory configuration, the factory-configuration logic performs the following operations:

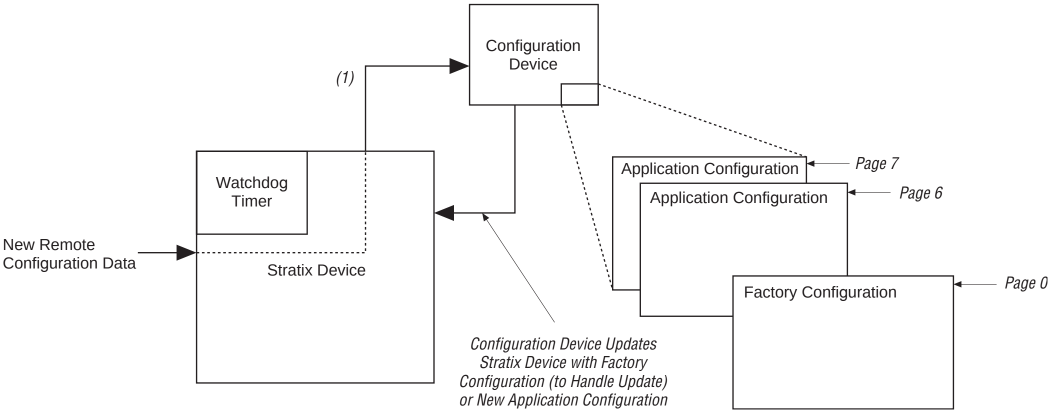
- Loads a remote update-control register to determine the page address of the new application configuration
- Determines whether to enable a user watchdog timer for the application configuration
- Determines what the watchdog timer setting should be if it is enabled

The user watchdog timer is a counter that must be continually reset within a specific amount of time in the user mode of an application configuration to ensure that valid configuration occurred during a remote update. Only valid application configurations designed for remote update can reset the user watchdog timer in user mode. If a valid application configuration does not reset the user watchdog timer in a specific amount of time, the timer updates a status register and loads the factory configuration. The user watchdog timer is automatically disabled for factory configurations.

If an error occurs in loading the application configuration, the configuration logic writes a status register to specify the cause of the error. Once this occurs, the Stratix device automatically loads the factory configuration, which reads the status register and determines the reason for reconfiguration. Based on the reason, the factory configuration will take appropriate steps and will write the remote update control register to specify the next application configuration page to be loaded.

When the Stratix device successfully loads the application configuration, it enters into user mode. The Stratix device then executes the main application of the user. Intellectual property (IP), such as a Nios® (16-bit ISA) and Nios® II (32-bit ISA) embedded processors, can help the Stratix device determine when remote update is coming. The Nios embedded processor or user logic receives incoming data, writes it to the configuration device, and loads the factory configuration. The factory configuration will read the remote update status register and determine the valid application configuration to load. Figure 3–2 shows the Stratix remote update. Figure 3–3 shows the transition diagram for remote update mode.

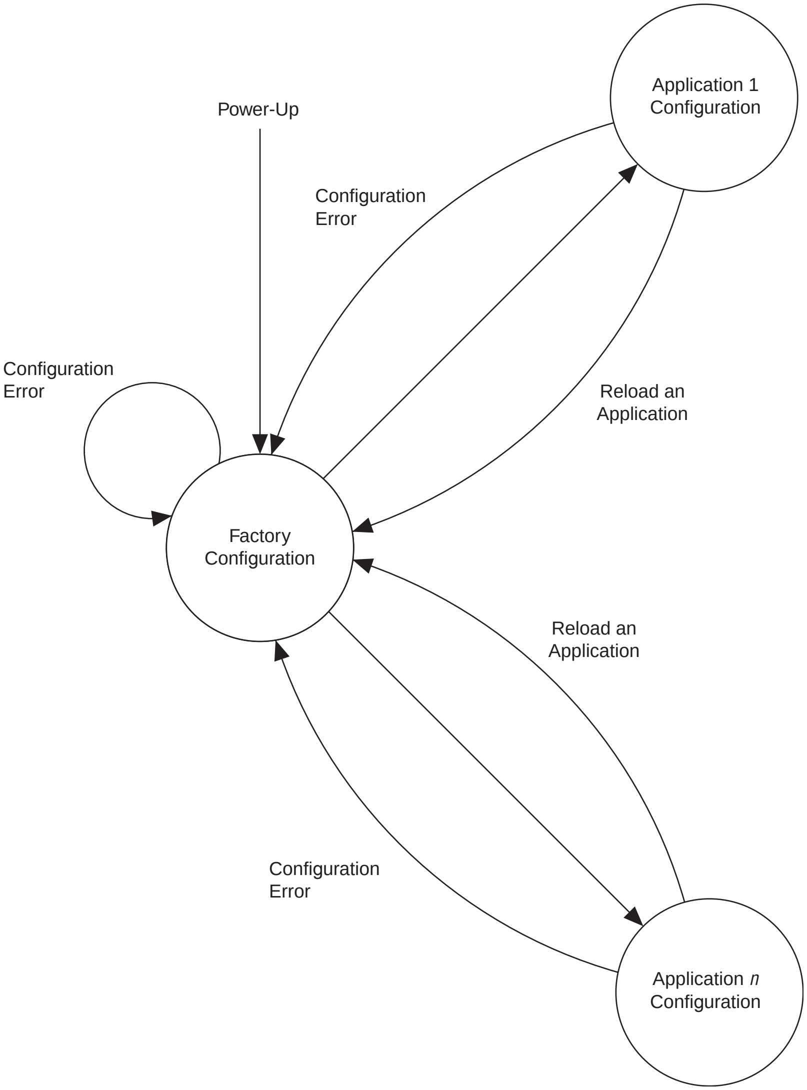
Figure 3–2. Stratix Device Remote Update



Note to Figure 3–2:

(1) When the Stratix device is configured with the factory configuration, it can handle update data from EPC16, EPC8, or EPC4 configuration device pages and point to the next page in the configuration device.

Figure 3–3. Remote Update Transition Diagram *Notes (1), (2)*



Notes to Figure 3–3:

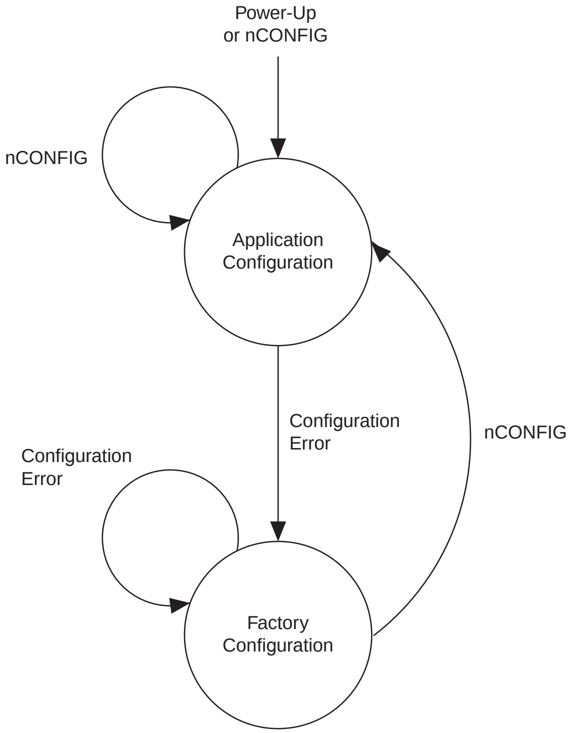
(1) Remote update of Application Configuration is controlled by a Nios embedded processor or user logic programmed in the Factory or Application configurations.

(2) Up to seven pages can be specified allowing up to seven different configuration applications.

Local Update Mode

Local update mode is a simplified version of the remote update. This feature is intended for simple systems that need to load a single application configuration immediately upon power up without loading the factory configuration first. Local update designs have only one application configuration to load, so it does not require a factory configuration to determine which application configuration to use. Figure 3–4 shows the transition diagram for local update mode.

Figure 3–4. Local Update Transition Diagram



Stratix Automated Single Event Upset (SEU) Detection

Stratix devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. FPGA devices that operate at high elevations or in close proximity to earth's North or South Pole will require periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by the **Device & Pin Options** dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

For Stratix, the CRC is computed by Quartus II and downloaded into the device as a part of the configuration bit stream. The CRC_ERROR pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

Custom-Built Circuitry

Dedicated circuitry is built in the Stratix devices to perform error detection automatically. Designers can use the built-in dedicated circuitry for error detection using CRC feature in Stratix devices, eliminating the need for external logic. This circuitry will perform error detection automatically when enabled. This error detection circuitry in Stratix devices constantly checks for errors in the configuration SRAM cells while the device is in user mode. Designers can monitor one external pin for the error and use it to trigger a re-configuration cycle. The designer can select the desired time between checks by adjusting a built-in clock divider.

Software Interface

In the Quartus II software version 4.1 and later, designers can turn on the automated error detection CRC feature in the **Device & Pin Options** dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 100 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the FPGA device.

For more information on CRC, see *AN 357: Error Detection Using CRC in Altera FPGA Devices*.

Temperature Sensing Diode

Stratix devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device such as a MAX1617A or MAX1619 from MAXIM Integrated Products. These devices steer bias current through the Stratix diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the package temperature of the Stratix device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix device to connect to the external temperature-sensing device, as shown in Figure 3–5. The temperature sensing diode is a passive element and therefore can be used before the Stratix device is powered.

Figure 3–5. External Temperature-Sensing Diode

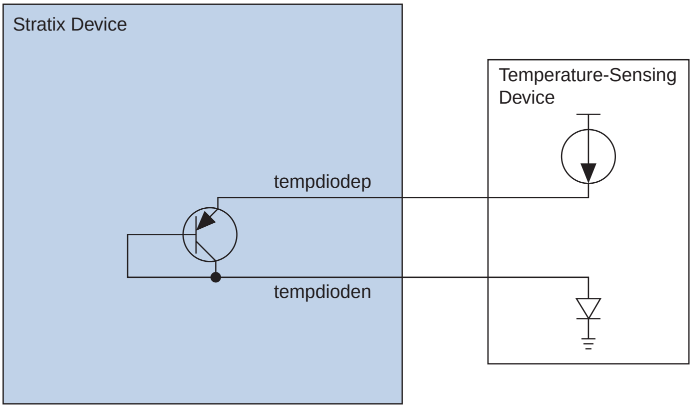


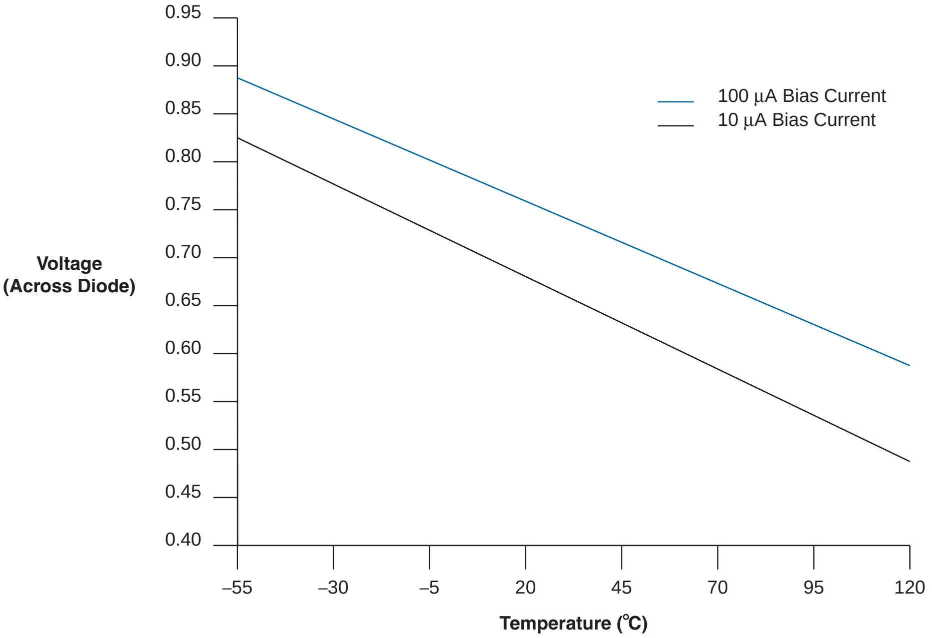
Table 3–6 shows the specifications for bias voltage and current of the Stratix temperature sensing diode.

Table 3–6. Temperature-Sensing Diode Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
I_{BIAS} high	80	100	120	µA
I_{BIAS} low	8	10	12	µA
$V_{BP} - V_{BN}$	0.3		0.9	V
V_{BN}		0.7		V
Series resistance			3	W

The temperature-sensing diode works for the entire operating range shown in Figure 3–6.

Figure 3–6. Temperature vs. Temperature-Sensing Diode Voltage



Chapter 4. DC & Switching Characteristics

S51004-3.1

Operating Conditions

Stratix® devices are offered in both commercial and industrial grades. Industrial devices are offered in -6 and -7 speed grades and commercial devices are offered in -5 (fastest), -6, -7, and -8 speed grades. This section specifies the operation conditions for operating junction temperature, V_{CCINT} and V_{CCIO} voltage levels, and input voltage requirements. The voltage specifications in this section are specified at the pins of the device (and not the power supply). If the device operates outside these ranges, then all DC and AC specifications are not guaranteed. Furthermore, the reliability of the device may be affected.

Tables 4–1 through 4–8 provide information on absolute maximum ratings.

Table 4–1. Stratix Device Absolute Maximum Ratings Notes (1), (2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage	With respect to ground	–0.5	2.4	V
V_{CCIO}			–0.5	4.6	V
V_I	DC input voltage (3)		–0.5	4.6	V
I_{OUT}	DC output current, per pin		–25	40	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_J	Junction temperature	BGA packages under bias		135	°C

Table 4–2. Stratix Device Recommended Operating Conditions (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(4)	1.425	1.575	V
V_{CCIO}	Supply voltage for output buffers, 3.3-V operation	(4), (5)	3.00 (3.135)	3.60 (3.465)	V
	Supply voltage for output buffers, 2.5-V operation	(4)	2.375	2.625	V
	Supply voltage for output buffers, 1.8-V operation	(4)	1.71	1.89	V
	Supply voltage for output buffers, 1.5-V operation	(4)	1.4	1.6	V

Table 4–2. Stratix Device Recommended Operating Conditions (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_I	Input voltage	(3), (6)	–0.5	4.0	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	85	°C
		For industrial use	–40	100	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 4–3. Stratix Device DC Operating Conditions *Note (7)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V *(8)*	–10		10	µA
I_{CC0}	V_{CC} supply current (standby) (All memory blocks in power-down mode)	V_I = ground, no load, no toggling inputs				mA
		EP1S10. V_I = ground, no load, no toggling inputs		37		mA
		EP1S20. V_I = ground, no load, no toggling inputs		65		mA
		EP1S25. V_I = ground, no load, no toggling inputs		90		mA
		EP1S30. V_I = ground, no load, no toggling inputs		114		mA
		EP1S40. V_I = ground, no load, no toggling inputs		145		mA
		EP1S60. V_I = ground, no load, no toggling inputs		200		mA
		EP1S80. V_I = ground, no load, no toggling inputs		277		mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	V_{CCIO} = 3.0 V *(9)*	20		50	kΩ
		V_{CCIO} = 2.375 V *(9)*	30		80	kΩ
		V_{CCIO} = 1.71 V *(9)*	60		150	kΩ

Table 4–4. LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –4 to –24 mA *(10)*	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 to 24 mA *(10)*		0.45	V

Table 4–5. LVCMOS Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.6	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, I_{OH} = –0.1 mA	V_{CCIO} – 0.2		V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, I_{OL} = 0.1 mA		0.2	V

Table 4–6. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.625	V
V_{IH}	High-level input voltage		1.7	4.1	V
V_{IL}	Low-level input voltage		–0.5	0.7	V
V_{OH}	High-level output voltage	I_{OH} = –0.1 mA	2.1		V
		I_{OH} = –1 mA	2.0		V
		I_{OH} = –2 to –16 mA *(10)*	1.7		V
V_{OL}	Low-level output voltage	I_{OL} = 0.1 mA		0.2	V
		I_{OL} = 1 mA		0.4	V
		I_{OL} = 2 to 16 mA *(10)*		0.7	V

Table 4–7. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.95	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	2.25	V
V_{IL}	Low-level input voltage		–0.3	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(10)*	$V_{CCIO} – 0.45$		V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(10)*		0.45	V

Table 4–8. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		1.4	1.6	V
V_{IH}	High-level input voltage		$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	V
V_{IL}	Low-level input voltage		–0.3	$0.35 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(10)*	$0.75 \times V_{CCIO}$		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(10)*		$0.25 \times V_{CCIO}$	V

Notes to Tables 4–1 through 4–8:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns, or overshoot to the voltage shown in Table 4–9, based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

(4) Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.

(5) V_{CCIO} maximum and minimum conditions for LVPECL, LVDS, and 3.3-V PCML are shown in parentheses.

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(7) Typical values are for $T_A = 25°C$, $V_{CCINT} = 1.5$ V, and $V_{CCIO} = 1.5$ V, 1.8 V, 2.5 V, and 3.3 V.

(8) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

(10) Drive strength is programmable according to values in Table 2–28 on page 2–118.

Table 4–9. Overshoot Input Voltage with Respect to Duty Cycle (Part 1 of 2)

Vin (V)	Maximum Duty Cycle (%)
4.0	100
4.1	90
4.2	50
4.3	30

Table 4–9. Overshoot Input Voltage with Respect to Duty Cycle (Part 2 of 2)

Vin (V)	Maximum Duty Cycle (%)
4.4	17
4.5	10

Figures 4–1 and 4–2 show receiver input and transmitter output waveforms, respectively, for all differential I/O standards (LVDS, 3.3-V PCML, LVPECL, and HyperTransport technology).

Figure 4–1. Receiver Input Waveforms for Differential I/O Standards

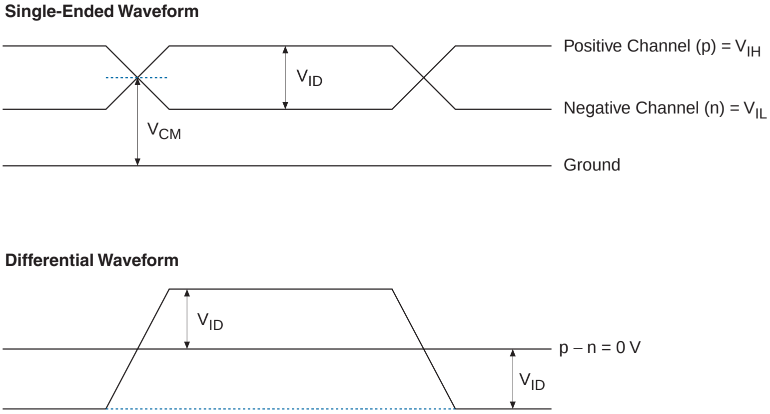
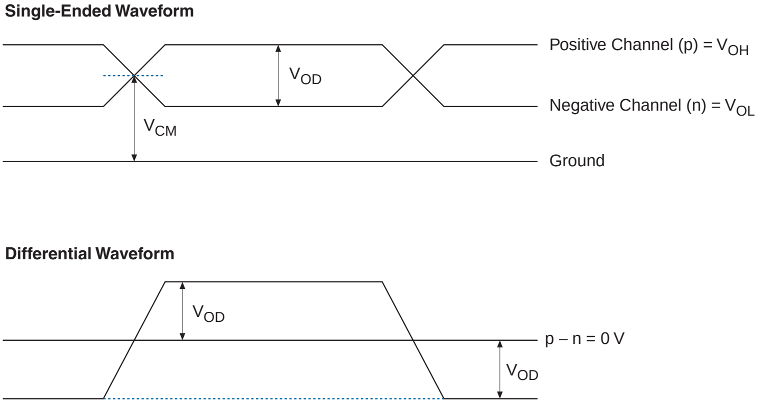


Figure 4–2. Transmitter Output Waveforms for Differential I/O Standards



Tables 4–10 through 4–33 recommend operating conditions, DC operating conditions, and capacitance for 1.5-V Stratix devices.

Table 4–10. 3.3-V LVDS I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID} *(6)*	Input differential voltage swing (single-ended)	$0.1\ V \leq V_{CM} < 1.1\ V$ *J* = 1 through 10	300		1,000	mV
		$1.1\ V \leq V_{CM} \leq 1.6\ V$ *J* = 1	200		1,000	mV
		$1.1\ V \leq V_{CM} \leq 1.6\ V$ *J* = 2 through10	100		1,000	mV
		$1.6\ V < V_{CM} \leq 1.8\ V$ *J* = 1 through 10	300		1,000	mV
V_{ICM}	Input common mode voltage *(6)*	LVDS $0.3\ V \leq V_{ID} \leq 1.0\ V$ *J* = 1 through 10	100		1,100	mV
		LVDS $0.3\ V \leq V_{ID} \leq 1.0\ V$ *J* = 1 through 10	1,600		1,800	mV
		LVDS $0.2\ V \leq V_{ID} \leq 1.0\ V$ *J* = 1	1,100		1,600	mV
		LVDS $0.1\ V \leq V_{ID} \leq 1.0\ V$ *J* = 2 through 10	1,100		1,600	mV
V_{OD} *(1)*	Output differential voltage (single-ended)	$R_L = 100\ \Omega$	250	375	550	mV
ΔV_{OD}	Change in V_{OD} between high and low	$R_L = 100\ \Omega$			50	mV
V_{OCM}	Output common mode voltage	$R_L = 100\ \Omega$	1,125	1,200	1,375	mV
ΔV_{OCM}	Change in V_{OCM} between high and low	$R_L = 100\ \Omega$			50	mV
R_L	Receiver differential input discrete resistor (external to Stratix devices)		90	100	110	Ω

Table 4–11. 3.3-V PCML Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID} (peak-to-peak)	Input differential voltage swing (single-ended)		300		600	mV
V_{ICM}	Input common mode voltage		1.5		3.465	V
V_{OD}	Output differential voltage (single-ended)		300	370	500	mV
ΔV_{OD}	Change in V_{OD} between high and low				50	mV
V_{OCM}	Output common mode voltage		2.5	2.85	3.3	V
ΔV_{OCM}	Change in V_{OCM} between high and low				50	mV
V_T	Output termination voltage			V_{CCIO}		V
R_1	Output external pull-up resistors		45	50	55	Ω
R_2	Output external pull-up resistors		45	50	55	Ω

Table 4–12. LVPECL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID} (peak-to-peak)	Input differential voltage swing (single-ended)		300		1,000	mV
V_{ICM}	Input common mode voltage		1		2	V
V_{OD}	Output differential voltage (single-ended)	R_L = 100 Ω	525	700	970	mV
V_{OCM}	Output common mode voltage	R_L = 100 Ω	1.5	1.7	1.9	V
R_L	Receiver differential input resistor		90	100	110	Ω

Table 4–13. HyperTransport Technology Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		2.375	2.5	2.625	V
V_{ID} (peak-to-peak)	Input differential voltage swing (single-ended)		300		900	mV
V_{ICM}	Input common mode voltage		300		900	mV
V_{OD}	Output differential voltage (single-ended)	$R_L = 100\ \Omega$	380	485	820	mV
ΔV_{OD}	Change in V_{OD} between high and low	$R_L = 100\ \Omega$			50	mV
V_{OCM}	Output common mode voltage	$R_L = 100\ \Omega$	440	650	780	mV
ΔV_{OCM}	Change in V_{OCM} between high and low	$R_L = 100\ \Omega$			50	mV
R_L	Receiver differential input resistor		90	100	110	Ω

Table 4–14. 3.3-V PCI Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.5		$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OUT} = -500\ \mu A$	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	$I_{OUT} = 1{,}500\ \mu A$			$0.1 \times V_{CCIO}$	V

Table 4–15. PCI-X 1.0 Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0		3.6	V
V_{IH}	High-level input voltage		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage		–0.5		$0.35 \times V_{CCIO}$	V
V_{IPU}	Input pull-up voltage		$0.7 \times V_{CCIO}$			V
V_{OH}	High-level output voltage	$I_{OUT} = -500\ \mu A$	$0.9 \times V_{CCIO}$			V
V_{OL}	Low-level output voltage	$I_{OUT} = 1{,}500\ \mu A$			$0.1 \times V_{CCIO}$	V

Table 4–16. GTL+ I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{TT}	Termination voltage		1.35	1.5	1.65	V
V_{REF}	Reference voltage		0.88	1.0	1.12	V
V_{IH}	High-level input voltage		$V_{REF} + 0.1$			V
V_{IL}	Low-level input voltage				$V_{REF} - 0.1$	V
V_{OL}	Low-level output voltage	$I_{OL} = 34$ mA *(3)*			0.65	V

Table 4–17. GTL I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{TT}	Termination voltage		1.14	1.2	1.26	V
V_{REF}	Reference voltage		0.74	0.8	0.86	V
V_{IH}	High-level input voltage		$V_{REF} + 0.05$			V
V_{IL}	Low-level input voltage				$V_{REF} - 0.05$	V
V_{OL}	Low-level output voltage	$I_{OL} = 40$ mA *(3)*			0.4	V

Table 4–18. SSTL-18 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.8	1.95	V
V_{REF}	Reference voltage		0.8	0.9	1.0	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.125			V
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.275			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.275	V
V_{OH}	High-level output voltage	I_{OH} = –6.7 mA *(3)*	V_{TT} + 0.475			V
V_{OL}	Low-level output voltage	I_{OL} = 6.7 mA *(3)*			V_{TT} – 0.475	V

Table 4–19. SSTL-18 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.8	1.95	V
V_{REF}	Reference voltage		0.8	0.9	1.0	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.125			V
$V_{IL(DC)}$	Low-level DC input voltage				V_{REF} – 0.125	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.275			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.275	V
V_{OH}	High-level output voltage	I_{OH} = –13.4 mA *(3)*	V_{TT} + 0.630			V
V_{OL}	Low-level output voltage	I_{OL} = 13.4 mA *(3)*			V_{TT} – 0.630	V

Table 4–20. SSTL-2 Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.18		3.0	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		V_{REF} – 0.18	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.35			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –8.1 mA *(3)*	V_{TT} + 0.57			V
V_{OL}	Low-level output voltage	I_{OL} = 8.1 mA *(3)*			V_{TT} – 0.57	V

Table 4–21. SSTL-2 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.375	2.5	2.625	V
V_{TT}	Termination voltage		V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
V_{REF}	Reference voltage		1.15	1.25	1.35	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.18		V_{CCIO} + 0.3	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		V_{REF} – 0.18	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.35			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.35	V
V_{OH}	High-level output voltage	I_{OH} = –16.4 mA *(3)*	V_{TT} + 0.76			V
V_{OL}	Low-level output voltage	I_{OL} = 16.4 mA *(3)*			V_{TT} – 0.76	V

Table 4–22. SSTL-3 Class I Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V

Table 4–22. SSTL-3 Class I Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		V_{REF} – 0.2	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.4			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.4	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(3)*	V_{TT} + 0.6			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(3)*			V_{TT} – 0.6	V

Table 4–23. SSTL-3 Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage		V_{REF} – 0.05	V_{REF}	V_{REF} + 0.05	V
V_{REF}	Reference voltage		1.3	1.5	1.7	V
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		V_{REF} – 0.2	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.4			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.4	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(3)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(3)*			V_{TT} – 0.8	V

Table 4–24. 3.3-V AGP 2× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		0.39 × V_{CCIO}		0.41 × V_{CCIO}	V
V_{IH}	High-level input voltage *(4)*		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(4)*				0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –0.5 mA	0.9 × V_{CCIO}		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 1.5 mA			0.1 × V_{CCIO}	V

Table 4–25. 3.3-V AGP 1× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{IH}	High-level input voltage *(4)*		$0.5 \times V_{CCIO}$		$V_{CCIO} + 0.5$	V
V_{IL}	Low-level input voltage *(4)*				$0.3 \times V_{CCIO}$	V
V_{OH}	High-level output voltage	$I_{OUT} = -0.5$ mA	$0.9 \times V_{CCIO}$		3.6	V
V_{OL}	Low-level output voltage	$I_{OUT} = 1.5$ mA			$0.1 \times V_{CCIO}$	V

Table 4–26. 1.5-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.3		$V_{REF} - 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA *(3)*	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA *(3)*			0.4	V

Table 4–27. 1.5-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		$V_{REF} + 0.1$			V
V_{IL} (DC)	DC low-level input voltage		–0.3		$V_{REF} - 0.1$	V
V_{IH} (AC)	AC high-level input voltage		$V_{REF} + 0.2$			V
V_{IL} (AC)	AC low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -16$ mA *(3)*	$V_{CCIO} - 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 16$ mA *(3)*			0.4	V

Table 4–28. 1.8-V HSTL Class I Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.80	1.95	V
V_{REF}	Input reference voltage		0.70	0.90	0.95	V
V_{TT}	Termination voltage			V_{CCIO} × 0.5		V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.5		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA *(3)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA *(3)*			0.4	V

Table 4–29. 1.8-V HSTL Class II Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.80	1.95	V
V_{REF}	Input reference voltage		0.70	0.90	0.95	V
V_{TT}	Termination voltage			V_{CCIO} × 0.5		V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.5		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(3)*	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(3)*			0.4	V

Table 4–30. 1.5-V Differential HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V

Table 4–31. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.05	3.3	3.6	V
V_{TT}/V_{REF}	Termination and input reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		$V_{REF} + 0.2$			V
V_{IL}	Low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA	$V_{REF} + 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA			$V_{REF} - 0.4$	V
I_O	Output leakage current (when output is high *Z*)	$GND \leq V_{OUT} \leq V_{CCIO}$	–10		10	µA

Table 4–32. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level								Unit
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	25		30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	-25		–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		160		200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		-160		–200		–300		–500	µA
Bus-hold trip point		0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

Table 4–33. Stratix Device Capacitance Note (5)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_{IOTB}	Input capacitance on I/O pins in I/O banks 3, 4, 7, and 8.		11.5		pF
C_{IOLR}	Input capacitance on I/O pins in I/O banks 1, 2, 5, and 6, including high-speed differential receiver and transmitter pins.		8.2		pF
C_{CLKTB}	Input capacitance on top/bottom clock input pins: `CLK[4:7]` and `CLK[12:15]`.		11.5		pF
C_{CLKLR}	Input capacitance on left/right clock inputs: `CLK1`, `CLK3`, `CLK8`, `CLK10`.		7.8		pF
C_{CLKLR+}	Input capacitance on left/right clock inputs: `CLK0`, `CLK2`, `CLK9`, and `CLK11`.		4.4		pF

Notes to Tables 4–10 through 4–33:

(1) When `tx_outclock` port of `altlvds_tx` megafunction is 717 MHz, $V_{OD(min)}$ = 235 mV on the output clock pin.

(2) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

(3) Drive strength is programmable according to values in Table 2–28 on page 2–118.

(4) V_{REF} specifies the center point of the switching range.

(5) Capacitance is sample-tested only. Capacitance is measured using time-domain reflections (TDR). Measurement accuracy is within ±0.5 pF.

(6) V_{IO} and V_{CM} have multiple ranges and values for J=1 through 10.

Power Consumption

Altera offers two ways to calculate power for a design: the Altera web power calculator and the PowerGauge™ feature in the Quartus® II software.

The interactive power calculator on the Altera web site is typically used prior to designing the FPGA in order to get a magnitude estimate of the device power. The Quartus II software PowerGauge feature allows designers to apply test vectors against their design for more accurate power consumption modeling.

In both cases, these calculations should only be used as an estimation of power, not as a specification.

Stratix devices require a certain amount of power-up current to successfully power up because of the small process geometry on which they are fabricated.

Table 4–34 shows the maximum power-up current (I_{CCINT}) required to power a Stratix device. This specification is for commercial operating conditions. Measurements were performed with an isolated Stratix device on the board to characterize the power-up current of an isolated device. Decoupling capacitors were not used in this measurement. To factor in the current for decoupling capacitors, sum up the current for each capacitor using the following equation:

$I = C\,(dV/dt)$

If the regulator or power supply minimum output current is more than the Stratix device requires, then the device may consume more current than the maximum current listed in Table 4–34. However, the device does not require any more current to successfully power up than what is listed in Table 4–34.

Table 4–34. Stratix Power-Up Current (I_{CCINT}) Requirements *Note (1)*

Device	Power-Up Current Requirement		Unit
	Typical	Maximum	
EP1S10	250	700	mA
EP1S20	400	1,200	mA
EP1S25	500	1,500	mA
EP1S30	550	1,900	mA
EP1S40	650	2,300	mA
EP1S60	800	2,600	mA
EP1S80	1,000	3,000	mA

Note to Table 4–34:

(1) The maximum test conditions are for 0° C and typical test conditions are for 40° C.

The exact amount of current consumed varies according to the process, temperature, and power ramp rate. Stratix devices typically require less current during power up than shown in Table 4–34. The user-mode current during device operation is generally higher than the power-up current.

The duration of the I_{CCINT} power-up requirement depends on the V_{CCINT} voltage supply rise time. The power-up current consumption drops when the V_{CCINT} supply reaches approximately 0.75 V.

Timing Model

The DirectDrive technology and MultiTrack interconnect ensure predictable performance, accurate simulation, and accurate timing analysis across all Stratix device densities and speed grades. This section describes and specifies the performance, internal, external, and PLL timing specifications.

All specifications are representative of worst-case supply voltage and junction temperature conditions.

Preliminary & Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 4–35 shows the status of the Stratix device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under worst-case voltage and junction temperature conditions.

Table 4–35. Stratix Device Timing Model Status

Device	Preliminary	Final
EP1S10		✓
EP1S20		✓
EP1S25		✓
EP1S30		✓
EP1S40		✓
EP1S60		✓
EP1S80		✓

Performance

Table 4–36 shows Stratix performance for some common designs. All performance values were obtained with Quartus II software compilation of LPM, or MegaCore functions for the FIR and FFT designs.

Table 4–36. Stratix Performance (Part 1 of 2) Notes (1), (2)

Applications		Resources Used			Performance				
		LEs	TriMatrix Memory Blocks	DSP Blocks	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Units
LE	16-to-1 multiplexer *(1)*	22	0	0	407.83	324.56	288.68	228.67	MHz
	32-to-1 multiplexer *(3)*	46	0	0	318.26	255.29	242.89	185.18	MHz
	16-bit counter	16	0	0	422.11	422.11	390.01	348.67	MHz
	64-bit counter	64	0	0	321.85	290.52	261.23	220.5	MHz
TriMatrix memory M512 block	Simple dual-port RAM 32 × 18 bit	0	1	0	317.76	277.62	241.48	205.21	MHz
	FIFO 32 × 18 bit	30	1	0	319.18	278.86	242.54	206.14	MHz
TriMatrix memory M4K block	Simple dual-port RAM 128 × 36 bit	0	1	0	290.86	255.55	222.27	188.89	MHz
	True dual-port RAM 128 × 18 bit	0	1	0	290.86	255.55	222.27	188.89	MHz
	FIFO 128 × 36 bit	34	1	0	290.86	255.55	222.27	188.89	MHz
TriMatrix memory M-RAM block	Single port RAM 4K × 144 bit	1	1	0	255.95	223.06	194.06	164.93	MHz
	Simple dual-port RAM 4K × 144 bit	0	1	0	255.95	233.06	194.06	164.93	MHz
	True dual-port RAM 4K × 144 bit	0	1	0	255.95	233.06	194.06	164.93	MHz
	Single port RAM 8K × 72 bit	0	1	0	278.94	243.19	211.59	179.82	MHz
	Simple dual-port RAM 8K × 72 bit	0	1	0	255.95	223.06	194.06	164.93	MHz
	True dual-port RAM 8K × 72 bit	0	1	0	255.95	223.06	194.06	164.93	MHz
	Single port RAM 16K × 36 bit	0	1	0	280.66	254.32	221.28	188.00	MHz
	Simple dual-port RAM 16K × 36 bit	0	1	0	269.83	237.69	206.82	175.74	MHz

Table 4–36. Stratix Performance (Part 2 of 2) *Notes (1), (2)*

Applications		Resources Used			Performance				
		LEs	TriMatrix Memory Blocks	DSP Blocks	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Units
TriMatrix memory M-RAM block	True dual-port RAM 16K × 36 bit	0	1	0	269.83	237.69	206.82	175.74	MHz
	Single port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	180.83	MHz
	Simple dual-port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	180.83	MHz
	True dual-port RAM 32K × 18 bit	0	1	0	275.86	244.55	212.76	180.83	MHz
	Single port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	187.26	MHz
	Simple dual-port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	187.26	MHz
	True dual-port RAM 64K × 9 bit	0	1	0	287.85	253.29	220.36	187.26	MHz
DSP block	9 × 9-bit multiplier *(3)*	0	0	1	335.0	293.94	255.68	217.24	MHz
	18 × 18-bit multiplier *(4)*	0	0	1	278.78	237.41	206.52	175.50	MHz
	36 × 36-bit multiplier *(4)*	0	0	1	148.25	134.71	117.16	99.59	MHz
	36 × 36-bit multiplier *(5)*	0	0	1	278.78	237.41	206.52	175.5	MHz
	18-bit, 4-tap FIR filter	0	0	1	278.78	237.41	206.52	175.50	MHz
Larger Designs	8-bit, 16-tap parallel FIR filter	58	0	4	141.26	133.49	114.88	100.28	MHz
	8-bit, 1,024-point FFT function	870	5	1	261.09	235.51	205.21	175.22	MHz

Notes to Table 4–36:

(1) These design performance numbers were obtained using the Quartus II software.
(2) Numbers not listed will be included in a future version of the data sheet.
(3) This application uses registered inputs and outputs.
(4) This application uses registered multiplier input and output stages within the DSP block.
(5) This application uses registered multiplier input, pipeline, and output stages within the DSP block.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–37 through 4–42 describe the Stratix device internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

Table 4–37. LE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	LE register setup time before clock
t_H	LE register hold time after clock
t_{CO}	LE register clock-to-output delay
t_{LUT}	LE combinatorial LUT delay for data-in to data-out
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Register minimum clock high or low time. The maximum core clock frequency can be calculated by $1/(2 \times t_{CLKHL})$.

Table 4–38. IOE Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU_R}	Row IOE input register setup time
t_{SU_C}	Column IOE input register setup time
t_H	IOE input and output register hold time after clock
t_{CO_R}	Row IOE input and output register clock-to-output delay
t_{CO_C}	Column IOE input and output register clock-to-output delay
$t_{PIN2COMBOUT\_R}$	Row input pin to IOE combinatorial output
$t_{PIN2COMBOUT\_C}$	Column input pin to IOE combinatorial output
$t_{COMBIN2PIN\_R}$	Row IOE data input to combinatorial output pin
$t_{COMBIN2PIN\_C}$	Column IOE data input to combinatorial output pin
t_{CLR}	Minimum clear pulse width
t_{PRE}	Minimum preset pulse width
t_{CLKHL}	Register minimum clock high or low time. The maximum I/O clock frequency can be calculated by $1/(2 \times t_{CLKHL})$. Performance may also be affected by I/O timing, use of PLL, and I/O programmable settings.

Table 4–39. DSP Block Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{SU}	Input, pipeline, and output register setup time before clock
t_{H}	Input, pipeline, and output register hold time after clock
t_{CO}	Input, pipeline, and output register clock-to-output delay
$t_{INREG2PIPE9}$	Input Register to DSP Block pipeline register in 9 × 9-bit mode
$t_{INREG2PIPE18}$	Input Register to DSP Block pipeline register in 18 × 18-bit mode
$t_{PIPE2OUTREG2ADD}$	DSP Block Pipeline Register to output register delay in Two-Multipliers Adder mode
$t_{PIPE2OUTREG4ADD}$	DSP Block Pipeline Register to output register delay in Four-Multipliers Adder mode
t_{PD9}	Combinatorial input to output delay for 9 × 9
t_{PD18}	Combinatorial input to output delay for 18 × 18
t_{PD36}	Combinatorial input to output delay for 36 × 36
t_{CLR}	Minimum clear pulse width
t_{CLKHL}	Register minimum clock high or low time. This is a limit on the min time for the clock on the registers in these blocks. The actual performance is dependent upon the internal point-to-point delays in the blocks and may give slower performance as shown in Table 4–36 on page 4–19 and as reported by the timing analyzer in the Quartus II software.

Table 4–40. M512 Block Internal Timing Microparameter Descriptions

Symbol	Parameter
t_{M512RC}	Synchronous read cycle time
t_{M512WC}	Synchronous write cycle time
$t_{M512WERESU}$	Write or read enable setup time before clock
$t_{M512WEREH}$	Write or read enable hold time after clock
$t_{M512CLKENSU}$	Clock enable setup time before clock
$t_{M512CLKENH}$	Clock enable hold time after clock
$t_{M512DATASU}$	Data setup time before clock
$t_{M512DATAH}$	Data hold time after clock
$t_{M512WADDRSU}$	Write address setup time before clock
$t_{M512WADDRH}$	Write address hold time after clock
$t_{M512RADDRSU}$	Read address setup time before clock
$t_{M512RADDRH}$	Read address hold time after clock
$t_{M512DATACO1}$	Clock-to-output delay when using output registers
$t_{M512DATACO2}$	Clock-to-output delay without output registers
$t_{M512CLKHL}$	Register minimum clock high or low time. This is a limit on the min time for the clock on the registers in these blocks. The actual performance is dependent upon the internal point-to-point delays in the blocks and may give slower performance as shown in Table 4–36 on page 4–19 and as reported by the timing analyzer in the Quartus II software.
$t_{M512CLR}$	Minimum clear pulse width

Table 4–41. M4K Block Internal Timing Microparameter Descriptions (Part 1 of 2)

Symbol	Parameter
t_{M4KRC}	Synchronous read cycle time
t_{M4KWC}	Synchronous write cycle time
$t_{M4KWERESU}$	Write or read enable setup time before clock
$t_{M4KWEREH}$	Write or read enable hold time after clock
$t_{M4KCLKENSU}$	Clock enable setup time before clock
$t_{M4KCLKENH}$	Clock enable hold time after clock
$t_{M4KBESU}$	Byte enable setup time before clock
t_{M4KBEH}	Byte enable hold time after clock
$t_{M4KDATAASU}$	A port data setup time before clock

Table 4–41. M4K Block Internal Timing Microparameter Descriptions (Part 2 of 2)

Symbol	Parameter
$t_{M4KDATAAH}$	A port data hold time after clock
$t_{M4KADDRASU}$	A port address setup time before clock
$t_{M4KADDRAH}$	A port address hold time after clock
$t_{M4KDATABSU}$	B port data setup time before clock
$t_{M4KDATABH}$	B port data hold time after clock
$t_{M4KADDRBSU}$	B port address setup time before clock
$t_{M4KADDRBH}$	B port address hold time after clock
$t_{M4KDATACO1}$	Clock-to-output delay when using output registers
$t_{M4KDATACO2}$	Clock-to-output delay without output registers
$t_{M4KCLKHL}$	Register minimum clock high or low time. This is a limit on the min time for the clock on the registers in these blocks. The actual performance is dependent upon the internal point-to-point delays in the blocks and may give slower performance as shown inTable 4–36 on page 4–19 and as reported by the timing analyzer in the Quartus II software.
t_{M4KCLR}	Minimum clear pulse width

Table 4–42. M-RAM Block Internal Timing Microparameter Descriptions (Part 1 of 2)

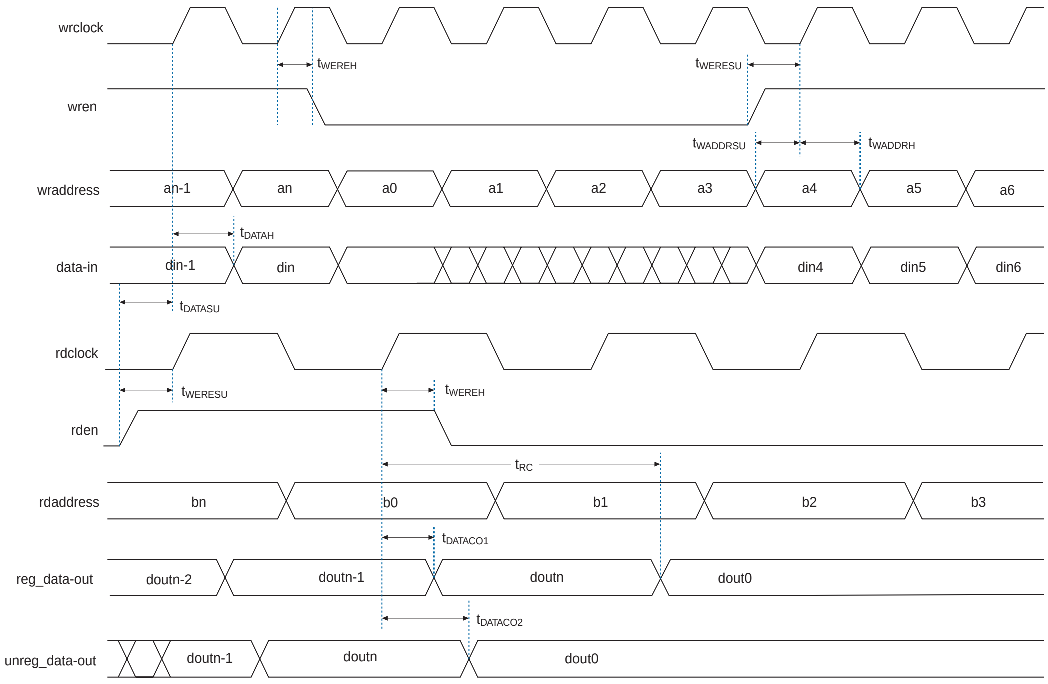
Symbol	Parameter
t_{MRAMRC}	Synchronous read cycle time
t_{MRAMWC}	Synchronous write cycle time
$t_{MRAMWERESU}$	Write or read enable setup time before clock
$t_{MRAMWEREH}$	Write or read enable hold time after clock
$t_{MRAMCLKENSU}$	Clock enable setup time before clock
$t_{MRAMCLKENH}$	Clock enable hold time after clock
$t_{MRAMBESU}$	Byte enable setup time before clock
$t_{MRAMBEH}$	Byte enable hold time after clock
$t_{MRAMDATAASU}$	A port data setup time before clock
$t_{MRAMDATAAH}$	A port data hold time after clock
$t_{MRAMADDRASU}$	A port address setup time before clock
$t_{MRAMADDRAH}$	A port address hold time after clock
$t_{MRAMDATABSU}$	B port setup time before clock

Table 4–42. M-RAM Block Internal Timing Microparameter Descriptions (Part 2 of 2)

Symbol	Parameter
$t_{MRAMDATABH}$	B port hold time after clock
$t_{MRAMADDRBSU}$	B port address setup time before clock
$t_{MRAMADDRBH}$	B port address hold time after clock
$t_{MRAMDATACO1}$	Clock-to-output delay when using output registers
$t_{MRAMDATACO2}$	Clock-to-output delay without output registers
$t_{MRAMCLKHL}$	Register minimum clock high or low time. This is a limit on the min time for the clock on the registers in these blocks. The actual performance is dependent upon the internal point-to-point delays in the blocks and may give slower performance as shown in Table 4–36 on page 4–19 and as reported by the timing analyzer in the Quartus II software.
$t_{MRAMCLR}$	Minimum clear pulse width

Figure 4–3 shows the TriMatrix memory waveforms for the M512, M4K, and M-RAM timing parameters shown in Tables 4–40 through 4–42 above.

Figure 4–3. Dual-Port RAM Timing Microparameter Waveform



Internal timing parameters are specified on a speed grade basis independent of device density. Tables 4–44 through 4–50 show the internal timing microparameters for LEs, IOEs, TriMatrix memory structures, DSP blocks, and MultiTrack interconnects.

Table 4–43. Routing Delay Internal Timing Microparameter Descriptions (Part 1 of 2)

Symbol	Parameter
t_{R4}	Delay for an R4 line with average loading; covers a distance of four LAB columns.
t_{R8}	Delay for an R8 line with average loading; covers a distance of eight LAB columns.

Table 4–43. Routing Delay Internal Timing Microparameter Descriptions (Part 2 of 2)

Symbol	Parameter
t_{R24}	Delay for an R24 line with average loading; covers a distance of 24 LAB columns.
t_{C4}	Delay for a C4 line with average loading; covers a distance of four LAB rows.
t_{C8}	Delay for a C8 line with average loading; covers a distance of eight LAB rows.
t_{C16}	Delay for a C16 line with average loading; covers a distance of 16 LAB rows.
t_{LOCAL}	Local interconnect delay, for connections within a LAB, and for the final routing hop of connections to LABs, DSP blocks, RAM blocks and I/Os.

Table 4–44. LE Internal Timing Microparameters

Parameter	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	10		10		11		13		ps
t_H	100		100		114		135		ps
t_{CO}		156		176		202		238	ps
t_{LUT}		366		459		527		621	ps
t_{CLR}	100		100		114		135		ps
t_{PRE}	100		100		114		135		ps
t_{CLKHL}	1000		1111		1190		1400		ps

Table 4–45. IOE Internal TSU Microparameter by Device Density (Part 1 of 2)

Device	Symbol	-5		-6		-7		-8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
EP1S10	t_{SU_R}	76		80		80		80		ps
	t_{SU_C}	176		80		80		80		ps
EP1S20	t_{SU_R}	76		80		80		80		ps
	t_{SU_C}	76		80		80		80		ps
EP1S25	t_{SU_R}	276		280		280		280		ps
	t_{SU_C}	276		280		280		280		ps

Table 4–45. IOE Internal TSU Microparameter by Device Density (Part 2 of 2)

Device	Symbol	-5		-6		-7		-8		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
EP1S30	t_{SU_R}	76		80		80		80		ps
	t_{SU_C}	176		180		180		180		ps
EP1S40	t_{SU_R}	76		80		80		80		ps
	t_{SU_C}	376		380		380		380		ps
EP1S60	t_{SU_R}	276		280		280		280		ps
	t_{SU_C}	276		280		280		280		ps
EP1S80	t_{SU_R}	426		430		430		430		ps
	t_{SU_C}	76		80		80		80		ps

Table 4–46. IOE Internal Timing Microparameters

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_H	68		71		82		96		ps
t_{CO_R}		171		179		206		242	ps
t_{CO_C}		171		179		206		242	ps
$t_{PIN2COMBOUT\_R}$		1,234		1,295		1,490		1,753	ps
$t_{PIN2COMBOUT\_C}$		1,087		1,141		1,312		1,544	ps
$t_{COMBIN2PIN\_R}$		3,894		4,089		4,089		4,089	ps
$t_{COMBIN2PIN\_C}$		4,299		4,494		4,494		4,494	ps
t_{CLR}	276		289		333		392		ps
t_{PRE}	260		273		313		369		ps
t_{CLKHL}	1,000		1,111		1,190		1,400		ps

Table 4–47. DSP Block Internal Timing Microparameters (Part 1 of 2)

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{SU}	0		0		0		0		ps
t_H	67		75		86		101		ps
t_{CO}		142		158		181		214	ps

Table 4–47. DSP Block Internal Timing Microparameters (Part 2 of 2)

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{INREG2PIPE9}$		2,613		2,982		3,429		4,035	ps
$t_{INREG2PIPE18}$		3,390		3,993		4,591		5,402	ps
$t_{PIPE2OUTREG2ADD}$		2,002		2,203		2,533		2,980	ps
$t_{PIPE2OUTREG4ADD}$		2,899		3,189		3,667		4,314	ps
t_{PD9}		3,709		4,081		4,692		5,520	ps
t_{PD18}		4,795		5,275		6,065		7,135	ps
t_{PD36}		7,495		8,245		9,481		11,154	ps
t_{CLR}	450		500		575		676		ps
t_{CLKHL}	1,350		1,500		1,724		2,029		ps

Table 4–48. M512 Block Internal Timing Microparameters

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{M512RC}		3,340		3,816		4,387		5,162	ps
t_{M512WC}		3,138		3,590		4,128		4,860	ps
$t_{M512WERESU}$	110		123		141		166		ps
$t_{M512WEREH}$	34		38		43		51		ps
$t_{M512CLKENSU}$	215		215		247		290		ps
$t_{M512CLKENH}$	–70		–70		–81		–95		ps
$t_{M512DATASU}$	110		123		141		166		ps
$t_{M512DATAH}$	34		38		43		51		ps
$t_{M512WADDRSU}$	110		123		141		166		ps
$t_{M512WADDRH}$	34		38		43		51		ps
$t_{M512RADDRSU}$	110		123		141		166		ps
$t_{M512RADDRH}$	34		38		43		51		ps
$t_{M512DATACO1}$		424		472		541		637	ps
$t_{M512DATACO2}$		3,366		3,846		4,421		5,203	ps
$t_{M512CLKHL}$	1,000		1,111		1,190		1,400		ps
$t_{M512CLR}$	170		189		217		255		ps

Table 4–49. M4K Block Internal Timing Microparameters

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{M4KRC}		3,807		4,320		4,967		5,844	ps
t_{M4KWC}		2,556		2,840		3,265		3,842	ps
$t_{M4KWERESU}$	131		149		171		202		ps
$t_{M4KWEREH}$	34		38		43		51		ps
$t_{M4KCLKENSU}$	193		215		247		290		ps
$t_{M4KCLKENH}$	–63		–70		–81		–95		ps
$t_{M4KBESU}$	131		149		171		202		ps
t_{M4KBEH}	34		38		43		51		ps
$t_{M4KDATAASU}$	131		149		171		202		ps
$t_{M4KDATAAH}$	34		38		43		51		ps
$t_{M4KADDRASU}$	131		149		171		202		ps
$t_{M4KADDRAH}$	34		38		43		51		ps
$t_{M4KDATABSU}$	131		149		171		202		ps
$t_{M4KDATABH}$	34		38		43		51		ps
$t_{M4KADDRBSU}$	131		149		171		202		ps
$t_{M4KADDRBH}$	34		38		43		51		ps
$t_{M4KDATACO1}$		571		635		729		858	ps
$t_{M4KDATACO2}$		3,984		4,507		5,182		6,097	ps
$t_{M4KCLKHL}$	1,000		1,111		1,190		1,400		ps
t_{M4KCLR}	170		189		217		255		ps

Table 4–50. M-RAM Block Internal Timing Microparameters (Part 1 of 2)

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{MRAMRC}		4,364		4,838		5,562		6,544	ps
t_{MRAMWC}		3,654		4,127		4,746		5,583	ps
$t_{MRAMWERESU}$	25		25		28		33		ps
$t_{MRAMWEREH}$	18		20		23		27		ps
$t_{MRAMCLKENSU}$	99		111		127		150		ps
$t_{MRAMCLKENH}$	–48		–53		–61		–72		ps

Table 4–50. M-RAM Block Internal Timing Microparameters (Part 2 of 2)

Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{MRAMBESU}$	25		25		28		33		ps
$t_{MRAMBEH}$	18		20		23		27		ps
$t_{MRAMDATAASU}$	25		25		28		33		ps
$t_{MRAMDATAAH}$	18		20		23		27		ps
$t_{MRAMADDRASU}$	25		25		28		33		ps
$t_{MRAMADDRAH}$	18		20		23		27		ps
$t_{MRAMDATABSU}$	25		25		28		33		ps
$t_{MRAMDATABH}$	18		20		23		27		ps
$t_{MRAMADDRBSU}$	25		25		28		33		ps
$t_{MRAMADDRBH}$	18		20		23		27		ps
$t_{MRAMDATACO1}$		1,038		1,053		1,210		1,424	ps
$t_{MRAMDATACO2}$		4,362		4,939		5,678		6,681	ps
$t_{MRAMCLKHL}$	1,000		1,111		1,190		1,400		ps
$t_{MRAMCLR}$	135		150		172		202		ps

Table 4–51. Routing Delay Internal Timing Parameters

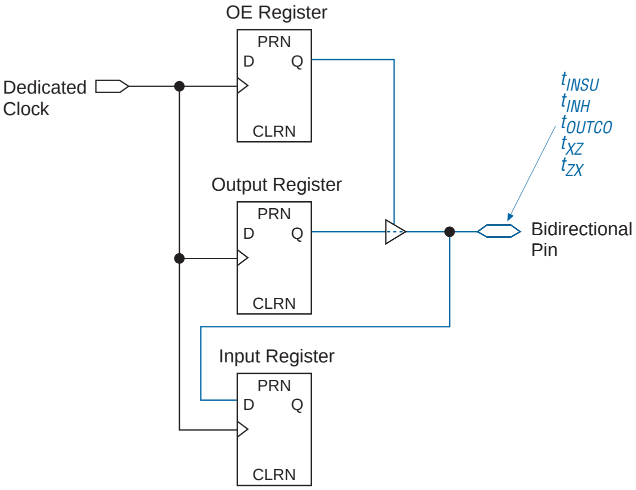
Symbol	-5		-6		-7		-8		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{R4}		268		295		339		390	ps
t_{R8}		371		349		401		461	ps
t_{R24}		465		512		588		676	ps
t_{C4}		440		484		557		641	ps
t_{C8}		577		634		730		840	ps
t_{C16}		445		489		563		647	ps
t_{LOCAL}		313		345		396		455	ps

Routing delays vary depending on the load on that specific routing line. The Quartus II software reports the routing delay information when running the timing analysis for a design.

External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 4–4 shows the pin-to-pin timing model for bidirectional IOE pin timing. All registers are within the IOE.

Figure 4–4. External Timing in Stratix Devices



All external timing parameters reported in this section are defined with respect to the dedicated clock pin as the starting point. All external I/O timing parameters shown are for 3.3-V LVTTL I/O standard with the 4-mA current strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in Tables 4–103 through 4–107.

Table 4–52 shows the external I/O timing parameters when using fast regional clock networks.

Table 4–52. Stratix Fast Regional Clock External I/O Timing Parameters *Notes (1), (2)*

Symbol	Parameter
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with fast regional clock fed by `FCLK` pin
t_{INH}	Hold time for input or bidirectional pin using IOE input register with fast regional clock fed by `FCLK` pin
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with fast regional clock fed by `FCLK` pin
t_{XZ}	Synchronous IOE output enable register to output pin disable delay using fast regional clock fed by `FCLK` pin
t_{ZX}	Synchronous IOE output enable register to output pin enable delay using fast regional clock fed by `FCLK` pin

Notes to Table 4–52:

(1) These timing parameters are sample-tested only.

(2) These timing parameters are for column and row IOE pins. Designers should use the Quartus II software to verify the external timing for any pin.

Table 4–53 shows the external I/O timing parameters when using regional clock networks.

Table 4–53. Stratix Regional Clock External I/O Timing Parameters (Part 1 of 2) *Notes (1), (2)*

Symbol	Parameter
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with regional clock fed by `CLK` pin
t_{INH}	Hold time for input or bidirectional pin using IOE input register with regional clock fed by `CLK` pin
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with regional clock fed by `CLK` pin
$t_{INSUPLL}$	Setup time for input or bidirectional pin using IOE input register with regional clock fed by Enhanced PLL with default phase setting
t_{INHPLL}	Hold time for input or bidirectional pin using IOE input register with regional clock fed by Enhanced PLL with default phase setting
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using IOE output register with regional clock Enhanced PLL with default phase setting

Table 4–53. Stratix Regional Clock External I/O Timing Parameters (Part 2 of 2) Notes (1), (2)	
Symbol	**Parameter**
t_{XZPLL}	Synchronous IOE output enable register to output pin disable delay using regional clock fed by Enhanced PLL with default phase setting
t_{ZXPLL}	Synchronous IOE output enable register to output pin enable delay using regional clock fed by Enhanced PLL with default phase setting

Notes to Table 4–53:

(1) These timing parameters are sample-tested only.

(2) These timing parameters are for column and row IOE pins. Designers should use the Quartus II software to verify the external timing for any pin.

Table 4–54 shows the external I/O timing parameters when using global clock networks.

Table 4–54. Stratix Global Clock External I/O Timing Parameters Notes (1), (2)	
Symbol	**Parameter**
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with global clock fed by `CLK` pin
t_{INH}	Hold time for input or bidirectional pin using IOE input register with global clock fed by `CLK` pin
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with global clock fed by `CLK` pin
$t_{INSUPLL}$	Setup time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting
t_{INHPLL}	Hold time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using IOE output register with global clock Enhanced PLL with default phase setting
t_{XZPLL}	Synchronous IOE output enable register to output pin disable delay using global clock fed by Enhanced PLL with default phase setting
t_{ZXPLL}	Synchronous IOE output enable register to output pin enable delay using global clock fed by Enhanced PLL with default phase setting

Notes to Table 4–54:

(1) These timing parameters are sample-tested only.

(2) These timing parameters are for column and row IOE pins. Designers should use

(3) the Quartus II software to verify the external timing for any pin.

Stratix External I/O Timing

These timing parameters are for both column IOE and row IOE pins. In EP1S30 devices and above, designers can decrease the t_{SU} time by using the `FPLLCLK`, but may get positive hold time in EP1S60 and EP1S80 devices. Designers should use the Quartus II software to verify the external devices for any pin.

Tables 4–55 through 4–60 show the external timing parameters on column and row pins for EP1S10 devices.

Table 4–55. EP1S10 External I/O Timing on Column Pins Using Fast Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.238		2.325		2.668		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.240	4.549	2.240	4.836	2.240	5.218	NA	NA	ns
t_{XZ}	2.180	4.423	2.180	4.704	2.180	5.094	NA	NA	ns
t_{ZX}	2.180	4.423	2.180	4.704	2.180	5.094	NA	NA	ns

Table 4–56. EP1S10 External I/O Timing on Column Pins Using Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max			
t_{INSU}	1.992		2.054		2.359		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.395	4.795	2.395	5.107	2.395	5.527	NA	NA	ns
t_{XZ}	2.335	4.669	2.335	4.975	2.335	5.403	NA	NA	ns
t_{ZX}	2.335	4.669	2.335	4.975	2.335	5.403	NA	NA	ns
$t_{INSUPLL}$	0.975		0.985		1.097		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA	NA	ns
$t_{OUTCOPLL}$	1.262	2.636	1.262	2.680	1.262	2.769	NA	NA	ns
t_{XZPLL}	1.202	2.510	1.202	2.548	1.202	2.645	NA	NA	ns
t_{ZXPLL}	1.202	2.510	1.202	2.548	1.202	2.645	NA	NA	ns

Table 4–57. EP1S10 External I/O Timing on Column Pins Using Global Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.647		1.692		1.940		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.619	5.184	2.619	5.515	2.619	5.999	NA	NA	ns
t_{XZ}	2.559	5.058	2.559	5.383	2.559	5.875	NA	NA	ns
t_{ZX}	2.559	5.058	2.559	5.383	2.559	5.875	NA	NA	ns
$t_{INSUPLL}$	1.239		1.229		1.374		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.109	2.372	1.109	2.436	1.109	2.492	NA	NA	ns
t_{XZPLL}	1.049	2.246	1.049	2.304	1.049	2.368	NA	NA	ns
t_{ZXPLL}	1.049	2.246	1.049	2.304	1.049	2.368	NA	NA	ns

Table 4–58. EP1S10 External I/O Timing on Row Pin Using Fast Regional Clock Network *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.212		2.403		2.759		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.391	4.838	2.391	5.159	2.391	5.569	NA	NA	ns
t_{XZ}	2.418	4.892	2.418	5.215	2.418	5.637	NA	NA	ns
t_{ZX}	2.418	4.892	2.418	5.215	2.418	5.637	NA	NA	ns

Table 4–59. EP1S10 External I/O Timing on Row Pins Using Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.161		2.336		2.685		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.434	4.889	2.434	5.226	2.434	5.643	NA	NA	ns
t_{XZ}	2.461	4.493	2.461	5.282	2.461	5.711	NA	NA	ns
t_{ZX}	2.461	4.493	2.461	5.282	2.461	5.711	NA	NA	ns
$t_{INSUPLL}$	1.057		1.172		1.315		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.327	2.773	1.327	2.848	1.327	2.940	NA	NA	ns
t_{XZPLL}	1.354	2.827	1.354	2.904	1.354	3.008	NA	NA	ns
t_{ZXPLL}	1.354	2.827	1.354	2.904	1.354	3.008	NA	NA	ns

Table 4–60. EP1S10 External I/O Timing on Row Pins Using Global Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.787		1.944		2.232		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.647	5.263	2.647	5.618	2.647	6.069	NA	NA	ns
t_{XZ}	2.674	5.317	2.674	5.674	2.674	6.164	NA	NA	ns
t_{ZX}	2.674	5.317	2.674	5.674	2.674	6.164	NA	NA	ns
$t_{INSUPLL}$	1.371		1.1472		1.654		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.144	2.459	1.144	2.548	1.144	2.601	NA	NA	ns
t_{XZPLL}	1.171	2.513	1.171	2.604	1.171	2.669	NA	NA	ns
t^{ZXPLL}	1.171	2.513	1.171	2.604	1.171	2.669	NA	NA	ns

Note to Tables 4–55 to 4–60:

(1) Only EP1S25, EP1S30, and EP1S40 have speed grade of -8.

Tables 4–61 through 4–66 show the external timing parameters on column and row pins for EP1S20 devices.

Table 4–61. EP1S20 External I/O Timing on Column Pins Using Fast Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.065		2.245		2.576		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.283	4.622	2.283	4.916	2.283	5.310	NA	NA	ns
t_{XZ}	2.223	4.496	2.223	4.784	2.223	5.186	NA	NA	ns
t_{ZX}	2.223	4.496	2.223	4.784	2.223	5.186	NA	NA	ns

Table 4–62. EP1S20 External I/O Timing on Column Pins Using Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.541		1.680		1.931		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.597	5.146	2.597	5.481	2.597	5.955	NA	NA	ns
t_{XZ}	2.537	5.020	2.537	5.349	2.537	5.831	NA	NA	ns
t_{ZX}	2.537	5.020	2.537	5.349	2.537	5.831	NA	NA	ns
$t_{INSUPLL}$	0.777		0.818		0.937		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.296	2.690	1.296	2.801	1.296	2.876	NA	NA	ns
t_{XZPLL}	1.236	2.564	1.236	2.669	1.236	2.752	NA	NA	ns
t_{ZXPLL}	1.236	2.564	1.236	2.669	1.236	2.752	NA	NA	ns

Table 4–63. EP1S20 External I/O Timing on Column Pins Using Global Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.351		1.479		1.699		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.732	5.380	2.732	5.728	2.732	6.240	NA	NA	ns
t_{XZ}	2.672	5.254	2.672	5.596	2.672	6.116	NA	NA	ns
t_{ZX}	2.672	5.254	2.672	5.596	2.672	6.116	NA	NA	ns
$t_{INSUPLL}$	0.923		0.971		1.098		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.210	2.544	1.210	2.648	1.210	2.715	NA	NA	ns
t_{XZPLL}	1.150	2.418	1.150	2.516	1.150	2.591	NA	NA	ns
t_{ZXPLL}	1.150	2.418	1.150	2.516	1.150	2.591	NA	NA	ns

Table 4–64. EP1S20 External I/O Timing on Row Pins Using Fast Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.032		2.207		2.535		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.492	5.018	2.492	5.355	2.492	5.793	NA	NA	ns
t_{XZ}	2.519	5.072	2.519	5.411	2.519	5.861	NA	NA	ns
t_{ZX}	2.519	5.072	2.519	5.411	2.519	5.861	NA	NA	ns

Table 4–65. EP1S20 External I/O Timing on Row Pins Using Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.815		1.967		2.258		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.633	5.235	2.663	5.595	2.663	6.070	NA	NA	ns
t_{XZ}	2.660	5.289	2.660	5.651	2.660	6.138	NA	NA	ns
t_{ZX}	2.660	5.289	2.660	5.651	2.660	6.138	NA	NA	ns
$t_{INSUPLL}$	1.060		1.112		1.277		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.325	2.770	1.325	2.908	1.325	2.978	NA	NA	ns
t_{XZPLL}	1.352	2.824	1.352	2.964	1.352	3.046	NA	NA	ns
t_{ZXPLL}	1.352	2.824	1.352	2.964	1.352	3.046	NA	NA	ns

Table 4–66. EP1S20 External I/O Timing on Row Pins Using Global Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.742		1.887		2.170		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.674	5.308	2.674	5.675	2.674	6.158	NA	NA	ns
t_{XZ}	2.701	5.362	2.701	5.731	2.701	6.226	NA	NA	ns
t_{ZX}	2.701	5.362	2.701	5.731	2.701	6.226	NA	NA	ns
$t_{INSUPLL}$	1.353		1.418		1.613		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.158	2.447	1.158	2.602	1.158	2.642	NA	NA	ns
t_{XZPLL}	1.185	2.531	1.158	2.602	1.185	2.710	NA	NA	ns
t_{ZXPLL}	1.185	2.531	1.158	2.602	1.185	2.710	NA	NA	ns

Note to Tables 4–61 to 4–66:

(1) Only EP1S25, EP1S30, and EP1S40 have speed grade of -8.

Tables 4–67 through 4–72 show the external timing parameters on column and row pins for EP1S25 devices.

Table 4–67. EP1S25 External I/O Timing on Column Pins Using Fast Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.412		2.613		2.968		3.468		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.196	4.475	2.196	4.748	2.196	5.118	2.196	5.603	ns
t_{XZ}	2.136	4.349	2.136	4.616	2.136	4.994	2.136	5.488	ns
t_{ZX}	2.136	4.349	2.136	4.616	2.136	4.994	2.136	5.488	ns

Table 4–68. EP1S25 External I/O Timing on Column Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.535		1.661		1.877		2.125		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.739	5.396	2.739	5.746	2.739	6.262	2.739	6.946	ns
t_{XZ}	2.679	5.270	2.679	5.614	2.679	6.138	2.679	6.831	ns
t_{ZX}	2.679	5.270	2.679	5.614	2.679	6.138	2.679	6.831	ns
$t_{INSUPLL}$	0.934		0.980		1.092		1.231		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.316	2.733	1.316	2.839	1.316	2.921	1.316	3.110	ns
t^{XZPLL}	1.256	2.607	1.256	2.707	1.256	2.797	1.256	2.995	ns
t_{ZXPLL}	1.256	2.607	1.256	2.707	1.256	2.797	1.256	2.995	ns

Table 4–69. EP1S25 External I/O Timing on Column Pins Using Global Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.371		1.471		1.657		1.916		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.809	5.516	2.809	5.890	2.809	6.429	2.809	7.155	ns
t_{XZ}	2.749	5.390	2.749	5.758	2.749	6.305	2.749	7.040	ns
t_{ZX}	2.749	5.390	2.749	5.758	2.749	6.305	2.749	7.040	ns
$t_{INSUPLL}$	1.271		1.327		1.491		1.677		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.124	2.396	1.124	2.492	1.124	2.522	1.124	2.602	ns
t_{XZPLL}	1.064	2.270	1.064	2.360	1.064	2.398	1.064	2.487	ns
t_{ZXPLL}	1.064	2.270	1.064	2.360	1.064	2.398	1.064	2.487	ns

Table 4–70. EP1S25 External I/O Timing on Row Pins Using Fast Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.429		2.631		2.990		3.503		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.376	4.821	2.376	5.131	2.376	5.538	2.376	6.063	ns
t_{XZ}	2.403	4.875	2.403	5.187	2.403	5.606	2.403	6.145	ns
t_{ZX}	2.403	4.875	2.403	5.187	2.403	5.606	2.403	6.145	ns

Table 4–71. EP1S25 External I/O Timing on Row Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.793		1.927		2.182		2.542		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.759	5.457	2.759	5.835	2.759	6.346	2.759	7.024	ns
t_{XZ}	2.786	5.511	2.786	5.891	2.786	6.414	2.786	7.106	ns
t_{ZX}	2.786	5.511	2.786	5.891	2.786	6.414	2.786	7.106	ns
$t_{INSUPLL}$	1.169		1.221		1.373		1.600		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.375	2.861	1.375	2.999	1.375	3.082	1.375	3.174	ns
t_{XZPLL}	1.402	2.915	1.402	3.055	1.402	3.150	1.402	3.256	ns
t_{ZXPLL}	1.402	2.915	1.402	3.055	1.402	3.150	1.402	3.256	ns

Table 4–72. EP1S25 External I/O Timing on Row Pins Using Global Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.665		1.779		2.012		2.372		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.834	5.585	2.834	5.983	2.834	6.516	2.834	7.194	ns
t_{XZ}	2.861	5.639	2.861	6.039	2.861	6.584	2.861	7.276	ns
t_{ZX}	2.861	5.639	2.861	6.039	2.861	6.584	2.861	7.276	ns
$t_{INSUPLL}$	1.538		1.606		1.816		2.121		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.164	2.492	1.164	2.614	1.164	2.639	1.164	2.653	ns
t_{XZPLL}	1.191	2.546	1.191	2.670	1.191	2.707	1.191	2.735	ns
t_{ZXPLL}	1.191	2.546	1.191	2.670	1.191	2.707	1.191	2.735	ns

Tables 4–73 through 4–78 show the external timing parameters on column and row pins for EP1S30 devices.

Table 4–73. EP1S30 External I/O Timing on Column Pins Using Fast Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.502		2.680		3.062		3.591		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.473	4.965	2.473	5.329	2.473	5.784	2.473	6.392	ns
t_{XZ}	2.413	4.839	2.413	5.197	2.413	5.660	2.413	6.277	ns
t_{ZX}	2.413	4.839	2.413	5.197	2.413	5.660	2.413	6.277	ns

Table 4–74. EP1S30 External I/O Timing on Column Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.286		2.426		2.769		3.249		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.641	5.225	2.641	5.629	2.641	6.130	2.641	6.796	ns
t_{XZ}	2.581	5.099	2.581	5.497	2.581	6.006	2.581	6.681	ns
t_{ZX}	2.581	5.099	2.581	5.497	2.581	6.006	2.581	6.681	ns
$t_{INSUPLL}$	1.200		1.185		1.344		1.662		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.108	2.367	1.108	2.534	1.108	2.569	1.108	2.517	ns
t_{XZPLL}	1.048	2.241	1.048	2.402	1.048	2.445	1.048	2.402	ns
t_{ZXPLL}	1.048	2.241	1.048	2.402	1.048	2.445	1.048	2.402	ns

Table 4–75. EP1S30 External I/O Timing on Column Pins Using Global Clock Networks (Part 1 of 2)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.935		2.029		2.310		2.709		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.814	5.532	2.814	5.980	2.814	6.536	2.814	7.274	ns

Table 4–75. EP1S30 External I/O Timing on Column Pins Using Global Clock Networks (Part 2 of 2)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{XZ}	2.754	5.406	2.754	5.848	2.754	6.412	2.754	7.159	ns
t_{ZX}	2.754	5.406	2.754	5.848	2.754	6.412	2.754	7.159	ns
$t_{INSUPLL}$	1.265		1.236		1.403		1.756		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.068	2.302	1.068	2.483	1.068	2.510	1.068	2.423	ns
t_{XZPLL}	1.008	2.176	1.008	2.351	1.008	2.386	1.008	2.308	ns
t_{ZXPLL}	1.008	2.176	1.008	2.351	1.008	2.386	1.008	2.308	ns

Table 4–76. EP1S30 External I/O Timing on Row Pins Using Fast Regional Clock Networks

Parameters	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.616		2.808		3.223		3.797		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.542	5.114	2.542	5.502	2.542	5.965	2.542	6.581	ns
t_{XZ}	2.569	5.168	2.569	5.558	2.569	6.033	2.569	6.663	ns
t_{ZX}	2.569	5.168	2.569	5.558	2.569	6.033	2.569	6.663	ns

Table 4–77. EP1S30 External I/O Timing on Row Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.322		2.467		2.828		3.342		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.731	5.408	2.731	5.843	2.731	6.360	2.731	7.036	ns
t_{XZ}	2.758	5.462	2.758	5.899	2.758	6.428	2.758	7.118	ns
t_{ZX}	2.758	5.462	2.758	5.899	2.758	6.428	2.758	7.118	ns
$t_{INSUPLL}$	1.291		1.283		1.469		1.832		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.192	2.539	1.192	2.737	1.192	2.786	1.192	2.742	ns
t_{XZPLL}	1.219	2.539	1.219	2.793	1.219	2.854	1.219	2.824	ns
t_{ZXPLL}	1.219	2.539	1.219	2.793	1.219	2.854	1.219	2.824	ns

Table 4–78. EP1S30 External I/O Timing on Row Pins Using Global Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.995		2.089		2.398		2.830		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.917	5.735	2.917	6.221	2.917	6.790	2.917	7.548	ns
t_{XZ}	2.944	5.789	2.944	6.277	2.944	6.858	2.944	7.630	ns
t_{ZX}	2.944	5.789	2.944	6.277	2.944	6.858	2.944	7.630	ns
$t_{INSUPLL}$	1.337		1.312		1.508		1.902		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.164	2.493	1.164	2.708	1.164	2.747	1.164	2.672	ns
t_{XZPLL}	1.191	2.547	1.191	2.764	1.191	2.815	1.191	2.754	ns
t_{ZXPLL}	1.191	2.547	1.191	2.764	1.191	2.815	1.191	2.754	ns

Tables 4–79 through 4–84 show the external timing parameters on column and row pins for EP1S40 devices.

Table 4–79. EP1S40 External I/O Timing on Column Pins Using Fast Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.696		2.907		3.290		2.899		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.506	5.015	2.506	5.348	2.506	5.809	2.698	7.286	ns
t_{XZ}	2.446	4.889	2.446	5.216	2.446	5.685	2.638	7.171	ns
t_{ZX}	2.446	4.889	2.446	5.216	2.446	5.685	2.638	7.171	ns

Table 4–80. EP1S40 External I/O Timing on Column Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.413		2.581		2.914		2.938		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.668	5.254	2.668	5.628	2.668	6.132	2.869	7.307	ns
t_{XZ}	2.608	5.128	2.608	5.496	2.608	6.008	2.809	7.192	ns
t_{ZX}	2.608	5.128	2.608	5.496	2.608	6.008	2.809	7.192	ns
$t_{INSUPLL}$	1.385		1.376		1.609		1.837		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.117	2.382	1.117	2.552	1.117	2.504	1.117	2.542	ns
t_{XZPLL}	1.057	2.256	1,057	2.420	1.057	2.380	1.057	2.427	ns
t_{ZXPLL}	1.057	2.256	1,057	2.420	1.057	2.380	1.057	2.427	ns

Table 4–81. EP1S40 External I/O Timing on Column Pins Using Global Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.126		2.268		2.558		2.930		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.856	5.585	2.856	5.987	2.856	6.541	2.847	7.253	ns
t_{XZ}	2.796	5.459	2.796	5.855	2.796	6.417	2.787	7.138	ns
t_{ZX}	2.796	5.459	2.796	5.855	2.796	6.417	2.787	7.138	ns
$t_{INSUPLL}$	1.466		1.455		1.711		1.906		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.092	2.345	1.092	2.510	1.092	2.455	1.089	2.473	ns
t_{XZPLL}	1.032	2.219	1.032	2.378	1.032	2.331	1.029	2.358	ns
t_{ZXPLL}	1.032	2.219	1.032	2.378	1.032	2.331	1.029	2.358	ns

Table 4–82. EP1S40 External I/O Timing on Row Pins Using Fast Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.472		2.685		3.083		3.056		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.631	5.258	2.631	5.625	2.631	6.105	2.745	7.324	ns
t_{XZ}	2.658	5.312	2.658	5.681	2.658	6.173	2.772	7.406	ns
t_{ZX}	2.658	5.312	2.658	5.681	2.658	6.173	2.772	7.406	ns

Table 4–83. EP1S40 External I/O Timing on Row Pins Using Regional Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.349		2.526		2.898		2.952		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.725	5.381	2.725	5.784	2.725	6.290	2.725	7.426	ns
t_{XZ}	2.752	5.435	2.752	5.840	2.752	6.358	2.936	7.508	ns
t_{ZX}	2.752	5.435	2.752	5.840	2.752	6.358	2.936	7.508	ns
$t_{INSUPLL}$	1.328		1.322		1.605		1.883		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.169	2.502	1.169	2.698	1.169	2.650	1.169	2.691	ns
t_{XZPLL}	1.196	2.556	1.196	2.754	1.196	2.718	1.196	2.773	ns
t_{ZXPLL}	1.196	2.556	1.196	2.754	1.196	2.718	1.196	2.773	ns

Table 4–84. EP1S40 External I/O Timing on Row Pins Using Global Clock Networks

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.020		2.171		2.491		2.898		ns
t_{INH}	0.000		0.000		0.000		0.000		ns
t_{OUTCO}	2.912	5.710	2.912	6.139	2.912	6.697	2.931	7.480	ns
t_{XZ}	2.939	5.764	2.939	6.195	2.939	6.765	2.958	7.562	ns
t_{ZX}	2.939	5.764	2.939	6.195	2.939	6.765	2.958	7.562	ns
$t_{INSUPLL}$	1.370		1.368		1.654		1.881		ns
t_{INHPLL}	0.000		0.000		0.000		0.000		ns
$t_{OUTCOPLL}$	1.144	2.460	1.144	2.652	1.144	2.601	1.170	2.693	ns
t_{XZPLL}	1.171	2.514	1.171	2.708	1.171	2.669	1.197	2.775	ns
t_{ZXPLL}	1.171	2.514	1.171	2.708	1.171	2.669	1.197	2.775	ns

Tables 4–85 through 4–90 show the external timing parameters on column and row pins for EP1S60 devices.

Table 4–85. EP1S60 External I/O Timing on Column Pins Using Fast Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.029		3.277		3.733		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.446	4.871	2.446	5.215	2.446	5.685	NA	NA	ns
t_{XZ}	2.386	4.745	2.386	5.083	2.386	5.561	NA	NA	ns
t_{ZX}	2.386	4.745	2.386	5.083	2.386	5.561	NA	NA	ns

Table 4–86. EP1S60 External I/O Timing on Column Pins Using Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.491		2.691		3.060		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.767	5.409	2.767	5.801	2.767	6.358	NA	NA	ns
t_{XZ}	2.707	5.283	2.707	5.669	2.707	6.234	NA	NA	ns
t_{ZX}	2.707	5.283	2.707	5.669	2.707	6.234	NA	NA	ns
$t_{INSUPLL}$	1.233		1.270		1.438		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.078	2.278	1.078	2.395	1.078	2.428	NA	NA	ns
t_{XZPLL}	1.018	2.152	1.018	2.263	1.018	2.304	NA	NA	ns
t_{ZXPLL}	1.018	2.152	1.018	2.263	1.018	2.304	NA	NA	ns

Table 4–87. EP1S60 External I/O Timing on Column Pins Using Global Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.000		2.152		2.441		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	3.051	5.900	3.051	6.340	3.051	6.977	NA	NA	ns
t_{XZ}	2.991	5.774	2.991	6.208	2.991	6.853	NA	NA	ns
t_{ZX}	2.991	5.774	2.991	6.208	2.991	6.853	NA	NA	ns
$t_{INSUPLL}$	1.315		1.362		1.543		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.029	2.196	1.029	2.303	1.029	2.323	NA	NA	ns
t_{XZPLL}	0.969	2.070	0.969	2.171	0.969	2.199	NA	NA	ns
t_{ZXPLL}	0.969	2.070	0.969	2.171	0.969	2.199	NA	NA	ns

Table 4–88. EP1S60 External I/O Timing on Row Pins Using Fast Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	3.144		3.393		3.867		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.643	5.275	2.643	5.654	2.643	6.140	NA	NA	ns
t_{XZ}	2.670	5.329	2.670	5.710	2.670	6.208	NA	NA	ns
t_{ZX}	2.670	5.329	2.670	5.710	2.670	6.208	NA	NA	ns

Table 4–89. EP1S60 External I/O Timing on Row Pins Using Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.775		2.990		3.407		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.867	5.644	2.867	6.057	2.867	6.600	NA	NA	ns
t_{XZ}	2.894	5.698	2.894	6.113	2.894	6.668	NA	NA	ns
t_{ZX}	2.894	5.698	2.894	6.113	2.894	6.668	NA	NA	ns
$t_{INSUPLL}$	1.523		1.577		1.791		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.174	2.507	1.174	2.643	1.174	2.664	NA	NA	ns
t_{XZPLL}	1.201	2.561	1.201	2.699	1.201	2.732	NA	NA	ns
t_{ZXPLL}	1.201	2.561	1.201	2.699	1.201	2.732	NA	NA	ns

Table 4–90. EP1S60 External I/O Timing on Row Pins Using Global Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.232		2.393		2.721		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	3.182	6.187	3.182	6.654	3.182	7.286	NA	NA	ns
t_{XZ}	3.209	6.241	3.209	6.710	3.209	7.354	NA	NA	ns
t_{ZX}	3.209	6.241	3.209	6.710	3.209	7.354	NA	NA	ns
$t_{INSUPLL}$	1.651		1.612		1.833		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.154	2.469	1.154	2.608	1.154	2.622	NA	NA	ns
t_{XZPLL}	1.181	2.523	1.181	2.664	1.181	2.690	NA	NA	ns
t_{ZXPLL}	1.181	2.523	1.181	2.664	1.181	2.690	NA	NA	ns

Note to Tables 4–85 to 4–90:

(1) Only EP1S25, EP1S30, and EP1S40 devices have the -8 speed grade.

Tables 4–91 through 4–96 show the external timing parameters on column and row pins for EP1S80 devices.

Table 4–91. EP1S80 External I/O Timing on Column Pins Using Fast Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.328		2.528		2.900		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.422	4.830	2.422	5.169	2.422	5.633	NA	NA	ns
t_{XZ}	2.362	4.704	2.362	5.037	2.362	5.509	NA	NA	ns
t_{ZX}	2.362	4.704	2.362	5.037	2.362	5.509	NA	NA	ns

Table 4–92. EP1S80 External I/O Timing on Column Pins Using Regional Clock Networks Note (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.760		1.912		2.194		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.761	5.398	2.761	5.785	2.761	6.339	NA	NA	ns
t_{XZ}	2.701	5.272	2.701	5.653	2.701	6.215	NA	NA	ns
t_{ZX}	2.701	5.272	2.701	5.653	2.701	6.215	NA	NA	ns
$t_{INSUPLL}$	0.462		0.606		0.785		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.661	2.849	1.661	2.859	1.661	2.881	NA	NA	ns
t_{XZPLL}	1.601	2.723	1.601	2.727	1.601	2.757	NA	NA	ns
t_{ZXPLL}	1.601	2.723	1.601	2.727	1.601	2.757	NA	NA	ns

Table 4–93. EP1S80 External I/O Timing on Column Pins Using Global Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	0.884		0.976		1.118		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	3.267	6.274	3.267	6.721	3.267	7.415	NA	NA	ns
t_{XZ}	3.207	6.148	3.207	6.589	3.207	7.291	NA	NA	ns
t_{ZX}	3.207	6.148	3.207	6.589	3.207	7.291	NA	NA	ns
$t_{INSUPLL}$	0.506		0.656		0.838		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.635	2.805	1.635	2.809	1.635	2.828	NA	NA	ns
t_{XZPLL}	1.575	2.679	1.575	2.677	1.575	2.704	NA	NA	ns
t_{ZXPLL}	1.575	2.679	1.575	2.677	1.575	2.704	NA	NA	ns

Table 4–94. EP1S80 External I/O Timing on Row Pins Using Fast Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.792		2.993		3.386		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.619	5.235	2.619	5.609	2.619	6.086	NA	NA	ns
t_{XZ}	2.646	5.289	2.646	5.665	2.646	6.154	NA	NA	ns
t_{ZX}	2.646	5.289	2.646	5.665	2.646	6.154	NA	NA	ns

Table 4–95. EP1S80 External I/O Timing on Row Pins Using Regional Clock Networks *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	2.295		2.454		2.767		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	2.917	5.732	2.917	6.148	2.917	6.705	NA	NA	ns
t_{XZ}	2.944	5.786	2.944	6.204	2.944	6.773	NA	NA	ns
t_{ZX}	2.944	5.786	2.944	6.204	2.944	6.773	NA	NA	ns
$t_{INSUPLL}$	1.011		1.161		1.372		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.808	3.169	1.808	3.209	1.808	3.233	NA	NA	ns
t_{XZPLL}	1.835	3.223	1.835	3.265	1.835	3.301	NA	NA	ns
t_{ZXPLL}	1.835	3.223	1.835	3.265	1.835	3.301	NA	NA	ns

Table 4–96. EP1S80 External I/O Timing on Rows Using Pin Global Clock Networks *Note (1)*

Symbol	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{INSU}	1.362		1.451		1.613		NA		ns
t_{INH}	0.000		0.000		0.000		NA		ns
t_{OUTCO}	3.457	6.665	3.457	7.151	3.457	7.859	NA	NA	ns
t_{XZ}	3.484	6.719	3.484	7.207	3.484	7.927	NA	NA	ns
t_{ZX}	3.484	6.719	3.484	7.207	3.484	7.927	NA	NA	ns
$t_{INSUPLL}$	o.994		1.143		1.351		NA		ns
t_{INHPLL}	0.000		0.000		0.000		NA		ns
$t_{OUTCOPLL}$	1.821	3.186	1.821	3.227	1.821	3.254	NA	NA	ns
t_{XZPLL}	1.848	3.240	1.848	3.283	1.848	3.322	NA	NA	ns
t_{ZXPLL}	1.848	3.240	1.848	3.283	1.848	3.322	NA	NA	ns

Note to Tables 4–91 to 4–96:

(1) Only EP1S25, EP1S30, and EP1S40 devices have the -8 speed grade.

Definition of I/O Skew

I/O skew is defined as the absolute value of the worst-case difference in clock-to-out times (t_{CO}) between any two output registers fed by a common clock source.

I/O bank skew is made up of the following components:

- Clock network skews: This is the difference between the arrival times of the clock at the clock input port of the two IOE registers.
- Package skews: This is the package trace length differences between (I/O pad A to I/O pin A) and (I/O pad B to I/O pin B).

Figure 4–5 shows an example of two IOE registers located in the same bank, being fed by a common clock source. The clock can come from an input pin or from a PLL output.

Figure 4–5. I/O Skew within an I/O Bank

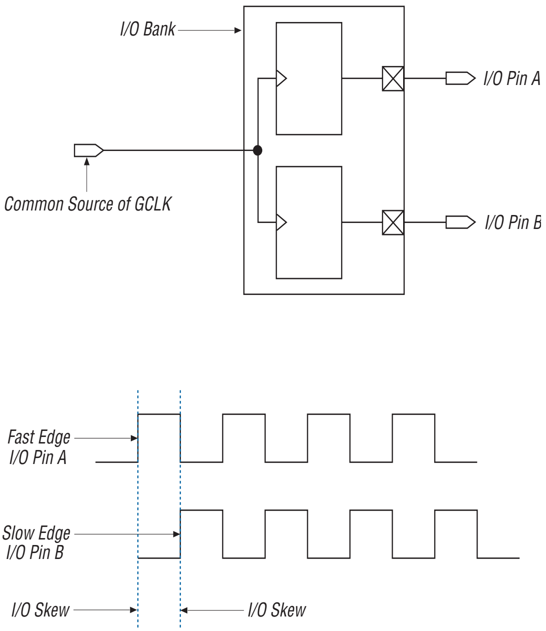
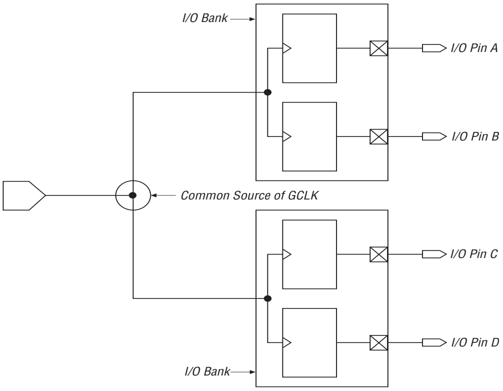


Figure 4–6 shows the case where four IOE registers are located in two different I/O banks.

Figure 4–6. I/O Skew Across Two I/O Banks



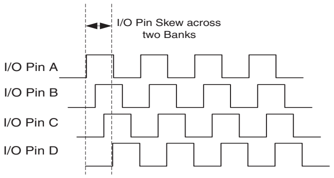


Table 4–97 defines the timing parameters used to define the timing for horizontal I/O pins (side banks 1, 2, 5, 6) and vertical I/O pins (top and bottom banks 3, 4, 7, 8). The timing parameters define the skew within an I/O bank, across two neighboring I/O banks on the same side of the device, across all horizontal I/O banks, across all vertical I/O banks, and the skew for the overall device.

Table 4–97. Output Pin Timing Skew Definitions (Part 1 of 2)

Symbol	Definition
t_{SB_HIO}	Row I/O (HIO) within one I/O bank *(1)*
t_{SB_VIO}	Column I/O (VIO) within one I/O bank *(1)*
t_{SS_HIO}	Row I/O (HIO) same side of the device, across two banks *(2)*
t_{SS_VIO}	Column I/O (VIO) same side of the device, across two banks *(2)*

Table 4–97. Output Pin Timing Skew Definitions (Part 2 of 2)

Symbol	Definition
t_{LR_HIO}	Across all HIO banks (1, 2, 5, 6); across four similar type I/O banks
t_{TB_VIO}	Across all VIO banks (3, 4, 7, 8); across four similar type I/O banks
$t_{OVERALL}$	Output timing skew for all I/O pins on the device.

Notes to Table 4–97:

(1) See Figure 4–5 on page 4–56.

(2) See Figure 4–6 on page 4–57.

Table 4–98 shows the I/O skews when using the same global or regional clock to feed IOE registers in I/O banks around each device. These values can be used for calculating the timing budget on the output (write) side of a memory interface. These values already factor in the package skew.

Table 4–98. Output Skew for Stratix by Device Density

Symbol	Skew (ps) *(1)*		
	EP1S10 to EP1S30	EP1S40	EP1S60 & EP1S80
t_{SB_HIO}	90	290	500
t_{SB_VIO}	160	290	500
t_{SS_HIO}	90	460	600
t_{SS_VIO}	180	520	630
t_{LR_HIO}	150	490	600
t_{TB_VIO}	190	580	670
$t_{OVERALL}$	430	630	880

Note to Table 4–98:

(1) The skew numbers above account for worst case package skews.

Skew on Input Pins

Table 4–99 shows the package skews that were considered to get the worst case I/O skew value. These values can be used, for example, when calculating the timing budget on the input (Read) side of a memory interface.

Table 4–99. Package Skew on Input Pins

Package Parameter	Worst-Case Skew (ps)
Pins in the same I/O bank	50
Pins in top/bottom (vertical I/O) banks	50
Pins in left/right side (horizontal I/O) banks	50
Pins across the entire device	100

PLL Counter & Clock Network Skews

Table 4–100 shows the clock skews between different clock outputs from the Stratix device PLL.

Table 4–100. PLL Counter & Clock Network Skews

Parameter	Worst-Case Skew (ps)
Clock skew between two external clock outputs driven by the same counter	100
Clock skew between two external clock outputs driven by the different counters with the same settings	150
Dual-purpose PLL dedicated clock output used as I/O pin vs. regular I/O pin	270 *(1)*
Clock skew between any two outputs of the PLL that drive global clock networks	150

Note to Table 4–100:

(1) The Quartus II software models 270 ps of delay on the PLL dedicated clock output (`PLL6_OUT[3..0]p/n` and `PLL5_OUT[3..0]p/n`) pins both when used as clocks and when used as I/O pins.

I/O Timing Measurement Methodology

Different I/O standards require different baseline loading techniques for reporting timing delays. Altera characterizes timing delays with the required termination and loading for each I/O standard. The timing information is specified from the input clock pin up to the output pin of the FPGA device. The Quartus II software calculates the I/O timing for each I/O standard with a default baseline loading as specified by the I/O standard.

Altera measures clock-to-output delays (t_{CO}) at worst-case process, minimum voltage, and maximum temperature (PVT) for the 3.3-V LVTTL I/O standard with 4 mA (default case) current drive strength setting and fast slew rate setting. I/O adder delays are measured to calculate the t_{CO} change at worst-case PVT across all I/O standards and current drive strength settings with the default loading shown in Table 4–101 on page 4–61. Timing derating data for additional loading is taken for t_{CO} across worst-case PVT for all I/O standards and drive strength settings. These three pieces of data are used to predict the timing at the output pin.

> t_{CO} at pin = t_{OUTCO} max for 3.3-V 4 mA LVTTL + I/O Adder + Output Delay Adder for Loading

Simulation using IBIS models is required to determine the delays on the PCB traces in addition to the output pin delay timing reported by Quartus II and the timing model in the device handbook.

1. Simulate the output driver of choice into the generalized test setup, using values from Table 4–101 on page 4–61.

2. Record the time to VMEAS.

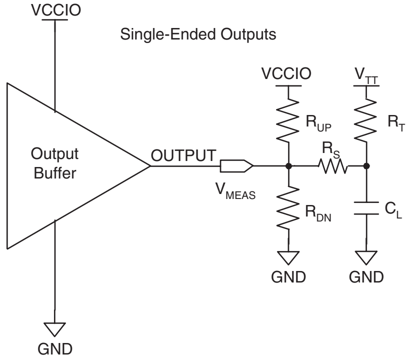
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS input buffer model or an equivalent capacitance value to represent the load.

4. Record the time to VMEAS.

5. Compare the results of steps 2 and 4. The increase or decrease in delay should be added to or subtracted from the I/O Standard Output Adder delays to yield the actual worst-case propagation delay (clock-to-input) of the PCB trace.

Quartus II reports maximum timing with the conditions shown in Table 4–101 on page 4–61 using the proceeding equation. Figure 4–7 on page 4–61 shows the model of the circuit that is represented by Quartus II output timing.

Figure 4–7. Output Delay Timing Reporting Setup Modeled by Quartus II



Notes to Figure 4–7:

(1) Output pin timing is reported at the output pin of the FPGA device. Additional delays for loading and board trace delay need to be accounted for with IBIS model simulations.

(2) VCCINT is 1.42-V unless otherwise specified.

Table 4–101. Reporting Methodology For Maximum Timing For Single-Ended Output Pins (Part 1 of 2) Notes (1), (2), (3)

I/O Standard	Loading and Termination							Measurement Point
	R_{UP} Ω	R_{DN} Ω	R_S Ω	R_T Ω	VCCIO (V)	VTT (V)	C_L (pF)	V_{MEAS}
3.3V LVTTL	–	–	0	–	2.950	2.95	10	1.500
2.5V LVTTL	–	–	0	–	2.370	2.37	10	1.200
1.8V LVTTL	–	–	0	–	1.650	1.65	10	0.880
1.5V LVTTL	–	–	0	–	1.400	1.40	10	0.750
3.3V LVCMOS	–	–	0	–	2.950	2.95	10	1.500
2.5V LVCMOS	–	–	0	–	2.370	2.37	10	1.200
1.8V LVCMOS	–	–	0	–	1.650	1.65	10	0.880
1.5V LVCMOS	–	–	0	–	1.400	1.40	10	0.750
3.3V GTL	–	–	0	25	2.950	1.14	30	0.740
2.5V GTL	–	–	0	25	2.370	1.14	30	0.740
3.3V GTL+	–	–	0	25	2.950	1.35	30	0.880
2.5V GTL+	–	–	0	25	2.370	1.35	30	0.880
3.3V SSTL-3 class 2	–	–	25	25	2.950	1.25	30	1.250

Table 4–101. Reporting Methodology For Maximum Timing For Single-Ended Output Pins (Part 2 of 2) *Notes (1), (2), (3)*

I/O Standard	Loading and Termination							Measurement Point
	R_{UP} Ω	R_{DN} Ω	R_S Ω	R_T Ω	VCCIO (V)	VTT (V)	C_L (pF)	V_{MEAS}
3.3V SSTL-3 class 1	–	–	25	50	2.950	1.250	30	1.250
2.5V SSTL-2 class 2	–	–	25	25	2.370	1.110	30	1.110
2.5V SSTL-2 class 1	–	–	25	50	2.370	1.110	30	1.110
1.8V SSTL-18 class 2	–	–	25	25	1.650	0.760	30	0.760
1.8V SSTL-18 class 1	–	–	25	50	1.650	0.760	30	0.760
1.5V HSTL class 2	–	–	0	25	1.400	0.700	20	0.680
1.5V HSTL class 1	–	–	0	50	1.400	0.700	20	0.680
1.8V HSTL class 2	–	–	0	25	1.650	0.700	20	0.880
1.8V HSTL class 1	–	–	0	50	1.650	0.700	20	0.880
3.3V PCI *(4)*	–/25	25/–	0	–	2.950	2.950	10	0.841/1.814
3.3V PCI-X 1.0 *(4)*	–/25	25/–	0	–	2.950	2.950	10	0.841/1.814
3.3V Compact PCI *(4)*	–/25	25/–	0	–	2.950	2.950	10	0.841/1.814
3.3V AGP 1X *(4)*	–/25	25/–	0	–	2.950	2.950	10	0.841/1.814
3.3V CTT	–	–	25	50	2.050	1.350	30	1.350

Notes to Table 4–101:

(1) Input measurement point at internal node is 0.5 × VCCINT.

(2) Output measuring point for data is V_{MEAS}.

(3) Input stimulus edge rate is 0 to VCCINT in 0.5 ns (internal signal) from the driver preceding the IO buffer.

(4) The first value is for output rising edge and the second value is for output falling edge. The hyphen (-) indicates infinite resistance or disconnection.

Table 4–102 shows the reporting methodology used by Quartus II for minimum timing information for output pins.

Table 4–102. Reporting Methodology For Minimum Timing For Single-Ended Output Pins (Part 1 of 2) Notes (1), (2), (3)

I/O Standard	Loading and Termination							Measurement Point
	R_{UP} Ω	R_{DN} Ω	R_S Ω	R_T Ω	VCCIO (V)	VTT (V)	C_L (pF)	V_{MEAS}
3.3V LVTTL	–	–	0	–	3.600	3.600	10	1.800
2.5V LVTTL	–	–	0	–	2.630	2.630	10	1.200
1.8V LVTTL	–	–	0	–	1.950	1.950	10	0.880
1.5V LVTTL	–	–	0	–	1.600	1.600	10	0.750
3.3V LVCMOS	–	–	0	–	3.600	3.600	10	1.800
2.5V LVCMOS	–	–	0	–	2.630	2.630	10	1.200
1.8V LVCMOS	–	–	0	–	1.950	1.950	10	0.880
1.5V LVCMOS	–	–	0	–	1.600	1.600	10	0.750
3.3V GTL	–	–	0	25	3.600	1.260	30	0.860
2.5V GTL	–	–	0	25	2.630	1.260	30	0.860
3.3V GTL+	–	–	0	25	3.600	1.650	30	1.120
2.5V GTL+	–	–	0	25	2.630	1.650	30	1.120
3.3V SSTL-3 class 2	–	–	25	25	3.600	1.750	30	1.750
3.3V SSTL-3 class 1	–	–	25	50	3.600	1.750	30	1.750
2.5V SSTL-2 class 2	–	–	25	25	2.630	1.390	30	1.390
2.5V SSTL-2 class 1	–	–	25	50	2.630	1.390	30	1.390
1.8V SSTL-18 class 2	–	–	25	25	1.950	1.040	30	1.040
1.8V SSTL-18 class 1	–	–	25	50	1.950	1.040	30	1.040
1.5V HSTL class 2	–	–	0	25	1.600	0.800	20	0.900
1.5V HSTL class 1	–	–	0	50	1.600	0.800	20	0.900
1.8V HSTL class 2	–	–	0	25	1.950	0.900	20	1.000
1.8V HSTL class 1	–	–	0	50	1.950	0.900	20	1.000
3.3V PCI *(4)*	–/25	25/–	0	–	3.600	1.950	10	1.026/2.214
3.3V PCI-X 1.0 *(4)*	–/25	25/–	0	–	3.600	1.950	10	1.026/2.214
3.3V Compact PCI *(4)*	–/25	25/–	0	–	3.600	3.600	10	1.026/2.214
3.3V AGP 1X *(4)*	–/25	25/–	0	–	3.600	3.600	10	1.026/2.214

Table 4–102. Reporting Methodology For Minimum Timing For Single-Ended Output Pins (Part 2 of 2) *Notes (1), (2), (3)*

I/O Standard	Loading and Termination							Measurement Point
	R_{UP} Ω	R_{DN} Ω	R_S Ω	R_T Ω	VCCIO (V)	VTT (V)	C_L (pF)	V_{MEAS}
3.3V CTT	–	–	25	50	3.600	1.650	30	1.650

Notes to Table 4–102:

(1) Input measurement point at internal node is 0.5 × VCCINT.

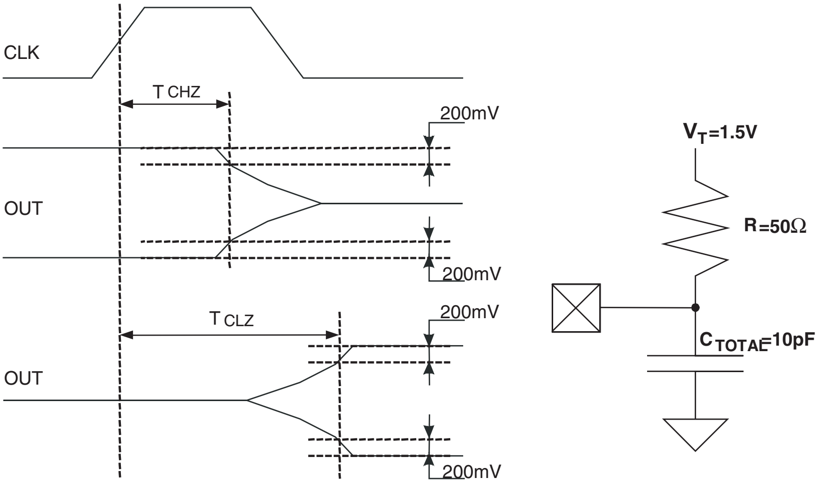
(2) Output measuring point for data is V_{MEAS}. When two values are given, the first is the measurement point on the rising edge and the other is for the falling edge.

(3) Input stimulus edge rate is 0 to VCCINT in 0.5 ns (internal signal) from the driver preceding the I/O buffer.

(4) The first value is for output rising edge and the second value is for output falling edge. The hyphen (-) indicates infinite resistance or disconnection.

Table 4–8 on page 4–64 shows the measurement setup for output disable and output enable timing. The T_{CHZ} stands for clock to high Z time delay and is the same as T_{XZ}. The T_{CLZ} stands for clock to low Z (driving) time delay and is the same as T_{ZX}.

Figure 4–8. Measurement Setup for T_{XZ} and T_{ZX}



External I/O Delay Parameters

External I/O delay timing parameters for I/O standard input and output adders and programmable input and output delays are specified by speed grade independent of device density. All of the timing parameters in this section apply to both flip-chip and wire-bond packages.

Tables 4–103 through 4–108 show the input adder delays associated with column and row I/O pins. If an I/O standard is selected other than 3.3-V LVTTL or LVCMOS, add the selected delay to the external t_{INSU} and $t_{INSUPLL}$ I/O parameters shown in Tables 4–54 through 4–96.

Table 4–103. Stratix I/O Standard Column Pin Input Delay Adders Notes (1)

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS		0		0		0		0	ps
3.3-V LVTTL		0		0		0		0	ps
2.5-V LVTTL		19		19		22		26	ps
1.8-V LVTTL		221		232		266		313	ps
1.5-V LVTTL		352		369		425		500	ps
GTL		–45		–48		–55		–64	ps
GTL+		–75		–79		–91		–107	ps
3.3-V PCI		0		0		0		0	ps
3.3-V PCI-X 1.0		0		0		0		0	ps
Compact PCI		0		0		0		0	ps
AGP 1×		0		0		0		0	ps
AGP 2×		0		0		0		0	ps
CTT		120		126		144		170	ps
SSTL-3 class I		–162		–171		–196		–231	ps
SSTL-3 class II		–162		–171		–196		–231	ps
SSTL-2 class I		–202		–213		–244		–287	ps
SSTL-2 class II		–202		–213		–244		–287	ps
SSTL-18 class I		78		81		94		110	ps
SSTL-18 class II		78		81		94		110	ps
1.5-V HSTL class I		–76		–80		–92		–108	ps
1.5-V HSTL class II		–76		–80		–92		–108	ps
1.8-V HSTL class I		73		77		88		104	ps
1.8-V HSTL class II		73		77		88		104	ps

***Table 4–104. Stratix I/O Standard Row Pin Input Delay Adders** Notes (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS		0		0		0		0	ps
3.3-V LVTTL		0		0		0		0	ps
2.5-V LVTTL		21		22		25		29	ps
1.8-V LVTTL		181		190		218		257	ps
1.5-V LVTTL		300		315		362		426	ps
GTL		0		0		0		0	ps
GTL+		–152		–160		–184		–216	ps
3.3-V PCI		0		0		0		0	ps
3.3-V PCI-X 1.0		0		0		0		0	ps
Compact PCI		0		0		0		0	ps
AGP 1×		0		0		0		0	ps
AGP 2×		0		0		0		0	ps
CTT		–168		–177		–203		–239	ps
SSTL-3 class I		–193		–203		–234		–275	ps
SSTL-3 class II		–193		–203		–234		–275	ps
SSTL-2 class I		–262		–276		–317		–373	ps
SSTL-2 class II		–262		–276		–317		–373	ps
SSTL-18 class I		–105		–111		–127		–150	ps
SSTL-18 class II		0		0		0		0	ps
1.5-V HSTL class I		–151		–159		–183		–215	ps
1.5-V HSTL class II		0		0		0		0	ps
1.8-V HSTL class I		73		77		88		104	ps
1.8-V HSTL class II		73		77		88		104	ps
LVDS *(1)*		–149		–157		–180		–212	ps
LVPECL *(1)*		–149		–157		–180		–212	ps
3.3-V PCML *(1)*		–65		–69		–79		–93	ps
HyperTransport *(1)*		77		–81		–93		–110	ps

Tables 4–105 through 4–108 show the output adder delays associated with column and row I/O pins for both fast and slow slew rates. If an I/O standard is selected other than 3.3-V LVTTL 4mA or LVCMOS 2 mA with

a fast slew rate, add the selected delay to the external t_{OUTCO}, $t_{OUTCOPLL}$, t_{XZ}, t_{ZX}, t_{XZPLL}, and t_{ZXPLL} I/O parameters shown in Table 4–55 on page 4–35 through Table 4–96 on page 4–55.

Table 4–105. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 1 of 2) *Note (1)*

Parameter		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		0		0		0		0	ps
	4 mA		–939		–986		–986		–986	ps
	8 mA		–1,706		–1,792		–1,792		–1,792	ps
	12 mA		–1,895		–1,990		–1,990		–1,990	ps
	24 mA		–2,052		–2,155		–2,155		–2,155	ps
3.3-V LVTTL	4 mA		0		0		0		0	ps
	8 mA		–548		–576		–576		–576	ps
	12 mA		–1,259		–1,322		–1,322		–1,322	ps
	16 mA		–1,334		–1,401		–1,401		–1,401	ps
	24 mA		-1,895		–1,990		–1,990		–1,990	ps
2.5-V LVTTL	2 mA		622		653		653		653	ps
	8 mA		–1,061		–1,115		–1,115		–1,115	ps
	12 mA		–1,391		–1,461		–1,461		–1,461	ps
	16 mA		–1,701		–1,787		–1,787		–1,787	ps
1.8-V LVTTL	2 mA		–591		–621		–621		–621	ps
	8 mA		–935		–982		–982		–982	ps
	12 mA		–935		–982		–982		–982	ps
1.5-V LVTTL	2 mA		4,785		5,024		5,024		5,024	ps
	4 mA		1,380		1,449		1,449		1,449	ps
	8 mA		–306		–322		–322		–322	ps
GTL			–1,879		–1,973		–1,973		–1,973	ps
GTL+			–1,886		–1,981		–1,981		–1.981	ps
3.3-V PCI			–1,845		–1,938		–1,938		–1,938	ps
3.3-V PCI-X 1.0			–1,845		–1,938		–1,938		–1,938	ps
Compact PCI			–1,845		–1,938		–1,938		–1,938	ps
AGP 1×			–1,845		–1,938		–1,938		–1,938	ps
AGP 2×			0		0		0		0	ps
CTT			–922		–969		–969		–969	ps
SSTL-3 class I			–1,176		–1,235		–1,235		–1,235	ps

Table 4–105. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Column Pins (Part 2 of 2) *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
SSTL-3 class II		–1,749		–1,837		–1,837		–1,837	ps
SSTL-2 class I		–1,217		–1,278		–1,278		–1,278	ps
SSTL-2 class II		–1,672		–1,756		–1,756		–1,756	ps
SSTL-18 class I		–863		–907		–907		–907	ps
SSTL-18 class II		–1,448		–1,521		–1,521		–1,521	ps
1.5-V HSTL class I		–1,235		–1,297		–1,297		–1,297	ps
1.5-V HSTL class II		–1,358		–1,426		–1,426		–1,426	ps
1.8-V HSTL class I		–200		–210		–210		–210	ps
1.8-V HSTL class II		–189		–199		–199		–199	ps

Table 4–106. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 1 of 2) Note (1)

Parameter		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		0		0		0		0	ps
	4 mA		–772		–811		–811		–811	ps
	8 mA		–1,422		–1,494		–1,494		–1,494	ps
	12 mA		–1,518		–1,594		–1,594		–1,594	ps
3.3-V LVTTL	4 mA		0		0		0		0	ps
	8 mA		–480		–504		–504		–504	ps
	12 mA		–997		–1,047		–1,047		–1,047	ps
	16 mA		–1,104		–1,160		–1,160		–1,160	ps
	24 mA		–1,518		–1,594		–1,594		–1,594	ps
2.5-V LVTTL	2 mA		514		539		539		539	ps
	8 mA		–819		–860		–860		–860	ps
	12 mA		–1,144		–1,202		–1,202		–1,202	ps
	16 mA		–1,353		–1,421		–1,421		–1,421	ps
1.8-V LVTTL	2 mA		2,196		2,305		2,305		2,305	ps
	8 mA		–463		–487		–487		–487	ps
	12 mA		–688		–723		–723		–723	ps
1.5-V LVTTL	2 mA		3,942		4,139		4,139		4,139	ps
	4 mA		1,172		1,230		1,230		1,230	ps
	8 mA		–120		–126		–126		–126	ps
GTL			0		0		0		0	ps
GTL+			–1,512		–1,588		–1,588		–1,588	ps
3.3-V PCI			0		0		0		0	ps
3.3-V PCI-X 1.0			0		0		0		0	ps
Compact PCI			0		0		0		0	ps
AGP 1×			0		0		0		0	ps
AGP 2×			0		0		0		0	ps
CTT			–673		–707		–707		–707	ps
SSTL-3 class I			–880		–924		–924		–924	ps
SSTL-3 class II			–1,374		–1,443		–1,443		–1,443	ps
SSTL-2 class I			–914		–960		–960		–960	ps
SSTL-2 class II			–1,307		–1,373		–1,373		–1,373	ps
SSTL-18 class I			–563		–592		–592		–592	ps

Table 4–106. Stratix I/O Standard Output Delay Adders for Fast Slew Rate on Row Pins (Part 2 of 2) *Note (1)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
SSTL-18 class II		0		0		0		0	ps
1.5-V HSTL class I		–785		–825		–825		–825	ps
1.5-V HSTL class II		0		0		0		0	ps
1.8-V HSTL class I		–200		–210		–210		–210	ps
1.8-V HSTL class II		–189		–199		–199		–199	ps
LVDS *(1)*		–1,714		–1,800		–1,800		–1,800	ps
LVPECL *(1)*		–1,666		–1,750		–1,750		–1,750	ps
PCML *(1)*		–1,665		–1,749		–1,749		–1,749	ps
HyperTransport technology *(1)*		–1,611		–1,692		–1,692		–1,692	ps

Note to Table 4–103 through 4–106:

(1) These parameters are only available on row I/O pins.

Table 4–107. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 1 of 2) *Notes (1), (2)*

Parameter		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,534		1,610		1,610		1,610	ps
	4 mA		396		415		415		415	ps
	8 mA		–55		–58		–58		–58	ps
	12 mA		–287		–302		–302		—302	ps
	24 mA		–896		–941		–941		–941	ps
3.3-V LVTTL	4 mA		1,534		1,610		1,610		1,610	ps
	8 mA		1,298		1,362		1,362		1,362	ps
	12 mA		398		417		417		417	ps
	16 mA		342		359		359		359	ps
	24 mA		–288		–303		–303		–303	ps
2.5-V LVTTL	2 mA		2,637		2,768		2,768		2,768	ps
	8 mA		1,208		1,268		1,268		1,268	ps
	12 mA		649		681		681		681	ps
	16 mA		715		750		750		750	ps
1.8-V LVTTL	2 mA		6,813		7,153		7,153		7,153	ps
	8 mA		3,332		3,498		3,498		3,498	ps
	12 mA		2,821		2,962		2,962		2,962	ps
1.5-V LVTTL	2 mA		10,653		11,185		11,185		11,185	ps
	4 mA		7,143		7,500		7,500		7,500	ps
	8 mA		5,702		5,987		5,987		5,987	ps
GTL			–1,247		–1,310		–1,310		–1,310	ps
GTL+			–726		–763		–763		–763	ps
3.3-V PCI			372		390		390		390	ps
3.3-V PCI-X 1.0			372		390		390		390	ps
Compact PCI			372		390		390		390	ps
AGP 1×			372		390		390		390	ps
AGP 2×			0		0		0		0	ps
CTT			343		360		360		360	ps
SSTL-3 class I			13		13		13		13	ps
SSTL-3 class II			–647		–680		–680		–680	ps
SSTL-2 class I			235		246		246		246	ps
SSTL-2 class II			–337		–354		–354		–354	ps

Table 4–107. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Column Pins (Part 2 of 2) *Notes (1), (2)*

Parameter	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
SSTL-18 class I		2,027		2,128		2,128		2,128	ps
SSTL-18 class II		435		456		456		456	ps
1.5-V HSTL class I		1,399		1,468		1,468		1,468	ps
1.5-V HSTL class II		807		847		847		847	ps
1.8-V HSTL class I		1,399		1,468		1,468		1,468	ps
1.8-V HSTL class II		807		847		847		847	ps

Table 4–108. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 1 of 2) *Notes (1), (2)*

I/O Standard		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
LVCMOS	2 mA		1,582		1,661		1,661		1,661	ps
	4 mA		605		635		635		635	ps
	8 mA		219		229		229		229	ps
	12 mA		11		11		11		11	ps
3.3-V LVTTL	4 mA		1,582		1,661		1,661		1,661	ps
	8 mA		1,404		1,474		1,474		1,474	ps
	12 mA		607		637		637		637	ps
	16 mA		573		601		601		601	ps
2.5-V LVTTL	2 mA		2,573		2,701		2,701		2,701	ps
	8 mA		1,354		1,421		1,421		1,421	ps
	12 mA		875		918		918		918	ps
	16 mA		956		1,003		1,003		1,003	ps
1.8-V LVTTL	2 mA		6,317		6,632		6,632		6,632	ps
	8 mA		3,380		3,549		3,549		3,549	ps
	12 mA		2,943		3,090		3,090		3,090	ps
1.5-V LVTTL	2 mA		9,770		10,258		10,258		10,258	ps
	4 mA		6,841		7,183		7,183		7,183	ps
	8 mA		5,710		5,995		5,995		5,995	ps
GTL			0		0		0		0	ps
GTL+			–322		–339		–339		–339	ps
3.3-V PCI			0		0		0		0	ps
3.3-V PCI-X 1.0			0		0		0		0	ps
Compact PCI			0		0		0		0	ps
AGP 1×			0		0		0		0	ps
AGP 2×			0		0		0		0	ps
CTT			602		632		632		632	ps
SSTL-3 class I			278		291		291		291	ps
SSTL-3 class II			–335		–352		–352		–352	ps
SSTL-2 class I			492		516		516		516	ps
SSTL-2 class II			–47		–50		–50		–50	ps
SSTL-18 class I			2,218		2,328		2,328		2,328	ps
SSTL-18 class II			0		0		0		0	ps

Table 4–108. Stratix I/O Standard Output Delay Adders for Slow Slew Rate on Row Pins (Part 2 of 2) Notes (1), (2)

I/O Standard	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
1.5-V HSTL class I		1,977		2,075		2,075‘		2,075	ps
1.5-V HSTL class II		0		0		0		0	ps
1.8-V HSTL class I		1,977		2,075		2,075		2,075	ps
1.8-V HSTL class II		0		0		0		0	ps
LVDS *(1)*		–1,714		–1,800		–1,800		–1,800	ps
LVPECL *(1)*		–1,666		–1,750		–1,750		–1,750	ps
3.3-V PCML *(1)*		–1,665		–1,749		–1,749		–1,749	ps
HyperTransport technology *(1)*		–1,611		–1,692		–1,692		–1,692	ps

Notes to Tables 4–103 through 4–108:

(1) These parameters are only available on row I/O pins.

(2) Tables 4–105 to 4–108 contain preliminary timing information.

Tables 4–109 and 4–110 show the adder delays for the column and row IOE programmable delays. These delays are controlled with the Quartus II software logic options listed in the Parameter column.

Table 4–109. Stratix IOE Programmable Delays on Column Pins (Part 1 of 2) Note (1)

Parameter	Setting	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off		3,970		4,367		5,022		5,908	ps
	Small		3,390		3,729		4,288		5,045	ps
	Medium		2,810		3,091		3,554		4,181	ps
	Large		224		235		270		318	ps
	On		224		235		270		318	ps
Decrease input delay to input register	Off		3,900		4,290		4,933		5,804	ps
	On		0		0		0		0	ps
Decrease input delay to output register	Off		1,240		1,364		1,568		1,845	ps
	On		0		0		0		0	ps
Increase delay to output pin	Off		0		0		0		0	ps
	On		397		417		417		417	ps

Table 4–109. Stratix IOE Programmable Delays on Column Pins (Part 2 of 2) Note (1)

Parameter	Setting	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Increase delay to output enable pin	Off		0		0		0		0	ps
	On		338		372		427		503	ps
Increase output clock enable delay	Off		0		0		0		0	ps
	Small		540		594		683		804	ps
	Large		1,016		1,118		1,285		1,512	ps
	On		1,016		1,118		1,285		1,512	ps
Increase input clock enable delay	Off		0		0		0		0	ps
	Small		540		594		683		804	ps
	Large		1,016		1,118		1,285		1,512	ps
	On		1,016		1,118		1,285		1,512	ps
Increase output enable clock enable delay	Off		0		0		0		0	ps
	Small		540		594		683		804	ps
	Large		1,016		1,118		1,285		1,512	ps
	On		1,016		1,118		1,285		1,512	ps
Increase t_{ZX} delay to output pin	Off		0		0		0		0	ps
	On		2,199		2,309		2,309		2,309	ps

Table 4–110. Stratix IOE Programmable Delays on Row Pins (Part 1 of 2) Note (1)

Parameter	Setting	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Decrease input delay to internal cells	Off		3,970		4,367		5,022		5,908	ps
	Small		3,390		3,729		4,288		5,045	ps
	Medium		2,810		3,091		3,554		4,181	ps
	Large		173		181		208		245	ps
	On		173		181		208		245	ps
Decrease input delay to input register	Off		3,900		4,290		4,933		5,804	ps
	On		0		0		0		0	ps
Decrease input delay to output register	Off		1,240		1,364		1,568		1,845	ps
	On		0		0		0		0	ps
Increase delay to output pin	Off		0		0		0		0	ps
	On		397		417		417		417	ps

Table 4–110. Stratix IOE Programmable Delays on Row Pins (Part 2 of 2) Note (1)

Parameter	Setting	-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Increase delay to output enable pin	Off		0		0		0		0	ps
	On		348		383		441		518	ps
Increase output clock enable delay	Off		0		0		0		0	ps
	Small		180		198		227		267	ps
	Large		260		286		328		386	ps
	On		260		286		328		386	ps
Increase input clock enable delay	Off		0		0		0		0	ps
	Small		180		198		227		267	ps
	Large		260		286		328		386	ps
	On		260		286		328		386	ps
Increase output enable clock enable delay	Off		0		0		0		0	ps
	Small		540		594		683		804	ps
	Large		1,016		1,118		1,285		1,512	ps
	On		1,016		1,118		1,285		1,512	ps
Increase t_{ZX} delay to output pin	Off		0		0		0		0	ps
	On		1,993		2,092		2,092		2,092	ps

Note to Table 4–109 and Table 4–110:

(1) The delay chain delays vary for different device densities. These timing values only apply to EP1S30 and EP1S40 devices. Reference the timing information reported by Quartus II software for other devices.

The scaling factors for column output pin timing in Tables 4–111 to 4–113 are shown in units of time per pF unit of capacitance (ps/pF). Add this delay to the t_{CO} or combinatorial timing path for output or bidirectional pins in addition to the I/O adder delays shown in Tables 4–103 through 4–108 and the IOE programmable delays in Tables 4–109 and 4–110.

Table 4–111. Output Delay Adder for Loading on LVTTL/LVCMOS Output Buffers

Conditions		Output Pin Adder Delay (ps/pF)				
Parameter	**Value**	**3.3-V LVTTL**	**2.5-V LVTTL**	**1.8-V LVTTL**	**1.5-V LVTTL**	**LVCMOS**
Drive Strength	24mA	15	–	–	-	8
	16mA	25	18	–	–	–
	12mA	30	25	25	–	15
	8mA	50	35	40	35	20
	4mA	60	–	–	80	30
	2mA	–	75	120	160	60

Note to Table 4–111:

(1) The timing information in this tables is preliminary.

Table 4–112. Output Delay Adder for Loading on SSTL/HSTL Output Buffers

Conditions	Output Pin Adder Delay (ps/pF)			
	SSTL-3	**SSTL-2**	**SSTL-1.8**	**1.5-V HSTL**
Class I	25	25	25	25
Class II	25	20	25	20

Note to Table 4–112:

(1) The timing information in this tables is preliminary.

Table 4–113. Output Delay Adder for Loading on GTL+/GTL/CTT/PCI Output Buffers

Conditions		Output Pin Adder Delay (ps/pF)				
Parameter	**Value**	**GTL+**	**GTL**	**CTT**	**PCI**	**AGP**
VCCIO Voltage Level	3.3V	18	18	25	20	20
	2.5V	15	18	-	-	-

Note to Table 4–113:

The timing information in this tables is preliminary.

Maximum Input & Output Clock Rates

Tables 4–114 through 4–119 show the maximum input clock rate for column and row pins in Stratix devices.

Table 4–114. Stratix Maximum Input Clock Rate for CLK[7..4] & CLK[15..12] Pins in Flip-Chip Packages

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	422	390	390	MHz
2.5 V	422	422	390	390	MHz
1.8 V	422	422	390	390	MHz
1.5 V	422	422	390	390	MHz
LVCMOS	422	422	390	390	MHz
GTL	300	250	200	200	MHz
GTL+	300	250	200	200	MHz
SSTL-3 class I	400	350	300	300	MHz
SSTL-3 class II	400	350	300	300	MHz
SSTL-2 class I	400	350	300	300	MHz
SSTL-2 class II	400	350	300	300	MHz
SSTL-18 class I	400	350	300	300	MHz
SSTL-18 class II	400	350	300	300	MHz
1.5-V HSTL class I	400	350	300	300	MHz
1.5-V HSTL class II	400	350	300	300	MHz
1.8-V HSTL class I	400	350	300	300	MHz
1.8-V HSTL class II	400	350	300	300	MHz
3.3-V PCI	422	422	390	390	MHz
3.3-V PCI-X 1.0	422	422	390	390	MHz
Compact PCI	422	422	390	390	MHz
AGP 1×	422	422	390	390	MHz
AGP 2×	422	422	390	390	MHz
CTT	300	250	200	200	MHz
Differential HSTL	400	350	300	300	MHz
LVPECL *(1)*	645	645	622	622	MHz
PCML *(1)*	300	275	275	275	MHz
LVDS *(1)*	645	645	622	622	MHz
HyperTransport technology *(1)*	500	500	450	450	MHz

Table 4–115. Stratix Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins & FPLL[10..7]CLK Pins in Flip-Chip Packages

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	422	390	390	MHz
2.5 V	422	422	390	390	MHz
1.8 V	422	422	390	390	MHz
1.5 V	422	422	390	390	MHz
LVCMOS	422	422	390	390	MHz
GTL	300	250	200	200	MHz
GTL+	300	250	200	200	MHz
SSTL-3 class I	400	350	300	300	MHz
SSTL-3 class II	400	350	300	300	MHz
SSTL-2 class I	400	350	300	300	MHz
SSTL-2 class II	400	350	300	300	MHz
SSTL-18 class I	400	350	300	300	MHz
SSTL-18 class II	400	350	300	300	MHz
1.5-V HSTL class I	400	350	300	300	MHz
1.5-V HSTL class II	400	350	300	300	MHz
1.8-V HSTL class I	400	350	300	300	MHz
1.8-V HSTL class II	400	350	300	300	MHz
3.3-V PCI	422	422	390	390	MHz
3.3-V PCI-X 1.0	422	422	390	390	MHz
Compact PCI	422	422	390	390	MHz
AGP 1×	422	422	390	390	MHz
AGP 2×	422	422	390	390	MHz
CTT	300	250	200	200	MHz
Differential HSTL	400	350	300	300	MHz
LVPECL *(1)*	717	717	640	640	MHz
PCML *(1)*	400	375	350	350	MHz
LVDS *(1)*	717	717	640	640	MHz
HyperTransport technology *(1)*	717	717	640	640	MHz

Table 4–116. Stratix Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins in Flip-Chip Packages

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	422	390	390	MHz
2.5 V	422	422	390	390	MHz
1.8 V	422	422	390	390	MHz
1.5 V	422	422	390	390	MHz
LVCMOS	422	422	390	390	MHz
GTL	300	250	200	200	MHz
GTL+	300	250	200	200	MHz
SSTL-3 class I	400	350	300	300	MHz
SSTL-3 class II	400	350	300	300	MHz
SSTL-2 class I	400	350	300	300	MHz
SSTL-2 class II	400	350	300	300	MHz
SSTL-18 class I	400	350	300	300	MHz
SSTL-18 class II	400	350	300	300	MHz
1.5-V HSTL class I	400	350	300	300	MHz
1.5-V HSTL class II	400	350	300	300	MHz
1.8-V HSTL class I	400	350	300	300	MHz
1.8-V HSTL class II	400	350	300	300	MHz
3.3-V PCI	422	422	390	390	MHz
3.3-V PCI-X 1.0	422	422	390	390	MHz
Compact PCI	422	422	390	390	MHz
AGP 1×	422	422	390	390	MHz
AGP 2×	422	422	390	390	MHz
CTT	300	250	200	200	MHz
Differential HSTL	400	350	300	300	MHz
LVPECL *(1)*	645	645	640	640	MHz
PCML *(1)*	300	275	275	275	MHz
LVDS *(1)*	645	645	640	640	MHz
HyperTransport technology *(1)*	500	500	450	450	MHz

Table 4–117. Stratix Maximum Input Clock Rate for CLK[7..4] & CLK[15..12] Pins in Wire-Bond Packages

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	390	390	MHz
2.5 V	422	390	390	MHz
1.8 V	422	390	390	MHz
1.5 V	422	390	390	MHz
LVCMOS	422	390	390	MHz
GTL	250	200	200	MHz
GTL+	250	200	200	MHz
SSTL-3 class I	300	250	250	MHz
SSTL-3 class II	300	250	250	MHz
SSTL-2 class I	300	250	250	MHz
SSTL-2 class II	300	250	250	MHz
SSTL-18 class I	300	250	250	MHz
SSTL-18 class II	300	250	250	MHz
1.5-V HSTL class I	300	180	180	MHz
1.5-V HSTL class II	300	180	180	MHz
1.8-V HSTL class I	300	180	180	MHz
1.8-V HSTL class II	300	180	180	MHz
3.3-V PCI	422	390	390	MHz
3.3-V PCI-X 1.0	422	390	390	MHz
Compact PCI	422	390	390	MHz
AGP 1×	422	390	390	MHz
AGP 2×	422	390	390	MHz
CTT	250	180	180	MHz
Differential HSTL	300	180	180	MHz
LVPECL *(1)*	422	400	400	MHz
PCML *(1)*	215	200	200	MHz
LVDS *(1)*	422	400	400	MHz
HyperTransport technology *(1)*	422	400	400	MHz

Table 4–118. Stratix Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins & FPLL[10..7]CLK Pins in Wire-Bond Packages

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	390	390	MHz
2.5 V	422	390	390	MHz
1.8 V	422	390	390	MHz
1.5 V	422	390	390	MHz
LVCMOS	422	390	390	MHz
GTL	250	200	200	MHz
GTL+	250	200	200	MHz
SSTL-3 class I	350	300	300	MHz
SSTL-3 class II	350	300	300	MHz
SSTL-2 class I	350	300	300	MHz
SSTL-2 class II	350	300	300	MHz
SSTL-18 class I	350	300	300	MHz
SSTL-18 class II	350	300	300	MHz
1.5-V HSTL class I	350	300	300	MHz
1.5-V HSTL class II	350	300	300	MHz
1.8-V HSTL class I	350	300	300	MHz
1.8-V HSTL class II	350	300	300	MHz
3.3-V PCI	422	390	390	MHz
3.3-V PCI-X 1.0	422	390	390	MHz
Compact PCI	422	390	390	MHz
AGP 1×	422	390	390	MHz
AGP 2×	422	390	390	MHz
CTT	250	200	200	MHz
Differential HSTL	350	300	300	MHz
LVPECL *(1)*	717	640	640	MHz
PCML *(1)*	375	350	350	MHz
LVDS *(1)*	717	640	640	MHz
HyperTransport technology *(1)*	717	640	640	MHz

Table 4–119. Stratix Maximum Input Clock Rate for CLK[1, 3, 8, 10] Pins in Wire-Bond Packages

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	422	390	390	MHz
2.5 V	422	390	390	MHz
1.8 V	422	390	390	MHz
1.5 V	422	390	390	MHz
LVCMOS	422	390	390	MHz
GTL	250	200	200	MHz
GTL+	250	200	200	MHz
SSTL-3 class I	350	300	300	MHz
SSTL-3 class II	350	300	300	MHz
SSTL-2 class I	350	300	300	MHz
SSTL-2 class II	350	300	300	MHz
SSTL-18 class I	350	300	300	MHz
SSTL-18 class II	350	300	300	MHz
1.5-V HSTL class I	350	300	300	MHz
1.5-V HSTL class II	350	300	300	MHz
1.8-V HSTL class I	350	300	300	MHz
1.8-V HSTL class II	350	300	300	MHz
3.3-V PCI	422	390	390	MHz
3.3-V PCI-X 1.0	422	390	390	MHz
Compact PCI	422	390	390	MHz
AGP 1×	422	390	390	MHz
AGP 2×	422	390	390	MHz
CTT	250	200	200	MHz
Differential HSTL	350	300	300	MHz
LVPECL *(1)*	645	622	622	MHz
PCML *(1)*	275	275	275	MHz
LVDS *(1)*	645	622	622	MHz
HyperTransport technology *(1)*	500	450	450	MHz

Note to Tables 4–114 through 4–119:

(1) These parameters are only available on row I/O pins.

Tables 4–120 through 4–123 show the maximum output clock rate for column and row pins in Stratix devices.

Table 4–120. Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins in Flip-Chip Packages (Part 1 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	350	300	250	250	MHz
2.5 V	350	300	300	300	MHz
1.8 V	250	250	250	250	MHz
1.5 V	225	200	200	200	MHz
LVCMOS	350	300	250	250	MHz
GTL	200	167	125	125	MHz
GTL+	200	167	125	125	MHz
SSTL-3 class I	200	167	167	133	MHz
SSTL-3 class II	200	167	167	133	MHz
SSTL-2 class I *(3)*	200	200	167	167	MHz
SSTL-2 class I *(4)*	200	200	167	167	MHz
SSTL-2 class I *(5)*	150	134	134	134	MHz
SSTL-2 class II *(3)*	200	200	167	167	MHz
SSTL-2 class II *(4)*	200	200	167	167	MHz
SSTL-2 class II *(5)*	150	134	134	134	MHz
SSTL-18 class I	150	133	133	133	MHz
SSTL-18 class II	150	133	133	133	MHz
1.5-V HSTL class I	250	225	200	200	MHz
1.5-V HSTL class II	225	200	200	200	MHz
1.8-V HSTL class I	250	225	200	200	MHz
1.8-V HSTL class II	225	200	200	200	MHz
3.3-V PCI	350	300	250	250	MHz
3.3-V PCI-X 1.0	350	300	250	250	MHz
Compact PCI	350	300	250	250	MHz
AGP 1×	350	300	250	250	MHz
AGP 2×	350	300	250	250	MHz
CTT	200	200	200	200	MHz
Differential HSTL	225	200	200	200	MHz
Differential SSTL-2 *(6)*	200	200	167	167	MHz
LVPECL *(2)*	500	500	500	500	MHz

Table 4–120. Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins in Flip-Chip Packages (Part 2 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
PCML *(2)*	350	350	350	350	MHz
LVDS *(2)*	500	500	500	500	MHz
HyperTransport technology *(2)*	350	350	350	350	MHz

Table 4–121. Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins in Flip-Chip Packages (Part 1 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	400	350	300	300	MHz
2.5 V	400	350	300	300	MHz
1.8 V	400	350	300	300	MHz
1.5 V	350	300	300	300	MHz
LVCMOS	400	350	300	300	MHz
GTL	200	167	125	125	MHz
GTL+	200	167	125	125	MHz
SSTL-3 class I	167	150	133	133	MHz
SSTL-3 class II	167	150	133	133	MHz
SSTL-2 class I	150	133	133	133	MHz
SSTL-2 class II	150	133	133	133	MHz
SSTL-18 class I	150	133	133	133	MHz
SSTL-18 class II	150	133	133	133	MHz
1.5-V HSTL class I	250	225	200	200	MHz
1.5-V HSTL class II	225	225	200	200	MHz
1.8-V HSTL class I	250	225	200	200	MHz
1.8-V HSTL class II	225	225	200	200	MHz
3.3-V PCI	250	225	200	200	MHz
3.3-V PCI-X 1.0	225	225	200	200	MHz
Compact PCI	400	350	300	300	MHz
AGP 1×	400	350	300	300	MHz
AGP 2×	400	350	300	300	MHz
CTT	300	250	200	200	MHz
Differential HSTL	225	225	200	200	MHz

Table 4–121. Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins in Flip-Chip Packages (Part 2 of 2)

I/O Standard	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVPECL *(2)*	717	717	500	500	MHz
PCML *(2)*	420	420	420	420	MHz
LVDS *(2)*	717	717	500	500	MHz
HyperTransport technology *(2)*	420	420	420	420	MHz

Table 4–122. Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins in Wire-Bond Packages (Part 1 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	175	150	150	MHz
2.5 V	175	150	150	MHz
1.8 V	175	150	150	MHz
1.5 V	175	150	150	MHz
LVCMOS	175	150	150	MHz
GTL	125	100	100	MHz
GTL+	125	100	100	MHz
SSTL-3 class I	110	90	90	MHz
SSTL-3 class II	133	125	125	MHz
SSTL-2 class I	166	133	133	MHz
SSTL-2 class II	133	100	100	MHz
SSTL-18 class I	110	100	100	MHz
SSTL-18 class II	110	100	100	MHz
1.5-V HSTL class I	167	167	167	MHz
1.5-V HSTL class II	167	133	133	MHz
1.8-V HSTL class I	167	167	167	MHz
1.8-V HSTL class II	167	133	133	MHz
3.3-V PCI	167	167	167	MHz
3.3-V PCI-X 1.0	167	133	133	MHz
Compact PCI	175	150	150	MHz
AGP 1×	175	150	150	MHz
AGP 2×	175	150	150	MHz
CTT	125	100	100	MHz

Table 4–122. Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins in Wire-Bond Packages (Part 2 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
Differential HSTL	167	133	133	MHz
Differential SSTL-2 *(1)*	110	100	100	MHz
LVPECL *(2)*	311	275	275	MHz
PCML *(2)*	250	200	200	MHz
LVDS *(2)*	311	275	275	MHz
HyperTransport technology *(2)*	311	275	275	MHz

Table 4–123. Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins in Wire-Bond Packages (Part 1 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
LVTTL	200	175	175	MHz
2.5 V	200	175	175	MHz
1.8 V	200	175	175	MHz
1.5 V	200	175	175	MHz
LVCMOS	200	175	175	MHz
GTL	125	100	100	MHz
GTL+	125	100	100	MHz
SSTL-3 class I	110	90	90	MHz
SSTL-3 class II	150	133	133	MHz
SSTL-2 class I	90	80	80	MHz
SSTL-2 class II	110	100	100	MHz
SSTL-18 class I	110	100	100	MHz
SSTL-18 class II	110	100	100	MHz
1.5-V HSTL class I	225	200	200	MHz
1.5-V HSTL class II	200	167	167	MHz
1.8-V HSTL class I	225	200	200	MHz
1.8-V HSTL class II	200	167	167	MHz
3.3-V PCI	200	175	175	MHz
3.3-V PCI-X 1.0	200	175	175	MHz
Compact PCI	200	175	175	MHz
AGP 1×	200	175	175	MHz

Table 4–123. Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins in Wire-Bond Packages (Part 2 of 2)

I/O Standard	-6 Speed Grade	-7 Speed Grade	-8 Speed Grade	Unit
AGP 2×	200	175	175	MHz
CTT	125	100	100	MHz
Differential HSTL	200	167	167	MHz
LVPECL *(2)*	311	270	270	MHz
PCML *(2)*	400	311	311	MHz
LVDS *(2)*	400	311	311	MHz
HyperTransport technology *(2)*	420	400	400	MHz

Notes to Tables 4–120 through 4–123:

(1) Differential SSTL-2 outputs are only available on column clock pins.

(2) These parameters are only available on row I/O pins.

(3) SSTL-2 in maximum drive strength condition. See Table 4–101 on page 4–61 for more information on exact loading conditions for each I/O standard.

(4) SSTL-2 in minimum drive strength with ≤ 10pF output load condition.

(5) SSTL-2 in minimum drive strength with > 10pF output load condition.

(6) Differential SSTL-2 outputs are only supported on column clock pins.

High-Speed I/O Specification

Table 4–124 provides high-speed timing specifications definitions.

Table 4–124. High-Speed Timing Specifications & Terminology

High-Speed Timing Specification	Terminology
t_C	High-speed receiver/transmitter input and output clock period.
f_{HSCLK}	High-speed receiver/transmitter input and output clock frequency.
t_{RISE}	Low-to-high transmission time.
t_{FALL}	High-to-low transmission time.
Timing unit interval (TUI)	The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency × Multiplication Factor) = t_C/w).
f_{HSDR}	Maximum LVDS data transfer rate (f_{HSDR} = 1/TUI).
Channel-to-channel skew (TCCS)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window (SW)	The period of time during which the data must be valid to be captured correctly. The setup and hold times determine the ideal strobe position within the sampling window. SW = t_{SW} (max) – t_{SW} (min).
Input jitter (peak-to-peak)	Peak-to-peak input jitter on high-speed PLLs.
Output jitter (peak-to-peak)	Peak-to-peak output jitter on high-speed PLLs.
t_{DUTY}	Duty cycle on high-speed transmitter output clock.
t_{LOCK}	Lock time for high-speed transmitter and receiver PLLs.

Tables 4–125 and 4–126 show the high-speed I/O timing for Stratix devices.

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 1 of 4) Notes (1), (2)

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (Clock frequency) (LVDS, LVPECL, HyperTransport technology) $f_{HSCLK} = f_{HSDR} / W$	*W* = 4 to 30 (Serdes used)	10		210	10		210	10		156	10		115.5	MHz
	W = 2 (Serdes bypass)	50		231	50		231	50		231	50		231	MHz
	W = 2 (Serdes used)	150		420	150		420	150		312	150		231	MHz
	W = 1 (Serdes bypass)	100		462	100		462	100		462	100		462	MHz
	W = 1 (Serdes used)	300		717	300		717	300		624	300		462	MHz
f_{HSDR} Device operation (LVDS, LVPECL, HyperTransport technology)	*J* = 10	300		840	300		840	300		624	300		462	Mbps
	J = 8	300		840	300		840	300		624	300		462	Mbps
	J = 7	300		840	300		840	300		624	300		462	Mbps
	J = 4	300		840	300		840	300		624	300		462	Mbps
	J = 2	100		462	100		462	100		462	100		462	Mbps
	J = 1 (LVDS and LVPECL only)	100		462	100		462	100		462	100		462	Mbps

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 2 of 4) *Notes (1), (2)*

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (Clock frequency) (PCML) $f_{HSCLK} = f_{HSDR}$ / W	*W* = 4 to 30 (Serdes used)	10		100	10		100	10		77.75	10		77.75	MHz
	W = 2 (Serdes bypass)	50		200	50		200	50		150	50		150	MHz
	W = 2 (Serdes used)	150		200	150		200	150		155.5	150		155.5	MHz
	W = 1 (Serdes bypass)	100		250	100		250	100		200	100		200	MHz
	W = 1 (Serdes used)	300		400	300		400	300		311	300		311	MHz
f_{HSDR} Device operation (PCML)	*J* = 10	300		400	300		400	300		311	300		311	Mbps
	J = 8	300		400	300		400	300		311	300		311	Mbps
	J = 7	300		400	300		400	300		311	300		311	Mbps
	J = 4	300		400	300		400	300		311	300		311	Mbps
	J = 2	100		400	100		400	100		300	100		300	Mbps
	J = 1	100		250	100		250	100		200	100		200	Mbps
TCCS	All			200			200			300			300	ps

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 3 of 4) *Notes (1), (2)*

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SW	PCML (*J* = 4, 7, 8, 10)	750			750			800			800			ps
	PCML (*J* = 2)	900			900			1,200			1,200			ps
	PCML (*J* = 1)	1,500			1,500			1,700			1,700			ps
	LVDS and LVPECL (*J* = 1)	500			500			550			550			ps
	LVDS, LVPECL, HyperTransport technology (*J* = 2 through 10)	440			440			500			500			ps
Input jitter tolerance (peak-to-peak)	All			250			250			250			250	ps
Output jitter (peak-to-peak)	All			160			160			200			200	ps
Output t_{RISE}	LVDS	80	110	120	80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology	110	170	200	110	170	200	120	170	200	120	170	200	ps
	LVPECL	90	130	150	90	130	150	100	135	150	100	135	150	ps
	PCML	80	110	135	80	110	135	80	110	135	80	110	135	ps
Output t_{FALL}	LVDS	80	110	120	80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology	110	170	200	110	170	200	110	170	200	110	170	200	ps
	LVPECL	90	130	160	90	130	160	100	135	160	100	135	160	ps
	PCML	105	140	175	105	140	175	110	145	175	110	145	175	ps

Table 4–125. High-Speed I/O Specifications for Flip-Chip Packages (Part 4 of 4) *Notes (1), (2)*

Symbol	Conditions	-5 Speed Grade			-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{DUTY}	LVDS (J = 2 through 10)	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	%
	LVDS (J =1) and LVPECL, PCML, HyperTransport technology	45	50	55	45	50	55	45	50	55	45	50	55	%
t_{LOCK}	All			100			100			100			100	µs

Notes to Table 4–125:

(1) When J = 4, 7, 8, and 10, the SERDES block is used.

(2) When J = 2 or J = 1, the SERDES is bypassed.

Table 4–126. High-Speed I/O Specifications for Wire-Bond Packages (Part 1 of 2)

Symbol	Conditions	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (Clock frequency) (LVDS,LVPECL, HyperTransport technology) $f_{HSCLK} = f_{HSDR}$ / W	*W* = 4 to 30 (Serdes used)	10		156	10		115.5	10		115.5	MHz
	W = 2 (Serdes bypass)	50		231	50		231	50		231	MHz
	W = 2 (Serdes used)	150		312	150		231	150		231	MHz
	W = 1 (Serdes bypass)	100		311	100		270	100		270	MHz
	W = 1 (Serdes used)	300		624	300		462	300		462	MHz
f_{HSDR} Device operation, (LVDS,LVPECL, HyperTransport technology)	J = 10	300		624	300		462	300		462	Mbps
	J = 8	300		624	300		462	300		462	Mbps
	J = 7	300		624	300		462	300		462	Mbps
	J = 4	300		624	300		462	300		462	Mbps
	J = 2	100		462	100		462	100		462	Mbps
	J = 1 (LVDS and LVPECL only)	100		311	100		270	100		270	Mbps
f_{HSCLK} (Clock frequency) (PCML) $f_{HSCLK} = f_{HSDR}$ / W	*W* = 4 to 30 (Serdes used)	10		77.75							MHz
	W = 2 (Serdes bypass)	50		150	50		77.5	50		77.5	MHz
	W = 2 (Serdes used)	150		155.5							MHz
	W = 1 (Serdes bypass)	100		200	100		155	100		155	MHz
	W = 1 (Serdes used)	300		311							MHz
Device operation, f_{HSDR} (PCML)	J = 10	300		311							Mbps
	J = 8	300		311							Mbps
	J = 7	300		311							Mbps
	J = 4	300		311							Mbps
	J = 2	100		300	100		155	100		155	Mbps
	J = 1	100		200	100		155	100		155	Mbps
TCCS	All			400			400			400	ps

Table 4–126. High-Speed I/O Specifications for Wire-Bond Packages (Part 2 of 2)

Symbol	Conditions	-6 Speed Grade			-7 Speed Grade			-8 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SW	PCML (J = 4, 7, 8, 10) only	800			800			800			ps
	PCML (J = 2) only	1,200			1,200			1,200			ps
	PCML (J = 1) only	1,700			1,700			1,700			ps
	LVDS and LVPECL (J = 1) only	550			550			550			ps
	LVDS, LVPECL, HyperTransport technology (J = 2 through 10) only	500			500			500			ps
Input jitter tolerance (peak-to-peak)	All			250			250			250	ps
Output jitter (peak-to-peak)	All			200			200			200	ps
Output t_{RISE}	LVDS	80	110	120	80	110	120	80	110	120	ps
	HyperTransport technology	120	170	200	120	170	200	120	170	200	ps
	LVPECL	100	135	150	100	135	150	100	135	150	ps
	PCML	80	110	135	80	110	135	80	110	135	ps
Output t_{FALL}	LVDS	80	110	120	80	110	120	80	110	120	ps
	HyperTransport	110	170	200	110	170	200	110	170	200	ps
	LVPECL	100	135	160	100	135	160	100	135	160	ps
	PCML	110	145	175	110	145	175	110	145	175	ps
t_{DUTY}	LVDS (J = 2 through10) only	47.5	50	52.5	47.5	50	52.5	47.5	50	52.5	%
	LVDS (J =1) and LVPECL, PCML, HyperTransport technology	45	50	55	45	50	55	45	50	55	%
t_{LOCK}	All			100			100			100	µs

PLL Specifications

Tables 4–127 through 4–129 describe the Stratix device enhanced PLL specifications.

Table 4–127. Enhanced PLL Specifications for -5 Speed Grades (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	3 *(1)*		684	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40		60	%
$t_{INJITTER}$	Input clock period jitter			±200 *(2)*	ps
$t_{EINJITTER}$	External feedback clock period jitter			±200 *(2)*	ps
t_{FCOMP}	External feedback clock compensation time *(3)*			6	ns
f_{OUT}	Output frequency for internal global or regional clock	0.3		500	MHz
f_{OUT_EXT}	Output frequency for external clock *(2)*	0.3		526	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45		55	%
t_{JITTER}	Period jitter for external clock output *(5)*			±100 ps for >200 MHz `outclk` ±20 mUI for <200 MHz `outclk`	ps or mUI
$t_{CONFIG5,6}$	Time required to reconfigure the scan chains for PLLs 5 and 6			$289/f_{SCANCLK}$	
$t_{CONFIG11,12}$	Time required to reconfigure the scan chains for PLLs 11 and 12			$193/f_{SCANCLK}$	
$t_{SCANCLK}$	`scanclk` frequency *(4)*			22	MHz
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(6)*			100	µs
t_{LOCK}	Time required to lock from end of device configuration	10		400	µs
f_{VCO}	PLL internal VCO operating range	300		800 *(7)*	MHz
t_{LSKEW}	Clock skew between two external clock outputs driven by the same counter		±50		ps
t_{SKEW}	Clock skew between two external clock outputs driven by the different counters with the same settings		±75		ps
f_{SS}	Spread spectrum modulation frequency	30		150	kHz

Table 4–127. Enhanced PLL Specifications for -5 Speed Grades (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
% spread	Percentage spread for spread spectrum frequency *(9)*	0.4	0.5	0.6	%
t_{ARESET}	Minimum pulse width on `areset` signal	10			ns

Table 4–128. Enhanced PLL Specifications for -6 Speed Grades (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	3 *(1)*		650	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40		60	%
$t_{INJITTER}$	Input clock period jitter			±200 *(2)*	ps
$t_{EINJITTER}$	External feedback clock period jitter			±200 *(2)*	ps
t_{FCOMP}	External feedback clock compensation time *(3)*			6	ns
f_{OUT}	Output frequency for internal global or regional clock	0.3		450	MHz
f_{OUT_EXT}	Output frequency for external clock *(2)*	0.3		500	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45		55	%
t_{JITTER}	Period jitter for external clock output *(5)*			±100 ps for >200 MHz `outclk` ±20 mUI for <200 MHz `outclk`	ps or mUI
$t_{CONFIG5,6}$	Time required to reconfigure the scan chains for PLLs 5 and 6			$289/f_{SCANCLK}$	
$t_{CONFIG11,12}$	Time required to reconfigure the scan chains for PLLs 11 and 12			$193/f_{SCANCLK}$	
$t_{SCANCLK}$	`scanclk` frequency *(4)*			22	MHz
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(6)* *(10)*	*(8)*		100	μs
t_{LOCK}	Time required to lock from end of device configuration *(10)*	10		400	μs
f_{VCO}	PLL internal VCO operating range	300		800 *(7)*	MHz
t_{LSKEW}	Clock skew between two external clock outputs driven by the same counter		±50		ps

Table 4–128. Enhanced PLL Specifications for -6 Speed Grades (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{SKEW}	Clock skew between two external clock outputs driven by the different counters with the same settings		±75		ps
f_{SS}	Spread spectrum modulation frequency	30		150	kHz
% spread	Percentage spread for spread spectrum frequency *(9)*	0.4	0.5	0.6	%
t_{ARESET}	Minimum pulse width on `areset` signal	10			ns

Table 4–129. Enhanced PLL Specifications for -7 & -8 Speed Grade (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	3 *(1)*		565	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40		60	%
$t_{INJITTER}$	Input clock period jitter			±200 *(2)*	ps
$t_{EINJITTER}$	External feedback clock period jitter			±200 *(2)*	ps
t_{FCOMP}	External feedback clock compensation time *(3)*			6	ns
f_{OUT}	Output frequency for internal global or regional clock	0.3		420	MHz
f_{OUT_EXT}	Output frequency for external clock *(2)*	0.3		434	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45		55	%
t_{JITTER}	Period jitter for external clock output *(5)*			±100 ps for >200 MHz `outclk` ±20 mUI for <200 MHz `outclk`	ps or mUI
$t_{CONFIG5,6}$	Time required to reconfigure the scan chains for PLLs 5 and 6			$289/f_{SCANCLK}$	
$t_{CONFIG11,12}$	Time required to reconfigure the scan chains for PLLs 11 and 12			$193/f_{SCANCLK}$	
$t_{SCANCLK}$	`scanclk` frequency *(4)*			22	MHz
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(6)* *(10)*	*(8)*		100	µs
t_{LOCK}	Time required to lock from end of device configuration *(10)*	10		400	µs
f_{VCO}	PLL internal VCO operating range	300		600 *(7)*	MHz

Table 4–129. Enhanced PLL Specifications for -7 & -8 Speed Grade (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{LSKEW}	Clock skew between two external clock outputs driven by the same counter		±50		ps
t_{SKEW}	Clock skew between two external clock outputs driven by the different counters with the same settings		±75		ps
f_{SS}	Spread spectrum modulation frequency	30		150	kHz
% spread	Percentage spread for spread spectrum frequency *(9)*	0.5		0.6	%
t_{ARESET}	Minimum pulse width on `areset` signal	10			ns

Notes to Tables 4–127 through 4–129:

(1) The minimum input clock frequency to the PFD (f_{IN}/N) must be at least 3 MHz for Stratix device enhanced PLLs.

(2) See "Maximum Input & Output Clock Rates" on page 4–78.

(3) t_{FCOMP} can also equal 50% of the input clock period multiplied by the pre-scale divider *n* (whichever is less).

(4) This parameter is timing analyzed by the Quartus II software because the `scanclk` and `scandata` ports can be driven by the logic array.

(5) Actual jitter performance may vary based on the system configuration.

(6) Total required time to reconfigure and lock is equal to $t_{DLOCK} + t_{CONFIG}$. If only post-scale counters and delays are changed, then t_{DLOCK} is equal to 0.

(7) The VCO range is limited to 500 to 800 MHz when the spread spectrum feature is selected.

(8) Lock time is a function of PLL configuration and may be significantly faster depending on bandwidth settings or feedback counter change increment.

(9) Exact, user-controllable value depends on the PLL settings.

(10) The LOCK circuit on Stratix PLLs does not work for industrial devices below -20C unless the PFD frequency > 200 MHz. See the *Stratix FPGA Errata Sheet* for more information on the PLL.

Tables 4–130 and 4–131 describe the Stratix device fast PLL specifications.

Table 4–130. Fast PLL Specifications for -5 & -6 Speed Grade Devices

Symbol	Parameter	Min	Max	Unit
f_{IN}	`CLKIN` frequency (for *m* = 1) *(1)*, *(2)*	300	717	MHz
	`CLKIN` frequency (for *m* = 2 to 19)	300/*m*	1,000/*m*	MHz
	`CLKIN` frequency (for *m* = 20 to 32)	10	1,000/*m*	MHz
f_{OUT}	Output frequency for internal global or regional clock *(3)*	9.4	420	MHz
f_{OUT_EXT}	Output frequency for external clock *(2)*	9.375	717	MHz
f_{VCO}	VCO operating frequency	300	1,000	MHz
t_{INDUTY}	`CLKIN` duty cycle	40	60	%
$t_{INJITTER}$	Period jitter for `CLKIN` pin		±200	ps
t_{DUTY}	Duty cycle for `DFFIO` 1× `CLKOUT` pin *(4)*	45	55	%
t_{JITTER}	Period jitter for DIFFIO clock out *(4)*		±80	ps
	Period jitter for internal global or regional clock		±100 ps for >200-MHz `outclk` ±20 mUI for <200-MHz `outclk`	ps or mUI
t_{LOCK}	Time required for PLL to acquire lock	10	100	µs
m	Multiplication factors for *m* counter *(4)*	1	32	Integer
*l*0, *l*1, *g*0	Multiplication factors for *l*0, *l*1, and *g*0 counter *(5)*, *(6)*	1	32	Integer
t_{ARESET}	Minimum pulse width on `areset` signal	10		ns

Table 4–131. Fast PLL Specifications for -7 & -8 Speed Grades (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
f_{IN}	`CLKIN` frequency (for *m* = 1) *(1)*,	300	640	MHz
	`CLKIN` frequency (for *m* = 2 to 19)	300/*m*	700/*m*	MHz
	`CLKIN` frequency (for *m* = 20 to 32)	10	700/*m*	MHz
f_{OUT}	Output frequency for internal global or regional clock *(3)*	9.375	420	MHz
f_{OUT_EXT}	Output frequency for external clock	9.4	500	MHz
f_{VCO}	VCO operating frequency	300	700	MHz
t_{INDUTY}	`CLKIN` duty cycle	40	60	%

Table 4–131. Fast PLL Specifications for -7 & -8 Speed Grades (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
$t_{INJITTER}$	Period jitter for `CLKIN` pin		±200	ps
t_{DUTY}	Duty cycle for `DFFIO` 1× `CLKOUT` pin *(4)*	45	55	%
t_{JITTER}	Period jitter for DIFFIO clock out *(4)*		±80	ps
	Period jitter for internal global or regional clock		±100 ps for >200 MHz `outclk` ±20 mUI for <200 MHz `outclk`	ps or mUI
t_{LOCK}	Time required for PLL to acquire lock	10	100	µs
m	Multiplication factors for *m* counter *(5)*	1	32	Integer
*l*0, *l*1, *g*0	Multiplication factors for *l*0, *l*1, and *g*0 counter *(5)*, *(6)*	1	32	Integer
t_{ARESET}	Minimum pulse width on `areset` signal	10		ns

Notes to Tables 4–130 and 4–131:

(1) See "Maximum Input & Output Clock Rates" on page 4–78.

(2) PLLs 7, 8, 9, and 10 in the EP1S80 device support up to 717-MHz input and output.

(3) When using the SERDES, high-speed differential I/O mode supports a maximum output frequency of 210 MHz to the global or regional clocks (i.e., the maximum data rate 840 Mbps divided by the smallest SERDES J factor of 4).

(4) This parameter is for high-speed differential I/O mode only.

(5) These counters have a maximum of 32 if programmed for 50/50 duty cycle. Otherwise, they have a maximum of 16.

(6) High-speed differential I/O mode supports *W* = 1 to 16 and *J* = 4, 7, 8, or 10.

DLL Jitter

Table 4–132 reports the jitter for the DLL in the DQS phase shift reference circuit.

Table 4–132. DLL Jitter for DQS Phase Shift Reference Circuit

Frequency (MHz)	DLL Jitter (ps)
197 to 200	± 100
160 to 196	± 300
100 to 159	± 500

For more information on DLL jitter, see the *DDR SRAM* section in the *Stratix Architecture* chapter in the *Stratix Device Handbook, Volume 1*.

Chapter 5. Reference & Ordering Information

S51005-2.1

Software

Stratix® devices are supported by the Altera® Quartus® II design software, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration. See the *Design Software Selector Guide* for more details on the Quartus II software features.

The Quartus II software supports the Windows XP/2000/NT/98, Sun Solaris, Linux Red Hat v7.1 and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

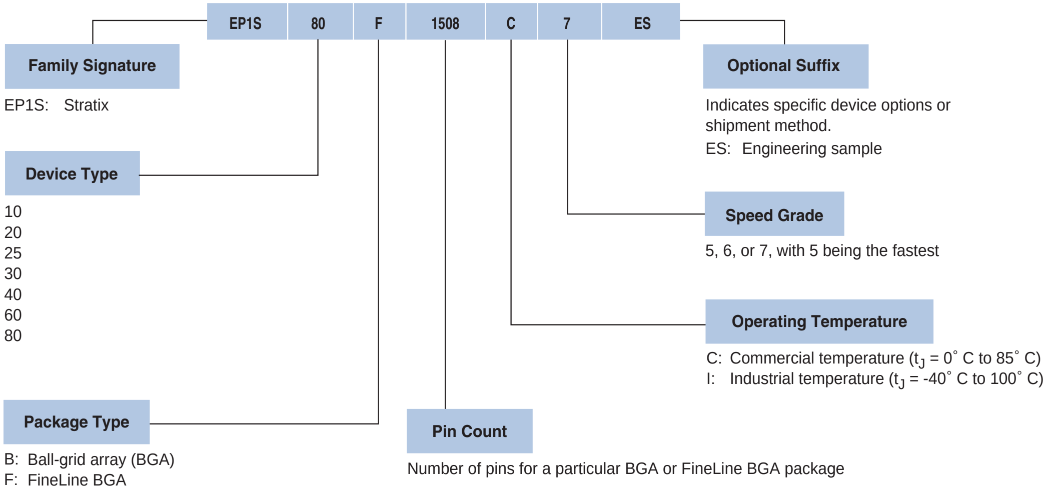
Device Pin-Outs

Stratix device pin-outs can be found on the Altera web site **(www.altera.com).**

Ordering Information

Figure 5–1 describes the ordering codes for Stratix devices. For more information on a specific package, see the *Package Information for Stratix Devices* chapter.

Figure 5–1. Stratix Device Packaging Ordering Information



Family Signature

EP1S: Stratix

Device Type

10
20
25
30
40
60
80

Package Type

B: Ball-grid array (BGA)
F: FineLine BGA

Pin Count

Number of pins for a particular BGA or FineLine BGA package

Operating Temperature

C: Commercial temperature (t_J = 0° C to 85° C)
I: Industrial temperature (t_J = -40° C to 100° C)

Speed Grade

5, 6, or 7, with 5 being the fastest

Optional Suffix

Indicates specific device options or shipment method.

ES: Engineering sample