Features

- High-performance 24-macrocell EPLD
  - Combinatorial speeds with t_{PD} = 30 ns
  - Counter frequencies up to 33 MHz
  - Pipelined data rates up to 41 MHz
- Pin-, function-, and JEDEC-File-compatible with Altera's EP910A and EP910T EPLDs
- 100% generically testable to provide 100% programming yield
- Available in windowed ceramic and one-time-programmable (OTP) plastic chip carrier packages
  - 44-pin J-lead chip carrier (JLCC and PLCC)
  - 40-pin dual in-line package (CerDIP and PDIP)
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flip-flops, or for combinatorial operation
- Extensive third-party software and programming support
- MAX+PLUS II and A+PLUS software support includes schematic capture, Boolean equation, state machine, and netlist design entry methods; Altera Hardware Description Language (AHDL), waveform entry, and an EDIF 2 0 0 interface are available with MAX+PLUS II.

General Description

Altera's EP910 Erasable Programmable Logic Device (EPLD) can implement up to 900 equivalent gates of SSI and MSI logic. It is available in windowed ceramic or OTP plastic 40-pin DIP and 44-pin J-lead chip carrier packages. See Figure 7.

Figure 7. EP910 Package Pin-Out Diagrams

Package outlines not drawn to scale.