HDMI 1.4 Splitter
EP9142

User Guide
V0.1

Revised: Apr. 26, 2011

Original Release Date: May. 12, 2010

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Explore

Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	May/12/2010	Jerry Chen	Initial Version
0.1	Apr/26/2011	Ether Lai	Revise Pin Sequence; Add detailed Package Outline Information; Revise Control Register Descriptions;

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Section 1 Introduction

1.1 Overview

EP9142 is a 2-Port DVI/HDMI splitter with integrated HDCP decryption/encryption engines and is compliant with HDMI Rev 1.4 and HDCP Rev 1.3 specifications. EP9142 receives DVI/HDMI inputs, process HDCP decryption and encryption and transmits the data to 2 DVI/HDMI ports.

1.2 Features

- DVI Specification 1.0 Compliant
- HDMI Specification 1.4a Compliant
- Integrated HDCP decryption/encryption engines which are compliant with HDCP Rev 1.3 specification
- Wide Frequency Range: 25MHz - 340MHz
- Supports 12-bit Deep Full HD, Full 3D and 4K2K video.
- Supports Standard Audio, DSD Audio and HD (HBR) Audio
- Supports 1 DVI/HDMI input port and 2 DVI/HDMI output ports
- Supports conversion of HDMI signaling to DVI signaling
- Supports HDCP Repeater
- Cascadable to make more than 4 output ports
- 64-Pin TQFP (Pb-Free; E-PAD)

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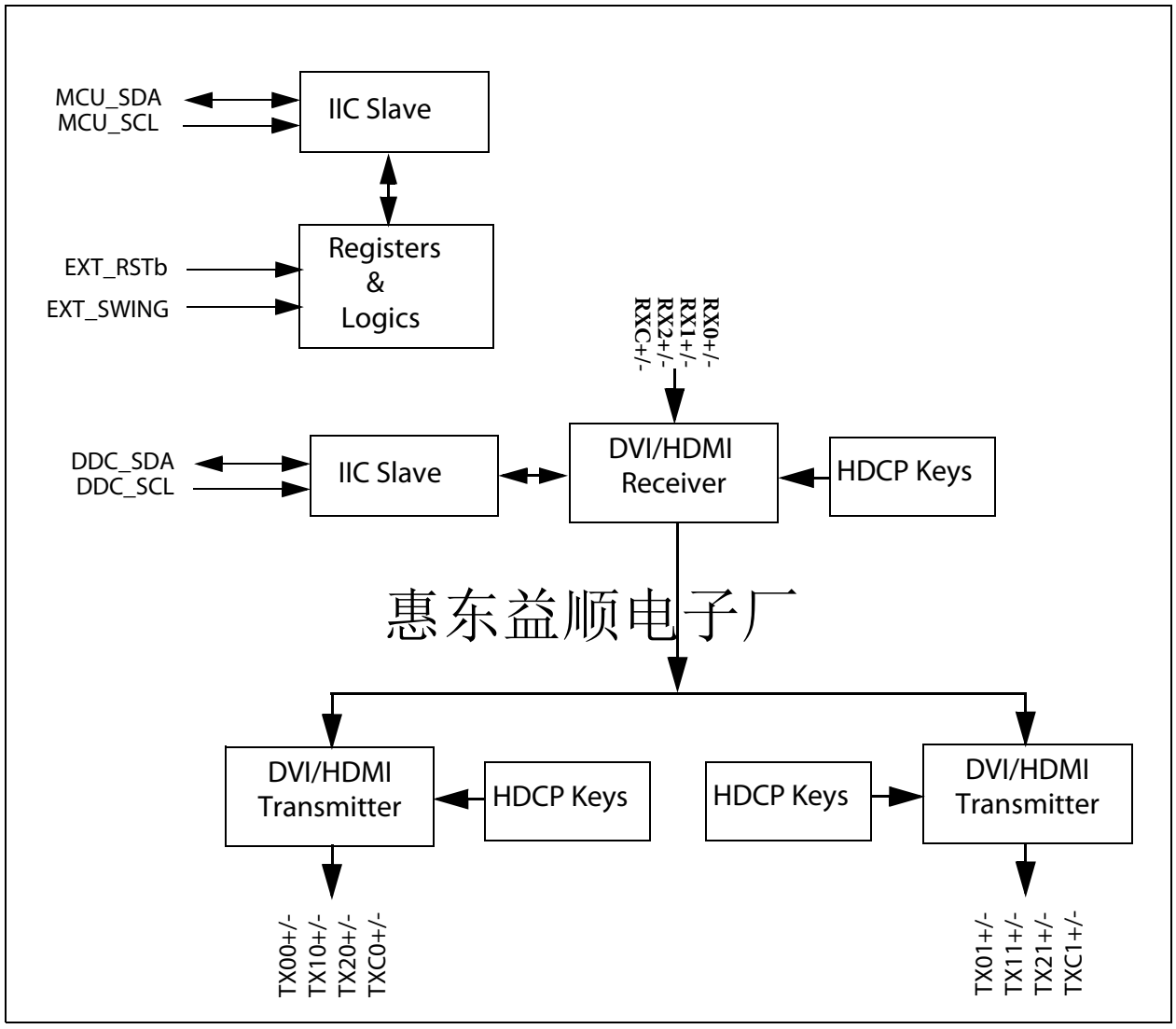
Section 2 Overview

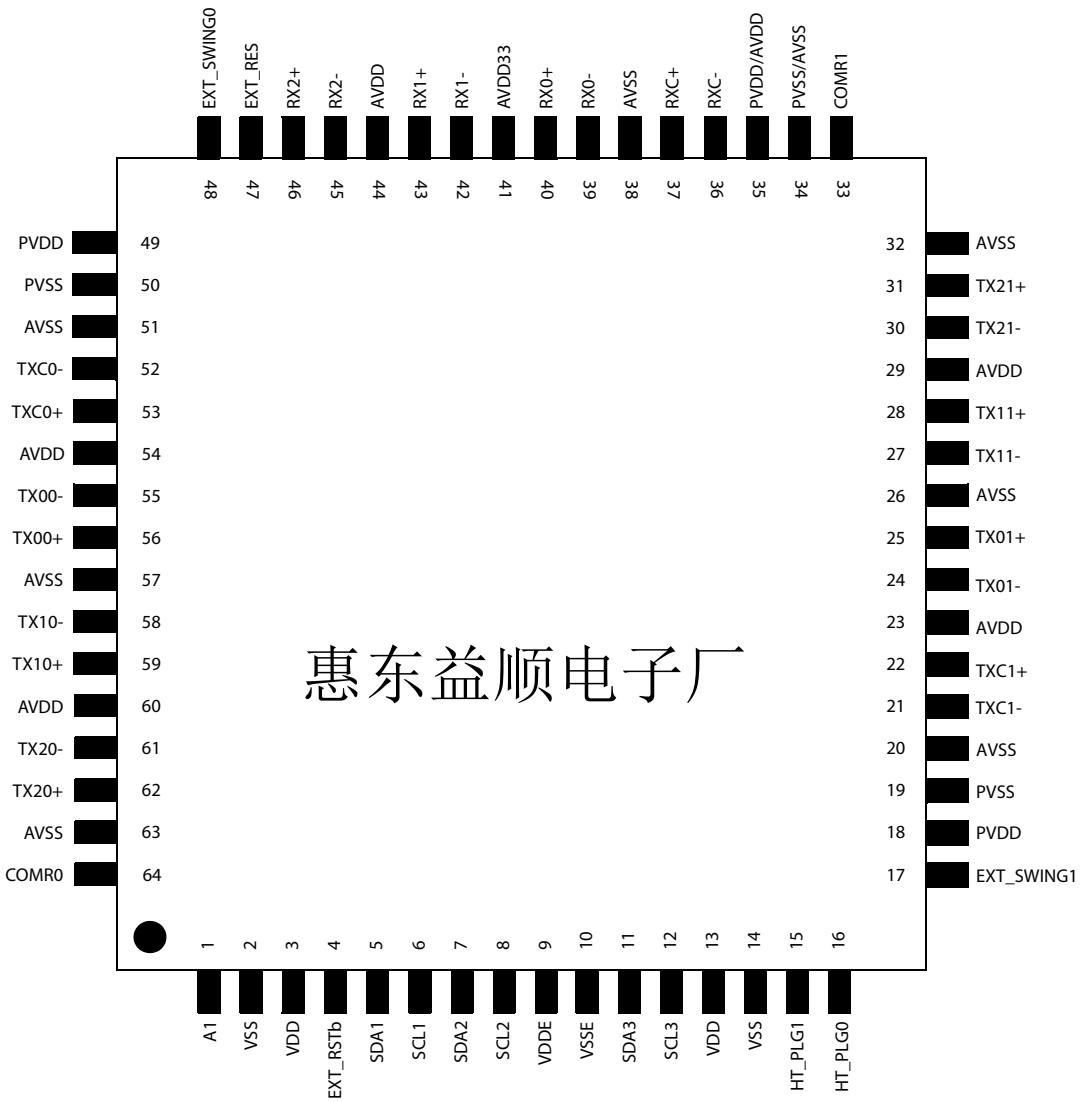
2.1 Block Diagram

Figure 2-1 Block Diagram



2.2 Pin Diagram

Figure 2-2 Pin Diagram



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 IIC Pins

NAME	IN / OUT	DESCRIPTION
DDC_SCL	IN	IIC SCL signal for receiver port DDC
DDC_SDA	IO	IIC SDA signal for receiver port DDC (open drain)
EE_SCL	OUT	SCL input for EE IIC port. Connect this pin to 4.7K pull up resistor. (open drain)
EE_SDA	IO	SDA in/out for EE. Connect this pin to 4.7K pull up resistor. (open drain)
EE_WPT	IN	WPT (write protect) input for EE. Connect this pin to 3.3V to prevent HDCP key loss.
MCU_SCL	IN	IIC SCL signal for internal registers access
MCU_SDA	IO	IIC SDA signal for internal registers access (open drain)
A1, A0	IN	Determine the lowest 2-bit of the IIC address for MCU IIC port

Table 2-2 Misc. Pins

NAME	IN / OUT	DESCRIPTION
EXT_RSTb	IN	External Reset (Active LOW). A HIGH level indicates normal operation and a LOW level causes all the logic on the chip to be reset.
V_OUT	OUT	Polarity corrected vertical sync pulse (active high) derived from receiver input

Table 2-3 Receiver Pins

NAME	IN / OUT	DESCRIPTION
RX0- RX0+ RX1- RX1+ RX2- RX2+	Analog	Differential Data Input Pairs for receiver port
RXC- RXC+		Differential Clock Input Pairs for receiver port
EXT_RES	Analog	DVI/HDMI External Termination Resistor

Table 2-4 Transmitter Pins

NAME	IN / OUT	DESCRIPTION
TX00- TX00+ TX10- TX10+ TX20- TX20+	Analog	Differential Data Output Pairs for transmitter port 0
TXC0- TXC0+		Differential Clock Output Pairs for transmitter port 0

Table 2-4 Transmitter Pins

NAME	IN / OUT	DESCRIPTION
HTPLG0	IN	Hot Plug Input This pin is used to monitor the "HOT PLUG" signal for transmitter port 0. Note: This input is only 3.3V tolerant and has no internal debouncing circuit.
EXT_SWING0	Analog	Voltage Swing Adjust for transmitter port 0. A resistor should tie this pin to AVDD18. This resistance determines the amplitude of the voltage swing. 270Ω is recommended.
COMR0	Analog	Common ground for pull-down resistors for transmitter port 0
TX01- TX01+ TX11- TX11+ TX21- TX21+	Analog	Differential Data Output Pairs for transmitter port 1
TXC1- TXC1+		Differential Clock Output Pairs for transmitter port 1
HTPLG1	IN	Hot Plug Input This pin is used to monitor the "HOT PLUG" signal for transmitter port 1. Note: This input is only 3.3V tolerant and has no internal debouncing circuit.
EXT_SWING1	Analog	Voltage Swing Adjust for transmitter port 1. A resistor should tie this pin to AVDD18. This resistance determines the amplitude of the voltage swing. 270Ω is recommended.
COMR1	Analog	Common ground for pull-down resistors for transmitter port 1

Table 2-5 Power and Ground Pins

NAME	IN / OUT	DESCRIPTION
VDDE	PWR	Digital Power, 3.3V
VSSE	GND	Digital Ground
VDD	PWR	Core Power, 1.8V
VSS	GND	Core Ground
AVDD	PWR	Analog Power, 1.8V
AVSS	GND	Analog Ground
PVDD	PWR	Analog Power for PLL, 1.8V
PVSS	GND	Analog Ground for PLL
AVDD33	PWR	HDMI Termination Power (3.3V)

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	-0.3		4.0	V
Vcc18	1.8V Supply Voltage	-0.3		2.5	V
V_I	Input Voltage	-0.3		V_{cc} + 0.3	V
V_O	Output Voltage	-0.3		V_{cc} + 0.3	V
T_A	Ambient Temperature (with power applied)	-25		105	℃
T_{STG}	Storage Temperature	-40		125	℃
P_{PD}	Package Power Dissipation			1	W

1 Permanent device damage may occur if absolute maximum conditions are exceeded.

2 Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	3.14	3.3	3.6	V
Vcc18	1.8V Supply Voltage	1.71	1.8	1.98	V
V_{CCN}	Supply Voltage Noise[1]	-0.3		100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	0	25	70	℃

1 Guaranteed by design.

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	uA

V_{ID}	Differential Input Voltage, Single Ended Amplitude		150		1000	mV

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Section 3 Detail Functional Descriptions

3.1 General

The chip provides an IIC (SCL3/SDA3) serial bus interface to communicate with the host. The IIC address for this slave IIC interface is “0111_0_A1_0_x” (where x=1 for read and x=0 for write). A1 is programmable by pin.

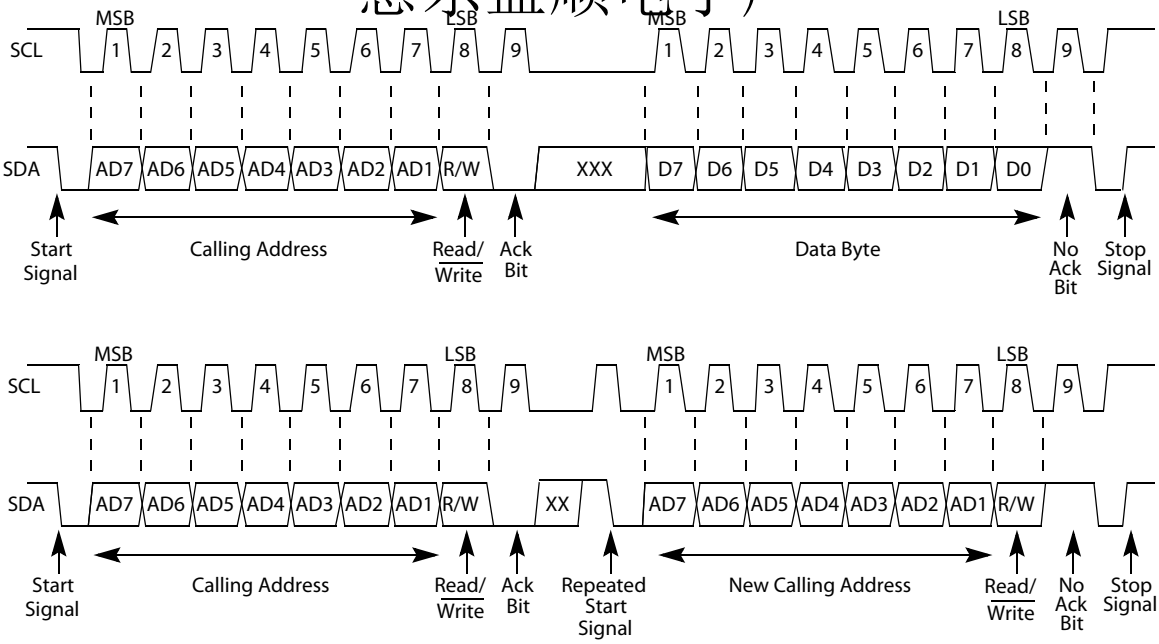
3.2 IIC Interface

The IIC bus interface uses a Serial Data line (SDA at pin SDA3) and a Serial Clock Line (SCL at pin SCL3) for data transfer. The chip acts as a slave for receiving and transmitting data over the serial interface. All devices connected to the IIC bus must have open drain or open collector outputs. Logic AND function is exercised on both lines with external pull-up resistors, the value of these resistors is system dependent. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable at the positive edge of SCL. If the SDA changes state while SCL is HIGH, the IIC interface interprets that action as a START or STOP sequence. Data on SDA must change only when SCL is LOW.

The standard IIC traffic protocol is illustrated in the following Figure:

Figure 3-1 IIC Bus Transmission Protocol



3.2.1 Basic Protocol

For EP9142, there are six components to serial bus operation:

- START Signal
- Slave Address Byte
- Base Register Address Byte
- Data Byte for Read/Write
- STOP Signal

When the serial interface is inactive (SCL and SDA are HIGH), communication are initiated by a START signal which is a HIGH-to-LOW transition on SDA while SCL is HIGH. The first eight bits of data transferred after a START signal comprising a seven bit slave address (the seven MSB bits) and a single R/W bit (the LSB bit). The R/W bit indicates the direction of data transfer, "1" means read from device and "0" means write to device. If the transmitted slave address matches the address of the device, the EP9142 sends the acknowledge by asserting SDA Low on the ninth SCL pulse. Else, the EP9142 does not assert the acknowledge.

Writing data to specific control registers of the chip requires that the 8-bits address of the control register is written after the slave address has been acknowledged. This control register address is the base address for the subsequent write operations. The base address auto-increments by one for each byte of data written after the data byte intended for the base address. The acknowledge bit will be sent on the ninth SCL pulse after every 8-bits data received.

Data are read from the control registers of the chip in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W bit of the slave address byte LOW to set up a sequential read operation.

Reading (the R/W bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the chip, a STOP signal must be sent. A STOP signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a START signal without first generating a STOP signal to terminate the current read/write sequence. This can be used to change the mode of communication (read, write) between the slave and master without releasing the bus.

3.2.2 Examples of the read/write sequence

Write to One Control Register

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte

- Data Byte to Base Address
- STOP Signal

Write to Multiple Control Registers

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- Data Byte to Base Address
- Data Byte to (Base Address + 1)
- Data Byte to (Base Address + 2)
- .....
- Data Byte to (Base Address + N)
- STOP Signal

Read from One Control Register

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- STOP Signal (Optional)
- START Signal
- Slave Address Byte (R/W = HIGH)
- Data Byte from Base Address
- STOP Signal

Read from Multiple Control Registers

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- STOP Signal (Optional)
- START Signal
- Slave Address Byte (R/W = HIGH)
- Data Byte from Base Address
- Data Byte from (Base Address + 1)
- Data Byte from (Base Address + 2)
- .....

- Data Byte from (Base Address + N)
- STOP Signal

3.3 Description of the Control Registers

The following table shows all the control registers of the DVI/HDMI Transmitter EP9142:

Table 3-1 IIC Control Registers

Addr	Mode	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	RESET
$07	R/W	RX_LINK_ON	RX_DE_ON	RX_HDMI	RX_ENC_ON	RX_PU	TX_test	TX_SEL[1:0]		02h
$08	R/W	TX_MUTE	RX_VSYNC	-	-	-	-	TX_ENC_OPT	TX_PU	01h
$09	R	-	-	-	-	-	TX_RSEN	TX_HTPLG	-	00h
$0A	R/W	RESERVED[3:0]				SOFT_RST	RX_RI_RST	-	-	80h
$0E	R/W	-	-	-	-	-	-	TX_EESS	TX_HDMI	01h
$0F	R/W	TX_AKSV_RDY	TX_ENC_ON	-	TX_RPTR	-	-	TX_RI_RDY	TX_ENC_EN	00h
$10	R/W	TX_BKSV_1								XXh
$11	R/W	TX_BKSV_2								XXh
$12	R/W	TX_BKSV_3								XXh
$13	R/W	TX_BKSV_4								XXh
$14	R/W	TX_BKSV_5								XXh
$15	R/W	TX_AN_1								XXh
$16	R/W	TX_AN_2								XXh
$17	R/W	TX_AN_3								XXh
$18	R/W	TX_AN_4								XXh
$19	R/W	TX_AN_5								XXh
$1A	R/W	TX_AN_6								XXh
$1B	R/W	TX_AN_7								XXh
$1C	R/W	TX_AN_8								XXh
$1D	R	TX_AKSV_1								XXh
$1E	R	TX_AKSV_2								XXh
$1F	R	TX_AKSV_3								XXh
$20	R	TX_AKSV_4								XXh
$21	R	TX_AKSV_5								XXh

$22	R	TX_RI_1							XXh
$23	R	TX_RI_2							XXh
$24	R/W	TX_IRATE							00h
$25	R	TX_M0_1							XXh
$26	R	TX_M0_2							XXh
$27	R	TX_M0_3							XXh
$28	R	TX_M0_4							XXh
$29	R	TX_M0_5							XXh
$2A	R	TX_M0_6							XXh
$2B	R	TX_M0_7							XXh
$2C	R	TX_M0_8							XXh
$40	R	-	-	-	-	-	-	-	RX_M0_READY	XXh
$41	R	RX_M0_1							XXh
$42	R	RX_M0_2							XXh
$43	R	RX_M0_3							XXh
$44	R	RX_M0_4							XXh
$45	R	RX_M0_5							XXh
$46	R	RX_M0_6							XXh
$47	R	RX_M0_7							XXh
$50	W	RX_BCAP							91h
$51	W	RX_BSTATUS[7:0]							00h
$52	W	-	-	-	-	RX_BSTATUS[11:8]			00h
$60	W	RX_SHA-1_HASH_0							XXh
$61	W	RX_SHA-1_HASH_1							XXh
$62	W	RX_SHA-1_HASH_2							XXh
$63	W	RX_SHA-1_HASH_3							XXh
$64	W	RX_SHA-1_HASH_4							XXh
$65	W	RX_SHA-1_HASH_5							XXh
$66	W	RX_SHA-1_HASH_6							XXh
$67	W	RX_SHA-1_HASH_7							XXh
$68	W	RX_SHA-1_HASH_8							XXh
$69	W	RX_SHA-1_HASH_9							XXh

$6A	W	RX_SHA-1_HASH_10							XXh
$6B	W	RX_SHA-1_HASH_11							XXh
$6C	W	RX_SHA-1_HASH_12							XXh
$6D	W	RX_SHA-1_HASH_13							XXh
$6E	W	RX_SHA-1_HASH_14							XXh
$6F	W	RX_SHA-1_HASH_15							XXh
$70	W	RX_SHA-1_HASH_16							XXh
$71	W	RX_SHA-1_HASH_17							XXh
$72	W	RX_SHA-1_HASH_18							XXh
$73	W	RX_SHA-1_HASH_19							XXh
$80 ~ $CF	W	RX_KSV_FIFO							XXh
$FB	R/W	0	0	EQ_SLICER[1:0]		0	0	0	EQ_GAIN	00h
$FC	R/W	VCO_GAIN2[0]	VCO_GAIN1[1:0]		VCO0_GAIN0[1:0]		LF2_DIS	LF1_DIS	LF0_DIS	00h
$FD	R/W	FLOCK_CTL1[2:0]			FLOCK_CTL0[3:0]				VCO_GAIN2[1]	00h
$FE	R/W	TX_TERM	0	DSWING[1:0]		0	0	0	0	00h
$FF	R/W	SCLK_DLY	TPHY_RST	RSEN_DIS	0	VCO_GAIN[1:0]		PHD_CUR[1:0]		00h

3.3.1 Register Descriptions

Detailed usage of these IIC registers is described in the following section.

3.3.1.1 Control Register 0

Table 3-2 Control Register 0

$07

	6	5	4	3	2	1	0
R	RX_LINK_ON	RX_DE_ON	RX_HDMI	RX_ENC_ON	RX_PU	RSVDL	RSVDL	TX_SEL
W	-	-	-	-				
	-	-	-	-	1	0	0	0

RX_LINK_ON — Receiver Link On

This bit indicates whether a valid signal appears at the clock input of the receiver port. This bit is valid even when the receiver is powered off.

1 = Clock presents at the input of the receiver port

0 = No clock is detected at the input of the receiver port

RX_DE_ON — Receiver DE On

This bit indicates whether DE signal is toggling at the receiver port. This bit is valid only when the receiver is powered on.

1 = DE signal is toggling at the receiver port
0 = DE signal is not toggling at the receiver port

RX_HDMI — Receiver HDMI signal

This bit indicates whether the receiver port is receiving DVI or HDMI signal

1 = HDMI
0 = DVI

RX_ENC_ON — Receiver Decryption On

This bit indicates whether the HDCP decryption is active at the receiver port.

1 = HDCP decryption at the receiver port is active
0 = HDCP decryption at the receiver port is not active

RSVDL -- This bit shall be set to LOW for Normal Operation!

RX_PU — Receiver Power Down Control Bit

This bit controls the power of the receiver port

1 = Normal operation.
0 = Power down Mode.

TX_SEL — Transmitter Port Select for IIC Access

The 2 transmitter ports share the same IIC register address. This register is used to select which transmitter port is addressed for IIC access.

0 = Port 0 is selected
1 = Port 1 is selected

3.3.1.2 Control Register 1

Table 3-3 Control Register 1

$08

	6	5	4	3	2	1	0
R W	TX_MUTE	RX_VSYNC -	-	-	-	-	TX_ENC_OPT	TX_PU
Reset:	0	-	-	0	-	-	0	1

TX_MUTE — Video Mute Transmitter

The bit is used to mute the video for the selected transmitter port.

1 = Selected transmitter port is video muted
0 = Normal

RX_VSYNC — Vertical Sync Status Bit

The VSYNC bit gives the current status of the vertical sync signal received by the receiver.

TX_ENC_OPT — Transmitter Encryption Option

1 = Not affected by RX encryption status.
0 = Force not to encrypt if RX is not encrypted.

TX_PU — Transmitter Power Down Control Bit

This bit controls the power of the selected transmitter port

1 = Normal operation.
0 = Put the selected transmitter port in power down mode.

3.3.1.3 Control Register 2

Table 3-4 Control Register 2

$09

	6	5	4	3	2	1	0
R	-	-	-	-	-	TX_RSEN	TX_HTPLG	-
W						-	-	
Reset:	-	-	-	-	-	-	-	-

TX_RSEN — Transmitter Analog Output Status Bit

The TX_RSEN bit indicates the analog output status at the selected transmitter port.

1 = The selected transmitter analog outputs are connected to the receiver
0 = The selected transmitter analog outputs are disconnected

TX_HTPLG — Transmitter Hot Plug Status Bit

The TX_HTPLG bit indicates the hot plug status at the selected transmitter port.

1 = Hot Plug detected at the selected transmitter port.
0 = Hot Plug not detected at the selected transmitter port.

3.3.1.4 Control Register 3

Table 3-5 Control Register 3

$0A

	6	5	4	3	2	1	0
R	DK[3:1]		DKEN	SOFT_RST	RX_RI_RST	-	-
W							
Reset:	1	0	0	0	0	0	-	-

DK[3:1] — De-skewing Setting Control Bits

The DK[3:1] setting the clock to data riming for de-skew purpose. Eight steps can be selected and the time difference for each step is 200 ps. The default is 0 step.

000 = -4 step with minimum setup time and maximum hold time.
001 = -3 step
010 = -2 step
011 = -1 step
100 = 0 step
101 = +1 step
110 = +2 step
111 = +3 step with maximum setup time and minimum hold time

DKEN — De-Skew (Clock to Data De-skewing) Enable Bit

1 = De-Skew Enabled
0 = De-Skew Disabled, 0 step is selected

SOFT_RST — Soft Reset

1 = Reset all logic except IIC register values
0 = Normal.

RX_RI_RST — Reset HDCP Ri value for the RX port

1 = Reset HDCP Ri value to 0 for the RX port.
0 = Normal.

3.3.1.5 Control Register 3

Table 3-6 Control Register 3

$0A

	6	5	4	3	2	1	0
R W	RESERVED[3:0]			SOFT_RST	RX_RI_RST	-	-
Reset:	1	0	0	0	0	0	-	-

RESERVED[3:0] — RESERVED Control Bits

Set the reserved registers to 0x80 as the default value.

SOFT_RST — Soft Reset

1 = Reset all logic except IIC register values
0 = Normal.

RX_RI_RST — Reset HDCP Ri value for the RX port

1 = Reset HDCP Ri value to 0 for the RX port.
0 = Normal.

3.3.1.6 Control Register 4

Table 3-7 Control Register 4

$0E

	6	5	4	3	2	1	0
R W	-	-	-	-	-	-	TX_EESS	TX_HDMI
Reset:	-	-	-	-	-	-	0	1

TX_EESS — Enable Enhanced Encryption Signalling for the selected transmitter port

1 = Using Enhanced Encryption Signalling for the selected transmitter port.

0 = Using Original Encryption Signalling for the selected transmitter port. This is only valid if the selected transmitter is working in DVI mode (TX_HDMI = 0).

TX_HDMI — Set HDMI mode for the selected transmitter port

1 = Put the selected transmitter port working in HDMI mode. This is valid only if the receiver is receiving HDMI signal.

0 = Put the selected transmitter port working in DVI mode.

3.3.1.7 Control Register 5

Table 3-8 Control Register 5

$0F

	6	5	4	3	2	1	0
R	TX_AKSV_RDY	TX_ENC_ON	-	TX_RPTR	-	TX_RI_RDY	TX_ENC_EN
W							
	-	-	-	0	-	-	-	0

TX_AKSV_RDY — Transmitter AKSV Ready

The TX_AKSV_RDY bit indicates whether the HDCP keys and AKSV has been successfully downloaded from external EE or not for the selected transmitter port. This bit is read only.

1 = HDCP keys and AKSV has been successfully downloaded from external EE. AKSV is ready for read.

0 = HDCP keys and AKSV downloading has not been completed. AKSV is not ready for read.

TX_ENC_ON — Transmitter HDCP Encryption On

The TX_ENC_ON bit indicates whether the HDCP encryption for the selected transmitter port is active or not. This bit is read only.

1 = HDCP encryption is active.

0 = HDCP encryption is not active.

TX_RPTR — Transmit to Repeater

The TX_RPTR bit should be set if the receiver side which is connected to the selected transmitter port is a repeater. It should be cleared otherwise.

1 = The selected transmitter port is connecting to a repeater.

0 = The selected transmitter port is not connecting to a repeater.

TX_RI_RDY — Transmitter RI Ready

This bit indicates that the first Ri value is available for the selected transmitter port. This bit is read only.

1 = First Ri value is available for the selected transmitter port.
0 = First Ri value is not available for the selected transmitter port.

TX_ENC_EN — Transmitter ENC Enable

1 = Enable HDCP encryption for the selected transmitter port.
0 = Disable HDCP encryption the selected transmitter port.

3.3.1.8 TX_BKSV Registers - TX_BKSV_1 ~ TX_BKSV_5

Table 3-9 TX_BKSV Registers

$10 ~ $14

bit	7	6	5	4	3	2	1	0
R W	TX_BKSV1[7:0] ~ TX_BKSV5[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 5 registers for the selected transmitter port should be programmed with receiver's Key Selection Vector. TX_BKSV_1 is the LSB and TX_BKSV_5 is the MSB. TX_BKSV_5 should be written last, as it triggers the authentication process.

3.3.1.9 TX_AN Registers - TX_AN_1 ~ TX_AN_8

Table 3-10 TX_AN Registers

$15 ~ $1C

bit	7	6	5	4	3	2	1	0
R W	TX_AN1[7:0] ~ TX_AN8[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 8 registers for the selected transmitter port should be programmed with a 64-bit pseudo-random value before triggering the authentication process. TX_AN_1 is the LSB and TX_AN_8 is the MSB.

3.3.1.10 TX_AKSV Registers - TX_AKSV_1 ~ TX_AKSV_5

Table 3-11 TX_AKSV Registers

$1D ~ $21

bit	7	6	5	4	3	2	1	0
R W	TX_AKSV1[7:0] ~ TX_AKSV5[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 5 registers are read only which hold transmitter's Key Selection Vector for the selected transmitter port. TX_AKSV_1 is the LSB and TX_AKSV_5 is the MSB. All five bytes should be read from here and then written to the receiver. Byte 5 should be written last to the receiver, as it will trigger authentication there. These 5 registers should not be read until TX_AKSV_RDY bit is 1.

3.3.1.11 TX_RI Registers - TX_RI_1 ~ TX_RI_2

Table 3-12 TX_RI Registers

$22 ~ $23

bit	7	6	5	4	3	2	1	0
R W	TX_RI_1[7:0] ~ TX_RI_2[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 2 registers hold transmitter's Ri value for the selected transmitter port. They should be read and compared against the Ri value of the receiver to ensure that the encryption process on the transmitter and receiver is synchronized.

3.3.1.12 TX_M0 Registers ($25 ~ $2C) - TX_M0_1 ~ TX_M0_8

Table 3-13 TX_M0 Registers

$25 ~ $2C

bit	7	6	5	4	3	2	1	0
R	TX_M0_1[7:0] ~ TX_M0_8[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 8 registers are read only which hold transmitter's M0 values which calculated from HDCP engine. These values will be used for SHA calculation.

3.3.1.13 RX_M0_RDY Register

Table 3-14 RX_M0_RDY Register

$40

bit	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	RX_M0_RDY
Reset:	0	0	0	0	0	0	0	0

The RX_M0_RDY bit will be set to 1 while the last byte of AKSV is written and the HDCP engine completes the M0 calculation.

3.3.1.14 RX_M0 Registers ($41 ~ $48) - RX_M0_1 ~ RX_M0_8

Table 3-15 RX_M0 Registers

$41 ~ $48

bit	7	6	5	4	3	2	1	0
R	RX_M0_1[7:0] ~ RX_M0_8[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 8 registers are read only which hold receiver's M0 values which calculated from HDCP engine. These values can be read while the RX_M0_RDY bit is 1 and can be used for SHA calculation.

3.3.1.15 RX_Bcaps Register

Table 3-16 RX_Bcaps Register

$50

bit	7	6	5	4	3	2	1	0
W	HDMI_CAP	REPEATER	FIFO_RDY	FAST	RSVD	RSVD	1.1_FEATURE	FAST_REAUTH
Reset:	1	0	0	1	0	0	0	1

This register is write only. The value writes to this register can be read by the upstream source through the DDC link while the HDCP is invoked.

HDMI_CAP — HDMI Reserved Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 7, HDMI_RESERVED bit. Use of this bit is reserved. HDCP receivers not capable of supporting HDMI must clear this bit to 0.

REPEATER — REPEATER Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 6, REPEATER bit.

FIFO_RDY — READY Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 5, READY bit.

FAST — FAST Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 4, FAST bit.

1.1_FEATURE — 1.1_FEATURE Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 1, 1.1_FEATURE bit. This bit shall set to 0 always.

FAST_REAUTH — FAST_REAUTHENTICATION Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 0, FAST_REAUTHENTICATION bit.

3.3.1.16 RX_Bstatus Registers ($51 ~ $52)

Table 3-17 RX_Bstatus (LSB, [7:0]) Register

$51

bit	7	6	5	4	3	2	1	0
W	DEV_EXCEED	DEVICE_CNT[6:0]						
Reset:	0	0	0	0	0	0	0	0

Table 3-18 RX_Bstatus (MSB, [15:8]) Register

$52

bit	7	6	5	4	3	2	1	0
W	-	-	-	-	CASC_EXCEED	DEPTH[2:0]		
Reset:	0	0	0	0	0	0	0	0

These 2 bytes registers are write only. The value writes to this register can be read by the upstream source through the DDC link while the HDCP is invoked.

DEV_EXCEED — MAX_DEVS_EXCEEDED Bit in HDCP Bstatus register

Value written into this bit will reflect to the HDCP Bstatus register, bit 7, MAX_DEVS_EXCEEDED bit.

DEVICE_COUNT[6:0] — DEVICE_COUNT Bits in HDCP Bstatus register

Value written into this bit will reflect to the HDCP Bstatus register, bit 6 ~ bit 0, DEVICE_COUNT[6:0] bit.

CASC_EXCEED — MAX_CASCADE_EXCEEDED Bit in HDCP Bstatus register

Value written into this bit will reflect to the HDCP Bstatus register, bit 11, MAX_CASCADE_EXCEEDED bit.

DEPTH[2:0] — DEPTH Bits in HDCP Bstatus register

Value written into this bit will reflect to the HDCP Bstatus register, bit 10 ~ bit 8, DEPTH[2:0] bit.

3.3.1.17 RX_SHA-1_HASH Registers ($60 ~ $73)

These 20-bytes registers are write only. The value writes to this register can be read by the upstream source through the DDC link while the HDCP is invoked.

Table 3-19 HDCP SHA-1 Hash Value Registers

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset
0x60	RX_SHA-1_HASH_0								xxh
0x61	RX_SHA-1_HASH_1								xxh
0x62	RX_SHA-1_HASH_2								xxh
0x63	RX_SHA-1_HASH_3								xxh
0x64	RX_SHA-1_HASH_4								xxh
0x65	RX_SHA-1_HASH_5								xxh
0x66	RX_SHA-1_HASH_6								xxh
0x67	RX_SHA-1_HASH_7								xxh
0x68	RX_SHA-1_HASH_8								xxh
0x69	RX_SHA-1_HASH_9								xxh
0x6A	RX_SHA-1_HASH_10								xxh
0x6B	RX_SHA-1_HASH_11								xxh
0x6C	RX_SHA-1_HASH_12								xxh

Table 3-19 HDCP SHA-1 Hash Value Registers

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset
0x6D	RX_SHA-1_HASH_13								xxh
0x6E	RX_SHA-1_HASH_14								xxh
0x6F	RX_SHA-1_HASH_15								xxh
0x70	RX_SHA-1_HASH_16								xxh
0x71	RX_SHA-1_HASH_17								xxh
0x72	RX_SHA-1_HASH_18								xxh
0x73	RX_SHA-1_HASH_19								xxh

3.3.1.18 RX_KSV_FIFO Registers ($80 ~ $CF)

These 80-bytes registers are write only. The value writes to this register can be read by the upstream source through the DDC link while the HDCP is invoked. The MCU shall write 0x00 to these registers to be the default values. Each KSV list contains 5 bytes registers and the register structure is shown below.

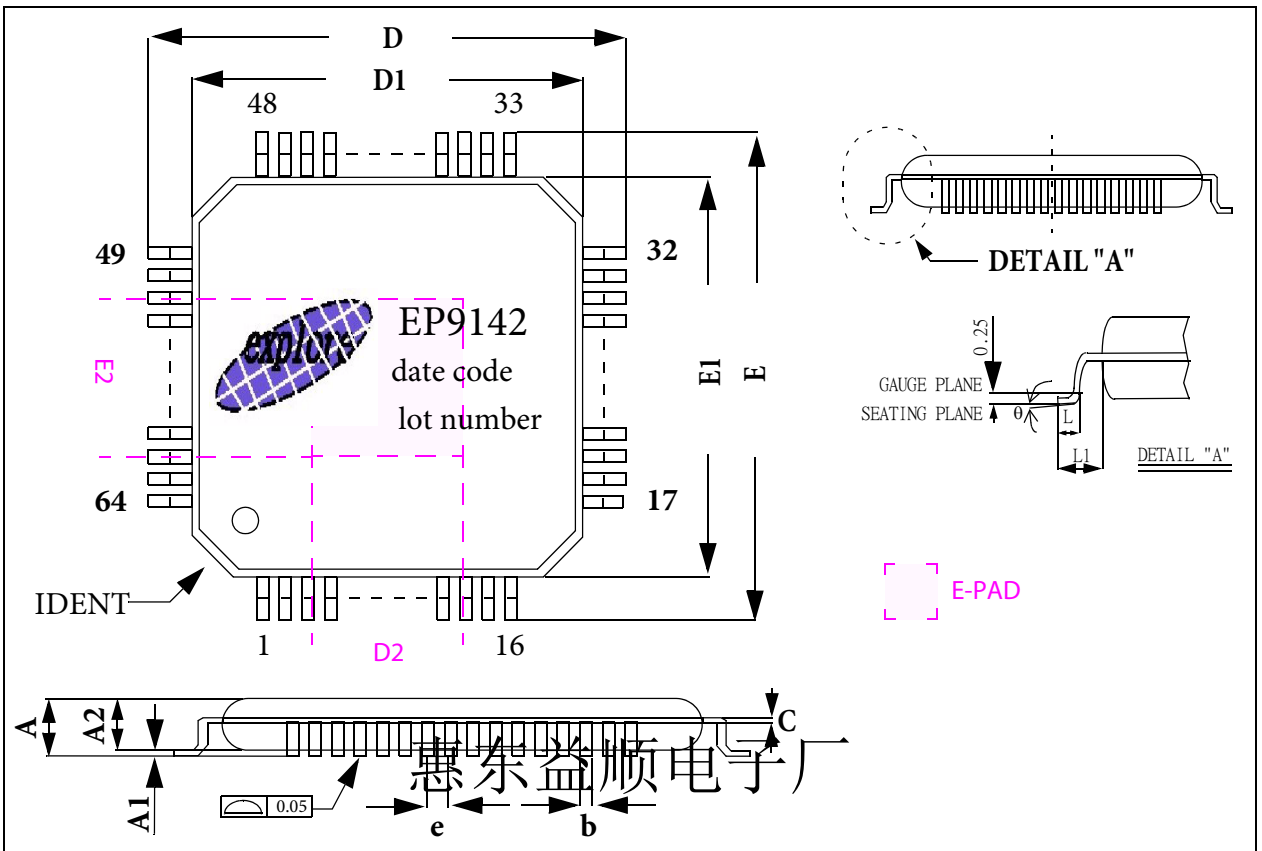
Table 3-20 KSV_FIFO Registers

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset
0x80 + 5 * (X-1)	KSVx[7:0]								xxh
0x81 + 5 * (X-1)	KSVx[15:8]								xxh
0x82 + 5 * (X-1)	KSVx[23:16]								xxh
0x83 + 5 * (X-1)	KSVx[31:24]								xxh
0x84 + 5 * (X-1)	KSVx[39:32]								xxh

NOTE: X = downstream device count

Appendix A Package

Figure A-1 EP9142 Footprint Diagram



Footprint Variations (mm)

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.05	0.1	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
C	0.09	-	0.20
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
D2	4.27	-	5.33
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
E2	4.27	-	5.33
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0"	3.5"	7"

NOTES:
1. JEDEC OUTLINE : MS-026 ACD-HD
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

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