HDMI 1.3 Repeater with Audio Output

EP91A1K

User Guide

V0.2

Revised Release Date: Aug. 25, 2009
Original Release Date: Aug. 04, 2009

Explore

Revision History

Version Number	Revision Date	Author	Description of Changes
0.1	Aug/04/2009	Ether Lai	Initial Version
0.2	Aug/25/2009	Ether Lai	Revise Feature List; Add Power Consumption;

Section 1 Introduction

1.1 Overview

EP91A1K is an HDMI Repeater with Audio Output which is suitable for low cost Audio Amplifier application. The chip supports 1 HDMI input port, 1 HDMI output port and Audio Outputs in IIS and SPDIF. The chip also supports on-chip EDID RAM. This will save system cost quite a bit. The chip is compliant with HDMI 1.3a and supports SD/HD Audio and Video in 12-bit Deep Color up to 1080p (225 Mhz TMDS clock).

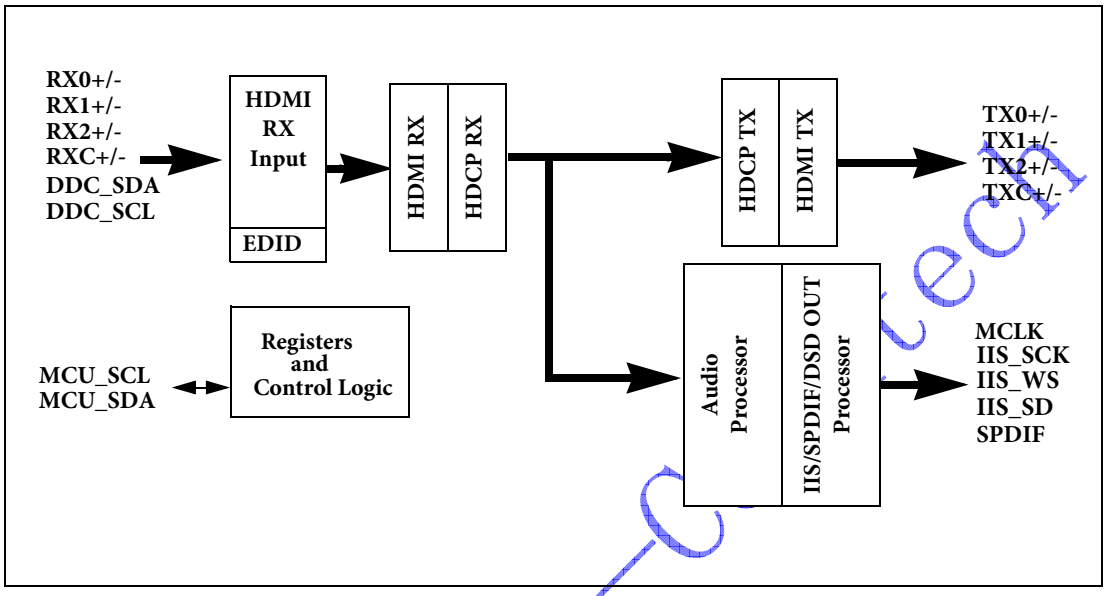
1.2 Features

- On-chip 1-IN 1-OUT HDMI Repeater with Equalizer
- Support wide Frequency Range: 25MHz - 225MHz TMDS clock
- On-chip HDMI Receiver and Transmitter core which are compliant with HDMI 1.3a specification and HDMI 1.3c Compliance Test Specification (CTS)
- Support 3D video format in HDMI 1.4
- On-chip HDCP Engine which supports Repeater and is compliant with HDCP 2.0 specification
- Supports on-chip EDID RAM for HDMI RX port.
- On-chip Audio Decoder which support 2-channel IIS/DSD and SPDIF audio outputs
- Support audio soft mute
- Support SPDIF Channel Status extraction
- Register-programmable via slave IIC interface
- Flexible interrupt registers with interrupt pin
- Link On and Valid DE Detection
- Controllable tri-state for Audio output pins
- Low stand-by current (< 2mA) at power down mode
- 64-pin LQFP package

Section 2 Overview

2.1 Chip Block Diagram

Figure 2-1 Chip Block Diagram



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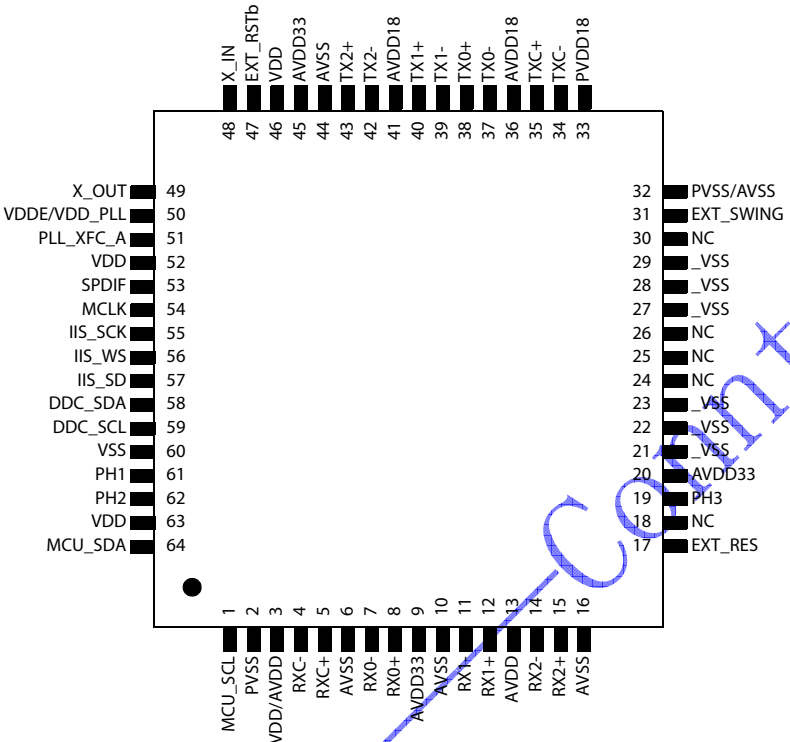
2.2 Pin Diagram

Figure 2-2 Pin Diagram



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 HDMI Input Ports

Name	In/Out	Description
RXC-	IN	Differential Clock Input Pair for HDMI Input
RXC+	IN	Differential Clock Input Pair for HDMI Input
RX0-	IN	Differential Data Input Pair0 for HDMI Input
RX0+	IN	Differential Data Input Pair0 for HDMI Input
RX1-	IN	Differential Data Input Pair1 for HDMI Input
RX1+	IN	Differential Data Input Pair1 for HDMI Input
RX2-	IN	Differential Data Input Pair2 for HDMI Input
RX2+	IN	Differential Data Input Pair2 for HDMI Input
EXT_RES	IN	External Termination Resistor for all HDMI Input Ports. A resistor should tie this pin to AVDD33. 470Ω is recommended.

Table 2-2 HDMI Output Ports

Name	In/Out	Description
TXC-	OUT	Differential Clock Output Pair for HDMI Output
TXC+	OUT	Differential Clock Output Pair for HDMI Output
TX0-	OUT	Differential Data Output Pair0 for HDMI Output
TX0+	OUT	Differential Data Output Pair0 for HDMI Output
TX1-	OUT	Differential Data Output Pair1 for HDMI Output
TX1+	OUT	Differential Data Output Pair1 for HDMI Output
TX2-	OUT	Differential Data Output Pair2 for HDMI Output
TX2+	OUT	Differential Data Output Pair2 for HDMI Output
EXT_SWING	Analog	Voltage Swing Adjust for HDMI Output. A resistor should tie this pin to AVDD18. This resistance determines the amplitude of the voltage swing. 270Ω is recommended.

Table 2-3 Audio Outputs

Name	In/Out	Description
MCLK	OUT	System Clock output for audio DAC (128/256/384/512 * $F_{Sampling\_Clock}$. Connecting a pull-up (logic 1) or pull-down (logic 0) resistor at this pin defines bit 4 of the slave IIC Address
IIS_SCK	OUT	IIS SCK output for IIS audio port. Sampling clock output for DSD.
IIS_WS	OUT	IIS WS output for all IIS audio ports. DSD audio output port (Right Channel).
IIS_SD	OUT	IIS SD output for audio port. DSD audio output port (Left Channel).
SPDIF	OUT	SPDIF output.

Table 2-4 DDC/IIC/MCU

Name	In/Out	Description
MCU_SCL	IN	SCL signal for slave IIC port
MCU_SDA	IO	SDA signal for slave IIC port
DDC_SCL	IN	IIC SCL signal for HDMI Receiver DDC Port
DDC_SDA	IO	IIC SDA signal for HDMI Receiver DDC Port
PH1	Analog	Connect with 2KΩ pull-up resistor to 3V3.
PH2	Analog	Connect with 2KΩ pull-up resistor to 3V3.
PH3	Analog	Connect with 1KΩ pull-up resistor to 3V3.

Table 2-5 Misc. Pins

Name	In/Out	Description
X_IN	Analog	External Crystal Input, 18.432 Mhz
X_OUT	Analog	External Crystal Output, 18.432 Mhz
EXT_RSTb	IN	External Reset input (Active Low) with internal weak pull-up.
PLL_XFC_A	Analog	For connecting a capacitor to ground for on-chip PLL

Table 2-6 Power Pins

Name	In/Out	Description
AVDD	PWR	HDMI Receiver Analog Power (1.8V)
PVDD	PWR	HDMI Receiver PLL Analog Power (1.8V)
AVDD33	PWR	HDMI Termination Power (3.3V)
AVDD18	PWR	HDMI Transmitter Analog Power (1.8V)
PVDD18	PWR	HDMI Transmitter PLL Analog Power
AVSS, PVSS	GND	Analog Ground
VDDE/VDD_PLL	PWR	I/O Power (3.3V)
VDD	PWR	Internal Logic Power (1.8V)
VSS	GND	I/O & Logic Ground
_VSS	GND	Common Ground

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	-0.3		4.0	V
Vcc18	1.8V Supply Voltage	-0.3		2.5	V
V_I	Input Voltage	-0.3		V_{cc33} + 0.3	V
V_O	Output Voltage	-0.3		V_{cc33} + 0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-40		125	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		44		°C/W

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	3.14	3.3	3.6	V
Vcc18	1.8V Supply Voltage	1.71	1.8	1.98	V
V_{CCN}	Supply Voltage Noise[1]	-0.3		100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	uA

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DC Analogue Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak to peak amplitude	R_{LOAD} = 50 ohm R_{EXT_SWING} = 270 ohm		510	550	590	mV
V_{DOH}	Differential High-level Output Voltage[1]				AVCC		V
I_{DOS}	Differential Output Short Circuit Current	V_{OUT} = 0V; TX_TERM bit is 0				5	uA
I_{PD}	Power-Down Current[2]	25°C Ambient	3V3		1		mA
			1V8		2		mA
I_{CCD}	Supply Current (25°C Ambient, RX/TX are Active R_{EXT_RES} = 470 ohm, R_{EXT_SWING} = 270 ohm, TX_TERM bit is 1)	1080p Resolution (12-bit)	3V3		93		mA
			1V8		256		mA
		1080p Resolution (8-bit)	3V3		90		mA
			1V8		210		mA

1 Guaranteed by design.

2 Assumes all HDMI/DVI I/O ports are not connected and all digital inputs are silent.

Receiver AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]				0.4	T_{bit}
T_{CCS}	Channel to Channel Differential Input Skew[1]				1.0	T_{pixel}
T_{IJIT}	Differential Input Clock Jitter Tolerance[2,3]				0.3	T_{bit}
F_{CIP}	TMDS CLK Frequency		25		225	MHz

NOTES:

1. Guaranteed by design.
2. Jitter defines as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electronic Measurement Procedures*

Transmitter AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
S_{LHT}	Differential Swing Low-to-High Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm, R_{EXT_SWING} = 270 ohm	170	200	230	ps
S_{HLT}	Differential Swing High-to-Low Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm, R_{EXT_SWING} = 270 ohm	170	200	230	ps

I2S Audio AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{sck}	SCK Clock Period	C_L = 10pF		1		T_{sck}
T_{sck_d}	SCK Clock Duty Cycle	C_L = 10pF	40%		60%	T_{sck}
T_{sck_h}	SCK Clock High Time	C_L = 10pF	40%		60%	T_{sck}
T_{sck_l}	SCK Clock LOW Time	C_L = 10pF	40%		60%	T_{sck}
T_{iis_s}	SCK to SD and WS (Setup Time)	C_L = 10pF	40%		-	T_{sck}
T_{iis_h}	SCK to SD and WS (Hold Time)	C_L = 10pF	40%		-	T_{sck}

SPDIF Audio AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{spdif}	SPDIF Cycle Time	C_L = 10pF		1		UI
T_{spdif_d}	SPDIF Duty Cycle	C_L = 10pF	90%		110%	UI

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Section 3 Functional Description

3.1 1-In 1-Out HDMI Repeater

The chip supports 1 HDMI Input Port, 1 HDMI Output Port and audio outputs. The incoming A/V source is HDCP decoded in HDMI RX and HDCP encoded again for HDMI Transmitter Port output.

3.2 Audio Output

Audio data is extracted and decoded from the HDMI RX. The conventional SD/HD Audio and 2 channel One Bit Audio are supported. The decoded audio data is buffered in an on-chip FIFO. An on-chip PLL is used to regenerate audio clock from the HDMI TMDS clock under the control of HDMI source. Digital audio signals in IIS, SPDIF or DSD format are generated based on this regenerated audio clock.

3.3 HDCP Engine & HDCP Keys

There are 2 HDCP engines on-chip. One is for HDMI RX port and the other is for HDMI TX Port. The on-chip HDCP (High-bandwidth Digital Content Protection) engines are compliant with HDCP 2.0 specification. The 2 HDCP key sets and BKSVs are downloaded from external EE at power up. The HDCP keys stored in external EE are scrambled for security purpose. The chip will descramble the keys after download.

3.4 InfoFrame Data

All types of Packet/InfoFrame data can be extracted, decoded from HDMI data stream and stored in the internal registers. The Audio InfoFrames is always extracted and put in dedicated buffers. Other Packet/InfoFrame type can be selectively extracted and stored in 2 shared packet buffers. Whenever an InfoFrame is received, an interrupt flag is set in an internal register. The MCU can poll the interrupt flags and extract the InfoFrame content through IIC bus.

Section 4 Detail Functional Descriptions

4.1 IIC Interface

The chip provides an IIC serial bus interface (SCL/SDA pins) for MCU to access the HDMI control/status registers and Repeater control/status registers. The IIC address for HDMI control/status registers is "110_IICA_100x" and the IIC address for Repeater control/status registers is "110_IICA_101x"(where x=1 for read and x=0 for write). IICA is programmable by connecting a pull-up (logic 1) or pull-down (logic 0) resistor at MCLK pin.

Table 4-1 IIC Address of HDMI and Repeater

	HDMI Module		REPEATER Module	
MCLK Pin	IIC write	IIC read	IIC write	IIC read
Pull-Down	C8	C9	CA	CB
Pull-Up	D8	D9	DA	DB

The IIC bus is a slave which uses a Serial Data line (SDA) at MCU_SDA pin and a Serial Clock Line (SCL) at MCU_SCL pin for receiving and transmitting data. All devices connected to the IIC bus must have open drain or open collector outputs. Logic AND function is exercised on both lines with external pull-up resistors, the value of these resistors is system dependent. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable at the positive edge of SCL. If the SDA changes state while SCL is HIGH, the IIC interface interprets that action as a START or STOP sequence. Data on SDA must change only when SCL is LOW.

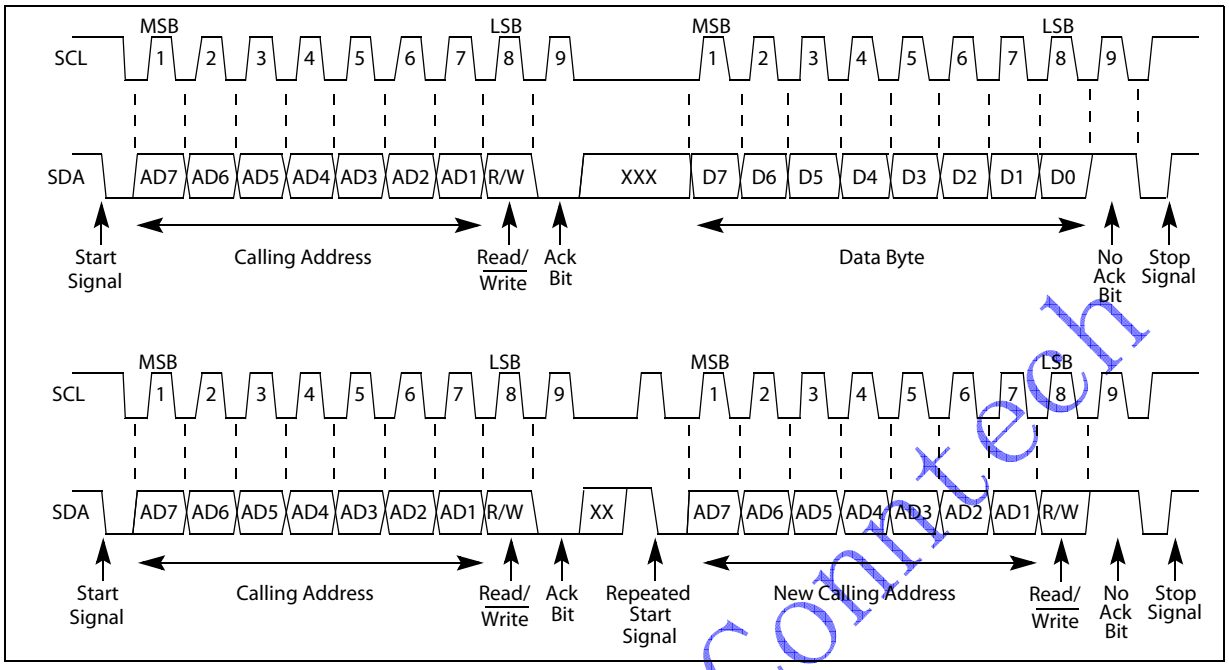
When the serial interface is inactive (SCL and SDA are HIGH), communication are initiated by a START signal which is a HIGH-to-LOW transition on SDA while SCL is HIGH. The first eight bits of data transferred after a START signal comprising a seven bit slave address (the seven MSB bits) and a single R/W bit (the LSB bit). The R/W bit indicates the direction of data transfer, "1" means read from device and "0" means write to device. If the transmitted slave address matches the address of the device, the chip sends the acknowledge by asserting SDA Low on the ninth SCL pulse. Else, the chip does not acknowledge.

To terminate a read/write sequence, a STOP signal must be sent. A STOP signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH.

A Repeated START signal occurs when the master device driving the serial interface generates a START signal without first generating a STOP signal to terminate the current read/write sequence. This can be used to change the mode of communication (read, write) between the slave and master without releasing the bus.

The standard IIC traffic protocol is illustrated in the following Figure:

Figure 4-1 IIC Bus Transmission Protocol



4.2 IIC Protocol for HDMI and Repeater Control/Status Register

4.2.1 HDMI Control/Status Register Access

HDMI control/status registers are organized by Register Sets. Each Register Set is comprised of one or more than one bytes of register. To address a register byte, a Word Address along with a Byte Address should be given. Word Address is used to address the register set and Byte Address is used to address the designated register byte within the addressed register set. There are 5 components in this IIC protocol:

- START Signal
- Slave Address Byte
- Word Address Byte for the Register Set
- Data Bytes for Read/Write from/to the Register Set
- STOP Signal

In Write Operation, data write starts from byte 0 of the register set and continue write to the next byte of the register set if data presents. The acknowledge bit will be sent on the ninth SCL pulse after every 8-bits data received.

In Read Operation, data are read from byte 0 of the register set in a similar manner. Reading requires two IIC transfer operations:

The Word Address must be written with the R/W bit of the slave address byte being LOW to set up the Word Address for the following read operations.

Start reading data with the R/W bit of the slave address byte being HIGH from the Word Address previously established. Data is read from byte 0 of the address register set and continue the next byte read if acknowledge presents.

Write to a Register Set:

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Word Address Byte
- Data Byte/Bytes to the register set starting from byte 0
- STOP Signal

Read from a Register Set:

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Word Address Byte
- Repeated START Signal
- Slave Address Byte (R/W = HIGH)
- Data Byte/Bytes from addressed register set starting from byte 0
- STOP Signal

4.2.2 Repeater Control/Status Register Access

Repeater control/status registers are organized by individual registers. To address a register byte, a Base Address should be given. Once the Base Address is established, single byte or multiple bytes data can be written or read from the registers starting from the Base Address. There are 5 components in this IIC protocol:

- START Signal
- Slave Address Byte
- Base Register Address Byte
- Data Byte for Read/Write
- STOP Signal

In Write Operation, data write starts from the Base Address and continue write to the next address register if data presents. The acknowledge bit will be sent on the ninth SCL pulse after every 8-bits data received.

In Read Operation, data are read from the Base Address in a similar manner. Reading requires two IIC transfer operations:

The Base Address must be written with the R/W bit of the slave address byte being LOW to set up the Base Address for the following read operations.

Start reading data with the R/W bit of the slave address byte being HIGH from the Base Address previously established. Data is read from Base Address and continue the next address read if acknowledge presents.

Write to One Control Register:

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- Data Byte to Base Address
- STOP Signal

Write to Multiple Control Registers:

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- Data Byte to Base Address
- Data Byte to (Base Address + 1)
- Data Byte to (Base Address + 2)
- .....
- Data Byte to (Base Address + N)
- STOP Signal

Read from One Control Register:

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- Repeated START Signal
- Slave Address Byte (R/W = HIGH)
- Data Byte from Base Address
- STOP Signal

Read from Multiple Control Registers:

- START Signal
- Slave Address Byte (R/W bit = LOW)

- Base Address Byte
- Repeated START Signal
- Slave Address Byte (R/W = HIGH)
- Data Byte from Base Address
- Data Byte from (Base Address + 1)
- Data Byte from (Base Address + 2)
- .....
- Data Byte from (Base Address + N)
- STOP Signal

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4.3 HDMI Control/Status Registers

4.3.1 Register Descriptions

4.3.1.1 Interrupt Control and Flags (Word Address = $29)

Table 4-2 Interrupt Register 0

Word Address = $29, Byte 0

bit	7	6	5	4	3	2	1	0
R	-	AVMC_F	AVMS_F	SEL2_F	SEL1_F	-	ADO_F	-
W	-	-	-	-	-	-	-	-
Pin Reset:	0	0	0	0	0	0	0	0

If this register is read, it gives Interrupt Flag information. Whenever a designated packet is received, the corresponding interrupt flag bit will be set. After MCU read this register, all the flag bits will be cleared automatically. Special care is taken by the design to prevent accidentally loss of any flag bit.

ADO_F — Audio InfoFrame Interrupt Flag

This bit is set when an Audio InfoFrame is received and is auto cleared when the register is read.

SEL1_F — 1st Selected Packet Interrupt Flag

This bit is set when the selected packet 1is received and is auto cleared when the register is read.

SEL2_F — 2nd Selected Packet Interrupt Flag

This bit is set when the selected packet 2 is received and is auto cleared when the register is read.

AVMS_F — AVMUTE Set Interrupt Flag

This bit is set when AVMUTE is set by General Control Packet and is auto cleared when the register is read.

AVMC_F — AVMUTE Clear Interrupt Flag

This bit is set when AVMUTE is cleared by General Control Packet and is auto cleared when the register is read.

Table 4-3 Interrupt Register 1

Word Address = $29, Byte 1

bit	7	6	5	4	3	2	1	0
R	AAMS_F	EXCP_F6	EXCP_F5	EXCP_F4	EXCP_F3	-	-	EXCP_F0
W	-	-	-	-	-	-	-	-
Pin Reset:	0	0	0	0	0	0	0	0

If this register is read, it gives Interrupt Flag information. Whenever an exception occurs, the corresponding interrupt flag bit will be set. After MCU read this register, all the flag bits will be cleared automatically. Special care is taken by the design to prevent accidentally loss of any flag bit.

EXCP_F0 — Exception 0 Interrupt Flag

This bit is set when a BCH error is detected.

EXCP_F3 — Exception 3 Interrupt Flag

This bit is set when audio mode change is detected from ADO packet.

EXCP_F4 — Exception 4 Interrupt Flag

This bit is set when audio sampling frequency change is detected.

EXCP_F5 — Exception 4 Interrupt Flag

This bit is set when audio FIFO overflow/underflow is detected.

EXCP_F6 — Exception 6 Interrupt Flag

This bit is set when HDMI signal changes from valid to invalid or from invalid to valid.

AAMS_F — Automatic Audio Mute Set Flag

This bit is set when A_MUTE bit is automatically set by AAM (Automatic Audio Mute) logic on detection of designated exception.

Table 4-4 Automatic Audio Mute Enable Register

Word Address = $29, Byte 2

bit	7	6	5	4	3	2	1	0
R W	-	AAM_EN6	AAM_EN5	AAM_EN4	AAM_EN3	-	-	AAM_EN0
Pin Reset:	0	0	0	0	0	0	0	0

This register controls the Automatic Audio Mute (AAM) function. Each bit controls whether the A_MUTE bit will be automatically set or not when the designated exception occurs. When A_MUTE bit is set, audio is mute.

AAM_EN0 — Automatic Audio Mute Enable 0

1 = A_MUTE bit will be automatically set when EXCP_F0 is set.
0 = A_MUTE bit is not affected by EXCP_F0.

AAM_EN3 — Automatic Audio Mute Enable 3

1 = A_MUTE bit will be automatically set when EXCP_F3 is set.
0 = A_MUTE bit is not affected by EXCP_F3.

AAM_EN4 — Automatic Audio Mute Enable 4

1 = A_MUTE bit will be automatically set when EXCP_F4 is set.
0 = A_MUTE bit is not affected by EXCP_F4.

AAM_EN5 — Automatic Audio Mute Enable 5

1 = A_MUTE bit will be automatically set when EXCP_F5 is set.
0 = A_MUTE bit is not affected by EXCP_F5.

AAM_EN6 — Automatic Audio Mute Enable 6

1 = A_MUTE bit will be automatically set when EXCP_F6 is set.
0 = A_MUTE bit is not affected by EXCP_F6.

4.3.1.2 Audio InfoFrame (Word Address = $2B)

The 7-byte Audio InfoFrame content is stored in the register set with Word Address $2B with Byte-0 being the version number, Byte-1 being the packet check sum, Byte-2 corresponding to the 1st byte of the InfoFrame and Byte-6 corresponding to the last byte of the InfoFrame.

Table 4-5 ADO InfoFrame Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x2B	0	R	Version Number							
	1		Checksum							
	2		CT3	CT2	CT1	CT0	0	CC2	CC1	CC0
	3		0	0	0	SF2	SF1	SF0	SS1	SS0
	4		0	0	0	0	0	0	0	0
	5		CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
	6		DM_INH	LSV3	LSV2	LSV1	LSV0	0	0	0

4.3.1.3 Selected Packet 1 (Word Address = $2D)

Any other packet with specified packet type can be extracted and stored in this register set. The specified packet type needs to be written into Byte-0. If 0 value is written, no packet will be extracted. If a packet with matched packet type is received, the 3-byte Packet Header and the 28-byte Packet Content are stored in the register set in sequence starting from Byte-0 and end at Byte-30.

4.3.1.4 Selected Packet 2 (Word Address = $2E)

Any other packet with specified packet type can be extracted and stored in this register set. The specified packet type needs to be written into Byte-0. If 0 value is written, no packet will be extracted. If a packet with

matched packet type is received, the 3-byte Packet Header and the 28-byte Packet Content are stored in the register set in sequence starting from Byte-0 and end at Byte-30.

Table 4-6 Selected Packet Type 1/2 Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x2D & 0x2E	0	R/W	Packet Header 0 (HB0, Selected Packet Type)							
	1	R	Packet Header 1 (HB1)							
	2		Packet Header 2 (HB2)							
	3		Data Byte 0 (PB0 / SB0)							
	4		Data Byte 1 (PB1 / SB1)							
	5		Data Byte 2 (PB2 / SB2)							
	6		Data Byte 3 (PB3 / SB3)							
	7		Data Byte 4 (PB4 / SB4)							
	8		Data Byte 5 (PB5 / SB5)							
	9		Data Byte 6 (PB6 /SB6)							
	10		Data Byte 7 (PB7 / SB0)							
	11		Data Byte 8 (PB8 / SB1)							
	12		Data Byte 9 (PB9 / SB2)							
	13		Data Byte 10 (PB10 / SB3)							
	14		Data Byte 11 (PB11 / SB4)							
	15		Data Byte 12 (PB12 / SB5)							
	16		Data Byte 13 (PB13 / SB6)							
	17		Data Byte 14 (PB14 / SB0)							
	18		Data Byte 15 (PB15 / SB1)							
	19		Data Byte 16 (PB16 / SB2)							
	20		Data Byte 17 (PB17 / SB3)							
	21		Data Byte 18 (PB18 / SB4)							
	22		Data Byte 19 (PB19 / SB5)							
	23		Data Byte 20 (PB20 / SB6)							
	24		Data Byte 21 (PB21 / SB0)							
	25		Data Byte 22 (PB22 / SB1)							
	26		Data Byte 23 (PB23 / SB2)							
	27		Data Byte 24 (PB24 / SB3)							
	28		Data Byte 25 (PB25 / SB4)							
	29		Data Byte 26 (PB26 / SB5)							
	30		Data Byte 27 (PB27 / SB6)							

4.3.1.5 Status Register 0 (Word Address = $3C, Byte 0)

Table 4-7 Status Register 0

Word Address = $3C, Byte 0

bit	7	6	5	4	3	2	1	0
R	-	-	AVMUTE	HDMI	-	-	DST_double	LAYOUT
W			AVMUTE_R					
	-	-	0	-	-	-	-	-

AVMUTE — (Read Only) AVMUTE signal decoded from HDMI General Control Packet.
1 = AVMUTE is in set state.
0 = AVMUTE is in clear state.

AVMUTE _R — (Write Only) AVMUTE reset.
1 = Clear AVMUTE.
0 = No operation.

HDMI — (Read Only) Primary RX HDMI/DVI signalling indicator
1 = HDMI signalling detected.
0 = DVI signalling detected.

DST_double — (Read Only) DST audio transfer rate indicator. Only valid if DST audio source is selected.
1 = DST audio is in double transfer rate.
0 = DST audio is in normal transfer rate.

LAYOUT — (Read Only) The LAYOUT bit extracted from HDMI audio packet.
1 = LAYOUT bit is 1 indicating 4 audio streams are being received.
0 = LAYOUT bit is 0 indicating 1 audio stream is being received.

4.3.1.6 Status Register 1 (Word Address = $3D, Byte 0)

Table 4-8 Status Register 1

Word Address = $3D, Byte 0

bit	7	6	5	4	3	2	1	0
R	LINK_ON	DE_VALID	-	A_UF	A_OF	-	-	-
W								
	-	-	-	-	-	-	-	-

LINK_ON — (Read Only) Link On indicator for Primary RX. Only valid when HDMI is not in power down mode.
1 = Valid clock signal detected at Primary RX Port.
0 = No clock signal presents at Primary RX Port.

DE_VALID — (Read Only) DE Valid indicator for Primary RX.
1 = Valid DE signal detected at Primary RX Port.
0 = No valid DE signal presents at Primary RX Port.

A_UF — (Read Only) Audio FIFO underflow flag. Set by audio logic. Cleared by read of Status Register 1.
1 = Audio FIFO underflow detected.
0 = Normal

A_OF — (Read Only) Audio FIFO overflow flag. Set by audio logic. Cleared by read of Status Register 1.
1 = Audio FIFO overflow detected.
0 = Normal

4.3.1.7 SPDIF Channel Status Register (Word Address = $3E)

The first 40 bits of the SPDIF Channel Status code (referred to as CS[39:0] with CS[0] being the first bit) are extracted from audio packets and put in this register set. CS[7:0] is stored in Byte-0[7:0], CS[15:8] is stored in Byte-1[7;0], CS[23:16] is stored in Byte-2[7:0], CS[31:24] is stored in Byte-3[7:0] and CS[39:32] is stored in Byte-4[7:0].

Most of the bits in this register set is Read Only except CS[2] and CS[15:8] which are writable. If CS_OW_EN bit is set, the written bits will replace the extracted bits and appear in SPDIF output.

Refer to IEC60958 specification for the detailed description of each bit. The following table shows the bit definition for Consumer Use Application.

Table 4-9 SPDIF Channel Status Registers (Consumer Use)

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x3E	0	R	MODE[1:0]		PRE[2:0]			COPY	PCM	PRO = 0
	1		CAT_CODE[7:0]							
	2		CH_NUM[3:0]				SRC_NUM[3:0]			
	3		RSVD		CLK_ACC[1:0]		SAMP_FREQ[3:0]			
	4		ORG_SAMP_FREQ[3:0]				SAMP_LEN[2:0]			MAX_LEN

4.3.1.8 Status Register 2 (Word Address = $3F, Byte 0)

Table 4-10 Status Register 2

Word Address = $3F, Byte 0

bit	7	6	5	4	3	2	1	0
R	EE_SUM[7:0]							
W								
	-	-	-	-	-	-	-	-

EE_SUM[7:0] — (Read Only) EE Check Sum.

When EE download is completed, the 8-bit EE Check Sum is put in this register by download logic.

4.3.1.9 General Control Register 0 (Word Address = $40, Byte 0)

Table 4-11 General Control Register 0

Word Address = $40, Byte 0

bit	7	6	5	4	3	2	1	0
R W	MUTE_POL	-	DE_RST_EN	EE_DL	SOFT_RST	PWR_DWN	-	-
Pin Reset:	0	1	0	0	0	0	0	0

MUTE_POL — A_MUTE output polarity control

1 = A_MUTE pin output is active low. A low level indicate mute.
0 = A_MUTE pin output is active high. A high level indicate mute.

DE_RST_EN — Enable invalid DE to reset HDCP
1 = Allow HDCP logic to be reset when invalid DE is detected. HDCP will start from non-authed and non-encrypted state after this reset.
0 = Normal.

EE_DL — Write 1 followed by write 0 will trigger HDCP key downloading from EE.
The HDCP engine has to be reset by asserting the RX_HDCP_RST and RX_RI_RST control bits in REPEATER section before the HDCP Key re-download process is triggered.

SOFT_RST — Soft Reset
1 = Reset all the HDMI and HDCP logic except IIC registers.
0 = Normal.

PWR_DWN — Power Down
1 = HDMI is in Power Down mode. HDMI and HDCP logic are reset except IIC registers
0 = Normal.

4.3.1.10 General Control Register 1 (Word Address = $41, Byte 0)

Table 4-12 General Control Register 1

Word Address = $41, Byte 0

bit	7	6	5	4	3	2	1	0
R W	-	-	-	-	AOUT_DIS[1:0]		-	-
Pin Reset:	0	0	0	0	0	0	0	0

AOUT_DIS[1:0] — Audio Output Disable mode
00 = MCLK, IIS_SCK, IIS_SD0, IIS_WS and SPDIF pins are normal outputs.
01 = IIS_SCK, IIS_SD0, IIS_WS pins are put in tri-state. MCLK and SPDIF pins are normal output.
10 = SPDIF pin is put in tri-state with weak pull-down. MCLK, IIS_SCK, IIS_SD0, IIS_SD1, IIS_SD2, IIS_SD3, IIS_WS pins are normal output.
11 = MCLK, IIS_SCK, IIS_SD0, IIS_SD1, IIS_SD2, IIS_SD3, IIS_WS and SPDIF pins are all put in tri-state with weak pull-down.

4.3.1.11 General Control Register 2 (Word Address = $42, Byte 0)

Table 4-13 General Control Register 2

Word Address = $42, Byte 0

bit	7	6	5	4	3	2	1	0
R W	-	-	EDID_EN3	EDID_EN2	EDID_EN1	EDID_EN0	EDID_SEL[1:0]	
Pin Reset:	0	0	0	0	0	0	0	0

EDID_EN3 — On-Chip Port 3 EDID control
1 = Enable Port 3 on-chip EDID.
0 = Disable Port 3 On-chip EDID.

EDID_EN2 — On-Chip Port 2 EDID control
1 = Enable Port 2 on-chip EDID.
0 = Disable Port 2 On-chip EDID.

EDID_EN1 — On-Chip Port 1 EDID control
1 = Enable Port 1 on-chip EDID.
0 = Disable Port 1 On-chip EDID.

EDID_EN0 — On-Chip Port 0 EDID control
1 = Enable Port 0 on-chip EDID.
0 = Disable Port 0 On-chip EDID.

EDID_SEL[1:0] — EDID RAM selection for IIC access or down loading
00 = Select Port 0 EDID RAM for IIC access
01 = Select Port 1 EDID RAM for IIC access
10 = Select Port 2 EDID RAM for IIC access
11 = Select Port 3 EDID RAM for IIC access

4.3.1.12 General Control Register 3 (Word Address = $43, Byte 0)

Table 4-14 General Control Register 3

Word Address = $43, Byte 0

bit	7	6	5	4	3	2	1	0
R W	-	-	-	-	-	-	-	A_MUTE
Pin Reset:	0	0	0	0	0	0	0	1

A_MUTE — Audio Mute Control
1 = Audio is mute
0 = Normal

4.3.1.13 General Control Register 4 (Word Address = $44, Byte 0)

Table 4-15 General Control Register 4

Word Address = $44, Byte 0

bit	7	6	5	4	3	2	1	0
R	LNK_RST_DIS	CTS_ADJ_DIS	A_source[1:0]		-	SF_R[2:0]		
W						-		
Pin Reset:	0	0	0	0	0	0	0	0

LINK_RST_DIS — Disable HDCP reset by link-off condition
1 = HDCP is not reset by link-off condition
0 = HDCP is reset by link-off condition

CTS_ADJ_DIS — Disable CTS auto adjustment
1 = CTS is not adjusted
0 = CTS is auto adjusted to prevent FIFO overflow or underflow

A_source — Audio Source Selection
00 = Select audio source from Standard Audio Sample Packets
01 = Select audio source from One Bit Audio Sample Packets
10 = Select audio source from High Bit Rate Audio Sample Packets
11 = Reserved

SF_R[2:0] — (Read Only) Audio Sampling Frequency information derived from Audio Clock Regeneration Packet while the X_IN frequency is 18.432MHz
000 = 32 KHz
001 = 44.1 KHz
010 = 48 KHz
011 = 88.2 KHz
100 = 96 KHz
101 = 176.4 KHz
110 = 192 KHz
111 = 768 KHz

4.3.1.14 General Control Register 5 (Word Address = $45, Byte 0)

Table 4-16 General Control Register 5

Word Address = $45, Byte 0

bit	7	6	5	4	3	2	1	0
R	SCK_POL	WS_POL	WS_M	IIS_SS	CS_OW_EN	AMUTE_EN	MCLK_SEL[1:0]	
W								
Pin Reset:	0	0	0	0	0	0	0	0

SCK_POL — IIS_SCK output polarity
1 = Inverse from IIS standard.

0 = IIS standard.

WS_POL — IIS_WS output polarity
1 = Inverse from IIS standard.
0 = IIS standard.

WS_M — IIS_WS output timing mode
1 = IIS_WS is one clock delayed compared with standard IIS timing.
0 = IIS standard.

IIS_SS — IIS sample size
1 = IIS outputs 32 bits sample size.
0 = IIS outputs 16 bits sample size.

CS_OW_EN — Channel Status Over Write Enable
1 = Enable SPDIF Channel Status Over Write.
0 = Disable SPDIF Channel Status Over Write.

AMUTE_EN — Audio mute enable
1 = Enable on-chip audio mute logic.
0 = Disable on-chip audio mute logic. Audio mute shall be performed in external Audio DAC.

MCLK_SEL[1:0] — MCLK Selection

These 2 bits select audio system clock (MCLK) frequency.
00 = MCLK frequency is 128 times of audio sampling frequency
01 = MCLK frequency is 256 times of audio sampling frequency. Not valid for HBR Audio.
10 = MCLK frequency is 384 times of audio sampling frequency. Not valid for HBR Audio.
11 = MCLK frequency is 512 times of audio sampling frequency. Not valid for HBR Audio.

4.3.1.15 General Control Register 6 (Word Address = $46, Byte 0)

Table 4-17 General Control Register 6

Word Address = $46, Byte 0

bit	7	6	5	4	3	2	1	0
R W	SD3_PA[1:0]		SD2_PA[1:0]		SD1_PA[1:0]		SD0_PA[1:0]	
Reset:	1	1	1	0	0	1	0	0

SD3_PA[1:0] — Audio Stream assignment for IIS_SD3 output or DSD3(R/L) output
00 = Output Audio Stream 0
01 = Output Audio Stream 1
10 = Output Audio Stream 2
11 = Output Audio Stream 3

SD2_PA[1:0] — Audio Stream assignment for IIS_SD2 output or DSD2(R/L) output
00 = Output Audio Stream 0

01 = Output Audio Stream 1
10 = Output Audio Stream 2
11 = Output Audio Stream 3

SD1_PA[1:0] — Audio Stream assignment for IIS_SD1 output or DSD1(R/L) output
00 = Output Audio Stream 0
01 = Output Audio Stream 1
10 = Output Audio Stream 2
11 = Output Audio Stream 3

SD0_PA[1:0] — Audio Stream assignment for IIS_SD0 output or DSD0(R/L) output
00 = Output Audio Stream 0
01 = Output Audio Stream 1
10 = Output Audio Stream 2
11 = Output Audio Stream 3

4.3.1.16 General Control Register 8 (Word Address = $48, Byte 0)

Table 4-18 General Control Register 8

Word Address = $48, Byte 0

bit	7	6	5	4	3	2	1	0
R W	CTS_ADJ_mode[1:0]		TCYCLE[2:0]			MOD_PLL	HDCP_AM_EN	DSD_OPT
Pin Reset:	0	0	0	0	0	0	0	0

CTA_ADJ_mode[1:0] — A parameter to control audio tracking speed when CTS_ADJ_DIS is cleared. These bits shall be set to 0 for normal operation.

TCYCLE[2:0] — A parameter to control data judgement of HDMI sampling logic. These bit shall be set to a non-zero values for normal operation.

MOD_PLL — ACR1 Option
1 = Configure ACR1 PLL to modulo type and increase reference frequency by 16 times to reduce jitter.
0 = ACR1 PLL reference frequency is determined by CTS/N parameter which sent from HDMI TX.

HDCP_AM_EN — HDCP AVMUTE Option
1 = HDCP will be forced not to do descryption when AVMUTE is set.
0 = HDCP will do descryption disregard of AVMUTE bit status. This is recommended in normal operation.

DSD_OPT — DSD Audio Output Option
1 = DSD Audio output to DSP.
0 = DSD Audio output to DAC.

4.3.1.17 General Control Register 9 (Word Address = $49, Byte 0)

Table 4-19 General Control Register 9

Word Address = $49, Byte 0

bit	7	6	5	4	3	2	1	0
R W	RSVD	TX_ON	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Pin Reset:	0	0	0	0	0	0	0	0

RSVD— This reserved bit shall be set to 0 for normal operation

TX_ON— HDMI TX Output Port Enable Control
1 = Enable HDMI TX Output Port.
0 = Disable HDMI TX Output Port.

4.3.1.18 General Control Register 10 (Word Address = $4A, Byte 0)

Table 4-20 General Control Register 10

Word Address = $4A, Byte 0

bit	7	6	5	4	3	2	1	0
R W	-	-	RESERVED			DK_A[2:0]		
Pin Reset:	0	0	1	0	0	1	0	0

DK_A[2:0] — De-skewing Setting Control Bits

DK_A[2:0] sets the clock to data riming for de-skew purpose for the HDMI transmitter of Output Port A. Eight steps can be selected and the time difference for each step is 200 ps. The default is 0 step.

000 = -4 step
001 = -3 step
010 = -2 step
011 = -1 step
100 = 0 step
101 = +1 step
110 = +2 step
111 = +3 step

4.3.1.19 Analog Input Control Register (Word Address = $4B, Byte 0)

Table 4-21 Analog Input Control Register

Word Address = $4B, Byte 0

bit	7	6	5	4	3	2	1	0
R W	PLL_PHD	RX_PLL_REG	EQ_BIAS[1:0]		RX_PLL_PUMP[1:0]		RX_PLL_BW	EQ_GAIN
Pin Reset:	0	0	0	0	0	0	0	0

PLL_PHD — Audio PLL Phase Detector Control
1 = fixed
0 = variable

RX_PLL_REG — RX PLL Regulator Control
1 = Enable
0 = Disable

EQ_BIAS[1:0] — RX EQ Bias Current Control
00 = 150 uA
01 = 125 uA
10 = 100 uA
11 = 80 uA

RX_PLL_PUMP[1:0] — RX PLL Charge Pump Current Control
00 = 10 uA
01 = 20 uA
10 = 40 uA
11 = 40 uA

RX_PLL_BW — RX PLL Bandwidth Control
1 = 4.1MHz ~ 6.2MHz
0 = 4MHz

EQ_GAIN — RX EQ Gain Control
1 = 6 dB
0 = 11 dB

4.3.1.20 Analog Output Control Register (Word Address = $4C, Byte 0)

Table 4-22 Analog Output Control Register

Word Address = $4C, Byte 0

bit	7	6	5	4	3	2	1	0
R/W	TPLL_PUMP	PRE_DRIVE	TX_TERM	PRE_EM	TX_PLL_REG	TX_PRE_CTL	TX_SWING[1:0]	
Pin Reset:	0	0	0	0	0	0	0	0

TPLL_PUMP — TX PLL Charge Pump Current Control
1 = 30 uA
0 = 10 uA

PRE_DRIVE — TX Pre-Drive Current Control
1 = HIGH
0 = LOW

TX_TERM — TX on-chip 50 Ω Termination Select

1 = ON
0 = OFF

PRE_EM — TX Pre-Emphasis Strength Control
1 = High
0 = Low

TX_PLL_REG — TX PLL Regulator Control
1 = Enable
0 = Disable

TX_PRE_CTL — TX Output Pre-emphasis On/Off Control
1 = TX Output Pre-emphasis is enabled
0 = TX Output Pre-emphasis is disabled

TX_SWING[1:0] — TX Output Swing Control
00 = 100%
01 = 94%
10 = 88%
11 = 81%

4.3.1.21 EDID Data Register (Word Address = $FF, Byte 0~255)

Word Address from $FF is used for downloading the EDID data to the on-chip EDID RAM selected by EDID_SEL[1:0]. The 256 data bytes in this register set correspond to the 256 byte EDID data.

4.4 Repeater Control/Status Registers

The following table shows all the control/Status registers of the Repeater:

Table 4-23 Repeater Control/Status Registers

Addr	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	RESET
$07	R/W	RX_LINK_ON	RX_DE_ON	RX_HDMI	RX_ENC_ON	-	-	RSVD	RSVD	00h
$08	R/W	TX_MUTE	RX_VSYNC	-	-	-	-	TX_ENC_OPT	-	00h
$09	R	-	-	-	-	-	TX_RSEN	-	-	00h
$0A	W	-	-	-	-	-	RX_RI_RST	RX_DDC_DIS	RX_HDCP_RST	00h
$0E	R/W	-	-	-	-	-	-	TX_EESS	TX_HDMI	01h
$0F	R/W	TX_AKSV_RDY	TX_ENC_ON	-	TX_RPTR	-	-	TX_RI_RDY	TX_ENC_EN	00h
$10	R/W	TX_BKSV_1								XXh
$11	R/W	TX_BKSV_2								XXh
$12	R/W	TX_BKSV_3								XXh
$13	R/W	TX_BKSV_4								XXh
$14	R/W	TX_BKSV_5								XXh
$15	R/W	TX_AN_1								XXh
$16	R/W	TX_AN_2								XXh
$17	R/W	TX_AN_3								XXh
$18	R/W	TX_AN_4								XXh
$19	R/W	TX_AN_5								XXh
$1A	R/W	TX_AN_6								XXh
$1B	R/W	TX_AN_7								XXh
$1C	R/W	TX_AN_8								XXh
$1D	R	TX_AKSV_1								XXh
$1E	R	TX_AKSV_2								XXh
$1F	R	TX_AKSV_3								XXh
$20	R	TX_AKSV_4								XXh
$21	R	TX_AKSV_5								XXh
$22	R	TX_RI_1								XXh
$23	R	TX_RI_2								XXh
$25	R	TX_M0_1								XXh

$26	R	TX_M0_2							XXh
$27	R	TX_M0_3							XXh
$28	R	TX_M0_4							XXh
$29	R	TX_M0_5							XXh
$2A	R	TX_M0_6							XXh
$2B	R	TX_M0_7							XXh
$2C	R	TX_M0_8							XXh
$40	R	-	-	-	-	-	-	-	RX_M0_RDY	XXh
$41	R	RX_M0_1							XXh
$42	R	RX_M0_2							XXh
$43	R	RX_M0_3							XXh
$44	R	RX_M0_4							XXh
$45	R	RX_M0_5							XXh
$46	R	RX_M0_6							XXh
$47	R	RX_M0_7							XXh
$48	R	RX_M0_8							XXh
$50	W	RX_Bcaps							91h
$51	W	RX_Bstatus[7:0]							00h
$52	W	-	-	-	-	RX_Bstatus[11:8]			00h
$60	W	RX_SHA-1_HASH_0							XXh
$61	W	RX_SHA-1_HASH_1							XXh
$62	W	RX_SHA-1_HASH_2							XXh
$63	W	RX_SHA-1_HASH_3							XXh
$64	W	RX_SHA-1_HASH_4							XXh
$65	W	RX_SHA-1_HASH_5							XXh
$66	W	RX_SHA-1_HASH_6							XXh
$67	W	RX_SHA-1_HASH_7							XXh
$68	W	RX_SHA-1_HASH_8							XXh
$69	W	RX_SHA-1_HASH_9							XXh
$6A	W	RX_SHA-1_HASH_10							XXh
$6B	W	RX_SHA-1_HASH_11							XXh
$6C	W	RX_SHA-1_HASH_12							XXh
$6D	W	RX_SHA-1_HASH_13							XXh

$6E	W	RX_SHA-1_HASH_14	XXh
$6F	W	RX_SHA-1_HASH_15	XXh
$70	W	RX_SHA-1_HASH_16	XXh
$71	W	RX_SHA-1_HASH_17	XXh
$72	W	RX_SHA-1_HASH_18	XXh
$73	W	RX_SHA-1_HASH_19	XXh
$80 ~ $A7	W	RX_KSV_FIFOs	XXh

4.4.1 Register Descriptions

Detailed usage of these IIC registers is described in the following section.

4.4.1.1 Repeater Control Register 0

Table 4-24 Repeater Control Register 0

$07

bit	7	6	5	4	3	2	1	0
R	RX_LINK_ON	RX_DE_ON	RX_HDMI	RX_ENC_ON	-	-	RSVD	RSVD
W	-	-	-	-				
Reset:	-	-	-	-	-	-	0	0

RX_LINK_ON — Receiver Link On

This bit indicates whether a valid signal appears at the clock input of the RX. This bit is valid only when the RX is active (powered on and selected as output source).

1 = Clock presents at the input of the receiver port
0 = No clock is detected at the input of the receiver port

RX_DE_ON — Receiver DE On

This bit indicates whether DE signal is toggling at the RX. This bit is valid only when the RX is active (powered on and selected as output source).

1 = DE signal is toggling at the receiver port
0 = DE signal is not toggling at the receiver port

RX_HDMI — Receiver HDMI signal

This bit indicates whether the RX is receiving DVI or HDMI signal

1 = HDMI
0 = DVI

RX_ENC_ON — Receiver Decryption On

This bit indicates whether the HDCP decryption is active at the RX.
1 = HDCP decryption at the receiver port is active
0 = HDCP decryption at the receiver port is not active

RSVD— This reserved bit shall be set to 0 for normal operation

4.4.1.2 Repeater Control Register 1

Table 4-25 Repeater Control Register 1

$08

bit	7	6	5	4	3	2	1	0
R	TX_MUTE	RX_VSYNC	-	-	-	-	TX_ENC_OPT	-
W		-						
Reset:	0	-	-	0	-	-	0	0

TX_MUTE — Video Mute Transmitter

The bit is used to mute the video for the transmitter port.
1 = Transmitter port is video muted
0 = Normal

RX_VSYNC — RX Vertical Sync Status Bit

The RX_VSYNC bit gives the current status of the vertical sync signal for the RX.

TX_ENC_OPT — Transmitter Encryption Option
1 = Not affected by RX encryption status.
0 = Force not to encrypt if RX is not encrypted.

4.4.1.3 Repeater Control Register 2

Table 4-26 Repeater Control Register 2

$09

bit	7	6	5	4	3	2	1	0
R		-	-	-	-	TX_RSEN	-	-
W						-		
Reset:	-	-	-	-	-	-	-	-

TX_RSEN — Transmitter Analog Output Status Bit

The TX_RSEN bit indicates the analog output status at the transmitter port.
1 = The transmitter analog outputs are connected to the receiver
0 = The transmitter analog outputs are disconnected

4.4.1.4 Repeater Control Register 3

Table 4-27 Repeater Control Register 3

$0A

bit	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	-	-	-	-	-	RX_RI_RST	RX_DDC_DIS	RX_HDCP_RST
Reset:	-	-	-	-	-	0	0	0

RX_RI_RST — Reset HDCP Ri value for the RX
1 = Reset HDCP Ri value to 0 for the RX.
0 = Normal.

RX_DDC_DIS — Disable DDC ACK for the RX
1 = Disable DDC ACK for the RX.
0 = Normal.

RX_HDCP_RST — Reset HDCP for the RX
1 = Reset HDCP for the RX.
0 = Normal.

4.4.1.5 Repeater Control Register 4

Table 4-28 Repeater Control Register 4

$0E

bit	7	6	5	4	3	2	1	0
R W	-	-	-	-	-	-	TX_EESS	TX_HDMI
Reset:	-	-	-	-	-	-	0	1

TX_EESS — Enable Enhanced Encryption Signalling for the transmitter port
1 = Using Enhanced Encryption Signalling for the transmitter port.
0 = Using Original Encryption Signalling for the transmitter port. This is only valid if the transmitter is working in DVI mode (TX_HDMI = 0).

TX_HDMI — Set HDMI mode for the transmitter port
1 = Put the transmitter port working in HDMI mode. This is valid only if the receiver is receiving HDMI signal.
0 = Put the transmitter port working in DVI mode.

4.4.1.6 Repeater Control Register 5

Table 4-29 Repeater Control Register 5

$0F

bit	7	6	5	4	3	2	1	0
R	TX_AKSV_RDY	TX_ENC_ON	-	TX_RPTR	-	-	TX_RI_RDY	TX_ENC_EN
W								
	-	-	-	0	-	-	-	0

TX_AKSV_RDY — Transmitter AKSV Ready

The TX_AKSV_RDY bit indicates whether the HDCP keys and AKSV has been successfully downloaded from external EE or not for the transmitter port. This bit is read only.

1 = HDCP keys and AKSV has been successfully downloaded from external EE. AKSV is ready for read.

0 = HDCP keys and AKSV downloading has not been completed. AKSV is not ready for read.

TX_ENC_ON — Transmitter HDCP Encryption On

The TX_ENC_ON bit indicates whether the HDCP encryption for the transmitter port is active or not. This bit is read only.

1 = HDCP encryption is active.

0 = HDCP encryption is not active.

TX_RPTR — Transmit to Repeater

The TX_RPTR bit should be set if the receiver side which is connected to the transmitter port is a repeater. It should be cleared otherwise.

1 = The transmitter port is connecting to a repeater.

0 = The transmitter port is not connecting to a repeater.

TX_RI_RDY — Transmitter RI Ready

This bit indicates that the first Ri value is available for the transmitter port. This bit is read only.

1 = First Ri value is available for the transmitter port.

0 = First Ri value is not available for the transmitter port.

TX_ENC_EN — Transmitter ENC Enable

1 = Enable HDCP encryption for the transmitter port.

0 = Disable HDCP encryption the transmitter port.

4.4.1.7 Repeater TX_BKSV Registers - TX_BKSV_1 ~ TX_BKSV_5

Table 4-30 Repeater TX_BKSV Registers

$10 ~ $14

bit	7	6	5	4	3	2	1	0
R W	TX_BKSV1[7:0] ~ TX_BKSV5[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 5 registers for the transmitter port should be programmed with receiver's Key Selection Vector. TX_BKSV_1 is the LSB and TX_BKSV_5 is the MSB. TX_BKSV_5 should be written last, as it triggers the authentication process.

4.4.1.8 Repeater TX_AN Registers - TX_AN_1 ~ TX_AN_8

Table 4-31 Repeater TX_AN Registers

$15 ~ $1C

bit	7	6	5	4	3	2	1	0
R W	TX_AN1[7:0] ~ TX_AN8[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 8 registers for the transmitter port should be programmed with a 64-bit pseudo-random value before triggering the authentication process. TX_AN_1 is the LSB and TX_AN_8 is the MSB.

4.4.1.9 Repeater TX_AKSV Registers - TX_AKSV_1 ~ TX_AKSV_5

Table 4-32 Repeater TX_AKSV Registers

$1D ~ $21

bit	7	6	5	4	3	2	1	0
R W	TX_AKSV1[7:0] ~ TX_AKSV5[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 5 registers are read only which hold transmitter's Key Selection Vector for the transmitter port. TX_AKSV_1 is the LSB and TX_AKSV_5 is the MSB. All five bytes should be read from here and then written to the receiver. Byte 5 should be written last to the receiver, as it will trigger authentication there. These 5 registers should not be read until TX_AKSV_RDY bit is 1.

4.4.1.10 Repeater TX_RI Registers - TX_RI_1 ~ TX_RI_2

Table 4-33 Repeater TX_RI Registers

$22 ~ $23

bit	7	6	5	4	3	2	1	0
R W	TX_RI_1[7:0] ~ TX_RI_2[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 2 registers hold transmitter's Ri value for the transmitter port. They should be read and compared against the Ri value of the receiver to ensure that the encryption process on the transmitter and receiver is synchronized.

4.4.1.11 Repeater TX_M0 Registers

Table 4-34 Repeater TX_M0 Registers

$25 ~ $2C

bit	7	6	5	4	3	2	1	0
R W	TX_M0[7:0] ~ TX_M0[63:56]							
Reset:	-	-	-	-	-	-	-	-

This 8 byte registers are used to store the first secret value TX_M0 which calculated by the HDCP cipher function.

4.4.1.12 Repeater RX_M0_RDY Register

Table 4-35 Repeater RX_M0_RDY Register

$40

bit	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	RX_M0_RDY
Reset:	0	0	0	0	0	0	0	0

The RX_M0_RDY bit will be set to 1 while the last byte of AKSV is written and the HDCP engine completes the M0 calculation.

4.4.1.13 Repeater RX_M0 Registers ($41 ~ $48) - RX_M0_1 ~ RX_M0_8

Table 4-36 Repeater RX_M0 Registers

$41 ~ $48

bit	7	6	5	4	3	2	1	0
R	RX_M0_1[7:0] ~ RX_M0_8[7:0]							
Reset:	-	-	-	-	-	-	-	-

These 8 registers are read only which hold receiver's M0 values which calculated from HDCP engine. These values can be read while the RX_M0_RDY bit is 1 and can be used for SHA calculation.

4.4.1.14 Repeater RX_Bcaps Register

Table 4-37 Repeater RX_Bcaps Register

$50

bit	7	6	5	4	3	2	1	0
W	HDMI_CAP	REPEATER	FIFO_RDY	FAST	RSVD	RSVD	1.1_FEATURE	FAST_REAUTH
Reset:	1	0	0	1	0	0	0	1

This register is write only. The value writes to this register can be read by the upstream source through the DDC link while the HDCP is invoked.

HDMI_CAP — HDMI Reserved Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 7, HDMI_RESERVED bit. Use of this bit is reserved. HDCP receivers not capable of supporting HDMI must clear this bit to 0.

REPEATER — REPEATER Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 6, REPEATER bit.

FIFO_RDY — READY Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 5, READY bit.

FAST — FAST Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 4, FAST bit.

1.1_FEATURE — 1.1_FEATURE Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 1, 1.1_FEATURE bit. This bit shall set to 0 always.

FAST_REAUTH — FAST_REAUTHENTICATION Bit in HDCP Bcaps register

Value written into this bit will reflect to the HDCP Bcaps register, bit 0, FAST_REAUTHENTICATION bit.

4.4.1.15 Repeater RX_Bstatus Registers ($51 ~ $52)

Table 4-38 Repeater RX_Bstatus (LSB, [7:0]) Register

$51

bit	7	6	5	4	3	2	1	0
W	DEV_EXCEED	DEVICE_CNT[6:0]						
Reset:	0	0	0	0	0	0	0	0

Table 4-39 Repeater RX_Bstatus (MSB, [15:8]) Register

$52

bit	7	6	5	4	3	2	1	0
W	-	-	-	-	CASC_EXCEED	CASC_EXCEED		
Reset:	0	0	0	0	0	0	0	0

These 2 bytes registers are write only. The value writes to this register can be read by the upstream source through the DDC link while the HDCP is invoked.

DEV_EXCEED — MAX_DEVS_EXCEEDED Bit in HDCP Bstatus register

Value written into this bit will reflect to the HDCP Bstatus register, bit 7, MAX_DEVS_EXCEEDED bit.

DEVICE_COUNT[6:0] — DEVICE_COUNT Bits in HDCP Bstatus register

Value written into this bit will reflect to the HDCP Bstatus register, bit 6 ~ bit 0, DEVICE_COUNT[6:0] bit.

CASC_EXCEED — MAX_CASCADE_EXCEEDED Bit in HDCP Bstatus register

Value written into this bit will reflect to the HDCP Bstatus register, bit 11, MAX_CASCADE_EXCEEDED bit.

DEPTH[2:0] — DEPTH Bits in HDCP Bstatus register

Value written into this bit will reflect to the HDCP Bstatus register, bit 10 ~ bit 8, DEPTH[2:0] bit.

4.4.1.16 Repeater RX_SHA-1_HASH Registers ($60 ~ $73)

These 20-bytes registers are write only. The value writes to this register can be read by the upstream source through the DDC link while the HDCP is invoked.

Table 4-40 Repeater HDCP SHA-1 Hash Value Registers

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset
0x60	RX_SHA-1_HASH_0								xxh
0x61	RX_SHA-1_HASH_1								xxh
0x62	RX_SHA-1_HASH_2								xxh
0x63	RX_SHA-1_HASH_3								xxh
0x64	RX_SHA-1_HASH_4								xxh
0x65	RX_SHA-1_HASH_5								xxh
0x66	RX_SHA-1_HASH_6								xxh
0x67	RX_SHA-1_HASH_7								xxh
0x68	RX_SHA-1_HASH_8								xxh
0x69	RX_SHA-1_HASH_9								xxh
0x6A	RX_SHA-1_HASH_10								xxh
0x6B	RX_SHA-1_HASH_11								xxh
0x6C	RX_SHA-1_HASH_12								xxh

Table 4-40 Repeater HDCP SHA-1 Hash Value Registers

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset
0x6D	RX_SHA-1_HASH_13								xxh
0x6E	RX_SHA-1_HASH_14								xxh
0x6F	RX_SHA-1_HASH_15								xxh
0x70	RX_SHA-1_HASH_16								xxh
0x71	RX_SHA-1_HASH_17								xxh
0x72	RX_SHA-1_HASH_18								xxh
0x73	RX_SHA-1_HASH_19								xxh

4.4.1.17 Repeater RX_KSV_FIFO Registers ($80 ~ $A7)

These 40-bytes registers are write only. The value writes to this register can be read by the upstream source through the DDC link while the HDCP is invoked. The MCU shall write 0x00 to these registers to be the default values. Each KSV list contains 5 bytes registers and the register structure is shown below.

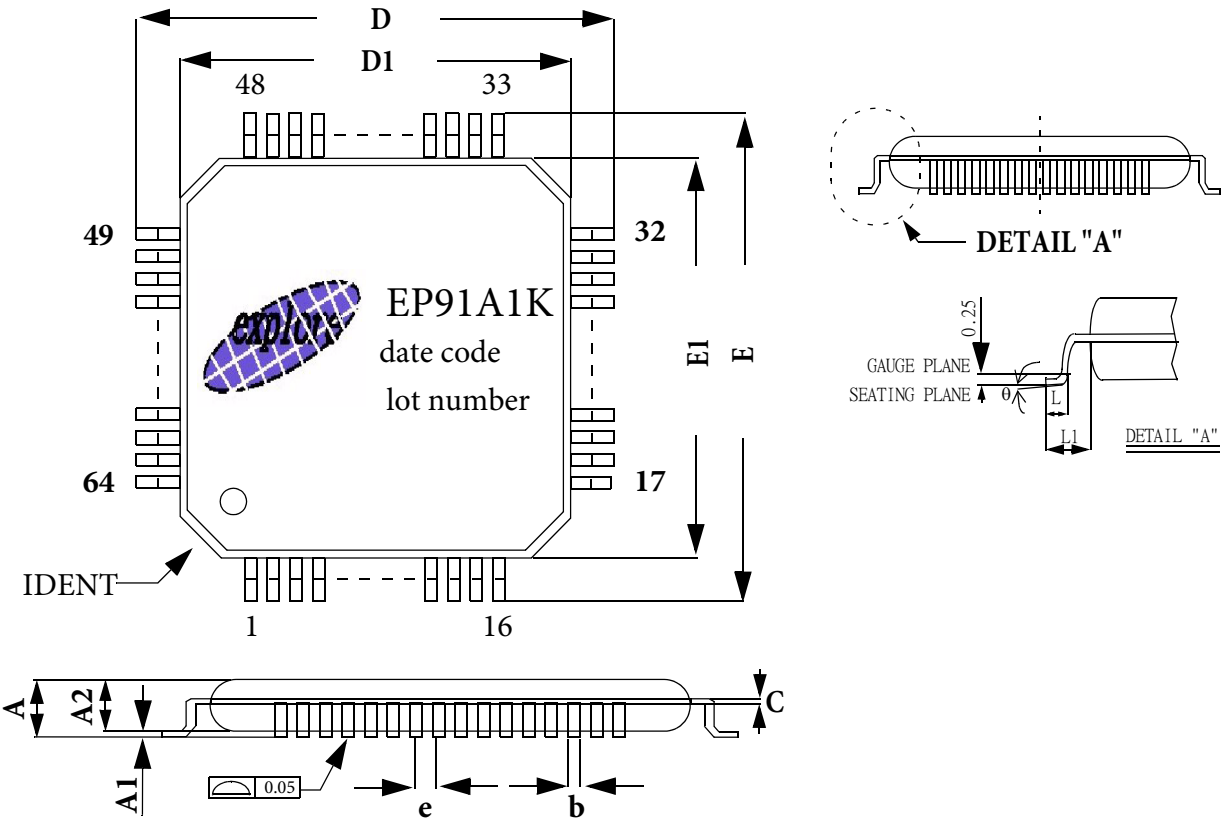
Table 4-41 Repeater KSV_FIFO Registers

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	reset
0x80 + 5 * (X-1)	KSVx[7:0]								xxh
0x81 + 5 * (X-1)	KSVx[15:8]								xxh
0x82 + 5 * (X-1)	KSVx[23:16]								xxh
0x83 + 5 * (X-1)	KSVx[31:24]								xxh
0x84 + 5 * (X-1)	KSVx[39:32]								xxh

NOTE: X = downstream device count

Appendix A Package

Figure A-1 EP91A1K Footprint Diagram



Footprint Variations (mm)

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	0.1	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
C	0.09	-	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0"	3.5"	7"

NOTES:
1. JEDEC OUTLINE : N/A
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

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