HDMI 1.4 3-In 1-Out Repeater/Switch/MCU Combo

EP92A2E

User Guide

V0.1

Original Release Date: Feb. 25, 2011
Revised Date: Oct. 18, 2011

Explore

Revision History

Version Number	Revision Date	Description of Changes
0.1	Oct/18/2011	Initial Version

Section 1 Introduction

1.1 Overview

EP92A2E is an HDMI 1.4a 3-IN 1-OUT Repeater/Switch/MCU combo suitable for Home Theater application. The on-chip HDMI/HDCP/CEC controller makes the user very easy to use the chip. It manages HDMI and HDCP automatically without the need for user to develop firmware. The CEC Controller provides the CEC physical layer transceiver and handles the protocol layer automatically. The chip supports 3 HDMI input ports (Port 0, Port 1 and Port 2) where Port 0 and Port 1 input to an HDMI Repeater and Port 2 input to an HDMI Switch. The HDMI Repeater supports HDCP decryption, audio outputs, audio inputs and HDCP re-encryption. The HDMI Switch supports TMDS switching and DDC switching. The chip supports ARC (Audio Return Channel) RX and is compliant with HDMI 1.4a. The chip supports SD/HD/DSD Audio in IIS and SPDIF format. The chip supports HD and 3-D Video up to 225 Mhz TMDS clock. The chip also supports 2 ports of on-chip EDID RAM and Power Regulator to save system cost.

1.2 Features

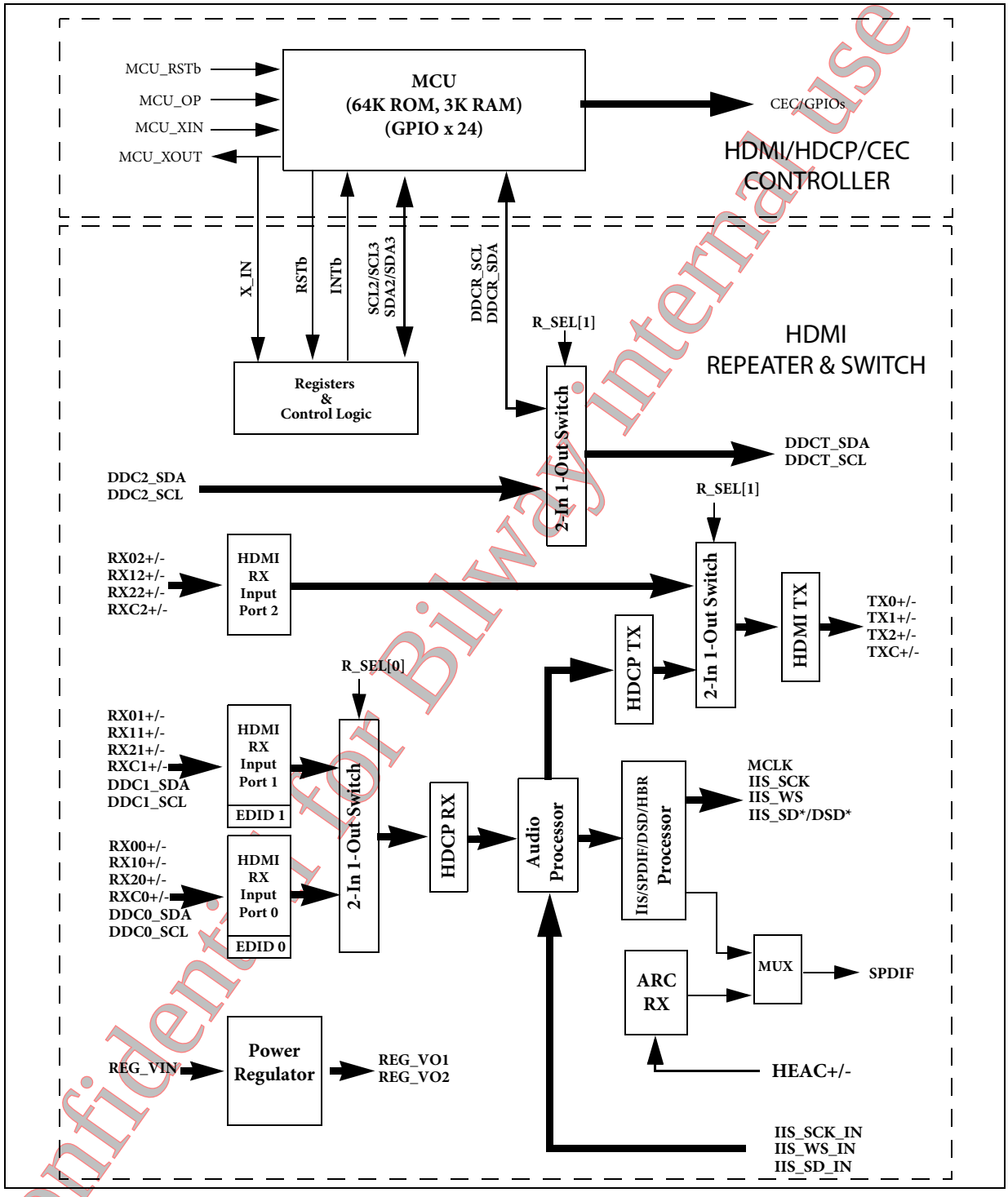
- On-chip HDMI/HDCP controller which manages HDMI and HDCP automatically without the need for user to develop firmware
- On-chip CEC controller which provides CEC Physical Layer Transceiver and handle the Protocol Layer without the need for user to develop firmware
- On-chip 3-IN 1-OUT HDMI Repeater/Switch with Equalizer
- On-chip HDMI Receiver and Transmitter core which are compliant with HDMI 1.4a specification
- On-chip HDCP Engine which supports Repeater and is compliant with HDCP 1.3 specification
- On-chip Audio Decoder which support 8-channel IIS/DSD and SPDIF audio outputs
- Supports Standard Audio, DSD Audio and HD (HBR) Audio
- Support wide Frequency Range: 25MHz - 225MHz TMDS clock
- Supports 12-bit Deep Full HD and 3D video
- Support HDMI 1.4a ARC (Audio Return Channel) RX
- Supports on-chip EDID RAM for Port 0 and Port 1
- Supports 1 HDMI output port
- Audio source for Repeater output can be from a regenerated LPCM audio source or the original audio from the selected Repeater input port.
- Supports audio soft mute
- Supports SPDIF Channel Status extraction
- Register-programmable via slave IIC interface

- Flexible interrupt registers with interrupt pin
- Link On and Valid DE Detection
- Controllable tri-state for Audio output pins
- HDCP keys is downloaded from external EE or embedded MCU
- On-chip Power Regulator which provides regulated programmable voltage
- Low stand-by current (< 3mA) at power down mode
- 128-pin LQFP package

Section 2 Overview

2.1 Chip Block Diagram

Figure 2-1 Chip Block Diagram



2.2 Pin Diagram

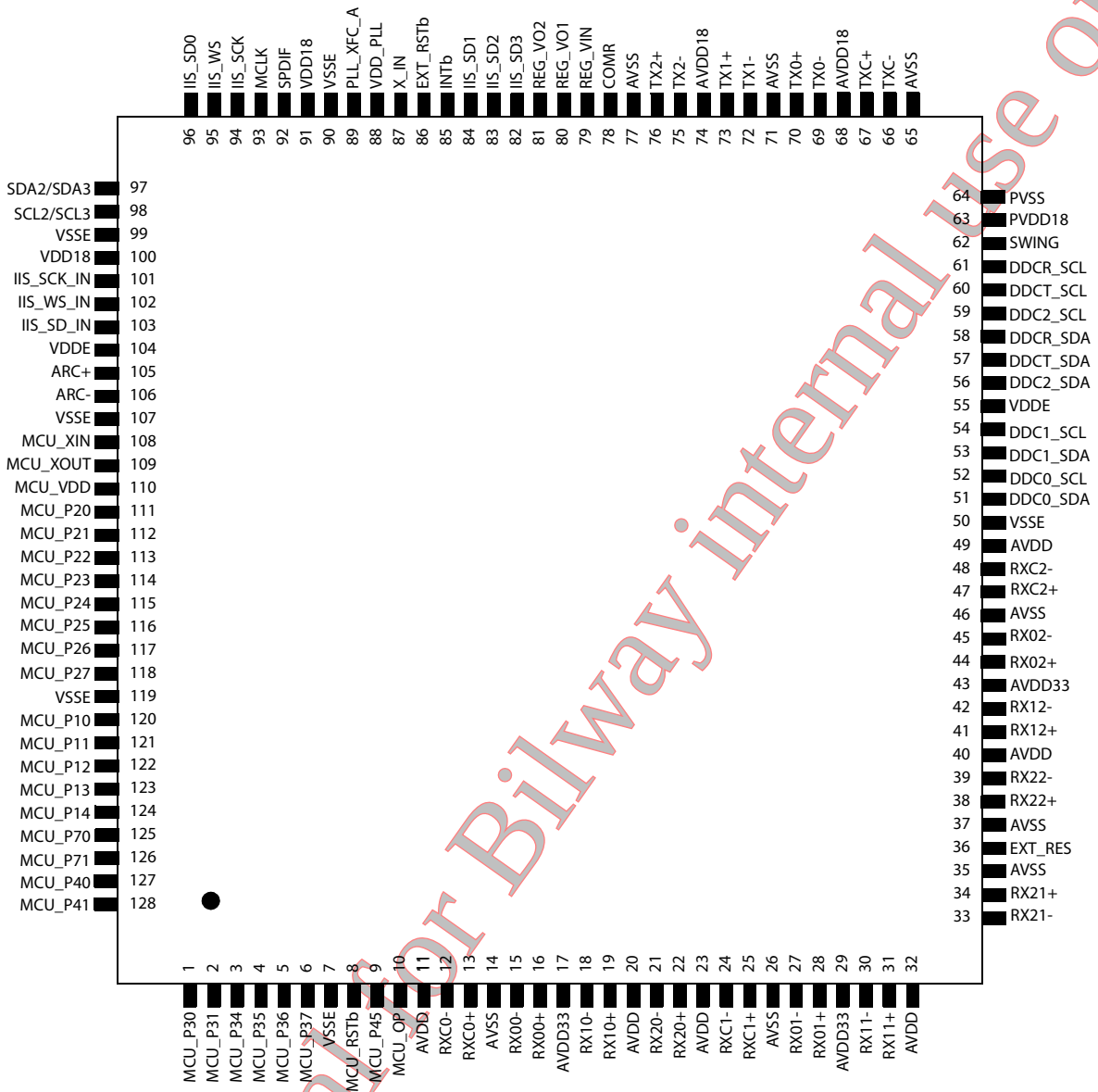


Figure 2-2 Pin Diagram

2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 HDMI Input Ports

Name	In/Out	Description
RXC0-	IN	Differential Clock Input Pair for HDMI Input Port 0
RXC0+	IN	Differential Clock Input Pair for HDMI Input Port 0
RX00-	IN	Differential Data Input Pair0 for HDMI Input Port 0
RX00+	IN	Differential Data Input Pair0 for HDMI Input Port 0
RX10-	IN	Differential Data Input Pair1 for HDMI Input Port 0
RX10+	IN	Differential Data Input Pair1 for HDMI Input Port 0
RX20-	IN	Differential Data Input Pair2 for HDMI Input Port 0
RX20+	IN	Differential Data Input Pair2 for HDMI Input Port 0
RXC1-	IN	Differential Clock Input Pair for HDMI Input Port 1
RXC1+	IN	Differential Clock Input Pair for HDMI Input Port 1
RX01-	IN	Differential Data Input Pair0 for HDMI Input Port 1
RX01+	IN	Differential Data Input Pair0 for HDMI Input Port 1
RX11-	IN	Differential Data Input Pair1 for HDMI Input Port 1
RX11+	IN	Differential Data Input Pair1 for HDMI Input Port 1
RX21-	IN	Differential Data Input Pair2 for HDMI Input Port 1
RX21+	IN	Differential Data Input Pair2 for HDMI Input Port 1
RXC2-	IN	Differential Clock Input Pair for HDMI Input Port 2
RXC2+	IN	Differential Clock Input Pair for HDMI Input Port 2
RX02-	IN	Differential Data Input Pair0 for HDMI Input Port 2
RX02+	IN	Differential Data Input Pair0 for HDMI Input Port 2
RX12-	IN	Differential Data Input Pair1 for HDMI Input Port 2
RX12+	IN	Differential Data Input Pair1 for HDMI Input Port 2
RX22-	IN	Differential Data Input Pair2 for HDMI Input Port 2
RX22+	IN	Differential Data Input Pair2 for HDMI Input Port 2
EXT_RES	IN	External Termination Resistor for all HDMI Input Ports. A resistor should tie this pin to AVDD33. 470Ω is recommended.

Table 2-2 HDMI Output Ports

Name	In/Out	Description
TXC-	OUT	Differential Clock Output Pair for HDMI Output
TXC+	OUT	Differential Clock Output Pair for HDMI Output
TX0-	OUT	Differential Data Output Pair0 for HDMI Output
TX0+	OUT	Differential Data Output Pair0 for HDMI Output
TX1-	OUT	Differential Data Output Pair1 for HDMI Output
TX1+	OUT	Differential Data Output Pair1 for HDMI Output
TX2-	OUT	Differential Data Output Pair2 for HDMI Output
TX2+	OUT	Differential Data Output Pair2 for HDMI Output
SWING	Analog	Voltage Swing Adjust for HDMI Output. A resistor should tie this pin to PVDD18. This resistance determines the amplitude of the voltage swing. 390Ω is recommended.
COMR	Analog	Common ground for pull-down resistors of HDMI Data Output

Table 2-3 ARC RX Pins

Name	In/Out	Description
ARC+/-	IN/OUT	AC coupled ARC input pins

Table 2-4 Audio Inputs/Outputs

Name	In/Out	Description
MCLK	OUT	System Clock output for audio DAC (128/256/384/512 * $F_{Sampling\_Clock}$). Connecting a pull-up (logic 1) or pull-down (logic 0) resistor at this pin defines bit 4 of the slave IIC Address
IIS_SCK	OUT	IIS SCK output for IIS audio port. Sampling clock output for DSD.
IIS_WS	OUT	IIS WS output for all IIS audio ports. DSD audio output port 0 (Right Channel).
IIS_SD0	OUT	IIS SD output for audio port 0 or HBR audio output. DSD audio output port 0 (Left Channel).
IIS_SD1	OUT	IIS SD output for audio port 1 or HBR audio output. DSD audio output port 1 (Right Channel).
IIS_SD2	OUT	IIS SD output for audio port 2 or HBR audio output. DSD audio output port 1 (Left Channel).
IIS_SD3	OUT	IIS SD output for audio port 3 or HBR audio output. DSD audio output port 2 (Right Channel).
SPDIF	OUT	SPDIF output. DSD audio output port 2 (Left Channel).
IIS_SCK_IN	IN	IIS SCK input for regenerated IIS audio.
IIS_WS_IN	IN	IIS WS input for regenerated IIS audio.
IIS_SD_IN	IN	IIS SD input for regenerated IIS audio.

Table 2-5 DDC/IIC/MCU/EEPROM

Name	In/Out	Description
INTb	OUT	Interrupt signal. Asserted when interrupt requests occur. This pin is open drain output when programmed as active low and external pull-up resistor is needed. This pin is push-pull when programmed as active high. Connect this pin to the GPIO pin of the HDMI controller externally.
SCL2/SCL3	IO	SCL signal for HDMI and HDCP Control Logic. Connect this pin to the GPIO pin of the HDMI controller with pull up resistor externally.
SDA2/SDA3	IO	SDA signal for HDMI and HDCP Control Logic. Connect this pin to the GPIO pin of the HDMI controller with pull up resistor externally.
DDC0_SCL	IN	IIC SCL signal for HDMI Receiver DDC Port 0
DDC0_SDA	IO	IIC SDA signal for HDMI Receiver DDC Port 0
DDC1_SCL	IN	IIC SCL signal for HDMI Receiver DDC Port 1
DDC1_SDA	IO	IIC SDA signal for HDMI Receiver DDC Port 1
DDC2_SCL	IN	IIC SCL signal for HDMI Receiver DDC Port 2
DDC2_SDA	IO	IIC SDA signal for HDMI Receiver DDC Port 2
DDCR_SCL	IN	IIC SCL signal for Repeater DDC Port
DDCR_SDA	IO	IIC SDA signal for Repeater DDC Port
DDCT_SCL	OUT	IIC SCL signal for HDMI Output DDC Port
DDCT_SDA	IO	IIC SDA signal for HDMI Output DDC Port

Table 2-6 Misc. Pins

Name	In/Out	Description
X_IN	Analog	External Crystal Input, 18.432 Mhz. Connect this pin to the GPIO pin of the HDMI controller externally.
PLL_XFC_A	Analog	For connecting a capacitor to ground for on-chip PLL
EXT_RSTb	IN	External Reset input (Active Low) with internal weak pull-up. Connect this pin to the GPIO pin of the HDMI controller externally.
REG_VIN	PWR	5V input to on-chip Power Regulator
REG_VO1	OUT	Programmable voltage output from on-chip Power Regulator. The selectable output voltage are 2.8V, 3.0V, 3.2V and 3.4V
REG_VO2	OUT	Programmable voltage output from on-chip Power Regulator. The selectable output voltage are 1.5V, 1.6V, 1.7V and 1.8V

Table 2-7 HDMI Controller Pins[1]

Name	In/Out	Description
MCU_RSTb	IN	External Reset (active low) with on-chip pull-up. When this pin is asserted low, the HDMI controller is totally reset.
MCU_OP	IN	HDMI Controller operation mode. 0: Normal mode 1: ICP (In Circuit Flash Programming) mode
MCU_XIN	IN	External Crystal Input, 18.432 Mhz
MCU_XOUT	OUT	External Crystal Output, 18.432 Mhz.
P2[7:0]	IN/OUT	GPIO port 2 with programmable Open Drain capability.

Table 2-7 HDMI Controller Pins[1]

Name	In/Out	Description
P1[4:0]	IN/OUT	GPIO port 1 or Keyboard Interrupt inputs with internal 20KΩ pull-up to VDD
P3[7:4, 1:0]	OD IN/OUT	Open Drain I/O port 3. P3 shared with IIC.
P4[5, 1:0]	IN/OUT	GPIO port 4 or External Interrupt inputs
P7[1:0]	IN/OUT	Open Drain I/O port 7. P7[1:0] shared with Serial Port.

NOTES:

1. Customer shall follow the pre-defined I/O pins application which shown in reference circuit for the correct operation of this chip.

Table 2-8 Power Pins

Name	In/Out	Description
AVDD	PWR	HDMI Receiver Analog Power (1.8V)
PVDD	PWR	HDMI Receiver PLL Analog Power (1.8V)
AVDD33	PWR	HDMI Termination Power (3.3V)
AVDD18	PWR	HDMI Transmitter Analog Power (1.8V)
PVDD18	PWR	HDMI Transmitter PLL Analog Power (1.8V)
AVSS, PVSS	GND	Analog Ground
VDDE	PWR	I/O Power (3.3V)
VSSE	GND	I/O Ground
VDD	PWR	Internal Logic Power (1.8V)
VSS	GND	Logic Ground
VDD_PLL	GND	Audio PLL Power (3.3V)
VSS_PLL	GND	Audio PLL Ground
MCU_VDD	GND	HDMI Controller Power (3.3V)

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	-0.3		4.0	V
Vcc18	1.8V Supply Voltage	-0.3		2.5	V
Vcc_REG	Embedded Regulator Supply Voltage	-0.3		5.7	V
V_I	Input Voltage	-0.3		V_{cc33} + 0.3	V
V_O	Output Voltage	-0.3		V_{cc33} + 0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-40		125	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)[1]		39.9		°C/W
θ_{JC}	Thermal Resistance (Junction to Case)[1]		13.1		°C/W

NOTES:
1. Analyzed by FEM (Finite Element Modeling) method with chip mounted on 4-layers PCB.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	3.14	3.3	3.6	V
Vcc18	1.8V Supply Voltage	1.71	1.8	1.98	V
Vcc_REG	Embedded Regulator Supply Voltage	4.5	5.0	5.5	V
V_{CCN}	Supply Voltage Noise	-0.3		100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REG_VO1}	Output Voltage of REG_VO1	Loading <= 30mA	2.6		3.6	V
V_{REG_VO2}	Output Voltage of REG_VO2	Loading <= 20mA	1.45		1.98	V
I_{REG_VO1}	Output Current of REG_VO1				30	mA
I_{REG_VO2}	Output Current of REG_VO2				20	mA
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V

V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	uA

DC Analogue Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak to peak amplitude	R_{LOAD} = 50 ohm R_{SWING} = 390 ohm		510	550	590	mV
V_{DOH}	Differential High-level Output Voltage[1]				AVCC		V
I_{DOS}	Differential Output Short Circuit Current	V_{OUT} = 0V; TX_TERM bit is 0				5	uA
I_{PD}	Power-Down Current[2] (25°C Ambient, REG_VO1 is not connected, MCU stay in STOP mode)	RSEN_DIS = 0	3V3		150		uA
			1V8		20		uA
		RSEN_DIS = 1	3V3		18		uA
			1V8		20		uA
I_{CCD}	Supply Current (25°C Ambient, RX0/TX are Active R_{EXT_RES} = 470 ohm, R_{EXT_SWING} = 390 ohm, TX_TERM bit is 0)	1080p Resolution (12-bit)	3V3		85		mA
			1V8		454		mA

1 Guaranteed by design.

2 Assumes all HDMI/DVI I/O ports are not connected and all digital inputs are silent.

Receiver AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]				0.4	T_{bit}
T_{CCS}	Channel to Channel Differential Input Skew[1]				1.0	T_{pixel}
T_{IJIT}	Differential Input Clock Jitter Tolerance[2,3]				0.3	T_{bit}
F_{CIP}	TMDS CLK Frequency		25		225	MHz

NOTES:

1. Guaranteed by design.
2. Jitter defines as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electronic Measurement Procedures*

Transmitter AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
S_{LHT}	Differential Swing Low-to-High Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm, R_{EXT_SWING} = 270 ohm	170	200	230	ps
S_{HLT}	Differential Swing High-to-Low Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm, R_{EXT_SWING} = 270 ohm	170	200	230	ps

I2S Audio AC Specifications (under normal operating conditions unless otherwise specified)

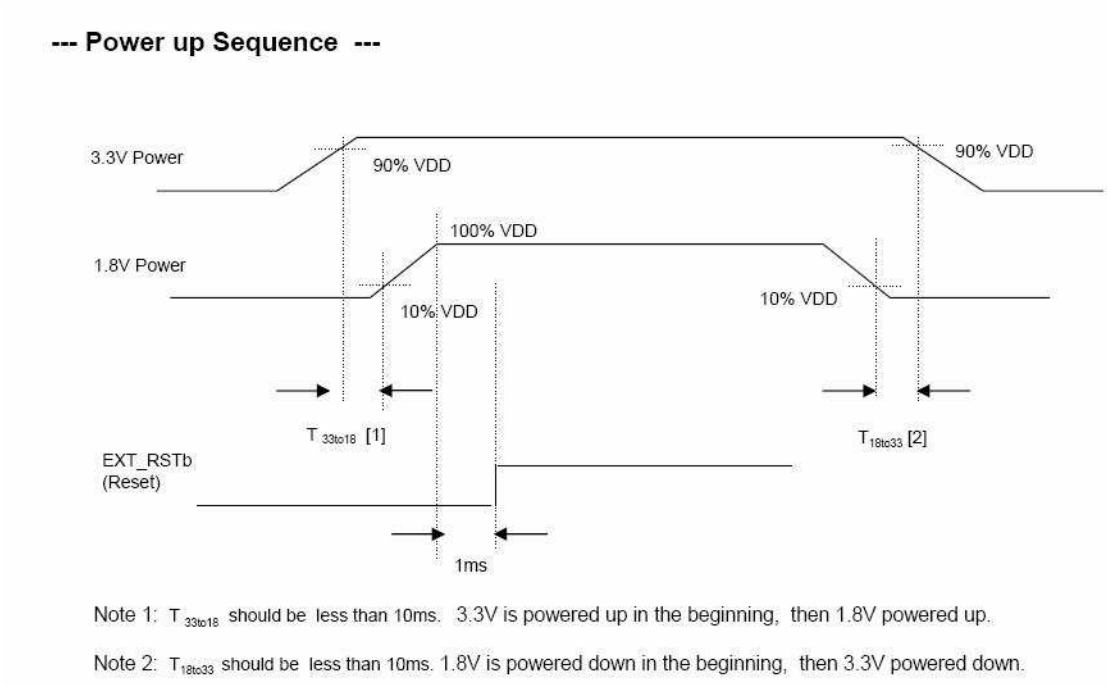
Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{sck}	SCK Clock Period	C_L = 10pF		1		T_{sck}
T_{sck_d}	SCK Clock Duty Cycle	C_L = 10pF	40%		60%	T_{sck}
T_{sck_h}	SCK Clock High Time	C_L = 10pF	40%		60%	T_{sck}
T_{sck_l}	SCK Clock LOW Time	C_L = 10pF	40%		60%	T_{sck}
T_{iis_s}	SCK to SD and WS (Setup Time)	C_L = 10pF	40%		-	T_{sck}
T_{iis_h}	SCK to SD and WS (Hold Time)	C_L = 10pF	40%		-	T_{sck}

SPDIF Audio AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{spdif}	SPDIF Cycle Time	C_L = 10pF		1		UI
T_{spdif_d}	SPDIF Duty Cycle	C_L = 10pF	90%		110%	UI

2.5 Power Up Sequence

Following figure shows the recommended power on sequence to EP92A2E:



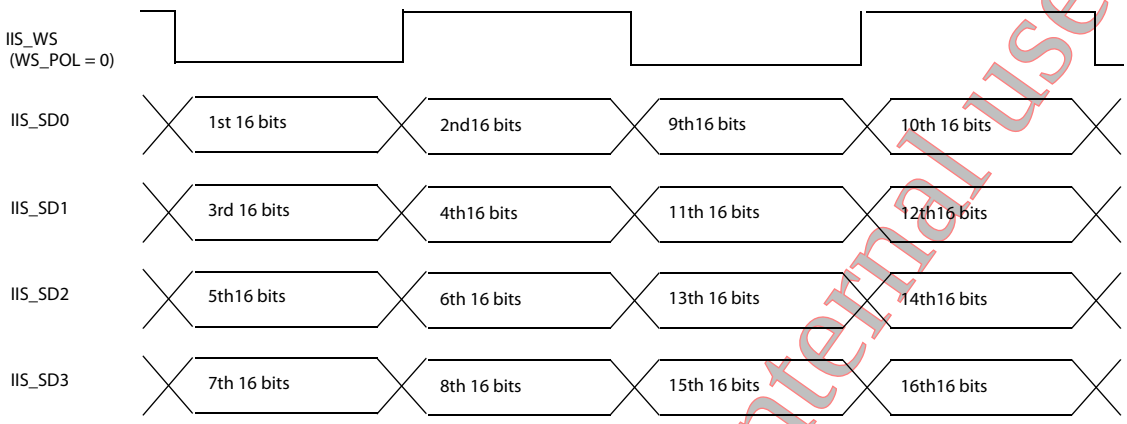
Note 1: T_{33to18} should be less than 10ms. 3.3V is powered up in the beginning, then 1.8V powered up.

Note 2: T_{18to33} should be less than 10ms. 1.8V is powered down in the beginning, then 3.3V powered down.

2.6 HBR Audio Input Format

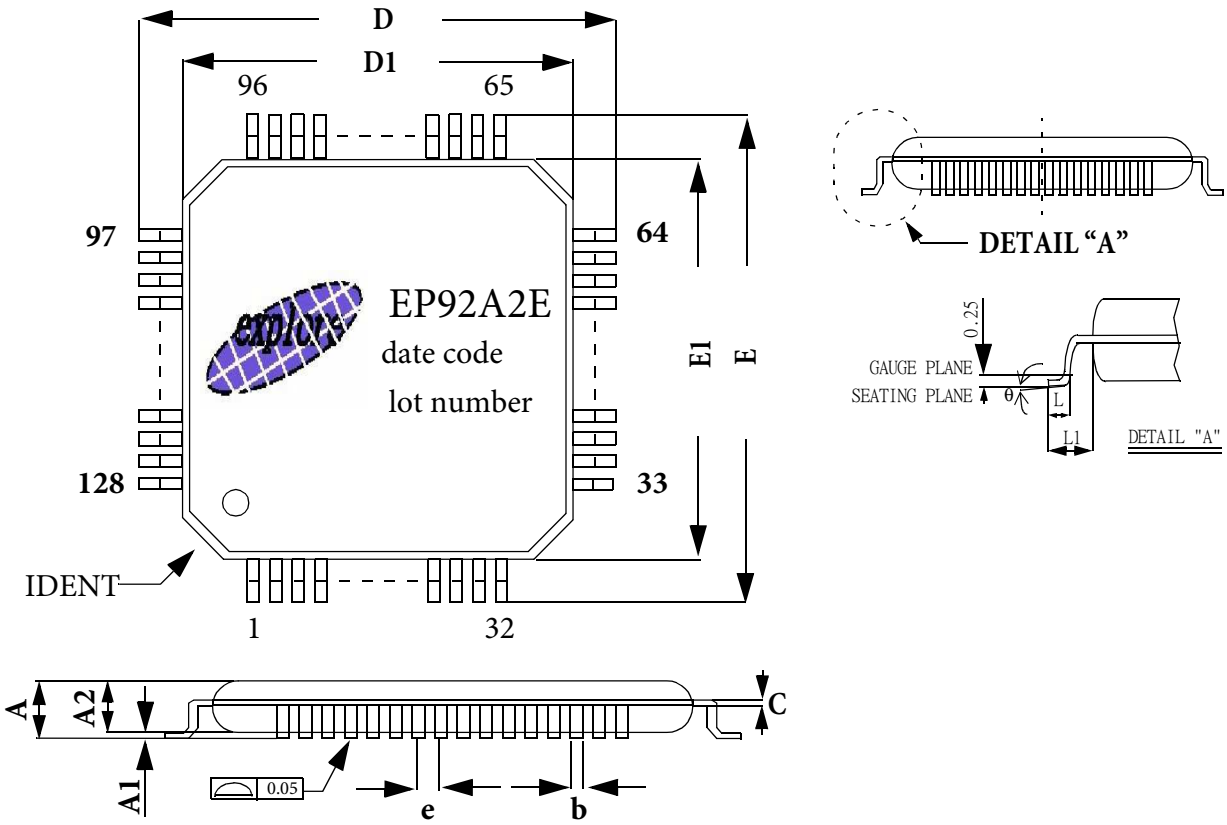
HBR (True HD High Bit Rate) audio is output from IIS pins as shown in the following figure:

Figure 2-3 HBR Audio Output Format



Appendix A Package

Figure A-1 EP92A2E Footprint Diagram



Footprint Variations (mm)

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.6
A1	0.05	0.1	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
C	0.09	-	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0"	3.5"	7"

NOTES:
1. JEDEC OUTLINE : N/A
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

Appendix A EP92A2E Application Guideline

This application note describes the guideline for the system designer to follow while preparing the application circuit and PCB layout in order to achieve the best performance of the EP92A2E.

A.1 GENERIC DESIGN GUIDELINE

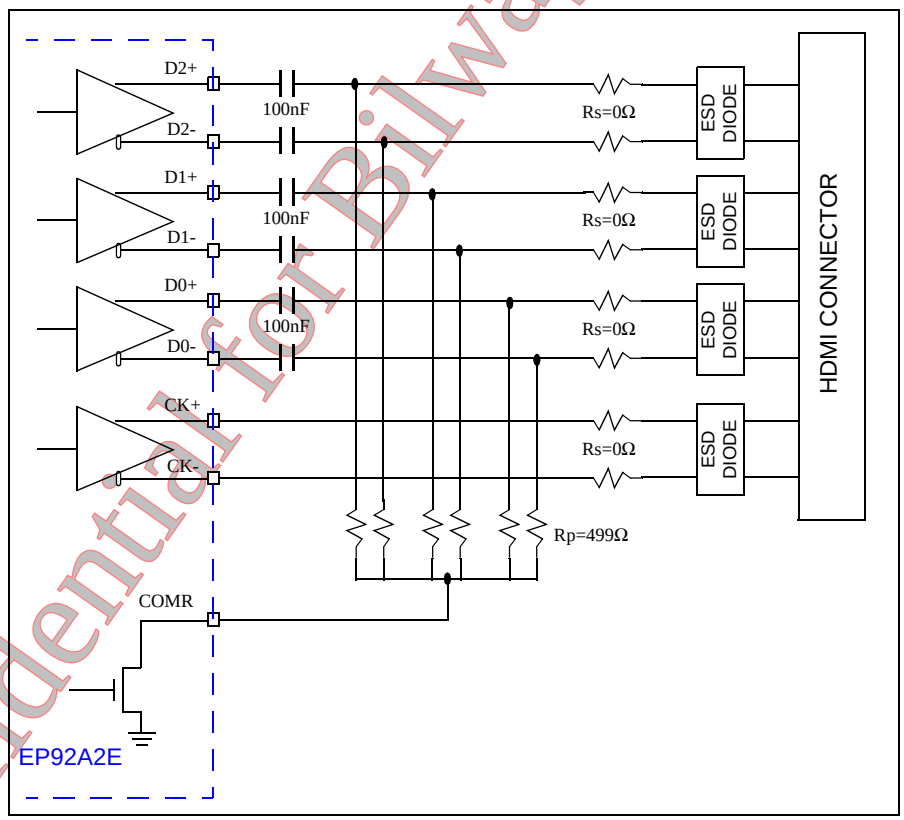
A.1.1 HDMI Receiver

- For receiver input, each differential pair shall be routed symmetrically. Also, the best performance will be expected if the differential pair is equal length. The maximum difference of the trace length between D+ and D- (intra-pair) is 12 mil.
- The receiver module can tolerate the skew among different pairs (inter-pair skew). Anyway, user can limit the maximum difference of the trace length among different pairs (inter-pair) to 150 mil.

A.1.2 HDMI Transmitter

The transmitter uses the new AC-coupling mechanism at its differential data output. The block diagram of the recommended transmitter output connection is shown in the following figure.

Figure A-1 Transmitter Output Connection



- The 100nF capacitor to implement the AC-coupling mechanism is needed for the EP92A2E TMDS differential data output. The differential clock output still keeps the DC-coupling mechanism.
- The 499Ω (Rp) pull down resistor for each differentail data output signal is needed for keeping the DC voltage to the TMDS connector output to be 3V3.
- In order to provide the higher level of the ESD protection in the HDMI TX output, a serial resistor (Rs) can be added between the external ESD device and the silicon HDMI transmitter output pad. The typical value of the serial resistor could be set to 0Ω first.
- For transmitter output, each differential data pair shall be routed symmetrically. The best performance will be expected if the differential data pairs are equal length. The maximum trace difference will depends on the connected receiver characteristics. In practice, try to minimize of the trace length differences of the intra-pair and inter-pairs of the differential data lines.
- For the best intra-pair skew between the single-ended CLK+ output and single-ended CLK- output, it is recommended to route the CLK+ with the trace length longer than CLK- for 400 mil to 600 mil. Keep the area of the CLK+ and CLK- current loop to have the minimum area while routing the additional trace of the CLK+ signal.
- Minimize the length from the HDMI TX pins to the HDMI connector. If possible, keep the length less than 1500 mil.

A.1.3 Embedded Regulator

The EP92A2E embeds two regulators to generate 3V3 and 1V8 voltage for its own use. The output of the embedded regulator can not be used for the other purpose. The regulator input is supplied from the +5V of the HDMI input connector. The low ESR capacitor shall be used and placed closely to the regulator output pin. The minimum capacitance of the low ESR capacitor is 1uF. The schotty diodes are needed to isolate the possible reverse current among different supplied power.

A.1.4 GENERIC LAYOUT GUIDELINE

- PVDD for TMDS transmitter (pin 63) shall be applied with the clean power, the common practice is to supply the power through the ferrite bead. The best practice is to provide the PVDD through the individual regulator. The minimum requirement is to follow the reference circuit to supply the power to PVDD.
- In order to provide a desirable return path for current, the solid ground plane is necessary. Also, connect the power and ground pins and all bypass capacitors to the appropriate power and ground plane with a via. Via is suggested to be as fat and as short as possible in order to reduce the inductance.
- Place one 0.1uF capacitor as close as possible between each power pin and ground. A bulk decoupling capacitor should be placed on the sub-plane of the power. Additional capacitors may be needed depending on the PCB design.
- Control the PCB impedance of all differential traces (both receiver and transmitter) to be 100Ω. This will be one of the critical points for the system performance at very high frequency operation. Following items are listed based on our experience:

  - If possible, the differential traces shall be routed on the TOP layer and the continuous ground plane shall be placed beneath the differential traces. The discontinuous ground plane will degrade the high speed differential signal integrity.
  - The ground traces stay with the differential traces on the same layer are not suggested.
  - Keep any TTL signals away from the differential traces as far as possible.
  - Avoid the differential traces cornering, crossing and the through holes.
- Choose the discrete ESD protection devices with the very low capacitance, the Semtech RClamp0524P or CMD (California Micro Devices) CM2020 is recommended. Place the ESD devices close to the HDMI connector for the best performance.
- Following diagram shows the differential traces routing example: