Low Power DVI/HDMI Transmitter

EP932M

User Guide

V0.1

Revised: May 21, 2009

Original Release Date: May 20, 2009

Explore

Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	May/20/2009	Ether Lai	Initial Version
0.1	May/21/2009	Ether Lai	Revise Feature List;

Section 1 Introduction

1.1 Overview

EP932M is an Low Power HDMI (High Definition Multimedia Interface) transmitter suitable for portable applications. The chip is compliant with HDMI Rev 1.3 and HDCP Rev 1.2 specifications. The chip converts input video data in RGB or YUV format and audio data in SPDIF or IIS format into HDMI differential signals. The chip supports display resolution from up to 720p/1080i and 1080p with a highly flexible interface with either a 12-bits mode or 24-bit mode input. In both modes, the chip supports single or dual edge clocking.

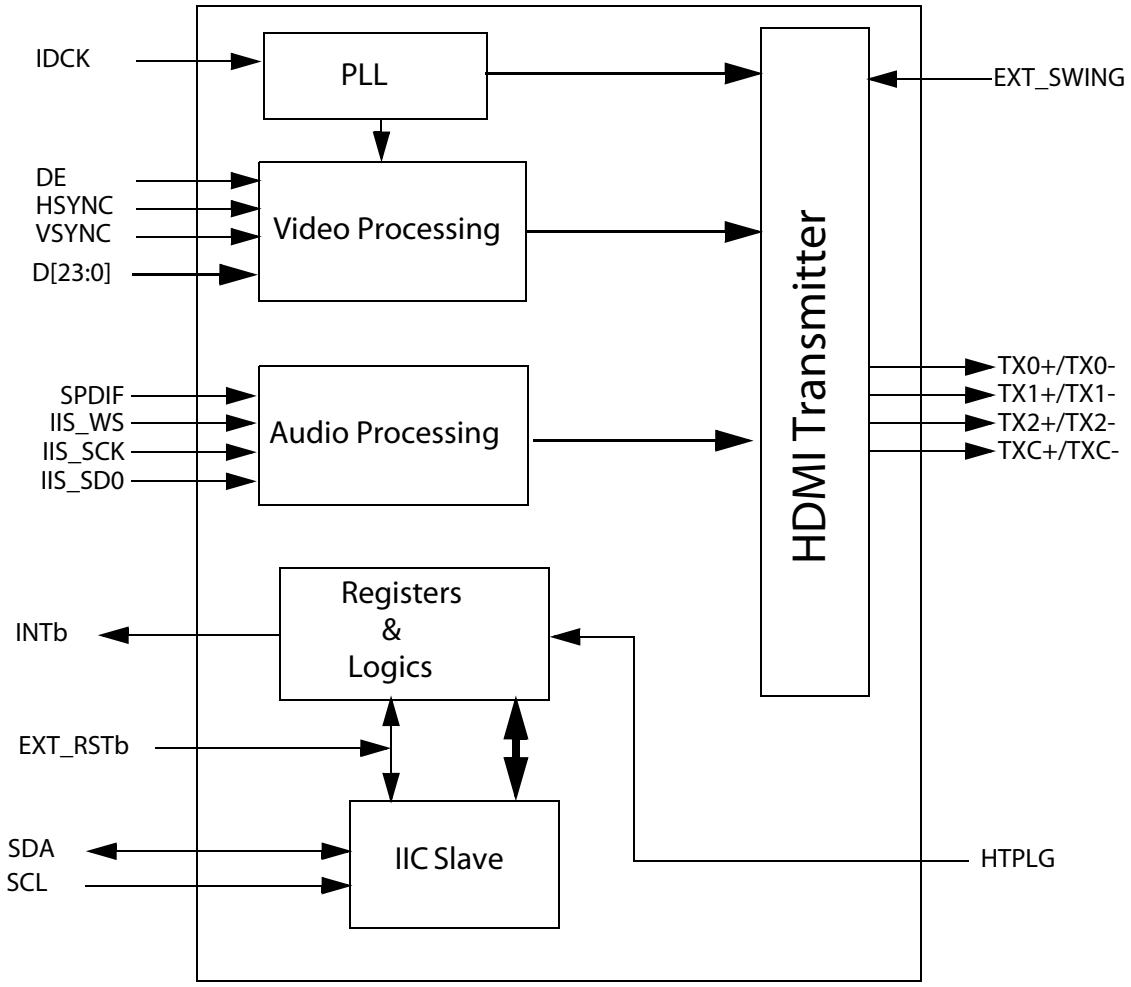
1.2 Features

- HDMI Specification 1.3 Compliant
- Integrated HDCP encryption engine which is compliant with HDCP Rev 1.2 Specification
- HDCP keys are downloadable from external MCU
- Wide Frequency Range: 25MHz - 165MHz
- Flexible Graphic Controller Interface: 12-bit and 24-bit mode in RGB or YUV, embedded sync or separate sync
- Support SPDIF audio input (with or without system clock) or 1 port of IIS audio input
- SPDIF system clock input is not required
- Supports audio down sampling at 1/2, 1/3 or 1/4 sampling rate for both SPDIF and IIS
- Supports CCIR YUV422 format input
- On-chip YUV422 to YUV444 conversion and YUV444 to YUV422 conversion
- On-chip YUV to RGB and RGB to YUB conversion in ITU-R BT.601 and 709 color space
- Programmable Single/Dual Edge Clocking Mode
- IIC Slave Programming Interface
- Programmable DE generation
- Supports x2, x4 and x8 Pixel Repetition
- Supports input De-Skewing
- Supports Receiver Hot Plug Detection and Receiver Connection Detection
- Downward compatible with DVI 1.0
- Supports Power Down Mode
- Flexible Supplied Power for System Design
- 64-Pin LQFP (7mm x 7mm)

Section 2 Overview

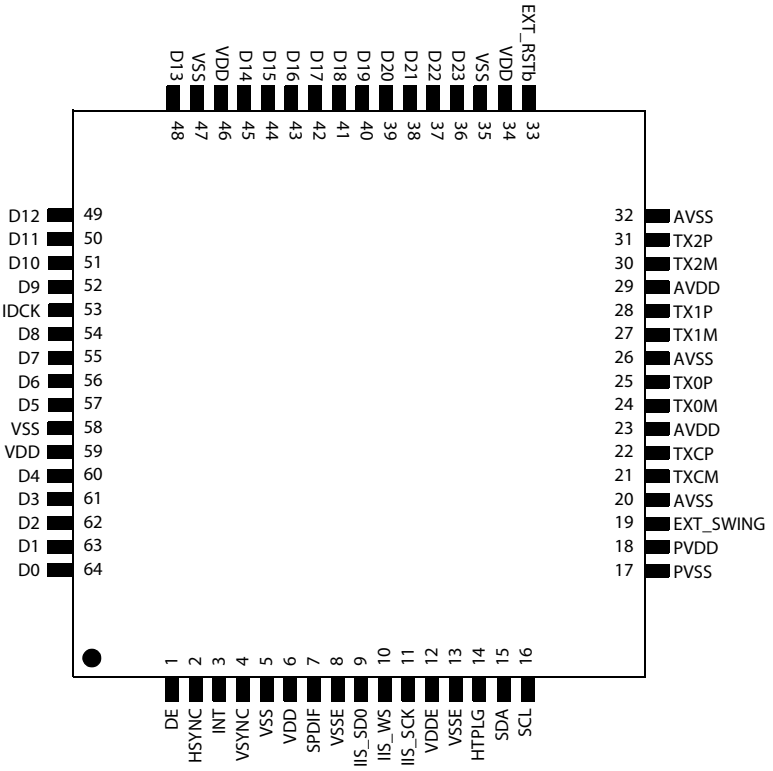
2.1 Block Diagram

Figure 2-1 Block Diagram



2.2 Pin Diagram (LQFP-64)

Figure 2-2 Pin Diagram (LQFP-64)



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 Input Control/Data/CLK Pins

NAME	IN / OUT	DESCRIPTION
D23 - D12	IN	Top half of 24-bit pixel bus When BSEL = HIGH, this bus inputs the top half of the 24-bit pixel bus When BSEL = LOW, these bits are not used to input pixel data. In this mode, the state of D[23:16] is input to the IIC register CFG. This allow 8-bits of user configuration data to be read by the graphics controller through the IIC interface. D[15:12] are not used and should be tied to GND.
D11 - D0	IN	Bottom half of 24-bit pixel bus / 12-bit pixel bus input When BSEL = HIGH, this bus inputs the bottom half of the 24-bit pixel bus When BSEL = LOW, this bus inputs 1/2 a pixel (12-bits) at every latch edge (both falling and/or rising) of the clock.
IDCK	IN	Input Data Clock
DE	IN	Data Enable Input. This signal is high when input pixel data is valid to the transmitter and low otherwise. It is critical that this signal have the same setup/hold timing as the data bus.
HSYNC	IN	Horizontal Sync Input.
VSYNC	IN	Vertical Sync Input.

Table 2-2 Status Pins

NAME	IN / OUT	DESCRIPTION
HTPLG	IN	Hot Plug Input. This pin is used to monitor the "HOT PLUG" signal. Note: This input is 5V tolerant.
INT	OUT	Interrupt. This pin is an open drain or push-pull output with weak pull-up (100K ohm). The output polarity and interrupt source are programmable through the IIC interface.

Table 2-3 Audio Input Pins

NAME	IN / OUT	DESCRIPTION
SPDIF	IN	SPDIF input for audio channel 0
IIS_SCK	IN	IIS SCK input for all audio channels
IIS_WS	IN	IIS WS input for all audio channels
IIS_SD0	IN	IIS SD input for audio channel 0

Table 2-4 IIC Pins

NAME	IN / OUT	DESCRIPTION
SCL	IN	IIC SCL signal for register programming
SDA	IO	IIC SDA signal for register programming (open drain)

Table 2-5 Misc. Pins

NAME	IN / OUT	DESCRIPTION
EXT_RSTb	IN	External Reset (Active LOW). A HIGH level indicates normal operation and a LOW level causes all the logic on the chip to be reset. This pin has to be set to LOW before the input video timing signals are not stable.

Table 2-6 Differential Signal Data Pins

NAME	IN / OUT	DESCRIPTION
TX0- TX0+ TX1- TX1+ TX2- TX2+	Analog	Differential Data Output Pairs.
TXC+ TXC-	Analog	Differential Clock Output Pairs.
EXT_SWING	Analog	Voltage Swing Adjust. A resistor should tie this pin to AVCC. This resistance determines the amplitude of the voltage swing. 330Ω is recommended.

Table 2-7 Power and Ground Pins

NAME	IN / OUT	DESCRIPTION
VDDE	PWR	Digital IO Power; voltage range: 1.71V ~ 3.6V; set to 2V5 typically
VSSE	GND	Digital IO Ground
VDD	PWR	Digital Core Power; voltage range: 1.71V ~ 1.9V; set to 1V8 typically
VSS	GND	Digital Core Ground
AVDD	PWR	Analog Power for HDMI transmitter; voltage range: 2.2V ~ 3.6V; set to 2V5 typically
AVSS	GND	Analog Ground for HDMI transmitter
PVDD	PWR	Analog Power for PLL; voltage range: 2.2V ~ 3.6V; set to 2V5 typically
PVSS	GND	Analog Ground for PLL

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{ANA_IO}	Analog & IO Supply Voltage	-0.3		4.0	V
V_{CORE}	Core Supply Voltage	-0.3		2.5	V
V_I	Input Voltage	-0.3		V_{cc} + 0.3	V
V_O	Output Voltage	-0.3		V_{cc} + 0.3	V
T_J	Junction Temperature			125	℃
T_{STG}	Storage Temperature	-40		125	℃
P_{PD}	Package Power Dissipation			1	W

1 Permanent device damage may occur if absolute maximum conditions are exceeded.

2 Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DDN}	Supply Voltage Noise			50	mV_{p-p}
V_{CVCC}	Power of Digital Core Logic	1.71	1.8	1.9	V
V_{VDDE}	Power of Digital I/O Cell	1.71	2.5	3.6	V
V_{AVDD}	Power of HDMI TX PHY	2.2	2.5	3.6	V
T_A	Ambient Temperature (with power applied)	0	25	70	℃

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		V_{CC} - 0.4			V
V_{IL}	Low-level Input Voltage				0.4	V
V_{CINL}	Input Clamp Voltage	I_{CL} = -10mA	- 0.8			V
V_{CIPL}	Input Clamp Voltage	I_{CL} = 10mA			V_{CC} + 0.8	V
I_{IL}	Input Leakage Current		-10		10	uA

DC Analogue Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak to peak amplitude	R_{LOAD} = 50 ohm R_{EXT_SWING} = 330 ohm		510	550	590	mV
V_{DOH}	Differential High-level Output Voltage				AVDD		mV
I_{PD}	Power-Down Current	25°C Ambient	1V8 (CVCC)		300		uA
			2V5 (VDDE, AVDD)		580		uA
			Watt		2.57		mW
I_{CCD}	Transmitter Supply Current 1080i (DCLK=74.25MHz, 25°C Ambient, 1 pixel/clock, R_{EXT_SWING} = 330 Ω)	Typical Case Pattern[1]	1V8 (CVCC)		26		mA
			2V5 (VDDE, AVDD)		26.5		mA
			Watt		114		mW
		Worst Case Pattern[2]	1V8 (CVCC)		31.5		mA
			2V5 (VDDE, AVDD)		26.7		mA
			Watt		124		mW
	Transmitter Supply Current 1080p (DCLK=148.5MHz, 25°C Ambient, 1 pixel/clock, R_{EXT_SWING} = 680 Ω)	Typical Case Pattern[1]	1V8 (CVCC)		39		mA
			3V3 (VDDE, AVDD)		44		mA
			Watt		216		mW
		Worst Case Pattern[2]	1V8 (CVCC)		43		mA
			3V3 (VDDE, AVDD)		45		mA
			Watt		226		mW

NOTES:
1. The typical Pattern contains a gray scale area, checkerboard area and text
2. Black and white checkerboard pattern, each checker is one pixel wide.

AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{CIP}	IDCK Period, 1-pixel/clock		6.06		40	ns
F_{CIP}	IDCK Frequency, 1-pixel/clock		25		165	MHz
T_{CIH}	IDCK High Time at 165MHz		2.0			ns
T_{CIL}	IDCK Low Time at 165MHz		2.0			ns
T_{IJIT}	Worst Case IDCK Clock Jitter[2,3]				2	ns
T_{SIDF}	Data, DE VSYNC, HSYNC Setup Time to IDCK falling edge	Single Edge (DSEL=0, DKEN=0, EDGE=0)	1.0			ns

T_{HIDF}	Data, DE VSYNC, HSYNC Hold Time to IDCK falling edge	Single Edge (DSEL=0, DKEN=0, EDGE=0)	0.9			ns
T_{SIDR}	Data, DE VSYNC, HSYNC Setup Time to IDCK rising edge[1]	Single Edge (DSEL=0, DKEN=0, EDGE=1)	1.0			ns
T_{HIDR}	Data, DE VSYNC, HSYNC Hold Time to IDCK rising edge[1]	Single Edge (DSEL=0, DKEN=0, EDGE=1)	0.9			ns
T_{SID}	Data, DE VSYNC, HSYNC Setup Time to IDCK falling/rising edge[1]	Dual Edge (DSEL=1, DKEN=0, EDGE=0)	0.6			ns
T_{HID}	Data, DE VSYNC, HSYNC Hold Time to IDCK falling/rising edge[1]	Dual Edge (DSEL=1, DKEN=0, EDGE=0)	1.3			ns
T_{DDF}	VSYNC, HSYNC delay from DE falling edge[1]		$1T_{CIP}$			ns
T_{DDR}	VSYNC, HSYNC delay from DE rising edge[1]		$1T_{CIP}$			ns
T_{HDE}	DE High Time[1]	Vertical Blanking Only			$8191T_{CIP}$	ns
T_{LDE}	DE Low Time[1,4]	Vertical Blanking Only	$128T_{CIP}$			ns
T_{STEP}	De-skew step size increment	DKEN = 1		260		ps
S_{LHT}	Differential Swing Low-to-High Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm, R_{EXT_SWING} = 510 ohm	170	200	230	ps
S_{HLT}	Differential Swing High-to-Low Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm, R_{EXT_SWING} = 510 ohm	170	200	230	ps

Figure 2-3 Clock Cycle and High/Low Timing Definition

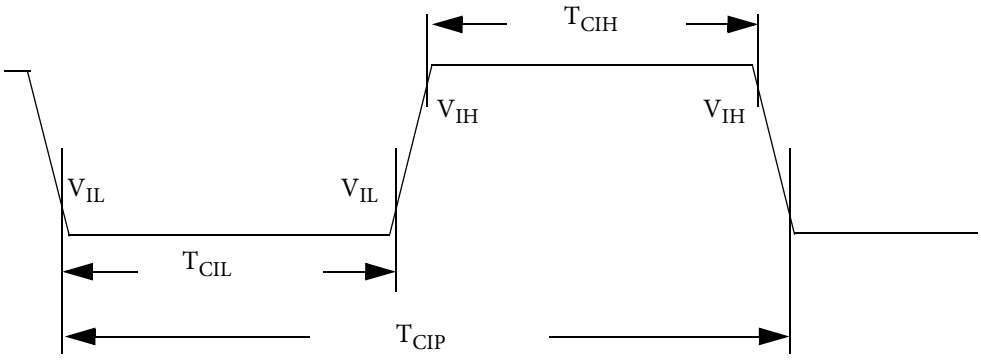


Figure 2-4 Single-Edge Clock to Data Setup/Hold Timing Definition

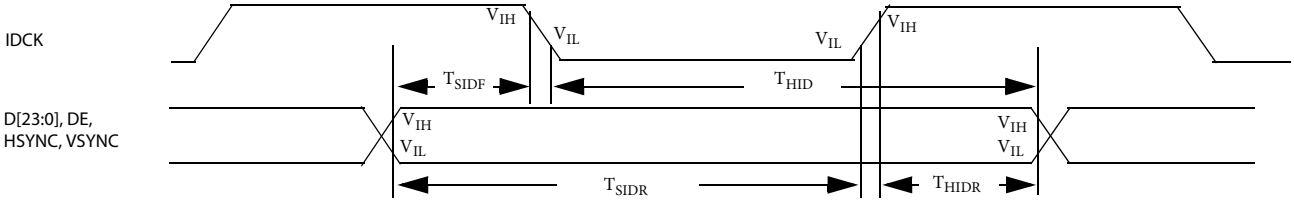


Figure 2-5 Dual-Edge Clock to Data Setup/Hold Timing Definition

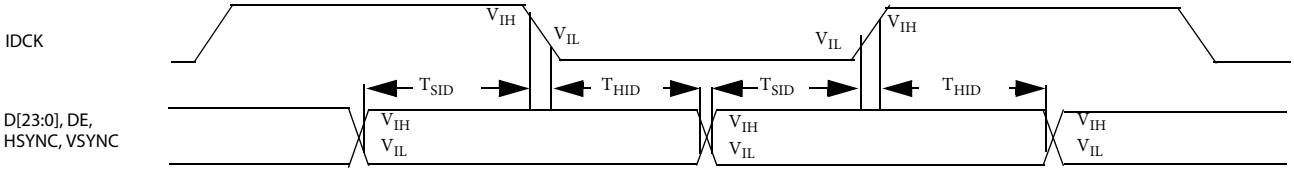


Figure 2-6 DE to HSYNC/VSYNC Delay Timing Definition

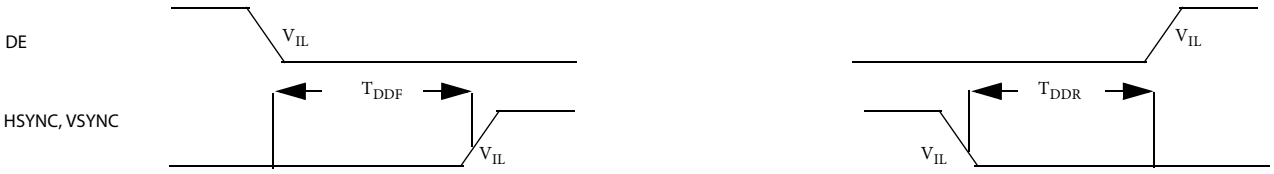


Figure 2-7 DE High/Low Timing Definition

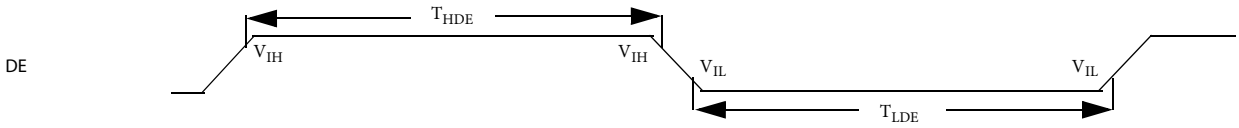
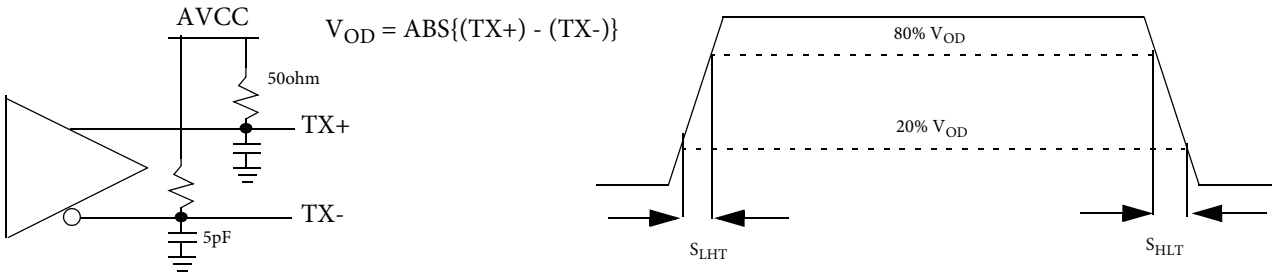


Figure 2-8 Differential Output Timing Definition



2.5 Data De-skew

Input clock to data setup/hold time can be adjusted through the use of the de-skew feature. It should be noted that it is the clock that is being adjusted. When DKEN=1, DK[3:1] can be used to vary the input setup/hold time by an amount T_{CD} given by the formula

$$T_{CD} = (DK[3:1] - 4) \times 200 \text{ ps.}$$

Where

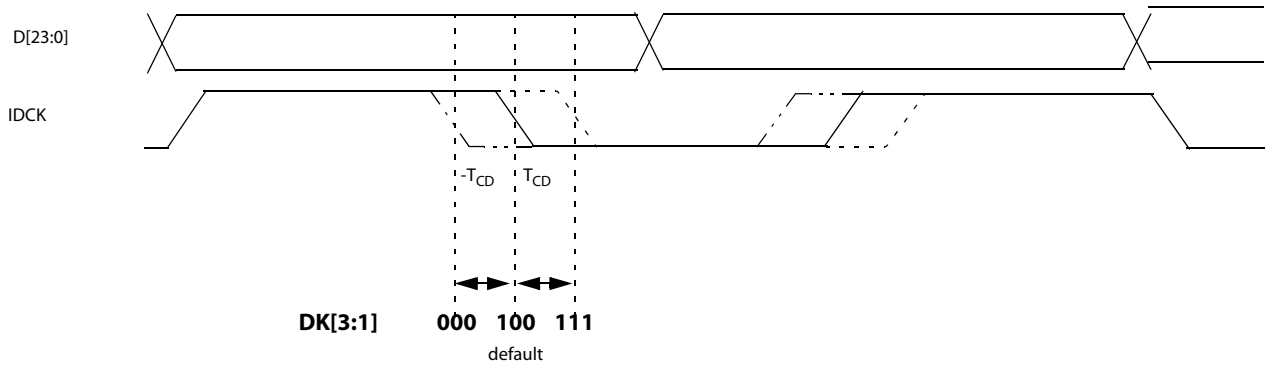
T_{CD} is the amount of setup/hold variation

DK[3:1] is the setting of the de-skew configuration pins or IIC registers

This feature can be used in both 12-bit and 24-bit mode.

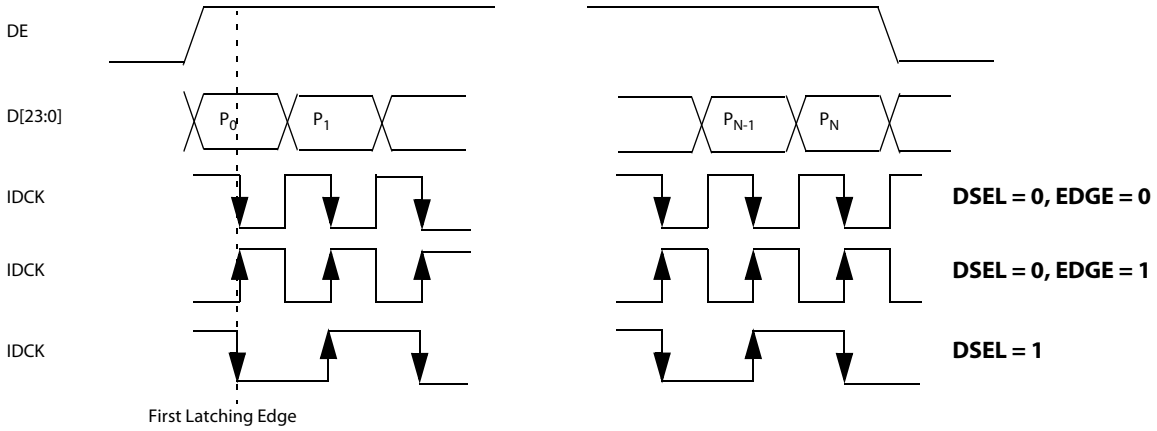
If Data De-skew is disabled, the default setting of T_{CD}=0 is used.

Figure 2-9 Single-Edge Clock to Data Setup/Hold Timing Definition



2.6 24-bit Data Mapping

Figure 2-10 24-bit Single/Dual Clock Edge Setting



Note: In Dual Clock Edge Mode, the transmitter will look at the first clock edge (either falling or rising) after DE goes HIGH to determine the first pixel data. In Embedded Sync mode, DE is extracted from EAV/SAV code according for CCIR-656 standard. EDGE pin has no affect in Dual Clock Edge Mode.

Table 2-8 24-bit Mode Data Mapping (BSEL = 1)[1,2,3]

Pin Name	RGB	YCbCr444	YCbCr422
D23	R[7]	Cr[7]	Cb/Cr[11]
D22	R[6]	Cr[6]	Cb/Cr[10]
D21	R[5]	Cr[5]	Cb/Cr[9]
D20	R[4]	Cr[4]	Cb/Cr[8]
D19	R[3]	Cr[3]	Cb/Cr[7]
D18	R[2]	Cr[2]	Cb/Cr[6]
D17	R[1]	Cr[1]	Cb/Cr[5]
D16	R[0]	Cr[0]	Cb/Cr[4]
D15	G[7]	Cr[7]	Y[11]/EAV[7]/SAV[7]
D14	G[6]	Y[6]	Y[10]/EAV[6]/SAV[6]
D13	G[5]	Y[5]	Y[9]/EAV[5]/SAV[5]
D12	G[4]	Y[4]	Y[8]/EAV[4]/SAV[4]
D11	G[3]	Y[3]	Y[7]/EAV[3]/SAV[3]
D10	G[2]	Y[2]	Y[6]/EAV[2]/SAV[2]
D9	G[1]	Y[1]	Y[5]/EAV[1]/SAV[1]
D8	G[0]	Y[0]	Y[4]/EAV[0]/SAV[0]
D7	B[7]	Cb[7]	Cb/Cr[3]
D6	B[6]	Cb[6]	Cb/Cr[2]
D5	B[5]	Cb[5]	Cb/Cr[1]
D4	B[4]	Cb[4]	Cb/Cr[0]
D3	B[3]	Cb[3]	Y[3]
D2	B[2]	Cb[2]	Y[2]

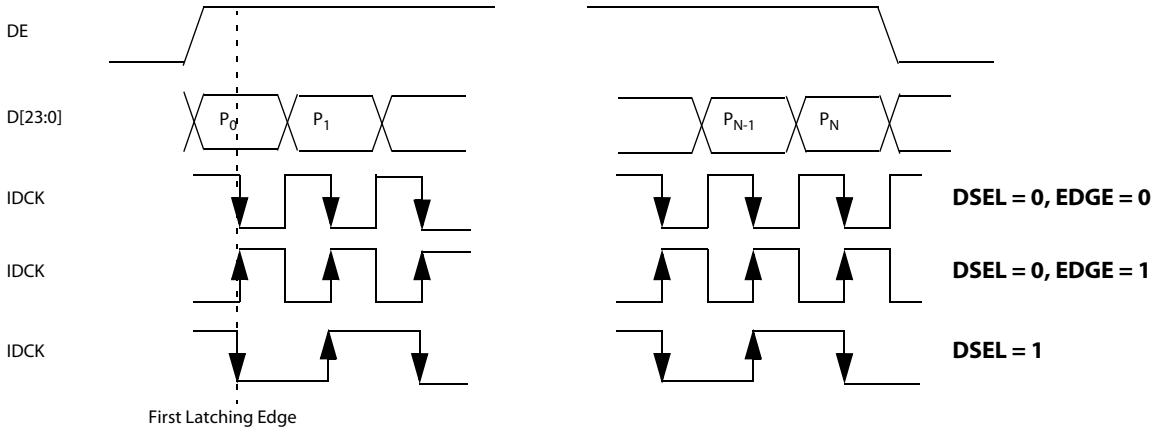
Table 2-8 24-bit Mode Data Mapping (BSEL = 1)[1,2,3]

Pin Name	RGB	YCbCr444	YCbCr422
D1	B[1]	Cb[1]	Y[1]
D0	B[0]	Cb[0]	Y[0]

NOTES:
1. In this figure, clock edges represents by arrows signify the latching edge
2. In 24-bit YCbCr422 input, Cb data comes in first clock edge and Cr data comes in next clock edge
3. For less than 12-bit YCbCr422 input, the MSB data should be connected to input bit [11] and unused low input bits should be connected to logic 0
4. Bit significance with in a pixel component : [7:0] = [MSB:LSB]
5. In embedded sync mode, Hsync, Vsync and DE signals are extracted from EAV/SAV codes according to CCIR 656 standard.

2.7 12-bit Data Mapping

Figure 2-11 12-bit Single/Dual Clock Edge Setting



Note: The clock timing is the same as that in 24-bit mode except that the frequency of latching edge is 2 times of pixel frequency.

Table 2-9 12-bit Mode Data Mapping (BSEL = 0)[1,2,3]

	RGB444(FMT12 = 0)		YCbCr444(FMT12 = 0)		YCbCr422(FMT12 = 1)	
Pin Name	1st clock	2nd clock	1st clock	2nd clock	1st clock	2nd clock
D15	-	-	-	-	Cb/Cr[11]/EAV[7]/SAV[7]	Y[11]/EAV[7]/SAV[7]
D14	-	-	-	-	Cb/Cr[10]/EAV[6]/SAV[6]	Y[10]/EAV[6]/SAV[6]
D13	-	-	-	-	Cb/Cr[9]/EAV[5]/SAV[5]	Y[9]/EAV[5]/SAV[5]
D12	-	-	-	-	Cb/Cr[8]/EAV[4]/SAV[4]	Y[8]/EAV[4]/SAV[4]
D11	G[3]	R[7]	Y[3]	Cr[7]	Cb/Cr[7]/EAV[3]/SAV[3]	Y[7]/EAV[3]/SAV[3]
D10	G[2]	R[6]	Y[2]	Cr[6]	Cb/Cr[6]/EAV[2]/SAV[2]	Y[6]/EAV[2]/SAV[2]
D9	G[1]	R[5]	Y[1]	Cr[5]	Cb/Cr[5]/EAV[1]/SAV[1]	Y[5]/EAV[1]/SAV[1]
D8	G[0]	R[4]	Y[0]	Cr[4]	Cb/Cr[4]/EAV[0]/SAV[0]	Y[4]/EAV[0]/SAV[0]
D7	B[7]	R[3]	Cb[7]	Cr[3]	-	-
D6	B[6]	R[2]	Cb[6]	Cr[2]	-	-

Table 2-9 12-bit Mode Data Mapping (BSEL = 0)[1,2,3]

	RGB444(FMT12 = 0)		YCbCr444(FMT12 = 0)		YCbCr422(FMT12 = 1)	
Pin Name	**1st clock**	**2nd clock**	**1st clock**	**2nd clock**	**1st clock**	**2nd clock**
D5	B[5]	R[1]	Cb[5]	Cr[1]	-	-
D4	B[4]	R[0]	Cb[4]	Cr[0]	-	-
D3	B[3]	G[7]	Cb[3]	Y[7]	Cb/Cr[3]	Y[3]
D2	B[2]	G[6]	Cb[2]	Y[6]	Cb/Cr[2]	Y[2]
D1	B[1]	G[5]	Cb[1]	Y[5]	Cb/Cr[1]	Y[1]
D0	B[0]	G[4]	Cb[0]	Y[4]	Cb/Cr[0]	Y[0]

NOTES:

1. In this figure, clock edges represents by arrows signify the latching edge. The primary latch edge is indicated by the dark rows. The lower half of the pixel (L) is latched by the primary clock edge.
2. In 12-bit YCbCr422 input, Cb data comes in first clock edge, Y comes in 2nd and 4th clock edges and Cr data comes in 3rd clock edge
3. For less than 12-bit YCbCr422 input, the MSB data should be connected to input bit [11] and unused low input bits should be connected to logic 0
4. Bit significance with in a pixel component : [7:0] = [MSB:LSB]
5. In embedded sync mode, Hsync, Vsync and DE signals are extracted from EAV/SAV codes according to CCIR 656 standard.
6. Unused pins should not left floating.

Section 3 Detail Functional Descriptions

3.1 General

The HDMI Transmitter provides an IIC serial bus interface to communicate with the host. The IIC address for this slave IIC interface is "0111_000x" (where x=1 for read and x=0 for write).

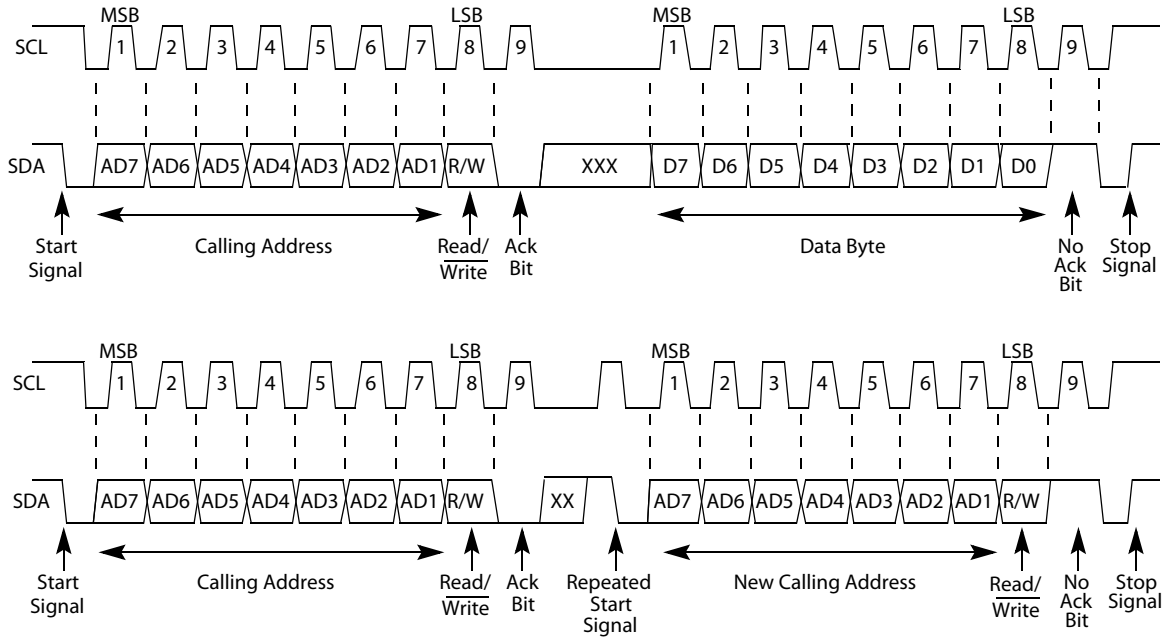
3.2 IIC Interface

The IIC bus interface uses a Serial Data line (SDA) and a Serial Clock Line (SCL) for data transfer. The HDMI Transmitter acts as a slave for receiving and transmitting data over the serial interface. All devices connected to the IIC bus must have open drain or open collector outputs. Logic AND function is exercised on both lines with external pull-up resistors, the value of these resistors is system dependent. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable at the positive edge of SCL. If the SDA changes state while SCL is HIGH, the IIC interface interprets that action as a START or STOP sequence. Data on SDA must change only when SCL is LOW.

The standard IIC traffic protocol is illustrated in the following Figure:

Figure 3-1 IIC Bus Transmission Protocol



3.2.1 Basic Protocol

For Flat Panel Display Controller, there are six components to serial bus operation:

- START Signal
- Slave Address Byte
- Base Register Address Byte
- Data Byte for Read/Write
- STOP Signal

When the serial interface is inactive (SCL and SDA are HIGH), communication are initiated by a START signal which is a HIGH-to-LOW transition on SDA while SCL is HIGH. The first eight bits of data transferred after a START signal comprising a seven bit slave address (the seven MSB bits) and a single R/W bit (the LSB bit). The R/W bit indicates the direction of data transfer, "1" means read from device and "0" means write to device. If the transmitted slave address matches the address of the device, the Flat Panel Controller sends the acknowledge by asserting SDA Low on the ninth SCL pulse. Else, the Flat Panel Controller does not acknowledge.

Writing data to specific control registers of the HDMI Transmitter requires that the 8-bits address of the control register is written after the slave address has been acknowledged. This control register address is the base address for the subsequent write operations. The base address auto-increments by one for each byte of data written after the data byte intended for the base address. The acknowledge bit will be sent on the ninth SCL pulse after every 8-bits data received.

Data are read from the control registers of the HDMI Transmitter in a similar manner. Reading requires two data transfer operations:

The base address must be written with the R/W bit of the slave address byte LOW to set up a sequential read operation.

Reading (the R/W bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.

To terminate a read/write sequence to the HDMI Transmitter, a STOP signal must be sent. A STOP signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH.

A REPEATED START signal occurs when the master device driving the serial interface generates a START signal without first generating a STOP signal to terminate the current read/write sequence. This can be used to change the mode of communication (read, write) between the slave and master without releasing the bus. The REPEATED START signal shall be used for reading the register data from EP932M.

3.2.2 Examples of the read/write sequence

Write to One Control Register

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- Data Byte to Base Address
- STOP Signal

Write to Multiple Control Registers

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- Data Byte to Base Address
- Data Byte to (Base Address + 1)
- Data Byte to (Base Address + 2)
- .....
- Data Byte to (Base Address + N)
- STOP Signal

Read from One Control Register

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- REPEATED START Signal
- Slave Address Byte (R/W = HIGH)
- Data Byte from Base Address
- STOP Signal

Read from Multiple Control Registers

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Base Address Byte
- REPEATED START Signal
- Slave Address Byte (R/W = HIGH)

- Data Byte from Base Address
- Data Byte from (Base Address + 1)
- Data Byte from (Base Address + 2)
- .....
- Data Byte from (Base Address + N)
- STOP Signal

3.3 Control Registers

Table 3-1 IIC Control Registers

Addr	Mode	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	RESET
$00	-	-								-
$01	-	-								-
$02	-	-								-
$03	-	-								-
$04	-	-								-
$05	-	-								-
$06	R	0	0	0	SMPRD[12:8]					-
$07	R	SMPRD[7:0]								-
$08	R/W	TSEL	INT_OD	INT_POL	VTX	DSEL	BSEL	EDGE	PU	36h
$09	R/W	RSEN	HTPLG	RIE	VIE	MIE	RIF	VIF	MIF	00h
$0A	R/W	DK[3:1]			DKEN	RI_RATE[3:0]				8Fh
$0B	R	CFG[7:0]								XXh
$0C	R/W	422_OUT	YCC_OUT	COLOR	YCC_range	V_MUTE	A_MUTE	TREG[1:0]		00h
$0D	R/W	CS_M	CTS_M	ADSR[1:0]		OSC_SEL	VSYNC	PR[1:0]		00h
$0E	R/W	FMT12	422_IN	YCC_IN	E_SYNC	VPOL_DET	HPOL_DET	EESS	HDMI	00h
$0F	R/W	AKSV_RDY	ENC_ON	RESERVED	RX_RPTR	RESERVED		RI_RDY	ENC_EN	00h
$10	R/W	BKSV_1								XXh
$11	R/W	BKSV_2								XXh
$12	R/W	BKSV_3								XXh
$13	R/W	BKSV_4								XXh
$14	R/W	BKSV_5								XXh
$15	R/W	AN_1								XXh
$16	R/W	AN_2								XXh
$17	R/W	AN_3								XXh
$18	R/W	AN_4								XXh
$19	R/W	AN_5								XXh
$1A	R/W	AN_6								XXh
$1B	R/W	AN_7								XXh

$1C	R/W	AN_8							XXh
$1D	R	AKSV_1							XXh
$1E	R	AKSV_2							XXh
$1F	R	AKSV_3							XXh
$20	R	AKSV_4							XXh
$21	R	AKSV_5							XXh
$22	R	RI_1							XXh
$23	R	RI_2							XXh
$24	R/W	RESERVED							00h
$25	R	M0[7:0]							XXh
$26	R	M0[15:8]							XXh
$27	R	M0[23:16]							XXh
$28	R	M0[31:24]							XXh
$29	R	M0[39:32]							XXh
$2A	R	M0[47:40]							XXh
$2B	R	M0[55:48]							XXh
$2C	R	M0[63:56]							XXh
$25~$31	R	RESERVED							XXh
$32	R/W	DE_DLY[7:0]							FFh
$33	R/W	RESERVED	DE_GEN	-	-	VSO_POL	HSO_POL	DE_DLY[9:8]	03h
$34	R/W	RESERVED	DE_TOP[6:0]						7Fh
$35	R	RESERVED							00h
$36	R/W	DE_CNT[7:0]							FFh
$37	R/W	RESERVED					DE_CNT[10:8]		07h
$38	R/W	DE_LIN[7:0]							00h
$39	R/W	RESERVED					DE_LIN[10:8]		00h
$3A	R	H_RES[7:0]							XXh
$3B	R	RESERVED				H_RES[11:8]			XXh
$3C	R	V_RES[7:0]							XXh
$3D	R	RESERVED				V_RES[11:8]			XXh
$3E	R	PA3[1:0]		PA2[1:0]		PA1[1:0]		PA0[1:0]	E4h
$3F	R/W	ACR_EN	AVI_EN	ADO_EN	AUDIO_EN	-	WS_M	WS_POL	SCK_POL	00h

$40	R/W	FLAT[3:0]				LAYOUT	IIS	-	PKT_RDY	00h
$41	R/W	HB0								XXh
$42	R/W	HB1								XXh
$43	R/W	HB2								XXh
$44	R/W	PB0								XXh
$45	R/W	PB1								XXh
$46	R/W	PB2								XXh
$47	R/W	PB3								XXh
$48	R/W	PB4								XXh
$49	R/W	PB5								XXh
$4A	R/W	PB6								XXh
$4B	R/W	PB7								XXh
$4C	R/W	PB8								XXh
$4D	R/W	PB9								XXh
$4E	R/W	PB10								XXh
$4F	R/W	PB11								XXh
$50	R/W	PB12								XXh
$51	R/W	PB13								XXh
$52	R/W	PB14								XXh
$53	R/W	PB15								XXh
$54	R/W	PB16								XXh
$55	R/W	PB17								XXh
$56	R/W	PB18								XXh
$57	R/W	PB19								XXh
$58	R/W	PB20								XXh
$59	R/W	PB21								XXh
$5A	R/W	PB22								XXh
$5B	R/W	PB23								XXh
$5C	R/W	PB24								XXh
$5D	R/W	PB25								XXh
$5E	R/W	PB26								XXh
$5F	R/W	PB27								XXh
$60	R/W	-	-	-	-	CTS[19:16]				XXh

$61	R/W	CTS[15:8]							XXh
$62	R/W	CTS[7:0]							XXh
$63	R/W	-	-	-	-	N[19:16]			XXh
$64	R/W	N[15:8]							XXh
$65	R/W	N[7:0]							XXh
$66	R/W	AVI0							XXh
$67	R/W	AVI1							XXh
$68	R/W	AVI2							XXh
$69	R/W	AVI3							XXh
$6A	R/W	AVI4							XXh
$6B	R/W	AVI5							XXh
$6C	R/W	AVI6							XXh
$6D	R/W	AVI7							XXh
$6E	R/W	AVI8							XXh
$6F	R/W	AVI9							XXh
$70	R/W	AVI10							XXh
$71	R/W	AVI11							XXh
$72	R/W	AVI12							XXh
$73	R/W	AVI13							XXh
$74	R/W	ADO0							XXh
$75	R/W	ADO1							XXh
$76	R/W	ADO2							XXh
$77	R/W	ADO3							XXh
$78	R/W	ADO4							XXh
$79	R/W	ADO5							XXh
$7A	R	SPF_R[3:0]				SPF_L[3:0]			XXh
$7B	R/W	CS[7:0]							XXh
$7C	R/W	CS[15:8]							XXh
$7D	R/W	CS[23:16]							XXh
$7E	R/W	CS[31:24]							XXh
$7F	R/W	CS[39:32]							XXh
$80	R/W	-	-	-	-	V_OFST_EN	V_ADJ_EN	V_ADJ_M	F_POL	00h
$81	R/W	H_DLY[7:0]							01h

$82	R/W	-	-	-	-	-	-	H_DLY[9:8]	00h
$83	R/W	H_WIDTH[7:0]							01h
$84	R/W	-	-	-	-	-	-	H_WIDTH[9:8]	00h
$85	R/W	-	-	V_DLY[5:0]					02h
$86	R/W	-	-	V_WIDTH[5:0]					02h
$87	R/W	V_OFST[7:0]							01h
$88	R/W	-	-	-	-	V_OFST[11:8]			00h
$F0	R/W	Key_Add							00h
$F1	R/W	Key_Data0							00h
$F2	R/W	Key_Data1							00h
$F3	R/W	Key_Data2							00h
$F4	R/W	Key_Data3							00h
$F5	R/W	Key_Data4							00h
$F6	R/W	Key_Data5							00h
$F7	R/W	Key_Data6							00h

3.3.1 Register Descriptions

Detailed usage of these IIC registers is described in the following section.

3.3.1.1 SMPRD Register ($06 ~ $07) - SMPRD[12:0]

This 13-bit register is read only. It gives the Audio Sample Period in terms of number of oscillator clocks.

3.3.1.2 Control Register 1

Table 3-2 Control Register 1

$08

	6	5	4	3	2	1	0
R/W	TSEL	INT_OD	INT_POL	VTX	DSEL	BSEL	EDGE	PU
Reset:	-	-	0	0	0	0	0	0

TSEL — Monitor Sense Interrupt Source Select Bit

The TSEL bit determines the Monitor Sense Interrupt Source.

1 = MIF Interrupt flag is set when rising or falling edge is detected at HTPLG pin
0 = MIF Interrupt flag is set when 0 to 1 or 1 to 0 transition is detected at RSEN bit

INT_OD — Interrupt Open Drain

The INT_OD bit determines the drive scheme for INT pin.
1 = INT pin is open drain output
0 = INT pin is push-pull output

INT_POL — Interrupt Polarity

The INT_POL bit determines the polarity for INT pin.
1 = Requesting host to service interrupt when INT pin is high
0 = Requesting host to service interrupt when INT pin is low

VTX — Transmit at Vertical Sync

The VTX bit enables transmission of data packet at Vertical Sync leading edge.
1 = Data packet transmission triggered by Vertical Sync leading edge.
0 = Data packet transmission triggered as soon as it is ready.

DSEL — Dual Edge Clock Select Bit

The DSEL bit determines whether the dual clock edge is enabled or not.
1 = Input Data is latched at both rising and falling clock edges.
0 = Input Data is latched at either rising or falling clock edge.

BSEL — Input Bus Format Select Bit

The BSEL bit determines what the input data bus format is.
1 = Input Data Bus is 24-bits wide.
0 = Input Data Bus is 12-bits wide.

EDGE — Data Latched Edge Select Bit

The EDGE bit determine the data latched edge.
1 = In single edge mode, input data is latched at the clock rising edge. In dual edge mode, the first data is latched ar the clock rising edge.
0 = In single edge mode, input data is latched at the clock falling edge. In dual edge mode, the first data is latched ar the clock falling edge.

PU — Power Down Control Bit

The PU bit controls the power of the HDMI transmitter
1 = Normal Operation.
0 = Power Down Mode.

3.3.1.3 Control Register 2

Table 3-3 Control Register 2

$09

	6	5	4	3	2	1	0
R	RSEN	HTPLG	RIE	VIE	MIE	RIF	VIF	MIF
W	-	-						
Reset:	-	-	0	0	0	0	0	1

RSEN — Analog Output Status Bit

The RSEN bit indicates the analog output status.
1 = Analog Outputs are connected to the receiver
0 = Analog Outputs are disconnected

HTPLG — Hot Plug Status Bit

The HTPLG bit indicates the hot plug status.
1 = Hot Plug Detected (HTPLG pin is high)
0 = Hot Plug Not Detected bit (HTPLG pin is low)

RIE — Ri Interrupt Enable
1 = If RIF interrupt flag is set, interrupt signal is generated at INT pin
0 = If RIF interrupt flag is set, interrupt signal is not generated at INT pin

VIE — Vertical Interrupt Enable
1 = If VIF interrupt flag is set, interrupt signal is generated at INT pin
0 = If VIF interrupt flag is set, interrupt signal is not generated at INT pin

MIE — Monitor Sense Interrupt Enable
1 = If MIF interrupt flag is set, interrupt signal is generated at INT pin
0 = If MIF interrupt flag is set, interrupt signal is not generated at INT pin

RIF — Ri Interrupt Flag

The RIF bit is set periodically at Ri interrupt period when ENC_EN bit is set. Ri interrupt period is defined by RI_RATE[3:0] register. When this bit is set, the INT pin will be active if RIE bit is set. This flag is cleared when an 1 is written to the same bit.

VIF — Vertical Interrupt Flag

The VIF bit is set periodically at every leading edge of Vsync signal. When this bit is set, the INT pin will be active if VIE bit is set. This flag is cleared when an 1 is written to the same bit.

MIF — Monitor Sense Interrupt Flag

The MIF bit is set when a Monitor Sense Interrupt (defined by TSEL bit) occurs. When this bit is set, the INT pin will be active if MIE bit is set. This flag is cleared when an 1 is written to the same bit.

3.3.1.4 Control Register 3

Table 3-4 Control Register 3

$0A

	6	5	4	3	2	1	0
R W	DK[3:1]		DKEN	RI_RATE[3:0]			
Reset:	1	0	0	0	1	1	1	1

DK[3:1] — De-skewing Setting Control Bits

The DK[3:1] setting the clock to data riming for de-skew purpose. Eight steps can be selected and the time difference for each step is 200 ps. The default is 0 step.

000 = -4 step
001 = -3 step
010 = -2 step
011 = -1 step
100 = 0 step
101 = +1 step
110 = +2 step
111 = +3 step

DKEN — De-Skew (Clock to Data De-skewing) Enable Bit

1 = De-Skew Enabled
0 = De-Skew Disabled, 0 step is selected

RI_RATE[3:0] — Ri Interrupt Rate

The RI_RATE[3:0] determines the time period for generating Ri interrupt which is used to inform the host to compare the HDCP Ri value between the transmitter and receiver.
Ri interrupt period = Vertical period * (RI_RATE[3:0] * 8 + 8)

3.3.1.5 Configuration Register ($0B) - CFG[7:0]

The CFG[7:0] is read only which contains state of input D[23:16] pins. These pins can be used to provide user selectable configuration data through the IIC bus. Only available in 12-bit mode.

3.3.1.6 Color Space Control Register

Table 3-5 Color Space Control Register

$0C

	6	5	4	3	2	1	0
R W	422_OUT	YCC_OUT	COLOR	YCC_range	V_MUTE	A_MUTE	TREG[1:0]	
Reset:	0	0	0	0	0	0	0	0

422_OUT— HDMI output in 422 format

This bit specifies whether the HDMI output is in 422 or 444 format
1 = HDMI is outputting 422 format
0 = HDMI is outputting 444 video

YCC_OUT— HDMI output in YCC video

This bit specifies whether the HDMI output is in YCC or RGB video
1 = HDMI is outputting YCC video
0 = HDMI is outputting RGB video

COLOR— Color Space

This bit specifies the color space to be used in color space conversion
1 = ITU-R BT.709
0 = ITU-R BT.601

YCC_range — Data range for YCC in RGB/YCC conversion
1 = Full range YCC (0~255).
0 = Limited range YCC (16~235 for Y, 16~240 for CbCr)

V_MUTE — Mute Video Output
1 = Mute Video Output.
0 = Normal

A_MUTE — Mute Audio Output

This function is only valid while the incoming audio is selected from IIS input.
1 = Mute Audio Output.
0 = Normal

TREG[1:0] — Transmitter Pre-emphasis Control bits

3.3.1.7 Pixel Repetition Control Register

Table 3-6 Pixel Repetition Control Register

$0D

	6	5	4	3	2	1	0
R	CS_M	CTS_M	ADSR[1:0]		OSC_SEL	VSYNC	PR[1:0]	
W						-		
Reset:	0	0	0	0	0	0	0	0

CS_M — SPDIF Channel Status Handling Mode
1 = SPDIF Channel Status block is transmitted using the contents in CS (Channel Status) registers.
0 = SPDIF Channel Status block is transmitted using the Channel Status block received from the SPDIF input.

CTS_M — CTS Handling Mode
1 = Using the written value to CTS register for ACR packet.
0 = Using the on-chip calculated CTS value for ACR packet.

ADSR[1:0] — Audio Down Sampling

This function is only valid while the incoming audio is selected from IIS input.

00 = No down sampling is performed at the audio inputs
01 = Audio is down sampled at 1/2 rate
10 = Audio is down sampled at 1/3 rate
11 = Audio is down sampled at 1/4 rate

OSC_SEL— Select on-chip oscillator frequence

1 = 160 Mhz.
0 = 20 Mhz

VSYNC — Vertical Sync Status Bit

The VSYNC bit gives the current status of the VSYNC input pin (if E_SYNC = 0) or the extracted embedded Vsync (if E_SYNC = 1). Monitor this bit with IIC to recognize the arrival of Vsync signal. This bit is read only.

PR[1:0] — Pixel Repetition

PR[1:0] specifies the number of times for each pixel to be repeated by the HDMI Transmitter.

00 = No pixel repetition is performed
01 = 1 pixel is repeated to 2 pixels
10 = 1 pixel is repeated to 4 pixels
11 = 1 pixel is repeated to 8 pixels (Only valid in 12-bit input mode, BSEL = 0)

3.3.1.8 Control Register 4

Table 3-7 Control Register 4

$0E	6	5	4	3	2	1	0
R	FMT12	422_IN	YCC_IN	E_SYNC	VPOL_DET	HPOL_DET	EESS	HDMI
W					-	-		
Reset:	0	0	0	0	0	0	0	0

FMT12 — 12-bit input format

The FMT12 bit determines data bit mapping in 12-bit input (BSEL = 0).

1 = Data bit mapping as shown in Table 2-12 is used. This mapping is used if input is in CCIR YUV422.
0 = Data bit mapping as shown in Table 2-11 is used.

422_IN — 422 to 444 conversion for digital input

1 = Enable 422 to 444 conversion. This is needed if input is in YUV422 and YUV to RGB conversion is enabled.
0 = 422 to 444 conversion is not done.

YCC_IN — Video Input in YCC video

This bit specifies whether the Video Input is in YCC or RGB video
1 = Video Input is YCC video
0 = Video Input is RGB video

E_SYNC — Embedded Sync
1 = Input is in Embedded Sync format. Hsync, Vsync and DE are extracted from EAV/SAV codes according to CCIR-656 standard. Hsync polarity is controlled by HS_POL bit and Vsync polarity is controlled by VS_POL bit.
0 = Input is in Separate Sync format. Hsync, Vsync and DE are from pins. HS_POL bit and VS_POL bit are used to tell the sync polarities coming from pins.

VPOL_DET — Vertical Sync Polarity Detection

The VPOL_DET bit gives the polarity for the VSYNC input pin.

HPOL_DET — Horizontal Sync Polarity Detection

The HPOL_DET bit gives the polarity for the HSYNC input pin

EESS — Enhanced Encryption Status Signalling
1 = Using Enhanced Encryption Status Signaling for HDCP encryption engine.
0 = Using Original Encryption Status Signaling for HDCP encryption engine. This is only valid if the HDMI Transmitter is working in DVI mode (HDMI = 0).

HDMI — HDMI mode
1 = HDMI Transmitter is working in HDMI mode.
0 = HDMI Transmitter is working in DVI mode. Audio and packet data will not be transmitted using this mode.

3.3.1.9 Control Register 5

Table 3-8 Control Register 5

$0F

	6	5	4	3	2	1	0
R	AKSV_RDY	ENC_ON	0	RX_RPTR	0	0	RI_RDY	ENC_EN
W								
	-	-	-	0	-	-	-	0

AKSV_RDY — AKSV Ready

The AKSV_RDY bit indicates whether the HDCP keys and AKSV has been successfully downloaded from external EE or not. This bit is read only.
1 = HDCP keys and AKSV has been successfully downloaded from external EE. AKSV is ready for read.
0 = HDCP keys and AKSV downloading has not been completed. AKSV is not ready for read.

ENC_ON — HDCP Encryption On

The ENC_ON bit indicates whether the HDCP encryption is in process or not. This bit is read only.

1 = HDCP encryption is in process.
0 = HDCP encryption is not in process.

RX_RPTR — Receiver Repeater

The RX_RPTR bit should be set if the receiver side is a repeater. It should be cleared otherwise.
1 = Receiver is a repeater.
0 = Receiver is not a repeater.

RI_RDY — RI Ready

The RI_RDY bit indicates that the first Ri value is available. This bit is read only.
1 = First Ri value is available.
0 = First Ri value is not available.

ENC_EN — ENC Enable
1 = Enable HDCP encryption.
0 = Disable HDCP encryption. This bit can not be cleared except by power up or pin reset.

3.3.1.10 BKSV Registers ($10 ~ $14) - BKSV_1 ~ BKSV_5

These 5 registers should be programmed with receiver's Key Selection Vector. BKSV_1 is the LSB and BKSV_5 is the MSB. BKSV_5 should be written last, as it triggers the authentication process.

3.3.1.11 AN Registers ($15 ~ $1c) - AN_1 ~ AN_8

These 8 registers should be programmed with a 64-bit pseudo-random value before triggering the authentication process. AN_1 is the LSB and AN_8 is the MSB.

3.3.1.12 AKSV Registers ($1D ~ $21) - AKSV_1 ~ AKSV_5

These 5 registers are read only which hold transmitter's Key Selection Vector. AKSV_1 is the LSB and AKSV_5 is the MSB. All five bytes should be read from here and then written to the receiver. Byte 5 should be written last to the receiver, as it will trigger authentication there. These 5 registers should not be read until AKSV_RDY bit is 1.

3.3.1.13 RI Registers ($22 ~ $23) - RI_1 ~ RI_2

These 2 registers hold transmitter's Ri value. They should be read and compared against the Ri value of the receiver to ensure that the encryption process on the transmitter and receiver is synchronized.

3.3.1.14 M0 Registers

This 8 byte registers are used to store the first secret value M0 which calculated by the HDCP cipher function.

3.3.1.15 DE_DLY Register ($32) - DE_DLY[9:0]

This 10-bit register is used for internal DE generation. It defines the number of pixels from HSYNC trailing edge to DE rising edge. For example, if the expected number of the horizontal back porch is 60 pixels per line, set DE_DLY[9:0] to 0x3C.

3.3.1.16 DE Control Register

Table 3-9 DE Control Register

$33	6	5	4	3	2	1	0
R	0	DE_GEN	-	-	0	0	DE_DLY[9:8]	
W					VSO_POL	HSO_POL		
Reset:	-	0	0	0	0	0	1	1

DE_GEN — Generate DE Enable
1 = Enable internal DE generation.
0 = Disable internal DE generation.

VSO_POL — Control Vertical Sync polarity for HDMI output
1 = Inverse Vertical Sync polarity from input
0 = Same Vertical Sync polarity as input

HSO_POL — Control Horizontal Sync polarity for HDMI output
1 = Inverse Horizontal Sync polarity from input
0 = Same Horizontal Sync polarity as input

3.3.1.17 DE_TOP Register ($34) - DE_TOP[6:0]

This 7-bit register is used for internal DE generation. It defines the number of lines from VSYNC trailing edge to the 1st DE in a frame. For example, if the expected number of the vertical back porch is 21 lines per frame, set DE_TOP[6:0] to 0x16.

3.3.1.18 DE_CNT Register ($36 ~ $37) - DE_CNT[10:0]

This 11-bit register is used for internal DE generation. It defines the width of active display in number of pixels. For example, if the expected number of active display is 720 pixels per line, set DE_CNT[10:0] to 0x2D0.

3.3.1.19 DE_LIN Register ($38 ~ $39) - DE_LIN[10:0]

This 11-bit register is used for internal DE generation. It defines the height of active display in number of lines. For example, if the expected number of active display is 480 lines per frame, set DE_LIN[10:0] to 0x1E0.

3.3.1.20 H_RES Register ($3A ~ $3B) - H_RES[11:0]

This 12-bit register is read only. It gives the number of pixels between 2 consecutive HSYNC pulses.

3.3.1.21 V_RES Register ($3C ~ $3D) - V_RES[11:0]

This 12-bit register is read only. It gives the number of lines between 2 consecutive VSYNC pulses.

3.3.1.22 Audio Subpacket Allocation Register

Table 3-10 Audio Subpacket Allocation Register

$3E	6	5	4	3	2	1	0
R W	PA3[1:0]		PA2[1:0]		PA1[1:0]		PA0[1:0]	
Reset:	1	1	1	0	0	1	0	0

PA3[1:0] — IIS port select for Audio Subpacket 3
- 00 = Select IIS_SD0 audio input
- 01 = Select IIS_SD1 audio input
- 10 = Select IIS_SD2 audio input
- 11 = Select IIS_SD3 audio input

PA2[1:0] — IIS port select for Audio Subpacket 2
- 00 = Select IIS_SD0 audio input
- 01 = Select IIS_SD1 audio input
- 10 = Select IIS_SD2 audio input
- 11 = Select IIS_SD3 audio input

PA1[1:0] — IIS port select for Audio Subpacket 1
- 00 = Select IIS_SD0 audio input
- 01 = Select IIS_SD1 audio input

10 = Select IIS_SD2 audio input
11 = Select IIS_SD3 audio input

PA0[1:0] — IIS port select for Audio Subpacket 0
00 = Select IIS_SD0 audio input
01 = Select IIS_SD1 audio input
10 = Select IIS_SD2 audio input
11 = Select IIS_SD3 audio input

3.3.1.23 IIS Control Register

Table 3-11 IIS Control Register

$3F

	6	5	4	3	2	1	0
R W	ACR_EN	AVI_EN	ADO_EN	AUDIO_EN	-	WS_M	WS_POL	SCK_POL
Reset:	0	0	0	0	0	0	0	0

ACR_EN — This bit, if set, enables auto transmission of ACR packets.
1 = Enable auto transmission of ACR packets.
0 = Disable auto transmission of ACR packets.

AVI_EN — This bit, if set, enables auto transmission of AVI packets in vertical blank period.
1 = Enable auto transmission of AVI packets in vertical blank period.
0 = Disable auto transmission of AVI packets in vertical blank period.

ADO_EN — This bit, if set, enables auto transmission of ADO packets in vertical blank period.
1 = Enable auto transmission of ADO packets in vertical blank period.
0 = Disable auto transmission of ADO packets in vertical blank period.

AUDIO_EN — This bit, if set, enables audio packet transmission.
1 = Enable auto transmission of audio packets.
0 = Disable auto transmission of audio packets.

WS_M — This bit specifies IIS_WS timing mode
1 = IIS_WS is one clock delayed compared with standard IIS timing.
0 = IIS_WS is in standard IIS timing.

WS_POL — This bit specifies IIS_WS polarity
1 = IIS_WS is in opposite polarity compared with standard IIS.
0 = IIS_WS is in standard IIS polarity.

SCK_POL — This bit specifies IIS_SCK polarity
1 = IIS_SCK is in opposite polarity compared with standard IIS.
0 = IIS_SCK is in standard IIS polarity.

3.3.1.24 Packet Control Register

Table 3-12 Packet Control Register

$40

	6	5	4	3	2	1	0
R W	FLAT3	FLAT2	FLAT1	FLAT0	LAYOUT	IIS	-	PKT_RDY
Reset:	0	0	0	0	0	0	0	0

FLAT3 — FLAT bit for Audio Sample 3

FLAT2 — FLAT bit for Audio Sample 2

FLAT1 — FLAT bit for Audio Sample 1

FLAT0 — FLAT bit for Audio Sample 0

LAYOUT — LAYOUT bit for Audio Sample Packet

IIS — Audio Input Selection

1 = Audio input is in IIS protocol. 4 IIS audio channels are supported in this mode.
0 = Audio input is in SPDIF protocol. Only 1 SPDIF audio channel is supported in this mode.

PKT_RDY — Data Packet Ready

This bit is set to indicate the data packet is ready for transmission. This bit can only be written to 1. It returns to zero after the data packet is transmitted.

1 = Data packet is ready. Request for transmission.
0 = Data packet transmitted.

3.3.1.25 Data Packet Header Register ($41 ~ $43) - HB0 ~ HB2

These 3 8-bit registers are used to program the header of the data packet. HB0 is the LSB and HB2 is the MSB.

3.3.1.26 Data Packet Register ($44 ~ $5F) - PB0 ~ PB27

These 28 8-bit registers are used to program the packet contents of the data packet. PB0 is the LSB and PB27 is the MSB.

3.3.1.27 CTS Registers

Table 3-13 CTS Registers 0

$60

	6	5	4	3	2	1	0
R W	-	-	-	-	CTS[19:16]		
Reset:	-	-	-	-	-	-	-	-

Table 3-14 CTS Registers 1

$61

	6	5	4	3	2	1	0
R W	CTS[15:8]						
Reset:	-	-	-	-	-	-	-	-

Table 3-15 CTS Registers 2

$62

	6	5	4	3	2	1	0
R W	CTS[7:0]						
Reset:	-	-	-	-	-	-	-	-

CTS[19:0]— This register, if written, defines a 20-bit CTS value as part of ACR packet. ACR packet is sent once per frame automatically at the beginning of vertical blank period if ACR_EN bit is set. If CTS_M bit is ‘set, the written value is used for ACR packet. Otherwise, an on-chip calculated CTS value is used for ACT packet. If this register is read, it presents the on-chip calculated CTS value. The on-chip calculated CTS value is derived based on the N value written to N register.

3.3.1.28 N Registers

Table 3-16 N Registers 0

$63

	6	5	4	3	2	1	0
R W	-	-	-	-	N[19:16]		
Reset:	-	-	-	-	-	-	-	-

Table 3-17 N Registers 1

$64

	6	5	4	3	2	1	0
R W	N[15:8]						
Reset:	-	-	-	-	-	-	-	-

Table 3-18 N Registers 2

$65

	6	5	4	3	2	1	0
R W	N[7:0]						
Reset:	-	-	-	-	-	-	-	-

N[19:0]— This register defines the 20-bit N value as part of ACR packet. If ACR_EN bit is set, ACR packet will be sent once per frame automatically at the beginning of vertical blank period.

3.3.1.29 AVI Packet Register - AVI0($66) ~ AVI13($73)

These 14 8-bit registers are used to program the packet contents of the AVI packet. AVI0 is the LSB and AVI13 is the MSB. AVI0 is the check-sum byte. If AVI_EN bit is set, AVI packet will be sent once per frame automatically at the beginning of vertical blank period.

3.3.1.30 ADO Packet Register - ADO0($74) ~ ADO5($79)

These 6 8-bit registers are used to program the packet contents of the ADO packet. ADO0 is the LSB and ADO5 is the MSB. ADO0 is the check-sum byte. If ADO_EN bit is set, ADO packet will be sent once per frame automatically at the beginning of vertical blank period.

3.3.1.31 SPDIF Sampling Frequency Registers

Table 3-19 SPDIF Sampling Frequency Registers

$7A

	6	5	4	3	2	1	0
R	SPF_R[3:0]			SPF_L[3:0]			
W	-			-			
Reset:	-	-	-	-	-	-	-	-

SPF_L[3:0]— This read-only register presents the 4-bit sampling frequency code which is extracted from bit[27:24] of the 192-bit Channel Status Block of Left Channel of the SPDIF input.

SPF_R[3:0]— This read-only register presents the 4-bit sampling frequency code which is extracted from bit[27:24] of the 192-bit Channel Status Block of Right Channel of the SPDIF input.

3.3.1.32 Channel Status Registers

Table 3-20 Channel Status Register 0

$7B

	6	5	4	3	2	1	0
R W	CS[7:0]						
Reset:	-	-	-	-	-	-	-	-

Table 3-21 Channel Status Register 1

$7C

	6	5	4	3	2	1	0
R W	CS[15:8]						
Reset:	-	-	-	-	-	-	-	-

Table 3-22 Channel Status Register 2

$7D

	6	5	4	3	2	1	0
R W	CS[23:16]						
Reset:	-	-	-	-	-	-	-	-

Table 3-23 Channel Status Register 3

$7E

	6	5	4	3	2	1	0
R W	CS[31:24]						
Reset:	-	-	-	-	-	-	-	-

Table 3-24 Channel Status Register 4

$7F

	6	5	4	3	2	1	0
R W	CS[39:32]						
Reset:	-	-	-	-	-	-	-	-

CS[39:0]— This 40-bit register defines the first 40 bits (bit[39:0]) of a 192-bit Channel Status Block which is to be sent along with the audio packets if IIS input is selected as the audio input source (IIS bit is set), or if SPDIF is selected as the audio input source and CS_M bit is set. The other undefined 162 bits are sent as zero bits.

3.3.1.33 Embedded Sync Control Register

Table 3-25 Embedded Sync Control Register

$80

	6	5	4	3	2	1	0
R W	-	-	-	-	V_OFST_EN	V_ADJ_EN	V_ADJ_M	F_POL
Reset:	0	0	0	0	0	0	0	0

V_OFST_EN — This bit, if set, enables Vsync off-set in 2nd field of an interlaced source. This only applies to Embedded Sync input.

1 = Enable Vsync off-set in 2nd field of an interlaced source.

0 = Disable Vsync off-set in 2nd field of an interlaced source.

V_ADJ_EN — This bit, if set, enables adjustment of the V_DLY value according to V_ADJ_M bit setting in 2nd field of an interlaced source. This only applies to Embedded Sync input.

1 = Enables adjustment of the V_DLY value according to V_ADJ_M bit setting in 2nd field of an interlaced source.

0 = Disable adjustment of the V_DLY value.

V_ADJ_M — V_ADJ adjustment mode

1 = V_ADJ value is incremented by 1 in 2nd field.

0 = V_ADJ value is decremental by 1 in 2nd field.

F_POL — Specifies the polarity of the F bit in Embedded Sync input

1 = 2nd field is indicated by F bit being 0.

0 = 2nd field is indicated by F bit being 1.

3.3.1.34 H Delay Register - H_DLY[9:0]

Table 3-26 H_DLY low Register

$81

	6	5	4	3	2	1	0
R W	H_DLY[7:0]						
Reset:	0	0	0	0	0	0	1

Table 3-27 H_DLY high Register

$82

	6	5	4	3	2	1	0
R W	-	-	-	-	-	-	H_DLY[9:8]
Reset:	0	0	0	0	0	0	0	0

This 10-bit register is used for Hsync generation in Embedded Sync input. It specifies the timing in number of pixels from the time when H bit (extracted from EAV/SAV code) changes from 0 to 1 to the leading edge of the Hsync signal generated. This register is used when E_SYNC bit is set. A 0 value is not valid.

3.3.1.35 H Width Register - H_WIDTH[9:0]

Table 3-28 H_WIDTH low Register

$83

	6	5	4	3	2	1	0
R W	H_WIDTH[7:0]						
Reset:	0	0	0	0	0	0	0	1

Table 3-29 H_WIDTH high Register

$84

	6	5	4	3	2	1	0
R W	-	-	-	-	-	-	H_WIDTH[9:8]
Reset:	0	0	0	0	0	0	0	0

This 10-bit register is used for Hsync generation in Embedded Sync input. It specifies the pulse width of the generated Hsync signal in number of pixels. This register is used when E_SYNC bit is set. A 0 value is not valid.

3.3.1.36 V Delay Register - V_DLY[5:0]

Table 3-30 V_DLY Register

$85

	6	5	4	3	2	1	0
R W	-	-	H_DLY[5:0]				
Reset:	0	0	0	0	0	0	1	0

This 6-bit register is used for Vsync generation in Embedded Sync input. It specifies the timing in number of lines from the time when V bit (extracted from EAV/SAV code) changes from 0 to 1 to the leading edge of the Vsync signal generated. The programmed value can be incremented or decremental by 1 in the 2nd field according the V_ADJ_M bit setting if V_ADJ_EN bit is set. This register is used when E_SYNC bit is set. A 0 value is not valid.

3.3.1.37 V Width Register - V_WIDTH[5:0]

Table 3-31 V_WIDTH Register

$86

	6	5	4	3	2	1	0
R W	-	-	V_WIDTH[5:0]				
Reset:	0	0	0	0	0	0	0	1

This 6-bit register is used for Vsync generation in Embedded Sync input. It specifies the pulse width of the generated Vsync signal in number of lines. This register is used when E_SYNC bit is set. A 0 value is not valid.

3.3.1.38 V Off-Set Register - V_OFST[11:0]

Table 3-32 V_OFST low Register

$87

	6	5	4	3	2	1	0
R W	V_OFST[7:0]						
Reset:	0	0	0	0	0	0	0	1

Table 3-33 V_OFST high Register

$88

	6	5	4	3	2	1	0
R W	-	-	-	-	V_OFST[11:8]		
Reset:	0	0	0	0	0	0	0	0

This 12-bit register is used for Vsync generation in Embedded Sync input. if V_OFST_EN bit is set, the Vsync signal is skewed and delayed by a number of pixels specified by this register in the 2nd field. The leading edge of the Vsync signal is always aligned with the Hsync leading edge in the 1st field. This register is used when E_SYNC bit is set. A 0 value is not valid.

Section 4 Package