Low Power HDMI 1.3 Receiver
EP9351/EP9351B

User Guide
V1.0

Revised Date: Nov. 10, 2011

Original Release Date: Nov. 08, 2010

Explore

Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	Nov/08/2010	Jerry Chen	Initial Version
0.1	Nov/12/2010	Ether Lai	Revise the Pin Diagram;
0.2	Nov/24/2010	Ether Lai	Revise the BGA Package Dimension; Add descriptions to Control Registers;
0.3	Jan/19/2011	Ether Lai	Revise the BGA Package ID Information; Revise descriptions in Section 1, Overview and Features; Remove the LQFP package;
0.4	Feb/17/2011	Ether Lai & Kyle Kuo	Change the name of the BGA to VFBGA; Update the Control Register Description (EDID_RAM & HDCP Keys); Add Power consumption at DC specifications
0.5	Feb/22/2011	Kyle Kuo	Revise some words Add 3.3V power consumption at DC specifications Revise A_Mute description in General Control Register3
0.6	May/11/2011	Kyle Kuo	intergate EP9351 information in this specification
0.7	May/20/2011	Kyle Kuo	Revised power consumption and some pin names
0.8	Aug/26/2011	Kyle Kuo	Revised 1V8 maximum voltage to 2.0V from 1.98
0.9	Nov/10/2011	Kyle Kuo	Add VDDE voltage specification
1.0	Nov/16/2011	Kyle Kuo	Add one notes at DC Disgital I/O Speciication

Section 1 Introduction

1.1 Overview

EP9351/EP9351B is a low power HDMI receiver which is compliant with HDMI 1.4a and supports HD Audio and Video up to 1080p. The chip integrates Equalizer Switch, HDMI core, HDCP engine and EDID RAM in a single chip.

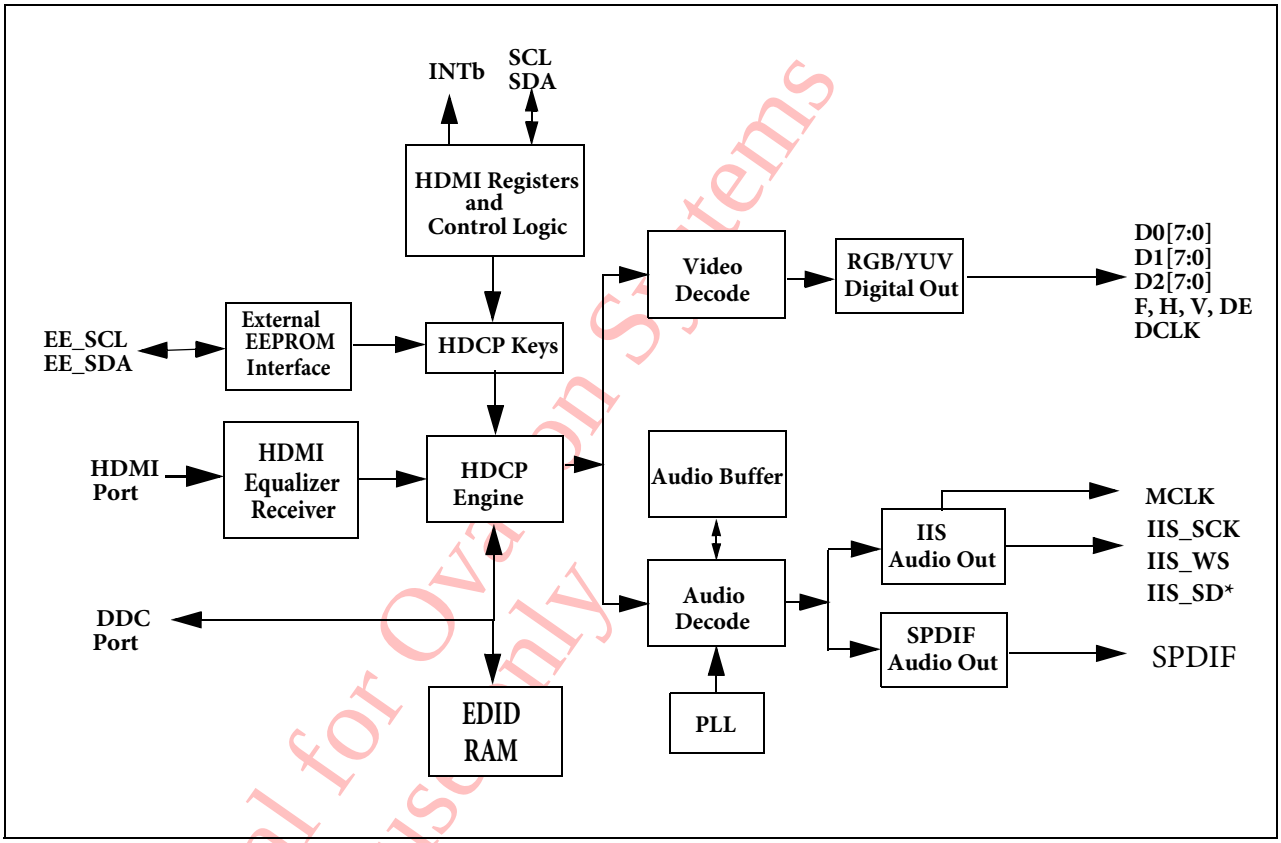
1.2 Features

- On-chip HDMI Receiver core which is compliant with HDMI 1.4a specification
- On-chip HDCP Engine which is compliant with HDCP 1.4 specification
- On-chip EDID RAM
- Supports 24-bit color mode up to 1080p
- On-chip Audio Decoder which support 8-channel IIS and S/PDIF audio outputs
- Support Standard Audio and HD (HBR) Audio
- Support audio soft mute
- Support SPDIF Channel Status extraction
- On-chip YCC422 to YCC444 conversion and YCC444 to YCC422 conversion
- On-chip YCC to RGB and RGB to YCC conversion in ITU-R BT.601 and 709 color space
- Support 24-bit RGB or 24-bit YCbCr 4:4:4 or 16-bit YCbCr 4:2:2 digital video output
- Support Bit Sequence Reverse and Port Swapping in video output ports to ease PCB layout
- Support DDR in digital video outputs
- Register-programmable via slave IIC interface
- Flexible interrupt registers with interrupt pin
- Link On and Valid DE Detection
- Controllable tri-state for output ports (1.8V swing)
- Low Power operation
- Low stand-by current (< 1mA) at power down mode
- EP9351 is 80 pin LQFP and the EP9351B is 81-ball VFBGA package

Section 2 Overview

2.1 Block Diagram

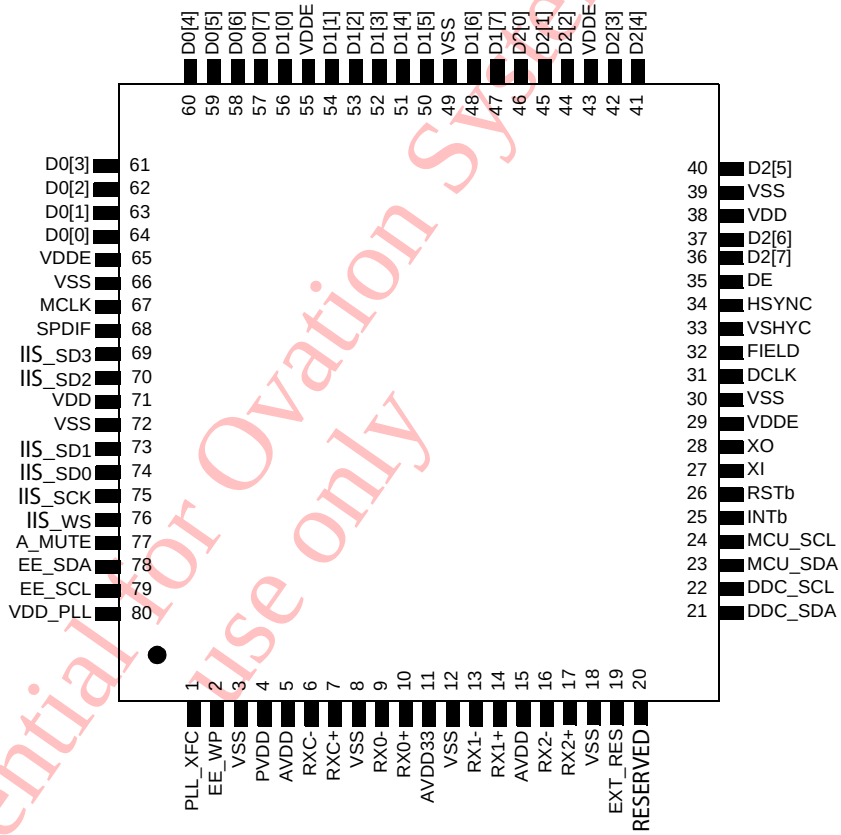
Figure 2-1 Block Diagram



2.2 Pin Diagram

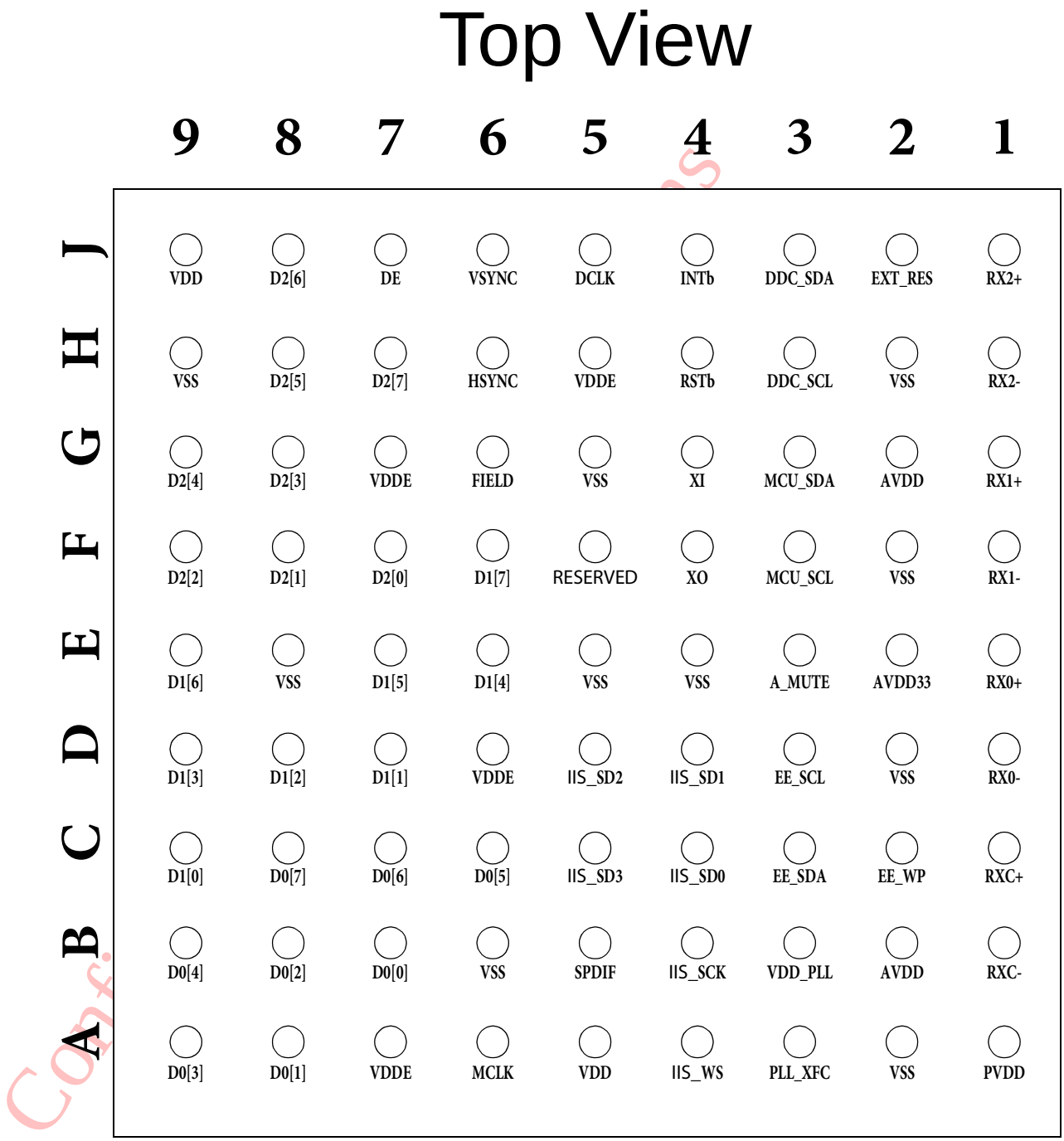
2.2.1 LQFP Pin Diagram

Figure 2-2 LQFP-80 Pin Diagram



2.2.2 BGA Pin Diagram

Figure 2-3 BGA-81 Pin Diagram



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 HDMI Receiver

Name	In/Out	Description
RXC-	IN	HDMI Receiver Differential Clock Input Pair
RXC+	IN	HDMI Receiver Differential Clock Input Pair
RX0-	IN	HDMI Receiver Differential Data Input Pair0
RX0+	IN	HDMI Receiver Differential Data Input Pair0
RX1-	IN	HDMI Receiver Differential Data Input Pair1
RX1+	IN	HDMI Receiver Differential Data Input Pair1
RX2-	IN	HDMI Receiver Differential Data Input Pair2
RX2+	IN	HDMI Receiver Differential Data Input Pair2
EXT_RES	IN	HDMI External Termination Resistor

Table 2-2 DDC/IIC/MCU/EEPROM

Name	In/Out	Description
RSTb	IN	Active Low Reset.
INTb	OUT	Interrupt signal (Active Low). Asserted when Information packet is received. This pin is open drain output with internal weak pull-up.
MCU_SCL	IN	SCL signal for HDMI slave IIC port
MCU_SDA	IO	SDA signal for HDMI slave IIC port
DDC_SCL	IN	IIC SCL signal for DDC Port
DDC_SDA	IO	IIC SDA signal for DDC Port
EE_SCL	OUT	SCL signal for EE IIC port
EE_SDA	IO	SDA signal for EE IIC port

Table 2-3 Video/Audio Output Pins

Name	In/Out	Description
A_MUTE	OUT	Audio Mute Output
DCLK	OUT	Data Clock Output.
VSYNC	OUT	Vertical Sync Output.
HSYNC	OUT	Horizontal Sync Output.
DE	OUT	Video Data Enable Output. When asserted, the data presents on D0, D1 and D2 pins is a valid video data.
FIELD	OUT	Field Output to indicate 1st field or 2nd field in an interlace video output. The polarity is programmable by register.
D0[7:0]	OUT	This 8-pin bus outputs port 0 digital Video Data.
D1[7:0]	OUT	This 8-pin bus outputs port 1 digital Video Data.
D2[7:0]	OUT	This 8-pin bus outputs port 2 digital Video Data.

Table 2-4 Audio Pins

Name	In/Out	Description
MCLK	OUT	System Clock output for audio DAC (128/256/384/512 * $F_{Sampling\_Clock}$)
IIS_SCK	OUT	IIS SCK output for all IIS audio ports. Sampling clock output for DSD.
IIS_WS/DSD0R	OUT	IIS WS output for all IIS audio ports. DSD audio output port 0 (Right Channel).
IIS_SD0/DSD0L	OUT	IIS SD output for audio port 0. DSD audio output port 0 (Left Channel).
IIS_SD1/DSD1R	OUT	IIS SD output for audio port 1. DSD audio output port 1 (Right Channel).
IIS_SD2/DSD1L	OUT	IIS SD output for audio port 2. DSD audio output port 1 (Left Channel).
IIS_SD3/DSD2R	OUT	IIS SD output for audio port 3. DSD audio output port 2 (Right Channel).
SPDIF/DSD2L	OUT	SPDIF output. DSD audio output port 2 (Left Channel).

Table 2-5 Misc. Pins

Name	In/Out	Description
XI	Analog	External Crystal Input, 18.432 Mhz
XO	Analog	External Crystal Output, 18.432 Mhz
PLL_XFC	Analog	For connecting a R/C components to ground for on-chip PLL
RESERVED	IN	Must be tied LOW for normal operation.

Table 2-6 Power Pins

Name	In/Out	Description
VDD_PLL	PWR	PLL VDD (3.3V)
AVDD33	PWR	HDMI Termination Power (3.3V)
AVDD	PWR	HDMI Receiver Analog Power (1.8V)
PVDD	PWR	HDMI Receiver PLL Analog Power (1.8V)
VDDE	PWR	I/O VDD (1.8V)
VDD	PWR	Internal Logic VDD (1.8V)
VSS	GND	Ground

2.4 Video Data Output Mapping

Table 2-7 Data Output Mapping[1,2,3]

Pin Name	RGB	YCbCr444	YCbCr422
D2[7]	R[7]	Cr[7]	Cb/Cr[7]
D2[6]	R[6]	Cr[6]	Cb/Cr[6]
D2[5]	R[5]	Cr[5]	Cb/Cr[5]
D2[4]	R[4]	Cr[4]	Cb/Cr[4]
D2[3]	R[3]	Cr[3]	Cb/Cr[3]
D2[2]	R[2]	Cr[2]	Cb/Cr[2]
D2[1]	R[1]	Cr[1]	Cb/Cr[1]
D2[0]	R[0]	Cr[0]	Cb/Cr[0]
D1[7]	G[7]	Y[7]	Y[7]
D1[6]	G[6]	Y[6]	Y[6]
D1[5]	G[5]	Y[5]	Y[5]
D1[4]	G[4]	Y[4]	Y[4]
D1[3]	G[3]	Y[3]	Y[3]
D1[2]	G[2]	Y[2]	Y[2]
D1[1]	G[1]	Y[1]	Y[1]
D1[0]	G[0]	Y[0]	Y[0]
D0[7]	B[7]	Cb[7]	-
D0[6]	B[6]	Cb[6]	-
D0[5]	B[5]	Cb[5]	-
D0[4]	B[4]	Cb[4]	-
D0[3]	B[3]	Cb[3]	-
D0[2]	B[2]	Cb[2]	-
D0[1]	B[1]	Cb[1]	-
D0[0]	B[0]	Cb[0]	-

NOTES:

1. In YCbCr444 output, if UVSW bit is set, Cb and Cr pin assignments are swapped.
2. In YCbCr422 output, Cb data is output in first clock and Cr data is output in next clock. If UVSW bit is set, Cb/Cr data sequence is reversed.
3. Bit significance in a pixel component: [7:0] = [MSB:LSB]
4. Bit sequence in a port will be reversed if BIT_REV bit is set.
5. D0 port and D2 port will be swapped if D02SW bit is set.

2.5 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{cc} [1]	3.3V Supply Voltage	-0.3		4.0	V
$V_{DD}1$	1.8V Supply Voltage	-0.3		2.5	V
V_I	Input Voltage	-0.3		V_{cc} + 0.3	V
V_O [2]	Output Voltage	-0.3		V_{cc} + 0.3	V
T_A	Ambient Temperature (with power applied)			125	°C
T_{STG}	Storage Temperature	-55		125	°C

NOTES:
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
Vcc	3.3V Supply Voltage		3.0	3.3	3.6	V
V_{DD}	1.8V Supply Voltage	AVDD, PVDD, VDD	1.62	1.8	2.0	V
		VDDE[1]	1.62	1.8	2.3	V
V_{CCN}	Supply Voltage Noise				100	mV_{p-p}
T_A	Ambient Temperature (with power applied)		0	25	70	°C

NOTES:
1. If VDDE supplied voltage is higher than 2.0V, it's recommended to supply the VDDE from the indiviudual power source. Meanwhile, the DDC_SCL input pin shall be adopt the application by using the external 2-stages schmitt inverters.

DC Digital I/O Specifications[1] (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		1.4			V
V_{IL}	Low-level Input Voltage				0.6	V
V_{OH}	High-level Output Voltage		1.5			V
V_{OL}	Low-level Output Voltage				0.4	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	uA

NOTES:
1. All input pins are 3.3V tolerant, and all output pins voltage are depend on VDDE.

DC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ID}	Differential Input Voltage, Single Ended Amplitude		150		1000	mV
I_{PD}	Power-Down Current	PWR_UP = LOW No RXC+/- input			1	mA
I_{CCR}	1.8V Operating Current (C_{LOAD} = 10pF, R_{EXT_RES} = 680 Ω)	DCLK=74.25MHz, Typical Pattern[1] Worst Case Pattern[2]		95 105		mA
		DCLK=148.5MHz, Typical Pattern Worst Case Pattern		130 180		mA
	3.3V Operating Current (C_{LOAD} = 10pF, R_{EXT_RES} = 680 Ω)	DCLK=74.25MHz, Typical Pattern Worst Case Pattern		50 50		mA
		DCLK=148.5MHz, Typical Pattern Worst Case Pattern		50 50		mA

NOTES:
1. The typical Pattern contains a gray scale area, checkerboard area and text
2. Black and white checkerboard pattern, each checker is one pixel wide

Video AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew				0.4	T_{bit}
T_{CCS}	Channel to Channel Differential Input Skew				1.0	T_{pixel}
T_{IJIT}	Differential Input Clock Jitter Tolerance				0.3	T_{bit}
D_{LH}	L-to-H Transition Time: CLK, Data and Controls	C_L = 10pF			3	ns
D_{HL}	H-to-L Transition Time: CLK, Data and Controls	C_L = 10pF			3	ns
T_{SETUP1}	D0, D1, D2, DE, VSYNC, HSYNC Setup Time to DCLK active edge at 165MHz	C_L = 10pF	2.5			ns
T_{HOLD1}	D0, D1, D2, DE, VSYNC, HSYNC Hold Time from DCLK active edge	C_L = 10pF	1.0			ns
T_{SETUP2}	D0, D1, D2, DE, VSYNC, HSYNC Setup Time to DCLK active edge at 165MHz	C_L = 10pF	1.2			ns
T_{HOLD2}	D0, D1, D2, DE, VSYNC, HSYNC Hold Time from DCLK active edge	C_L = 10pF	2.8			ns
T_{CIP}	DCLK Cycle Time		6.06		40	ns
F_{CIP}	DCLK Frequency		25		165	MHz

T_{CIH}	DCLK High Time	C_L = 10pF	2.0			ns
T_{CIL}	DCLK Low Time	C_L = 10pF	1.7			ns

I2S Audio AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{sck}	SCK Clock Period	C_L = 10pF		1		T_{sck}
T_{sck_d}	SCK Clock Duty Cycle	C_L = 10pF	40%		60%	T_{sck}
T_{sck_h}	SCK Clock High Time	C_L = 10pF	40%		60%	T_{sck}
T_{sck_l}	SCK Clock LOW Time	C_L = 10pF	40%		60%	T_{sck}
T_{iis_s}	SCK to SD and WS (Setup Time)	C_L = 10pF	40%		-	T_{sck}
T_{iis_h}	SCK to SD and WS (Hold Time)	C_L = 10pF	40%		-	T_{sck}

SPDIF Audio AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{spdif}	SPDIF Cycle Time	C_L = 10pF		1		UI
T_{spdif_d}	SPDIF Duty Cycle	C_L = 10pF	90%		110%	UI

2.6 Timing Diagrams

Figure 2-4 Digital Output Transition Timing Definition

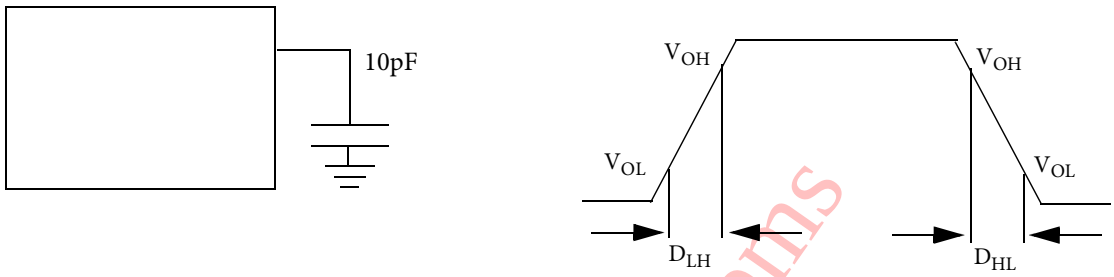


Figure 2-5 Clock Cycle and High/Low Timing Definition

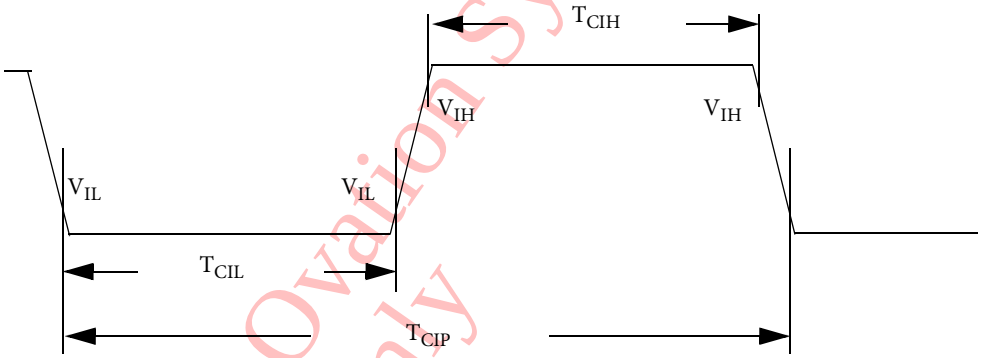


Figure 2-6 Channel to Channel Skew Timing Definition

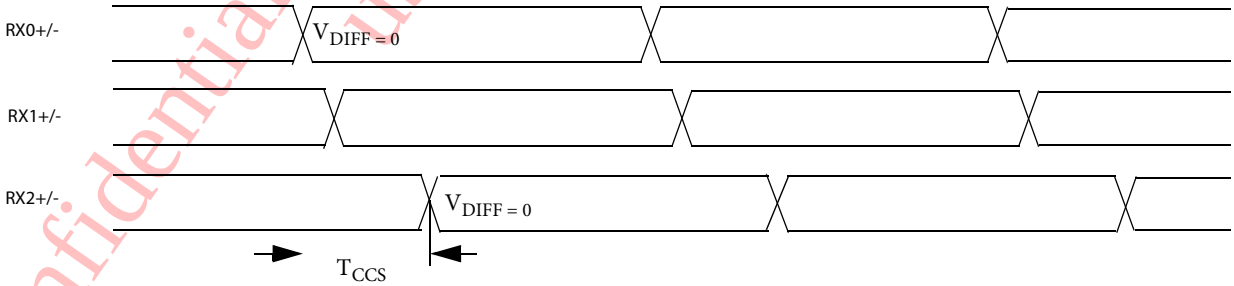


Figure 2-7 Output to DCLK Timing Definition

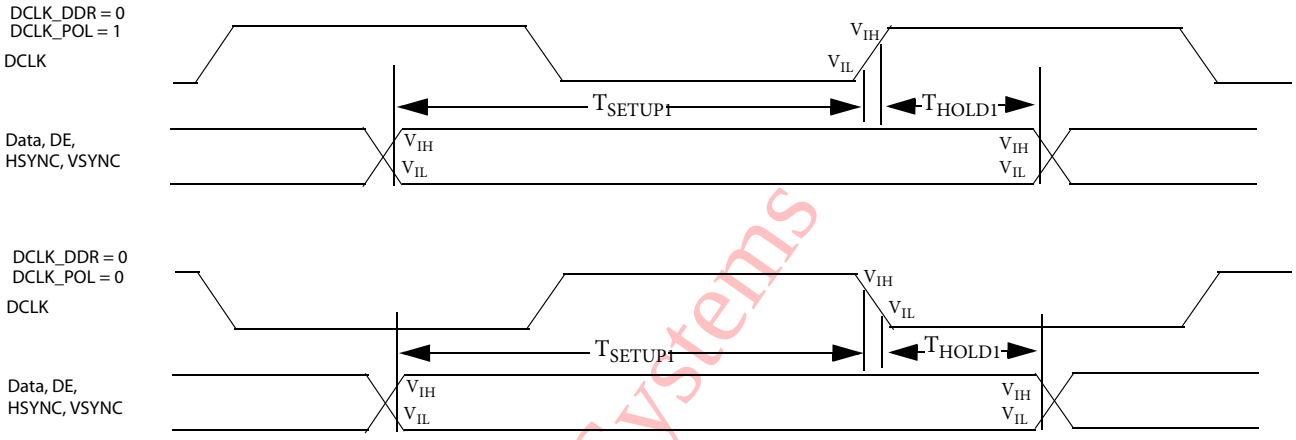


Figure 2-8 Output to DCLK Timing Definition

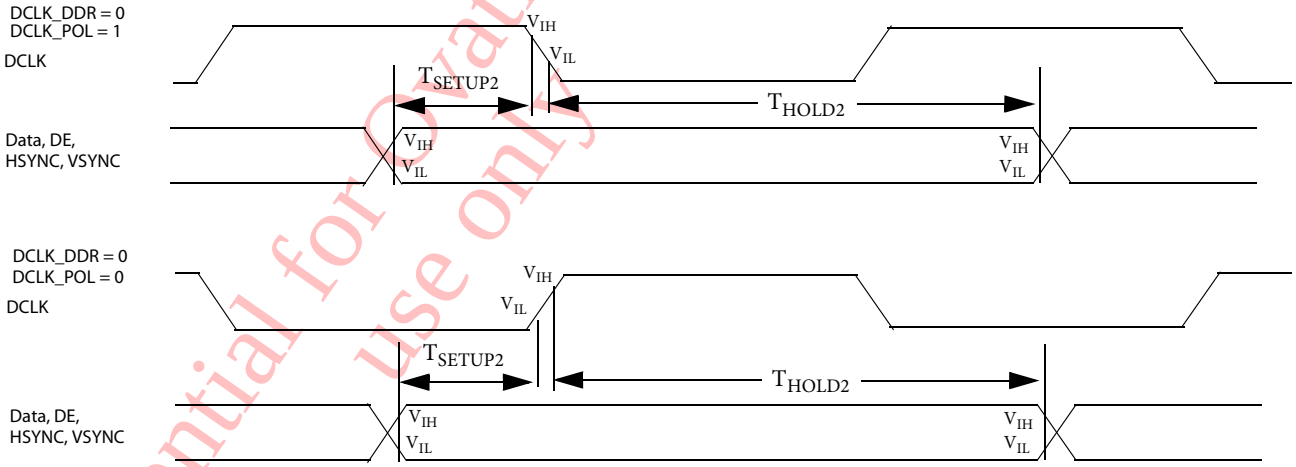
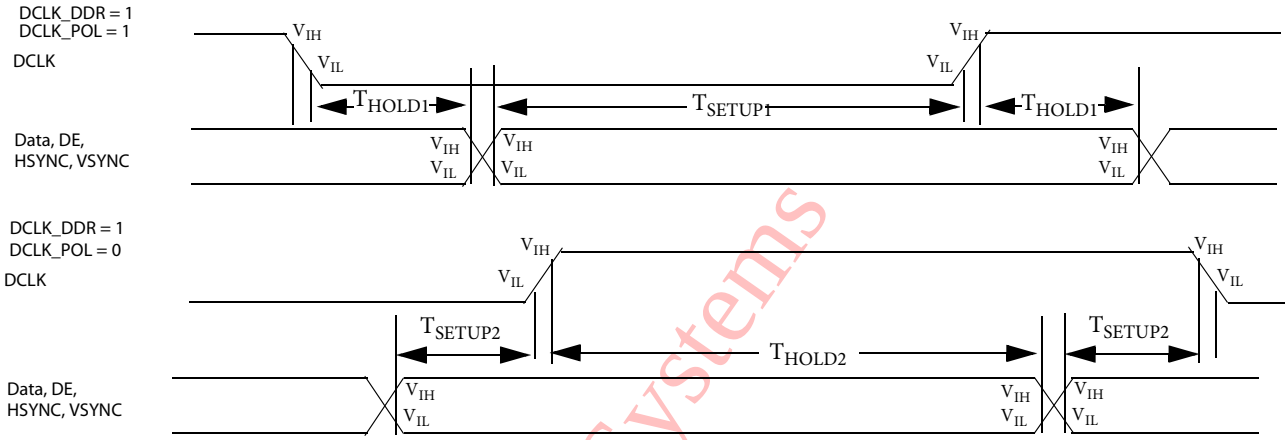
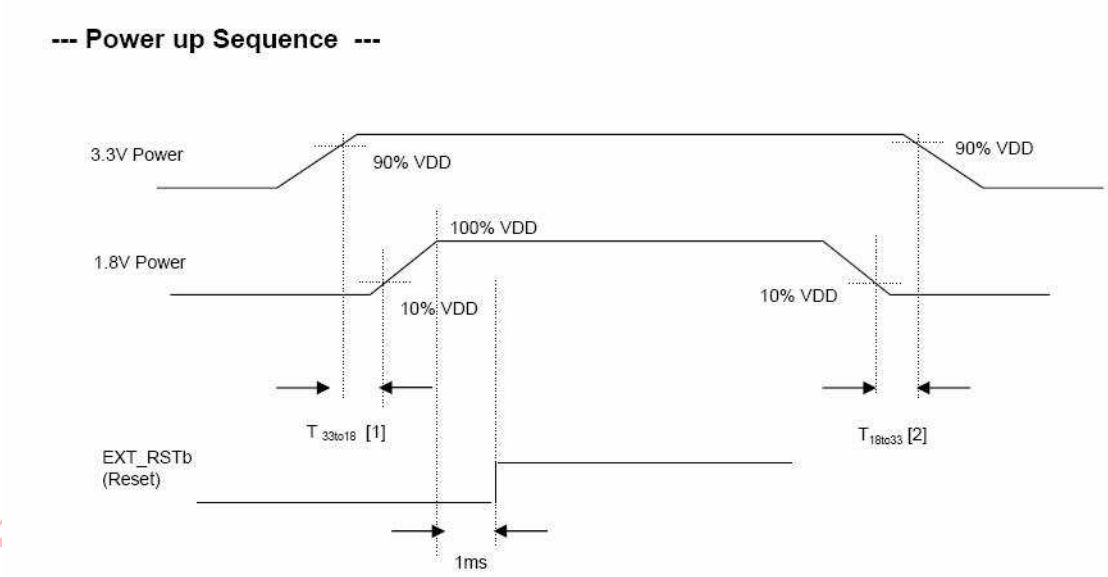


Figure 2-9 Output to DCLK Timing Definition



2.7 Power Up Sequence

Following figure shows the recommended power on sequence to EP9351/EP9351B:



Note 1: T_{33to18} should be less than 10ms. 3.3V is powered up in the beginning, then 1.8V powered up.

Note 2: T_{18to33} should be less than 10ms. 1.8V is powered down in the beginning, then 3.3V powered down.

Section 3 Detail Functional Descriptions

3.1 General

The chip provides an IIC serial bus interface (SCL/SDA pins) for MCU to access the HDMI control/status registers. To access the HDMI control/status registers, the IIC address of 0x78 should be given.

Built-in control/status registers are organized by Register Sets. Each Register Set is comprised of one or more than one bytes of register. To address a register byte, a Word Address along with a Byte Address should be given. Word Address is used to address the register set and Byte Address is used to address the designated register byte within the addressed register set.

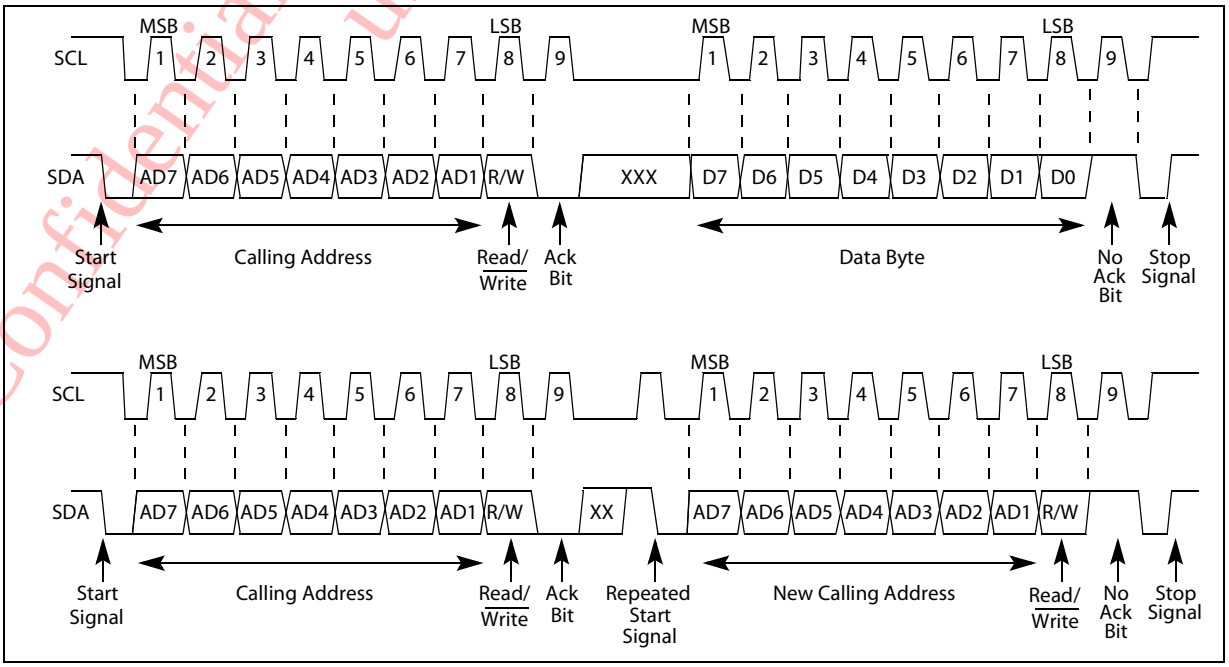
3.2 IIC Interface for HDMI control/status registers

On-chip HDMI control/status registers can be accessed by main MCU and/or the on-chip HDMI MCU through an IIC bus interface. The IIC bus is a slave (IIC address = 0x78) which uses a Serial Data line (SDA) at SDA pin and a Serial Clock Line (SCL) at SCL pin for receiving and transmitting data. All devices connected to the IIC bus must have open drain or open collector outputs. Logic AND function is exercised on both lines with external pull-up resistors, the value of these resistors is system dependent. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable at the positive edge of SCL. If the SDA changes state while SCL is HIGH, the IIC interface interprets that action as a START or STOP sequence. Data on SDA must change only when SCL is LOW.

The standard IIC traffic protocol is illustrated in the following Figure:

Figure 3-1 IIC Bus Transmission Protocol



3.2.1 Basic Protocol

There are 5 components in serial bus protocol:

- START Signal
- Slave Address Byte
- Word Address Byte for the Register Set
- Data Bytes for Read/Write from/to the Register Set
- STOP Signal

When the serial interface is inactive (SCL and SDA are HIGH), communication are initiated by a START signal which is a HIGH-to-LOW transition on SDA while SCL is HIGH. The first eight bits of data transferred after a START signal comprising a seven bit slave address (the seven MSB bits) and a single R/W bit (the LSB bit). The R/W bit indicates the direction of data transfer, "1" means read from device and "0" means write to device. If the transmitted slave address matches the address of the device, the chip sends the acknowledge by asserting SDA Low on the ninth SCL pulse. Else, the chip does not acknowledge.

On chip registers are organized by register set. Each register set is composed of single byte or multiple bytes. Each register set is assigned with a Word Address. Writing data to designated register set requires that the 8-bits Word Address of the register set is written after the slave address has been acknowledged. This Word Address selects the register set for the subsequent write operations. The write operation starts from byte 0 of the register set and continue write to the next byte of the register set if data presents. The acknowledge bit will be sent on the ninth SCL pulse after every 8-bits data received.

Data are read from address register set in a similar manner. Reading requires two IIC transfer operations:

The Word Address must be written with the R/W bit of the slave address byte being LOW to set up a sequential read operation.

Reading (the R/W bit of the slave address byte HIGH) begins at the previously established Word Address. Data is read from byte 0 of the address register set and continue the next byte read if acknowledge presents.

To terminate a read/write sequence, a STOP signal must be sent. A STOP signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a START signal without first generating a STOP signal to terminate the current read/write sequence. This can be used to change the mode of communication (read, write) between the slave and master without releasing the bus.

3.2.2 Examples of the read/write sequence

Write to a Register Set

- START Signal

- Slave Address Byte (R/W bit = LOW)
- Word Address Byte
- Data Byte/Bytes to the register set starting from byte 0
- STOP Signal

Read from a Register Set

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Word Address Byte
- STOP Signal (Optional)
- START Signal
- Slave Address Byte (R/W = HIGH)
- Data Byte/Bytes from addressed register set starting from byte 0
- STOP Signal

3.3 HDMI Control/Status Registers

3.3.1 Register Descriptions

3.3.1.1 HDCP key Area (Word Address = $00 ~ $28)

While the external EEPROM which store the encrypted HDCP Keys doesn't exist, the HDCP keys can be programmed from MCU. Word Address from $00 to $28 are used for downloading the encrypted 40 56-bit HDCP keys and the 40-bit BKSV from an external MCU. These areas are write only. The 40 HDCP keys are stored from Word Address $00 to $27. The 40-bit BKSV is stored at Word Address $28. For each HDCP key, bit 7~0 is stored in Byte-0 and bit 55~48 is stored in Byte-6. For BKSV, bit 7~0 is stored in Byte-0 and bit 39~32 is stored in Byte-4. The control bit EE_DIS (0x48, bit 2) shall be set to 1 before the MCU starts to write the HDCP Keys to the Key Area through the IIC interface.

3.3.1.2 Interrupt Flags (Word Address = $29)

Table 3-1 Interrupt Flags Register

Word Address = $29

	7	6	5	4	3	2	1	0
R		AVMC_F	AVMS_F	SEL2_F	SEL1_F	MS_F	ADO_F	AVI_F
Pin Reset:	0	0	0	0	0	0	0	0

This register is Read Only. The lower 7 bits of this register (bit 6-0) are used as interrupt flags for InfoFrame and other packets. Whenever a designated packet is received, the corresponding interrupt flag bit will be set and the HDMI_INTb pin will be asserted, if the corresponding interrupt enable bit is set, to inform MCU to read this register and download the data if needed. After MCU read this register, all the flag bits will be cleared automatically. Special care is taken by the design to prevent accidentally loss of any flag bit.

AVI_F — AVI InfoFrame Interrupt Flag

This bit is set when an AVI InfoFrame is received and is auto cleared when the register is read.

ADO_F — Audio InfoFrame Interrupt Flag

This bit is set when an Audio InfoFrame is received and is auto cleared when the register is read.

MS_F — MS InfoFrame Interrupt Flag

This bit is set when an MS InfoFrame is received and is auto cleared when the register is read.

SEL1_F — 1st Selected Packet Interrupt Flag

This bit is set when the selected packet 1is received and is auto cleared when the register is read.

SEL2_F — 2nd Selected Packet Interrupt Flag

This bit is set when the selected packet 2 is received and is auto cleared when the register is read.

AVMS_F — AVMUTE Set Interrupt Flag

This bit is set when AVMUTE is set by General Control Packet and is auto cleared when the register is read.

AVMC_F — AVMUTE Clear Interrupt Flag

This bit is set when AVMUTE is cleared by General Control Packet and is auto cleared when the register is read.

3.3.1.3 Interrupt Enable Register (Word Address = $29)

Table 3-2 Interrupt Enable Register

Word Address = $29

	7	6	5	4	3	2	1	0
W	INT_POL	AVMC_IEN	AVMS_IEN	SEL2_IEN	SEL1_IEN	MS_IEN	ADO_IEN	AVI_IEN
Pin Reset:	0	0	0	0	0	0	0	0

This register is Write Only. The lower 7 bits of this register (bit 0-6) are used as interrupt enable bits for Interrupt flags.

INT_POL — HDMI_INTb pin polarity
1 = HDMI_INTb pin is active high push pull.
0 = HDMI_INTb pin is active low with weak pull-up.

AVI_IEN — AVI_F interrupt enable
1 = HDMI_INTb pin will be asserted if AVI_F is set.
0 = HDMI_INTb pin is not affected by AVI_F.

ADO_IEN — ADO_F interrupt enable
1 = HDMI_INTb pin will be asserted if ADO_F is set.
0 = HDMI_INTb pin is not affected by ADO_F.

MS_IEN — MS_F interrupt enable
1 = HDMI_INTb pin will be asserted if MS_F is set.
0 = HDMI_INTb pin is not affected by MS_F.

SEL1_IEN — SEL1_F interrupt enable
1 = HDMI_INTb pin will be asserted if SEL1_F is set.
0 = HDMI_INTb pin is not affected by SEL1_F.

SEL2_IEN — SEL2_F interrupt enable
1 = HDMI_INTb pin will be asserted if SEL2_F is set.
0 = HDMI_INTb pin is not affected by SEL2_F.

AVMS_IEN — AVMS_F interrupt enable
1 = HDMI_INTb pin will be asserted if AVMS_F is set.
0 = HDMI_INTb pin is not affected by AVMS_F.

AVMC_IEN — AVMC_F interrupt enable
1 = HDMI_INTb pin will be asserted if AVMC_F is set.
0 = HDMI_INTb pin is not affected by AVMC_F.

3.3.1.4 AVI InfoFrame (Word Address = $2A)

The 15-byte AVI InfoFrame content is stored in the register set with Word Address $2A with Byte-0 being the version number, Byte-1 being the packet check sum, Byte-2 corresponding to the 1st byte of the InfoFrame and Byte-14 corresponding to the last byte of the InfoFrame.

Table 3-3 AVI InfoFrame Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x2A	0	R	Version Number							
	1		Checksum							
	2		0	Y1	Y0	A0	B1	B0	S1	S0
	3		C1	C0	M1	M0	R3	R2	R1	R0
	4		0	EC2	EC1	EC0	0	0	SC1	SC0
	5		0	VIC6	VIC5	VIC4	VIC3	VIC2	VIC1	VIC0
	6		0	0	0	0	PR3	PR2	PR1	PR0
	7		Line Number of End of Top Bar (lower 8 bits)							
	8		Line Number of End of Top Bar (upper 8 bits)							
	9		Line Number of Start of Bottom Bar (lower 8 bits)							
	10		Line Number of Start of Bottom Bar (upper 8 bits)							
	11		Pixel Number of End of Left Bar (lower 8 bits)							
	12		Pixel Number of End of Left Bar (upper 8 bits)							
	13		Pixel Number of Start of Right Bar (lower 8 bits)							
	14		Pixel Number of Start of Right Bar (upper 8 bits)							

3.3.1.5 Audio InfoFrame (Word Address = $2B)

The 7-byte Audio InfoFrame content is stored in the register set with Word Address $2B with Byte-0 being the version number, Byte-1 being the packet check sum, Byte-2 corresponding to the 1st byte of the InfoFrame and Byte-6 corresponding to the last byte of the InfoFrame.

Table 3-4 ADO InfoFrame Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x2B	0	R	Version Number							
	1		Checksum							
	2		CT3	CT2	CT1	CT0	0	CC2	CC1	CC0
	3		0	0	0	SF2	SF1	SF0	SS1	SS0
	4		0	0	0	0	0	0	0	0
	5		CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
	6		DM_INH	LSV3	LSV2	LSV1	LSV0	0	0	0

3.3.1.6 MS InfoFrame (Word Address = $2C)

The 7-byte MS InfoFrame content is stored in the register set with Word Address $2C with Byte-0 being the version number, Byte-1 being the packet check sum, Byte-2 corresponding to the 1st byte of the InfoFrame and Byte-6 corresponding to the last byte of the InfoFrame.

Table 3-5 MS InfoFrame Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x2C	0	R	Version Number							
	1		Checksum							
	2		MB#0 (MPEG Bit Rate: Hz Lower -> Upper)							
	3		MB#1							
	4		MB#2							
	5		MB#3 (Upper)							
	6		0	0	0	FR0	0	0	MF1	MF0

3.3.1.7 Selected Packet 1 (Word Address = $2D)

Any other packet with specified packet type can be extracted and stored in this register set. The specified packet type needs to be written into Byte-0. If 0 value is written, no packet will be extracted. If a packet with matched packet type is received, the 3-byte Packet Header and the 28-byte Packet Content are stored in the register set in sequence starting from Byte-0 and end at Byte-30.

3.3.1.8 Selected Packet 2 (Word Address = $2E)

Any other packet with specified packet type can be extracted and stored in this register set. The specified packet type needs to be written into Byte-0. If 0 value is written, no packet will be extracted. If a packet with matched packet type is received, the 3-byte Packet Header and the 28-byte Packet Content are stored in the register set in sequence starting from Byte-0 and end at Byte-30.

Table 3-6 Selected Packet Type 1/2 Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x2D & 0x2E	0	R/W	Packet Header 0 (HB0, Selected Packet Type)							
	1	R	Packet Header 1 (HB1)							
	2		Packet Header 2 (HB2)							
	3		Data Byte 0 (PB0 / SB0)							
	4		Data Byte 1 (PB1 / SB1)							
	5		Data Byte 2 (PB2 / SB2)							
	6		Data Byte 3 (PB3 / SB3)							
	7		Data Byte 4 (PB4 / SB4)							
	8		Data Byte 5 (PB5 / SB5)							
	9		Data Byte 6 (PB6 /SB6)							
	10		Data Byte 7 (PB7 / SB0)							
	11		Data Byte 8 (PB8 / SB1)							
	12		Data Byte 9 (PB9 / SB2)							
	13		Data Byte 10 (PB10 / SB3)							
	14		Data Byte 11 (PB11 / SB4)							
	15		Data Byte 12 (PB12 / SB5)							
	16		Data Byte 13 (PB13 / SB6)							
	17		Data Byte 14 (PB14 / SB0)							
	18		Data Byte 15 (PB15 / SB1)							
	19		Data Byte 16 (PB16 / SB2)							
	20		Data Byte 17 (PB17 / SB3)							
	21		Data Byte 18 (PB18 / SB4)							
	22		Data Byte 19 (PB19 / SB5)							
	23		Data Byte 20 (PB20 / SB6)							
	24		Data Byte 21 (PB21 / SB0)							
	25		Data Byte 22 (PB22 / SB1)							
	26		Data Byte 23 (PB23 / SB2)							
	27		Data Byte 24 (PB24 / SB3)							
	28		Data Byte 25 (PB25 / SB4)							
	29		Data Byte 26 (PB26 / SB5)							
	30		Data Byte 27 (PB27 / SB6)							

3.3.1.9 Timing Registers (Word Address = $3B)

The 12-bit **APPL[11:0] (Active Pixels Per Line) register** provides number of active pixels per line information. This register is read only. The lower 8-bit is given in Byte-0. The higher 4-bit is given in Byte-1 bit 3~0.

The 10-bit **HFP[9:0] (Horizontal Front Porch) register** provides number of pixels from the end of active data to the beginning of Horizontal Sync. This register is read only. The lower 8-bit is given in Byte-2. The higher 2-bit is given in Byte-3 bit 1~0.

The 10-bit **HBP[9:0] (Horizontal Back Porch) register** provides number of pixels from the end of Horizontal Sync to the beginning of active data. This register is read only. The lower 8-bit is given in Byte-4. The higher 2-bit is given in Byte-5 bit 1~0.

The 10-bit **HPW[9:0] (Horizontal Pulse Width) register** provides Horizontal Sync pulse width in number of pixels. This register is read only. The lower 8-bit is given in Byte-6. The higher 2-bit is given in Byte-7 bit 1~0.

The 12-bit **ALPF[11:0] (Active Lines Per Frame) register** provides number of active lines per frame information. This register is read only. The lower 8-bit is given in Byte-8. The higher 4-bit is given in Byte-9 bit 3~0.

The 8-bit **VFP[7:0] (Vertical Front Porch) register** provides number of lines from the end of active data to the beginning of Vertical Sync. This register is read only and is given in Byte-10.

The 8-bit **VBP[7:0] (Vertical Back Porch) register** provides number of lines from the end of Vertical Sync to the beginning of active data. This register is read only and is given in Byte-11.

The 7-bit **VPW[6:0] (Vertical Pulse Width) register** provides Vertical Sync pulse width in number of lines. This register is read only and is given in Byte-12 bit 6~0.

The 1-bit **INTL (Interlace) register** will be 1 if the video signal is in interlace mode, and 0 otherwise. This register is read only and is given in Byte-12 bit 7.

Table 3-7 Video Timing Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x3B	0	R	Active Pixels Per Line (APPL[7:0])							
	1		0	0	0	0	APPL[11:8]			
	2		Horizontal Front Porch (HFP[7:0])							
	3		0	0	0	0	0	0	HFP[9:8]	
	4		Horizontal Back Porch (HBP[7:0])							
	5		0	0	0	0	0	0	HBP[9:8]	
	6		Horizontal Pulse Width (HPW[7:0])							
	7		0	0	0	0	0	0	HPW[9:8]	
	8		Active Lines Per Frame (ALPF[7:0])							
	9		0	0	0	0	ALPF[11:8]			
	10		Vertical Front Porch (VFP[7:0])							
	11		Vertical Back Porch (VBP[7:0])							
	12		INTL	Vertical Pulse Width (VPW[6:0])						

3.3.1.10 Status Register 0 (Word Address = $3C, Byte 0)

Table 3-8 Status Register 0

Word Address = $3C, Byte 0

	7	6	5	4	3	2	1	0
R	-		AVMUTE	HDMI	AUTH	ENC_EN	DST_double	LAYOUT
W	-		AVMUTE_R					
Pin Reset:	0	1	0	-	-	-	-	-

AVMUTE — (Read Only) AVMUTE signal decoded from HDMI General Control Packet.
1 = AVMUTE is in set state.
0 = AVMUTE is in clear state.

AVMUTE _R — (Write Only) AVMUTE reset.
1 = Clear AVMUTE.
0 = No operation.

HDMI — (Read Only) HDMI/DVI signalling indicator
1 = HDMI signalling detected.
0 = DVI signalling detected.

AUTH — (Read Only) HDCP Authentication indicator
1 = Indicating HDCP Authentication is done.
0 = Indicating HDCP Authentication is not done.

ENC_EN — (Read Only) HDCP Encryption Enabled indicator
1 = Indicating incoming signal is HDCP encrypted.
0 = Indicating incoming signal is not HDCP encrypted.

DST_double — (Read Only) DST audio transfer rate indicator. Only valid if DST audio source is selected.
1 = DST audio is in double transfer rate.
0 = DST audio is in normal transfer rate.

LAYOUT — (Read Only) The LAYOUT bit extracted from HDMI audio packet.
1 = LAYOUT bit is 1 indicating 4 audio streams are being received.
0 = LAYOUT bit is 0 indicating 1 audio stream is being received.

3.3.1.11 Status Register 1 (Word Address = $3D, Byte 0)

Table 3-9 Status Register 1

Word Address = $3D, Byte 0

	7	6	5	4	3	2	1	0
R	LINK_ON	DE_VALID	-	A_UF	A_OF	-		
W								
Pin Reset:	-	-	-	-	-	1	0	0

LINK_ON — (Read Only) Link On indicator for selected HDMI Port. Only valid when HDMI is not in power down mode.
1 = Valid clock signal detected at selected HDMI Port.
0 = No clock signal presents at selected HDMI Port.

DE_VALID — (Read Only) DE Valid indicator for HDMI receiver.
1 = Valid DE signal detected at HDMI receiver.
0 = No valid DE signal presents at HDMI receiver.

A_UF — (Read Only) Audio FIFO underflow flag. Set by audio logic. Cleared by read of Status Register 1.
1 = Audio FIFO underflow detected.
0 = Normal

A_OF — (Read Only) Audio FIFO overflow flag. Set by audio logic. Cleared by read of Status Register 1.
1 = Audio FIFO overflow detected.
0 = Normal

3.3.1.12 SPDIF Channel Status Register (Word Address = $3E)

The first 40 bits of the SPDIF Channel Status code (referred to as CS[39:0] with CS[0] being the first bit) are extracted from audio packets and put in this register set. CS[7:0] is stored in Byte-0[7;0], CS[15:8] is stored in Byte-1[7;0], CS[23:16] is stored in Byte-2[7;0], CS[31:24] is stored in Byte-3[7;0] and CS[39:32] is stored in Byte-4[7;0]. All the bits in this register set are Read Only.

Refer to IEC60958 specification for the detailed description of each bit. The following table shows the bit definition for Consumer Use Application.

Table 3-10 SPDIF Channel Status Registers (Consumer Use)

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x3E	0	R	MODE[1:0]		PRE[2:0]			COPY	PCM	PRO = 0
	1		CAT_CODE[7:0]							
	2		CH_NUM[3:0]				SRC_NUM[3:0]			
	3		RSVD		CLK_ACC[1:0]		SAMP_FREQ[3:0]			
	4		ORG_SAMP_FREQ[3:0]				SAMP_LEN[2:0]			MAX_LEN

3.3.1.13 Status Register 2 (Word Address = $3F, Byte 0)

Table 3-11 Status Register 2

Word Address = $3F, Byte 0

	7	6	5	4	3	2	1	0
R	EE_SUM[7:0]							
W								
Pin Reset:	-	-	-	-	-	1	0	0

EE_SUM[7:0] — (Read Only) EE Check Sum.

When EE download is completed, the 8-bit EE Check Sum is put in this register by down load logic.

3.3.1.14 General Control Register 0 (Word Address = $40, Byte 0)

Table 3-12 General Control Register 0

Word Address = $40, Byte 0

	7	6	5	4	3	2	1	0
R W	MUTE_POL	DDC_DIS	DE_RST_EN	HDCP_RST	SOFT_RST	PWR_DWN	EDID_EN	-
Pin Reset:	0	0	0	0	0	0	0	0

MUTE_POL — AV_MUTE output polarity control

1 = AV_MUTE pin output is active low. A low level indicate mute.

0 = AV_MUTE pin output is active high. A high level indicate mute.

DDC_DIS — Disable DDC port connection
1 = Disable DDC port connection. On-chip DDC registers are not accessible by the HDMI source.
0 = Normal.

DE_RST_EN — Enable invalid DE to reset HDCP
1 = Allow HDCP logic to be reset when invalid DE is detected. HDCP will start from non-authed and non-encrypted state after this reset.
0 = Normal.

HDCP_RST — HDCP Reset
1 = Reset the HDCP logic. HDCP will start from non-authed and non-encrypted state after this reset.
0 = Normal.

SOFT_RST — Soft Reset
1 = Reset all the HDMI and HDCP logic except IIC registers.
0 = Normal.

PWR_DWN — Power Down
1 = HDMI is in Power Down mode. HDMI and HDCP logic are reset except IIC registers
0 = Normal.

EDID_EN — On-Chip EDID control
1 = Enable on-chip EDID.
0 = Disable On-chip EDID.

3.3.1.15 General Control Register 1 (Word Address = $41, Byte 0)

Table 3-13 General Control Register 1

Word Address = $41, Byte 0

	7	6	5	4	3	2	1	0
R	VPOL_R	HPOL_R	DCLK_POL	DCLK_DDR	AOUT_DIS[1:0]		VOUT_DIS[1:0]	
W	VPOL_W	HPOL_W						
Pin Reset:	0	0	0	0	0	0	0	0

V_POL_R — (Read Only) HDMI VSYNC polarity detection indicator
1 = HDMI VSYNC is active low (high during active period).
0 = HDMI VSYNC is active high (low during active period).

V_POL_W — (Write Only) VSYNC output polarity control
1 = Inverse VSYNC output polarity.
0 = Normal.

H_POL_R — (Read Only) HDMI HSYNC polarity detection indicator
1 = HDMI HSYNC is active low (high during active period).
0 = HDMI HSYNC is active high (low during active period).

H_POL_W — (Write Only) HSYNC output polarity control
1 = Inverse HSYNC output polarity.
0 = Normal.

CLK_POL — Data Clock Polarity
1 = Data at D0[7:0], D1[7:0] and D2[7:0] pins are changed at the rising edge of DCLK pin.
0 = Data at D0[7:0], D1[7:0] and D2[7:0] pins are changed at the falling edge of DCLK pin

DCLK_DDR — DCLK output DDR control
1 = DCLK output is divided by 2 (half the pixel rate).
0 = Normal.

AOUT_DIS[1:0] — Audio Output Disable mode
00 = MCLK, IIS_SCK, IIS_SD0, IIS_SD1, IIS_SD2, IIS_SD3, IIS_WS and SPDIF pins are normal outputs.
01 = IIS_SCK, IIS_SD0, IIS_SD1, IIS_SD2, IIS_SD3, IIS_WS pins are put in tri-state with weak pull-down. MCLK and SPDIF pins are normal output.
10 = SPDIF pin is put in tri-state with weak pull-down. MCLK, IIS_SCK, IIS_SD0, IIS_SD1, IIS_SD2, IIS_SD3, IIS_WS pins are normal output.
11 = MCLK, IIS_SCK, IIS_SD0, IIS_SD1, IIS_SD2, IIS_SD3, IIS_WS and SPDIF pins are all put in tri-state with weak pull-down.

VOUT_DIS[1:0] — Video Output Disable mode
00 = D0[7:0], D1[7:0], D2[7:0], DE, VSYNC, HSYNC, DCLK pins are normal outputs.
01 = D0[7:0], D1[7:0], D2[7:0], DE, VSYNC, HSYNC, DCLK pins are normal outputs.
10 = D0[7:0], D1[7:0], D2[7:0], DE, VSYNC, HSYNC, DCLK pins are normal outputs.
11 = D0[7:0], D1[7:0], D2[7:0], DE, VSYNC, HSYNC, DCLK pins are all put in tri-state with weak pull-down.

3.3.1.16 General Control Register 2 (Word Address = $42, Byte 0)

Table 3-14 General Control Register 2

Word Address = $42, Byte 0

	7	6	5	4	3	2	1	0
R/W	OUT422	IN422	OUT_YCC	IN_YCC	YCC_range	CS	PR[1:0]	
Pin Reset:	0	0	0	0	0	0	0	0

OUT422 — Output format control (digital output only)
1 = Digital output in 422 format
0 = Digital output in 444 format

IN422 — Specify HDMI input format
1 = HDMI input is in 422 format
0 = HDMI input is in 444 format

OUT_YCC — Output mode control (digital output only)
1 = Digital output in YCC mode
0 = Digital output in RGB mode

IN_YCC — Specify HDMI input mode
1 = HDMI input is in YCC mode
0 = HDMI input is in RGB mode

Table 3-15 Usage of IN_YCC, IN422, OUT_YCC and OUT422

Output / Input	RGB	YCC444	YCC422
RGB	IN_YCC = 0 IN422 = 0 OUT_YCC = 0 OUT422 = 0	IN_YCC = 0 IN422 = 0 OUT_YCC = 1 OUT422 = 0	IN_YCC = 0 IN422 = 0 OUT_YCC = 1 OUT422 = 1
YCC444	IN_YCC = 1 IN422 = 0 OUT_YCC = 0 OUT422 = 0	IN_YCC = 1 IN422 = 0 OUT_YCC = 1 OUT422 = 0	IN_YCC = 1 IN422 = 0 OUT_YCC = 1 OUT422 = 1
YCC422	IN_YCC = 1 IN422 = 1 OUT_YCC = 0 OUT422 = 0	IN_YCC = 1 IN422 = 1 OUT_YCC = 1 OUT422 = 0	IN_YCC = 1 IN422 = 1 OUT_YCC = 1 OUT422 = 1

YCC_range — Data range for YCC in RGB/YCC conversion
1 = Full range YCC (0~255).
0 = Limited range YCC (16~235 for Y, 16~240 for CbCr)

CS— Color space used for RGB/YCC conversion
1 = ITU-R BT.709
0 = ITU-R BT.601

PR[1:0] — Pixel Repetition

These 2 bits control pixel repetition for Video outputs. The number of pixels to be repeated is equal to the number specified by these 2 bits plus 1. A zero value in this register means no repetition

3.3.1.17 General Control Register 3 (Word Address = $43, Byte 0)

Table 3-16 General Control Register 3

Word Address = $43, Byte 0

	7	6	5	4	3	2	1	0
R W	RSVDL	RSVDL	RSVDL	UVSW	D02SW	BIT_REV	V_MUTE	A_MUTE
Pin Reset:	0	0	0	0	0	0	0	0

RSVDL — Reserved Bit. Shall be programmed as 0 for normal operation.

UVSW — UV Swap Control for YCC output
1 = UV Swap enabled
0 = Normal

D02SW — Port Swap Control for D0 and D2 ports
1 = D0/D2 Swap enabled
0 = Normal

BIT_REV — Bit sequence reverse control for D0, D1 and D2 ports
1 = Bit sequence reversed in D0, D1 and D2 ports
0 = Normal

V_MUTE — Video Mute Control
1 = Video is mute
0 = Normal

A_MUTE — A_Mute Pin Control
1 = Set A_Mute Pin to high Voltage
0 = Set A_Mute Pin to Low Voltage

3.3.1.18 General Control Register 4 (Word Address = $44, Byte 0)

Table 3-17 General Control Register 4

Word Address = $44, Byte 0

	7	6	5	4	3	2	1	0
R	LINK_RST_EN	-	A_source[1:0]		-	SF_R[2:0]		
W						-		
Pin Reset:	0	0	0	0	0	0	1	0

LINK_RST_EN — Link Reset Enable
1 = HDCP & Audio Logic is reset when LINK_ON = 0.
0 = HDCP & Audio Logic is NOT reset when LINK_ON = 0

A_source — Audio Source Selection
00 = Select audio source from Standard Audio Sample Packets
01 = Select audio source from One Bit Audio Sample Packets
10 = Select audio source from HBR Audio Sample Packets
11 = Select audio source from DST Audio Sample Packets

SF_R[2:0] — (Read Only) Audio Sampling Frequency information derived from Audio Clock Regeneration Packet
000 = 32 KHz
001 = 44.1 KHz
010 = 48 KHz
011 = 88.2 KHz
100 = 96 KHz

101 = 176.4 KHz
110 = 192 KHz
111 = 768 KHz

3.3.1.19 General Control Register 5 (Word Address = $45, Byte 0)

Table 3-18 General Control Register 5

Word Address = $45, Byte 0

	7	6	5	4	3	2	1	0
R/W	SCK_POL	WS_POL	WS_M	IIS_SS	reserved	AMUTE_EN	MCLK_SEL[1:0]	
Pin Reset:	0	0	0	0	0	0	0	0

SCK_POL — IIS_SCK output polarity
1 = Inverse from IIS standard.
0 = IIS standard.

WS_POL — IIS_WS output polarity
1 = Inverse from IIS standard.
0 = IIS standard.

WS_M — IIS_WS output timing mode
1 = IIS_WS is one clock delayed compared with standard IIS timing.
0 = IIS standard.

IIS_SS — IIS sample size
1 = IIS outputs 32 bits sample size.
0 = IIS outputs 16 bits sample size.

reserved — Must be programmed 0 for normal operation.

AMUTE_EN — Audio mute enable
1 = Enable audio mute when AVMUTE is set.
0 = Audio mute is not enabled.

MCLK_SEL[1:0] — MCLK Selection

These 2 bits select audio system clock (MCLK) frequency.
00 = MCLK frequency is 128 times of audio sampling frequency
01 = MCLK frequency is 256 times of audio sampling frequency. Not valid for HBR Audio.
10 = MCLK frequency is 384 times of audio sampling frequency. Not valid for HBR Audio.
11 = MCLK frequency is 512 times of audio sampling frequency. Not valid for HBR Audio.

3.3.1.20 General Control Register 6 (Word Address = $46, Byte 0)

Table 3-19 General Control Register 6

Word Address = $46, Byte 0

	7	6	5	4	3	2	1	0
R W	SD3_PA[1:0]		SD2_PA[1:0]		SD1_PA[1:0]		SD0_PA[1:0]	
Reset:	1	1	1	0	0	1	0	0

SD3_PA[1:0] — Audio Stream assignment for IIS_SD3 output or DSD3(R/L) output
- 00 = Output Audio Stream 0
- 01 = Output Audio Stream 1
- 10 = Output Audio Stream 2
- 11 = Output Audio Stream 3

SD2_PA[1:0] — Audio Stream assignment for IIS_SD2 output or DSD2(R/L) output
- 00 = Output Audio Stream 0
- 01 = Output Audio Stream 1
- 10 = Output Audio Stream 2
- 11 = Output Audio Stream 3

SD1_PA[1:0] — Audio Stream assignment for IIS_SD1 output or DSD1(R/L) output
- 00 = Output Audio Stream 0
- 01 = Output Audio Stream 1
- 10 = Output Audio Stream 2
- 11 = Output Audio Stream 3

SD0_PA[1:0] — Audio Stream assignment for IIS_SD0 output or DSD0(R/L) output
- 00 = Output Audio Stream 0
- 01 = Output Audio Stream 1
- 10 = Output Audio Stream 2
- 11 = Output Audio Stream 3

3.3.1.21 General Control Register 8 (Word Address = $48, Byte 0)

Table 3-20 General Control Register 8

Word Address = $48, Byte 0

	7	6	5	4	3	2	1	0
R W	CTS_ADJ_MODE[1:0]		TCYCLE[2:0]			EE_DIS	reserved	DSD_OPT
Pin Reset:	0	0	0	0	0	0	0	0

CTA_ADJ_mode[1:0] — A parameter to control audio tracking speed when CTS_ADJ_DIS is cleared. These bits shall be set to 0 for normal operation.

TCYCLE[2:0] — A parameter to control data judgement of HDMI sampling logic. These bit shall be set to a non-zero values for normal operation.

EE_DIS — EE Download Disable
1 = Disable HDCP key downloading from external EE. HDCP keys are written by MCU.
0 = Enable HDCP key downloading from external EE.

reserved— Should be programmed as 0 for normal operation

DSD_OPT — DSD Audio Output Option
1 = DSD Audio output to DSP.
0 = DSD Audio output to DAC.

3.3.1.22 RX PHY Control Register (Word Address = $49, Byte 0)

Table 3-21 Analog Input Control Register

Word Address = $49, Byte 0

bit	7	6	5	4	3	2	1	0
R/W	PLL_PHD	RX_PLL_REG	EQ_BIAS[1:0]		RX_PLL_PUMP[1:0]		RX_PLL_BW	EQ_GAIN
Pin Reset:	0	0	0	0	0	0	0	0

PLL_PHD — Audio PLL Phase Detector Control
1 = fixed
0 = variable

RX_PLL_REG — RX PLL Regulator Control
1 = Enable
0 = Disable

EQ_BIAS[1:0] — RX EQ Bias Current Control
00 = 150 uA
01 = 125 uA
10 = 100 uA
11 = 80 uA

RX_PLL_PUMP[1:0] — RX PLL Charge Pump Current Control
00 = 10 uA
01 = 20 uA
10 = 40 uA
11 = 40 uA

RX_PLL_BW — RX PLL Bandwidth Control
1 = 4.1MHz ~ 6.2MHz
0 = 4MHz

EQ_GAIN — RX EQ Gain Control
1 = 6 dB
0 = 11 dB

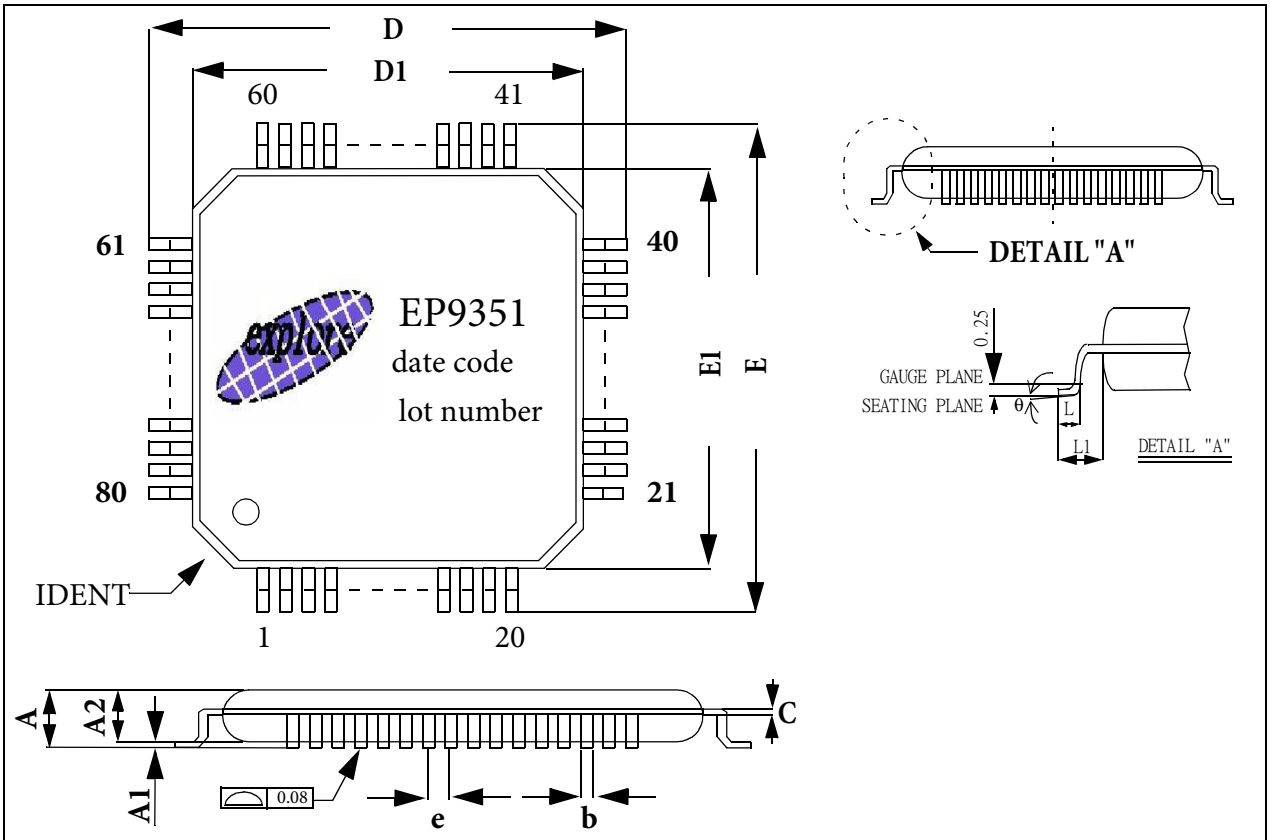
3.3.1.23 EDID Data Register (Word Address = $FF, Byte 0~255)

Word Address from $FF is used for downloading the EDID data to the on-chip EDID RAM. The 256 data bytes in this register set correspond to the 256 byte EDID data. The on-chip EDID RAM can be enabled or disabled by setting the control bit EDID_EN which located at Word Address 0x40, bit 1.

Appendix A Package

A.1 LQFP Package for EP9351

Figure A-1 LQFP Footprint Diagram V



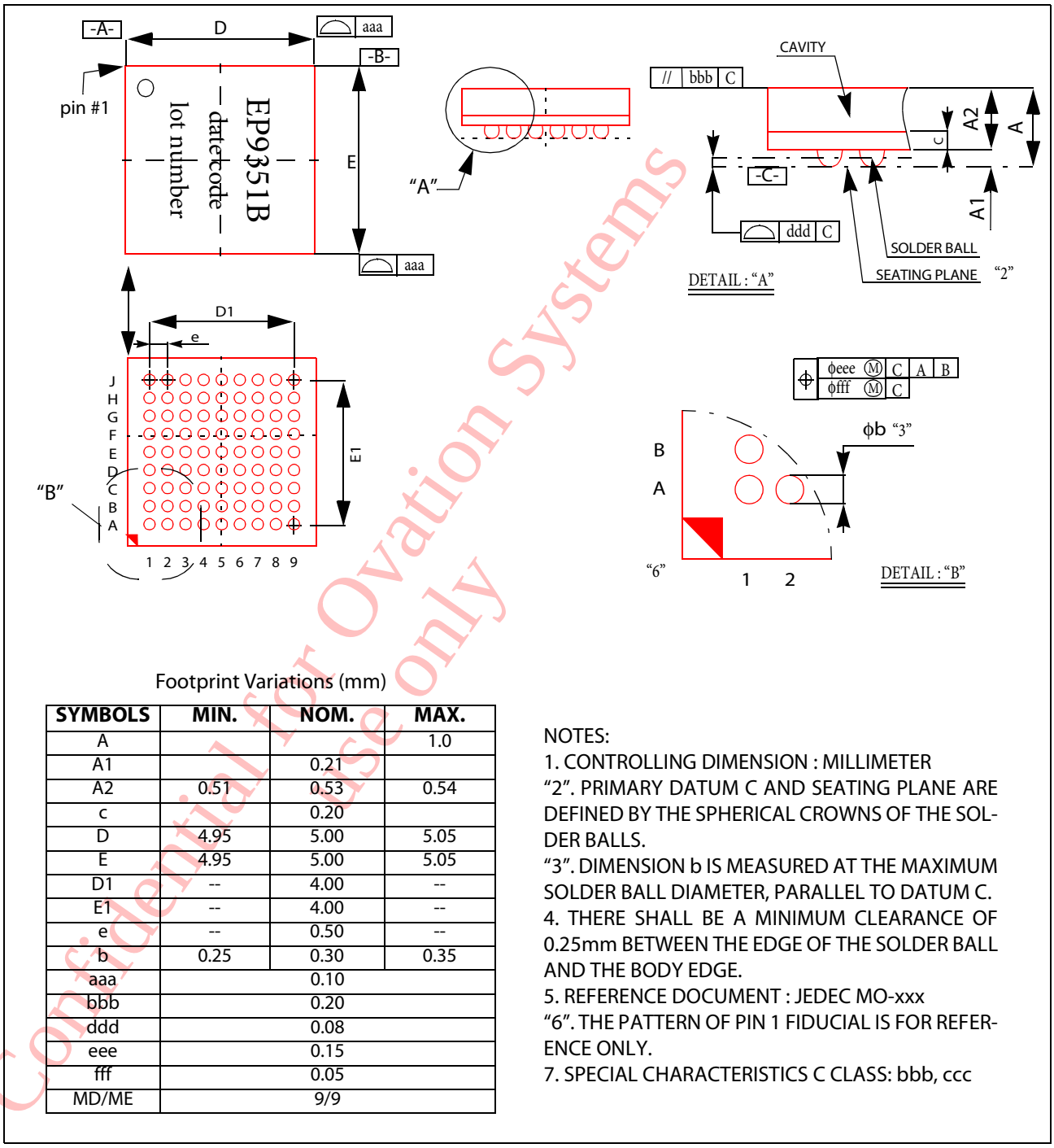
Footprint Variations (mm)

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
C	0.09	-	0.16
D	12.00 BSC		
D1	10.00 BSC		
e	0.40 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0"	3.5"	7"

NOTES:
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

A.2 VFBGA Package for EP9351B

Figure A-2 VFBGA-81 Footprint Diagram



Footprint Variations (mm)

SYMBOLS	MIN.	NOM.	MAX.
A			1.0
A1		0.21	
A2	0.51	0.53	0.54
c		0.20	
D	4.95	5.00	5.05
E	4.95	5.00	5.05
D1	--	4.00	--
E1	--	4.00	--
e	--	0.50	--
b	0.25	0.30	0.35
aaa		0.10	
bbb		0.20	
ddd		0.08	
eee		0.15	
fff		0.05	
MD/ME		9/9	

NOTES:
1. CONTROLLING DIMENSION : MILLIMETER
"2". PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
"3". DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERENCE DOCUMENT : JEDEC MO-xxx
"6". THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
7. SPECIAL CHARACTERISTICS C CLASS: bbb, ccc