HDMI 1.4 Repeater with Audio, VGA and Scaled LVDS Outputs

EP94Z3(K)

Data Sheet V0.4

Revised Date: Sep. 27, 2013

Original Release Date: Aug. 29, 2011

Explore

Revision History

Version Number	Revision Date	Author	Description of Changes
0.1	Nov/03/2011	Ether Lai	Initial Version
0.2	Apr/17/2012	Ether Lai	Revise the Electrical Characteristics; Add the optional part number EP94Z3K
0.3	May/03/2013	Ken Chen	Revised the MHL version to 2.0;
0.4	Sep/27/2013	Ken Chen	Remove the typo, EXT_RES.

Section 1 Introduction

1.1 Overview

EP94Z3(K) is an HDMI 1.4 Repeater with Audio, VGA and Scaled LVDS outputs. The chip supports 1 HDMI/MHL RX port and 1 HDMI TX port with repeater function. The chip also supports decoded Audio, VGA and scaled LVDS outputs.

With the Scaled LVDS output, the chip provides a converted video output which can be in a different resolution from that of the HDMI input. The on-chip Scaler is able to scale the input video up or down to any resolution within the range of 0.5X to 2X in both Horizontal and Vertical direction. This is adequate for converting an EIA standard video to fit an LCD panel in different resolution.

The chip is compliant with HDMI 1.4 and supports SD/HD Audio and HD/3D Video up to 1080p. The chip also supports on-chip HDCP RX/TX engines and EDID RAM.

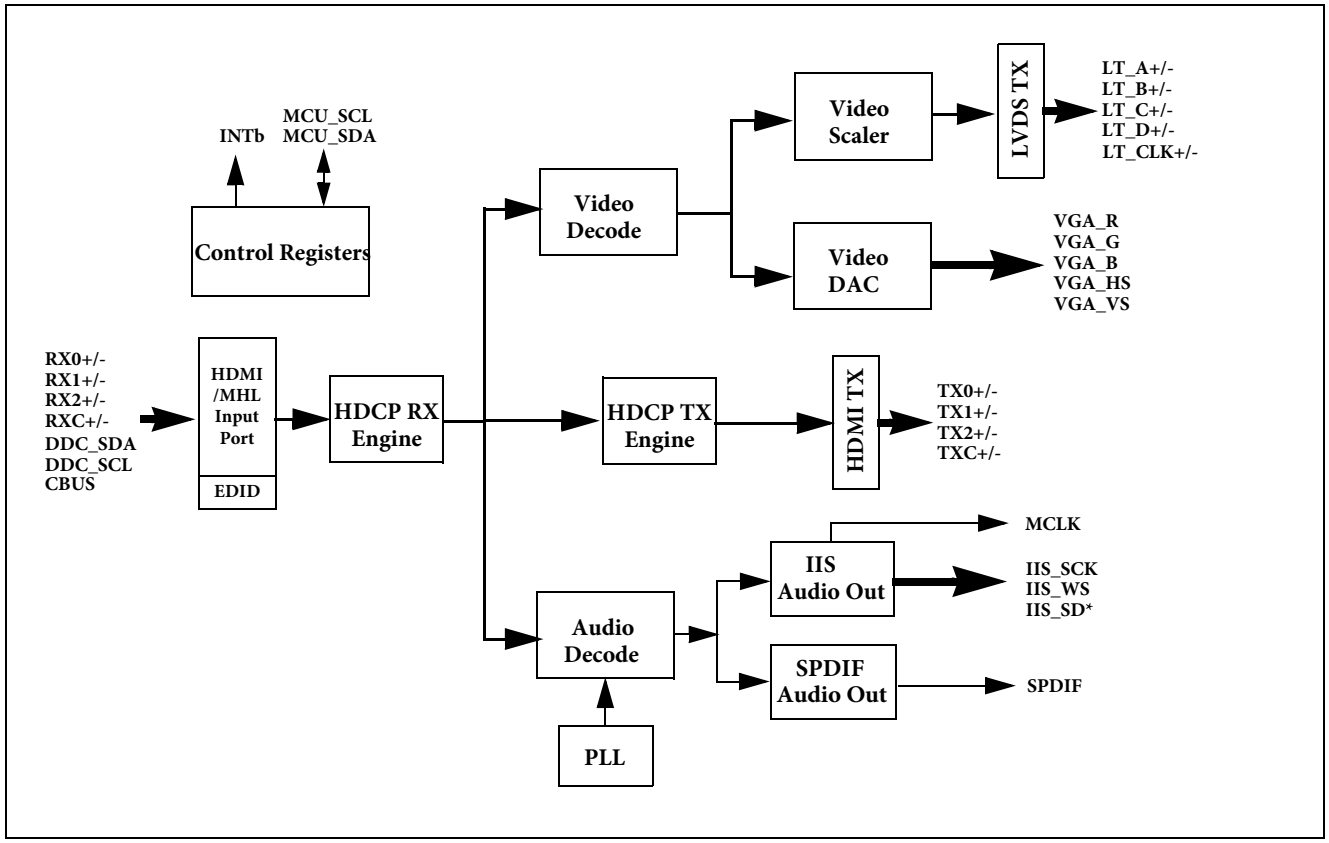
1.2 Features

- On-chip HDMI/MHL Receiver which is compliant with HDMI 1.4b and MHL 2.0 specification
- On-chip HDMI Transmitter core which is compliant with HDMI 1.4b specification
- On-chip HDCP RX/TX Engine which is compliant with HDCP 1.4 specification
- On-chip Video Up/Down Scaler
- On-chip LVDS Transmitter supporting up to 150 Mhz pixel rate
- On-chip DAC supporting up to 150 Mhz pixel rate for VGA output port
- On-chip EDID RAM
- On-Chip HDCP Key (Available for EP94Z3K)
- On-chip Audio Decoder which support 8-channel IIS, S/PDIF and DSD audio outputs
- Support HDMI Repeater function
- Support YCC422 to YCC444 conversion
- Support YCC to RGB conversion in ITU-R BT.601 and 709 color space
- Support Separate Sync and/or SOG (Sync On Green) on VGA output
- Support LPCM, Compressed Surround Audio, HD (HBR) Audio and DSD audio
- Support audio soft mute
- Support SPDIF Channel Status extraction
- Register-programmable via slave IIC interface
- Low stand-by current (< 1mA) at power down mode
- 80-pin LQFP package

Section 2 Overview

2.1 Block Diagram

Figure 2-1 Block Diagram



2.2 Pin Diagram

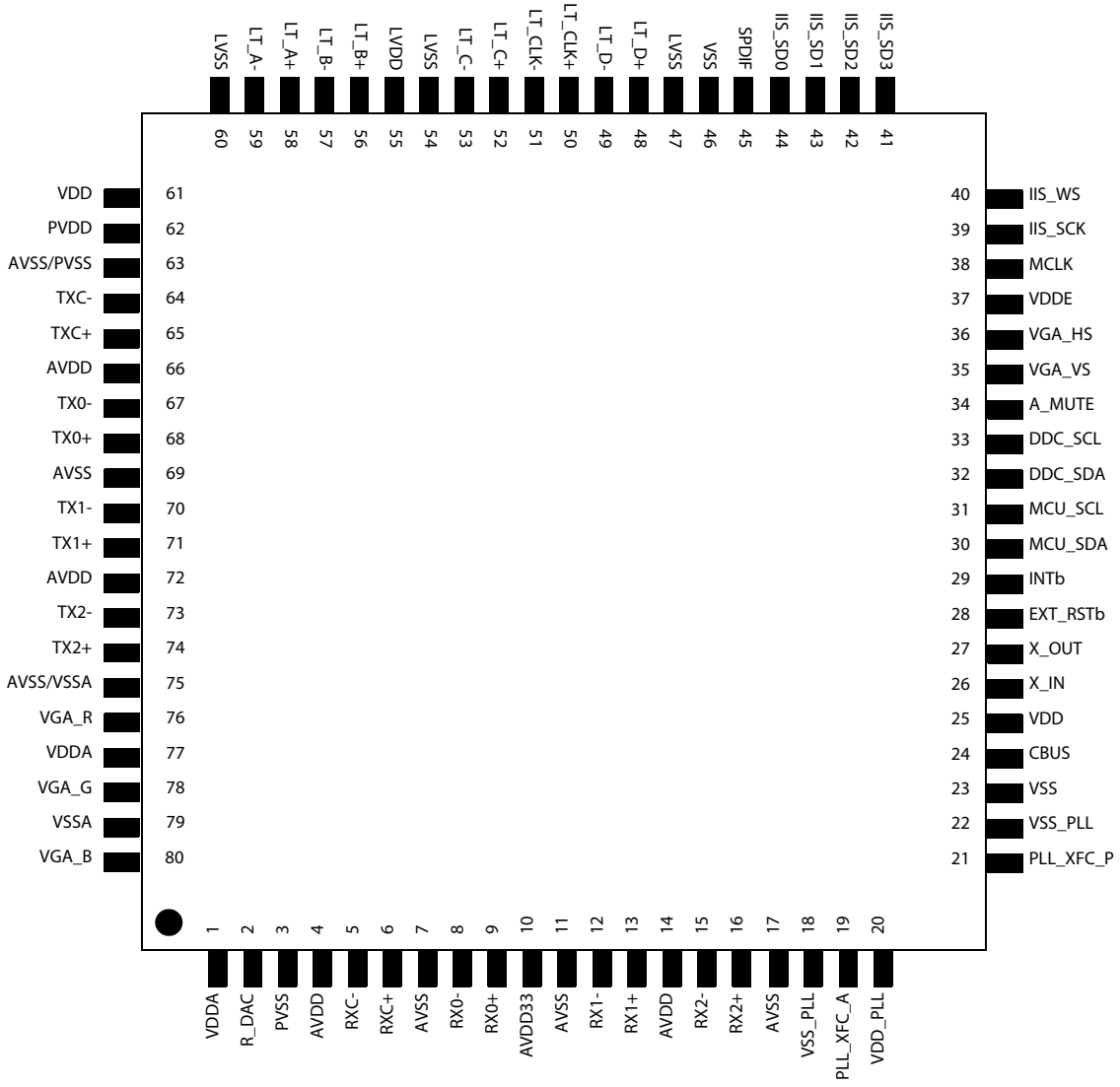


Figure 2-2 Pin Diagram

2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 HDMI/MHL Input Port

Name	In/Out	Description
RXC-	IN	HDMI Receiver Differential Clock Input Pair
RXC+	IN	HDMI Receiver Differential Clock Input Pair
RX0-	IN	HDMI/MHL Receiver Differential Data Input Pair1
RX0+	IN	HDMI/MHL Receiver Differential Data Input Pair1
RX1-	IN	HDMI Receiver Differential Data Input Pair1
RX1+	IN	HDMI Receiver Differential Data Input Pair1
RX2-	IN	HDMI Receiver Differential Data Input Pair2
RX2+	IN	HDMI Receiver Differential Data Input Pair2
DDC_SCL	IN	IIC SCL signal for HDMI RX DDC Port
DDC_SDA	IO	IIC SDA signal for HDMI RX DDC Port
CBUS	IO	CBUS signal for MHL RX Port

Table 2-2 LVDS Output Port

Name	In/Out	Description
LT_CLK-	OUT	Differential Clock Output Pair for LVDS Output
LT_CLK+	OUT	Differential Clock Output Pair for LVDS Output
LT_A-	OUT	Differential Data Output PairA for LVDS Output
LT_A+	OUT	Differential Data Output PairA for LVDS Output
LT_B-	OUT	Differential Data Output PairB for LVDS Output
LT_B+	OUT	Differential Data Output PairB for LVDS Output
LT_C-	OUT	Differential Data Output PairC for LVDS Output
LT_C+	OUT	Differential Data Output PairC for LVDS Output
LT_D-	OUT	Differential Data Output PairD for LVDS Output
LT_D+	OUT	Differential Data Output PairD for LVDS Output

Table 2-3 HDMI Output Port

Name	In/Out	Description
TXC-	OUT	Differential Clock Output Pair for HDMI Output
TXC+	OUT	Differential Clock Output Pair for HDMI Output
TX0-	OUT	Differential Data Output Pair0 for HDMI Output
TX0+	OUT	Differential Data Output Pair0 for HDMI Output
TX1-	OUT	Differential Data Output Pair1 for HDMI Output
TX1+	OUT	Differential Data Output Pair1 for HDMI Output
TX2-	OUT	Differential Data Output Pair2 for HDMI Output
TX2+	OUT	Differential Data Output Pair2 for HDMI Output

Table 2-4 VGA Output Port

Name	In/Out	Description
VGA_B	OUT	VGA Analogue Blue output
VGA_G	OUT	VGA Analogue Green output
VGA_R	OUT	VGA Analogue Red output
R_DAC	Analog	For connecting a resistor to VSSA to set DAC output current
VGA_VS	IN/OUT	Vertical Sync Output.
VGA_HS	IN/OUT	Horizontal Sync Output.

Table 2-5 Audio Outputs

Name	In/Out	Description
MCLK	OUT	System Clock output for audio DAC (128/256/384/512 * $F_{Sampling\_Clock}$. Connecting a pull-up (logic 1) or pull-down (logic 0) resistor at this pin defines bit 4 of the slave IIC Address
IIS_SCK	OUT	IIS SCK output for IIS audio port. Sampling clock output for DSD.
IIS_WS/DSD2R	OUT	IIS WS output for all IIS audio ports. DSD audio output port 2 (Right Channel).
IIS_SD0/DSD0L	OUT	IIS SD output for audio port 0 or HBR audio output. DSD audio output port 0 (Left Channel).
IIS_SD1/DSD0R	OUT	IIS SD output for audio port 1 or HBR audio output. DSD audio output port 0 (Right Channel).
IIS_SD2/DSD1L	OUT	IIS SD output for audio port 2 or HBR audio output. DSD audio output port 1 (Left Channel).
IIS_SD3/DSD1R	OUT	IIS SD output for audio port 3 or HBR audio output. DSD audio output port 1 (Right Channel).
SPDIF/DSD2L	OUT	SPDIF output. DSD audio output port 2 (Left Channel).
A_MUTE	OUT	Audio Mute Output

Table 2-6 Misc. Pins

Name	In/Out	Description
MCU_SCL	IN	SCL signal for slave IIC port
MCU_SDA	IO	SDA signal for slave IIC port
INTb	OUT	Interrupt output to MCU.
EXT_RSTb	IN	External Reset input (Active Low) with internal weak pull-up.
X_IN	Analog	External Crystal Input, 24 Mhz
X_OUT	Analog	External Crystal Output, 24 Mhz
PLL_XFC_A	Analog	For connecting the R/C components to ground for on-chip PLL
PLL_XFC_P	Analog	For connecting the R/C components to ground for on-chip PLL

Table 2-7 Power Pins

Name	In/Out	Description
AVDD33	PWR	HDMI Termination Power (3.3V)
AVDD	PWR	HDMI RX/TX Analog Power (1.8V)
AVSS	GND	HDMI RX/TX Analog Ground
PVDD	PWR	HDMI RX/TX PLL Analog Power (1.8V)
PVSS	GND	HDMI RX/TX PLL Analog Ground
LVDD	PWR	LVDS Analog Power (3.3V)
LVSS	GND	LVDS Analog Ground
VDDA	PWR	ADC Analog Power (1.8V)
VSSA	GND	ADC Analog Ground
VDDE	PWR	I/O Logic Power (3.3V)
VDD	PWR	Core Logic Power (1.8V)
VSS	GND	Digital Ground
VDD_PLL	GND	PLL VDD (1.8V)
VSS_PLL	GND	PLL Ground

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	-0.3		4.0	V
Vcc18	1.8V Supply Voltage	-0.3		2.5	V
V_I	Input Voltage	-0.3		V_{cc33} + 0.3	V
V_O	Output Voltage	-0.3		V_{cc33} + 0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-40		125	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		50		°C/W
θ_{JC}	Thermal Resistance (Junction to Case)		11		°C/W

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc33	3.3V Supply Voltage	3.14	3.3	3.6	V
Vcc18	1.8V Supply Voltage	1.71	1.8	1.98	V
V_{CCN}	Supply Voltage Noise[1]	-0.3		100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	uA

CBUS I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH_CBUS}	CBUS High-level Input Voltage		1.0			V
V_{IL_CBUS}	CBUS Low-level Input Voltage				0.6	V
V_{OH_CBUS}	CBUS High-level Output Voltage	VDD = 1.8V	1.5		1.9	V
V_{OL_CBUS}	CBUS Low-level Output Voltage				0.2	V
I_{IH_CBUS}/I_{IL_CBUS}	Input Leakage Current	High Impedance	-1		1	uA
$Z_{CBUS\_SINK\_DISCOVER}$	CBUS Pull Down Resistance	Discovery	800		1200	Ω
$Z_{CBUS\_SINK\_ON}$	CBUS Pull Down Resistance	Active	90K		110K	Ω

DC Analogue Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OD}	Differential Output Voltage Single ended peak to peak amplitude	R_{LOAD} = 50 ohm		510	550	590	mV
V_{DOH}	Differential High-level Output Voltage[1]				AVCC		V
I_{DOS}	Differential Output Short Circuit Current	V_{OUT} = 0V; TX_TERM bit is 0				5	uA
I_{PD}	Power-Down Current[2]	25°C Ambient	3V3		10		uA
			1V8		30		uA
I_{CCD}	Supply Current (25°C Ambient, HDMI RX/TX are Active, TX_TERM bit is 1)	1080p 12-bits	3V3		32		mA
			1V8		380		mA
	Supply Current (25°C Ambient, HDMI RX/TX, VGA and LVDS TX are Active, TX_TERM bit is 1)	1080p 8 bits	3V3		56		mA
			1V8		398		mA
		720p 8 bits	3V3		56		mA
			1V8		328		mA
	Supply Current (25°C Ambient, MHL RX, HDMI TX, VGA and LVDS TX are Active, TX_TERM bit is 1)	720p, 60Hz, RGB444	3V3		47		mA
			1V8		243		mA

1 Guaranteed by design.

2 Assumes all HDMI/DVI I/O ports are not connected and all digital inputs are silent.

HDMI/MHL Receiver AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]				0.4	T_{bit}
T_{CCS}	Channel to Channel Differential Input Skew[1]				1.0	T_{pixel}
T_{IJIT}	Differential Input Clock Jitter Tolerance[2,3]				0.3	T_{bit}
F_{CIP1}	TMDS CLK Frequency (HDMI mode)		25		225	MHz
F_{CIP2}	Common Mode Input Frequency (MHL mode)		25		75	MHz

NOTES:

1. Guaranteed by design.
2. Jitter defines as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electronic Measurement Procedures*

HDMI Transmitter AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
S_{LHT}	Differential Swing Low-to-High Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm, R_{EXT_SWING} = 270 ohm	170	200	230	ps
S_{HLT}	Differential Swing High-to-Low Transition Time	C_{LOAD} = 5pF, R_{LOAD} = 50 ohm, R_{EXT_SWING} = 270 ohm	170	200	230	ps

I2S Audio AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{sck}	SCK Clock Period	C_L = 10pF		1		T_{sck}
T_{sck_d}	SCK Clock Duty Cycle	C_L = 10pF	40%		60%	T_{sck}
T_{sck_h}	SCK Clock High Time	C_L = 10pF	40%		60%	T_{sck}
T_{sck_l}	SCK Clock LOW Time	C_L = 10pF	40%		60%	T_{sck}
T_{iis_s}	SCK to SD and WS (Setup Time)	C_L = 10pF	40%		-	T_{sck}
T_{iis_h}	SCK to SD and WS (Hold Time)	C_L = 10pF	40%		-	T_{sck}

SPDIF Audio AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units

T_{spdif}	SPDIF Cycle Time	C_L = 10pF		1		UI
T_{spdif_d}	SPDIF Duty Cycle	C_L = 10pF	90%		110%	UI

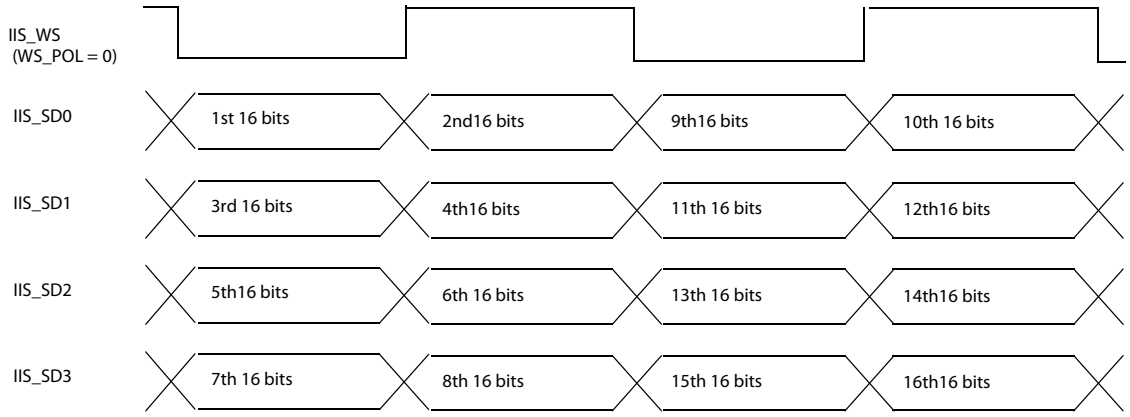
LVDS Transmitter DC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage	R_L = 100 Ω, Normal Swing (LVDS_SWING = 1)	250	350	450	mV
		R_L = 100 Ω, Reduced Swing (LVDS_SWING = 0)	100	200	300	
ΔV_{OD}	Change in V_{OD} between complimentary output states	R_L = 100 Ω			35	mV
V_{OC}	Common Mode Voltage		1.125	1.25	1.375	V
ΔV_{OC}	Change in V_{OC} between complimentary output states				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100 Ω			-10	mA
I_{OZ}	Output Tri-State Current	LVDS_ON = 0;		+/- 1	+/- 10	uA

2.5 HBR Audio Output Format

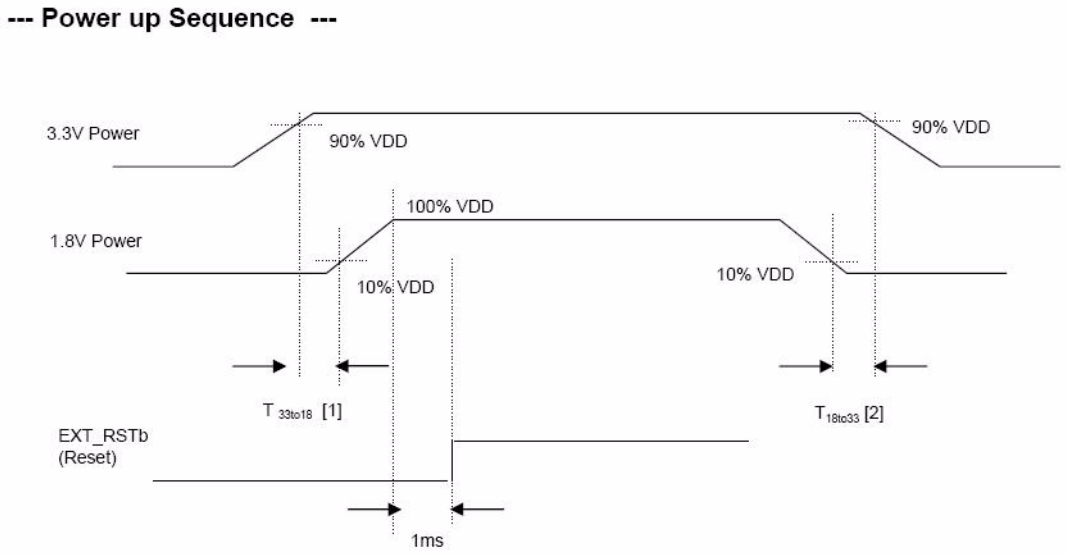
HBR (True HD High Bit Rate) audio is output from IIS pins as shown in the following figure:

Figure 2-3 HBR Audio Output Format



2.6 Power Up Sequence

Following figure shows the recommended power on sequence:



Note 1: T_{33to18} should be less than 10ms. 3.3V is powered up in the beginning, then 1.8V powered up.

Note 2: T_{18to33} should be less than 10ms. 1.8V is powered down in the beginning, then 3.3V powered down.

2.7 LVDS Output Data Mapping

The LVDS Clock wave form is shown in the following figure. Note that the rising edge of the LVDS clock occurs two LVDS sub symbols before the current cycle of data. The clock is composed of a 4 LVDS sub symbol HIGH time and a 3 LVDS sub symbol LOW time. Two types of RGB data mapping are supported. RGB data mapping is defined by a register bit LVDS_MAP.

Figure 2-4 LVDS Inputs Data (LVDS_MAP = 0)

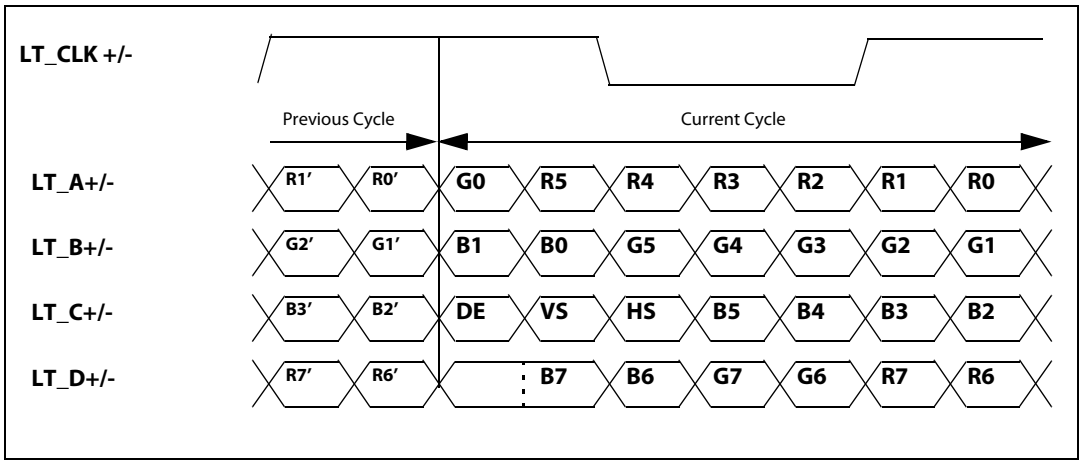
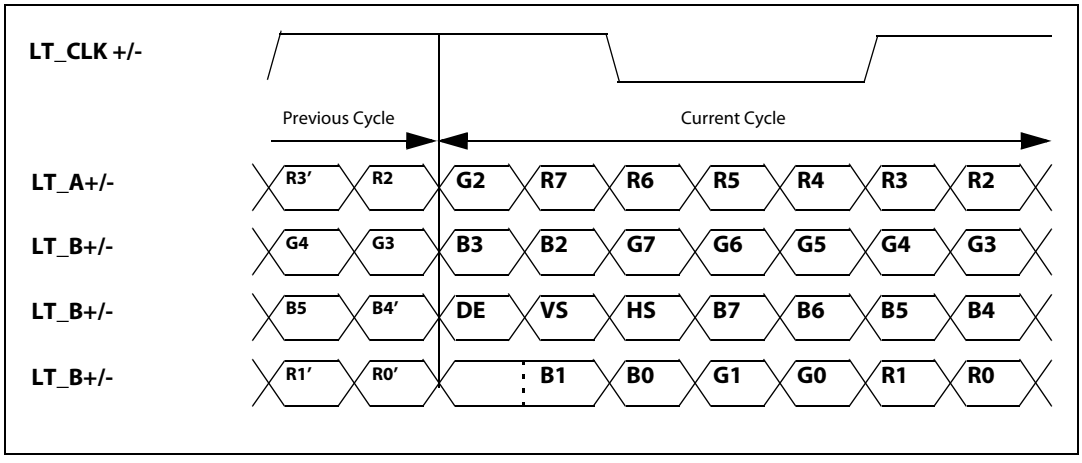
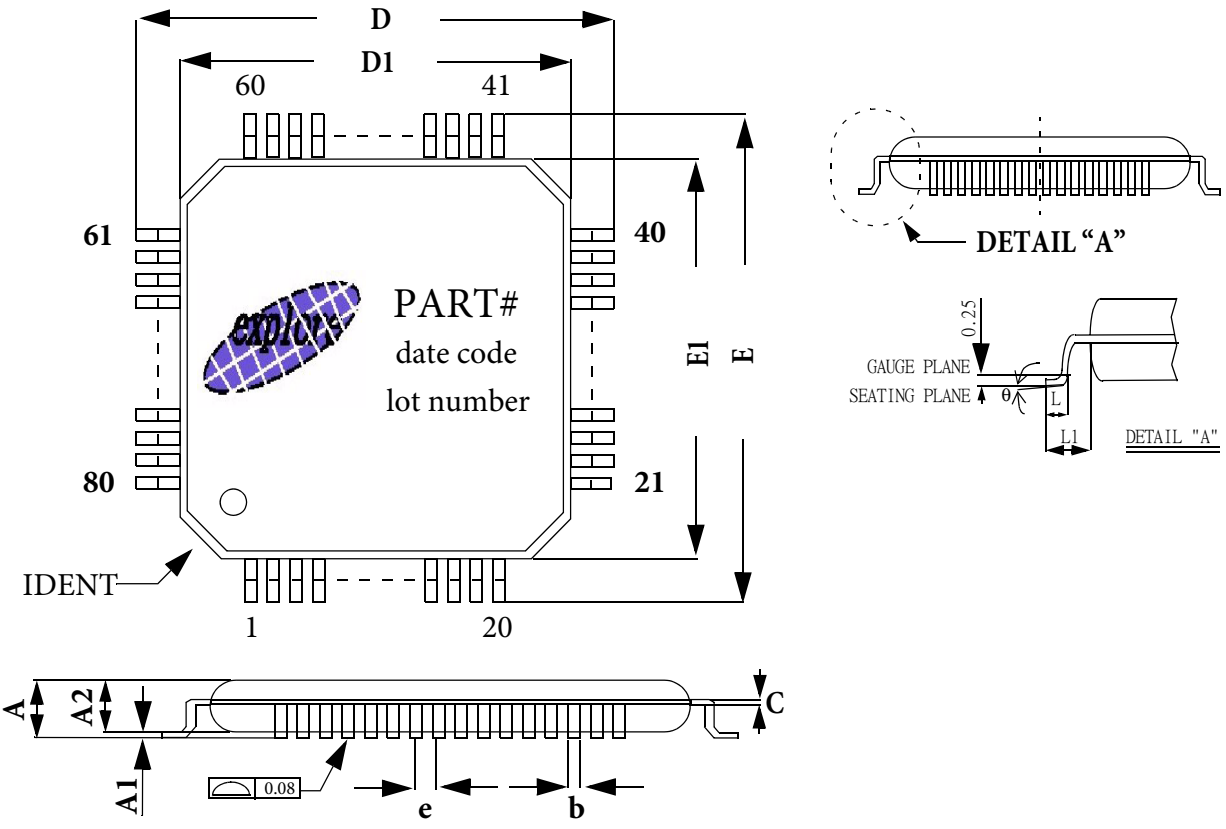


Figure 2-5 LVDS Inputs Data (LVDS_MAP = 1)



Appendix A Package

Figure A-1 EP94Z3(K) Footprint Diagram



Footprint Variations (mm)

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.6
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
C	0.09	-	0.16
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0"	3.5"	7"

NOTES:
1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.