SMD 14-Pin 5 Tap TTL Compatible Active Delay Lines

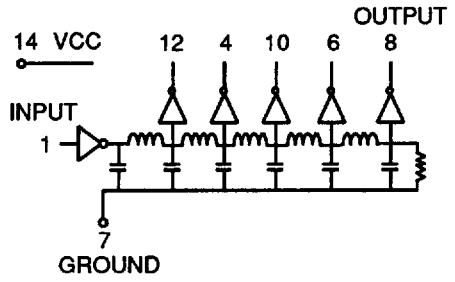
TAP DELAYS ±5% or ±2 nS	TOTAL DELAYS ±5% or ±2 nS	PART NUMBER	TAP DELAYS ±5% or ±2 nS	TOTAL DELAYS ±5% or ±2 nS	PART NUMBER
5, 10, 15, 20	25	EPA073-25	80, 160, 240, 320	400	EPA073-400
6, 12, 18, 24	30	EPA073-30	84, 168, 252, 336	420	EPA073-420
7, 14, 21, 28	35	EPA073-35	88, 176, 264, 352	440	EPA073-440
8, 16, 24, 32	40	EPA073-40	90, 180, 270, 360	450	EPA073-450
9, 18, 27, 36	45	EPA073-45	94, 188, 282, 376	470	EPA073-470
10, 20, 30, 40	50	EPA073-50	100, 200, 300, 400	500	EPA073-500
12, 24, 36, 48	60	EPA073-60	110, 220, 330, 440	550	EPA073-550
15, 30, 45, 60	75	EPA073-75	120, 240, 360, 480	600	EPA073-600
20, 40, 60, 80	100	EPA073-100	130, 260, 390, 520	650	EPA073-650
25, 50, 75, 100	125	EPA073-125	140, 280, 420, 560	700	EPA073-700
30, 60, 90, 120	150	EPA073-150	150, 300, 450, 600	750	EPA073-750
35, 70, 105, 140	175	EPA073-175	160, 320, 480, 640	800	EPA073-800
40, 80, 120, 160	200	EPA073-200	170, 340, 510, 680	850	EPA073-850
45, 90, 135, 180	225	EPA073-225	180, 360, 540, 720	900	EPA073-900
50, 100, 150, 200	250	EPA073-250	190, 380, 570, 760	950	EPA073-950
60, 120, 180, 240	300	EPA073-300	200, 400, 600, 800	1000	EPA073-1000
70, 140, 210, 280	350	EPA073-350			

Delay times referenced from input to leading edges at 25°C, 5.0V.

DC Electrical Characteristics

	Parameter	Test Conditions	Min	Max	Unit
V_{OH}	High-Level Output Voltage	V_{CC} = min. V_{IL} = max. I_{OH} = max	2.7		V
V_{OL}	Low-Level Output Voltage	V_{CC} = min. V_{IH} = min. I_{OL} = max		0.5	V
V_{IK}	Input Clamp Voltage	V_{CC} = min. I_I = I_{IK}		-1.2	V
I_{IH}	High-Level Input Current	V_{CC} = max. V_{IN} = 2.7V		50	µA
		V_{CC} = max. V_{IN} = 5.25V		1.0	mA
I_{IL}	Low-Level Input Current	V_{CC} = max. V_{IN} = 0.5V		-2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = max. V_{OUT} = 0. (One output at a time)	-40	-100	mA
I_{CCH}	High-Level Supply Current	V_{CC} = max. V_{IN} = OPEN		75	mA
I_{CCL}	Low-Level Supply Current	V_{CC} = max. V_{IN} = 0		75	mA
T_{RO}	Output Rise Time	Td ≤ 500 nS (0.75 to 2.4 Volts)		4	nS
		Td > 500 nS		5	nS
N_H	Fanout High-Level Output	V_{CC} = max. V_{OH} = 2.7V		20 TTL LOAD	
N_L	Fanout Low-Level Output	V_{CC} = max. V_{OL} = 0.5V		10 TTL LOAD	

Schematic

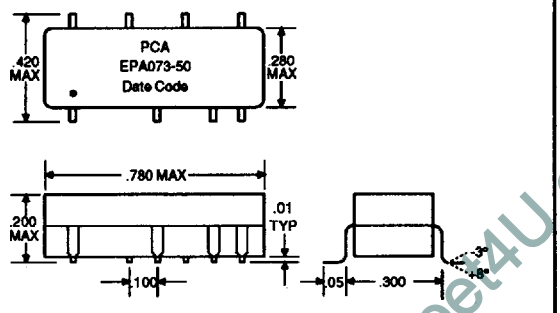


Recommended Operating Conditions

		Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IH}	High-Level Input Voltage	2.0		V
V_{IL}	Low-Level Input Voltage		0.8	V
I_{IK}	Input Clamp Current		-18	mA
I_{OH}	High-Level Output Current		-1.0	mA
I_{OL}	Low-Level Output Current		20	mA
P_W*	Pulse Width of Total Delay	40		%
d*	Duty Cycle		40	%
T_A	Operating Free-Air Temperature	0	+70	°C

**These two values are inter-dependent.*

Package Dimensions



Input Pulse Test Conditions @ 25° C

			Unit
E_{IN}	Pulse Input Voltage	3.2	Volts
P_W	Pulse Width % of Total Delay	110	%
T_{RI}	Pulse Rise Time (0.75 - 2.4 Volts)	2.0	nS
P_{RR}	Pulse Repetition Rate @ Td ≤ 200 nS	1.0	MHz
	Pulse Repetition Rate @ Td > 200 nS	100	KHz
V_{CC}	Supply Voltage	5.0	Volts

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