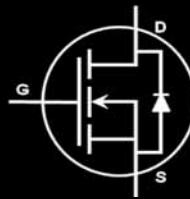


EPC1009 – Enhancement Mode Power Transistor

V_{DSS} , 60 V

$R_{DS(ON)}$, 30 mΩ

I_D , 6 A



Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 5 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(ON)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage	60	V
I_D	Continuous ($T_A = 25^\circ C$, $\theta_{JA} = 20$)	6	A
	Pulsed ($25^\circ C$, $T_{pulse} = 300 \mu s$)	25	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-5	
T_J	Operating Temperature	-40 to 125	°C
T_{STG}	Storage Temperature	-40 to 150	



EPC Power Transistors are supplied only in passivated die form with solder bumps

Applications

- High Speed DC-DC conversion
- Class D Audio
- Hard Switched and High Frequency Circuits

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Static Characteristics ($T_J = 25^\circ C$ unless otherwise stated)						
BV_{DSS}	Drain-to-Source Voltage	60			V	
I_{DSS}	Drain Source Leakage		20	60	μA	
I_{GSS}	Gate-Source Forward Leakage	$V_{GS} = 5 V$	0.25	2	mA	
	Gate-Source Reverse Leakage	$V_{GS} = -5 V$	0.1	0.5		
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1.2 mA$	0.7	1.4	2.5	V
$R_{DS(ON)}$	Drain-Source On Resistance	$V_{GS} = 5 V, I_D = 6 A$	24	30	mΩ	
Dynamic Characteristics ($T_J = 25^\circ C$ unless otherwise stated)						
C_{ISS}	Input Capacitance	$V_{DS} = 30 V, V_{GS} = 0 V$	196		pF	
C_{OSS}	Output Capacitance		120			
C_{RSS}	Reverse Transfer Capacitance		11			
Q_G	Total Gate Charge ($V_{GS} = 5 V$)	$V_{DS} = 30 V, I_D = 6 A$	2.4		nC	
Q_{GD}	Gate to Drain Charge		0.63			
Q_{GS}	Gate to Source Charge		0.75			
Q_{OSS}	Output Charge		5.8			
Q_{RR}	Source-Drain Recovery Charge		0			
Source-Drain Characteristics ($T_J = 25^\circ C$ unless otherwise stated)						
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.5 A, V_{GS} = 0 V, T = 25^\circ C$	1.8		V	
		$I_S = 0.5 A, V_{GS} = 0 V, T = 125^\circ C$	1.75			

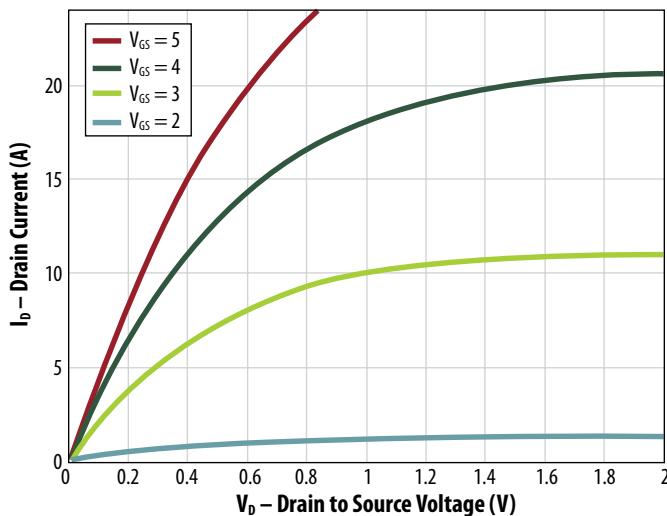
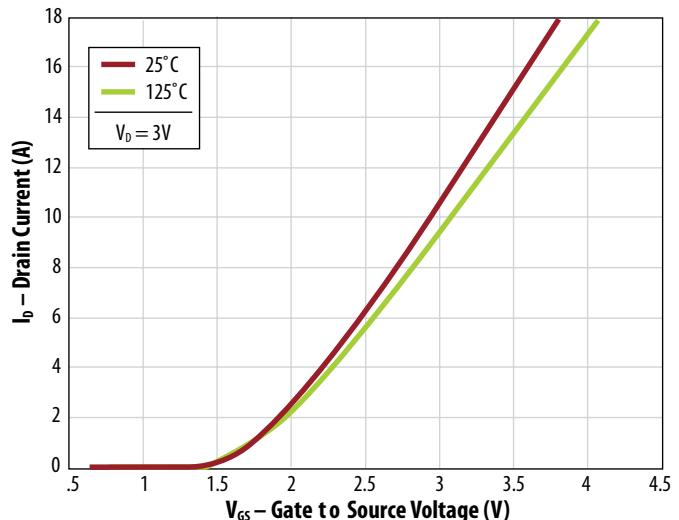
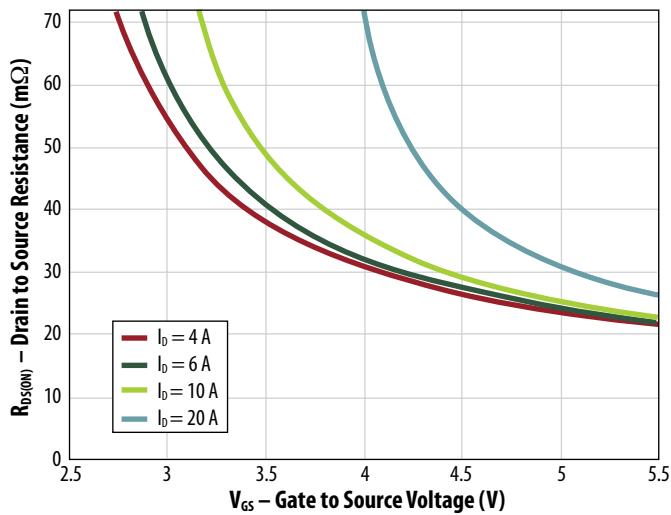
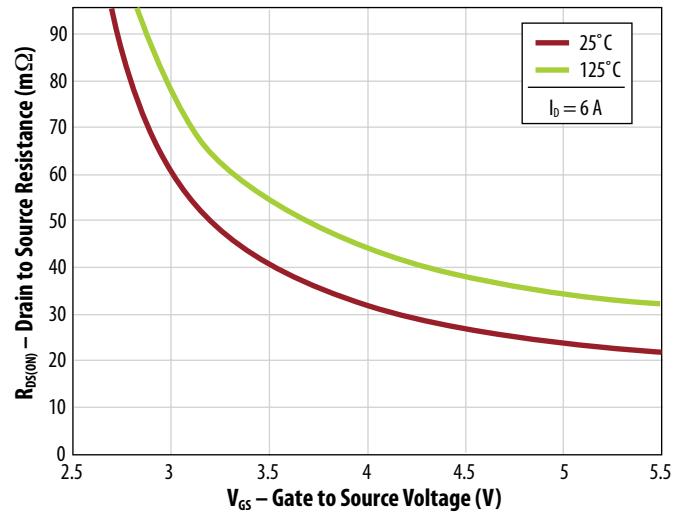
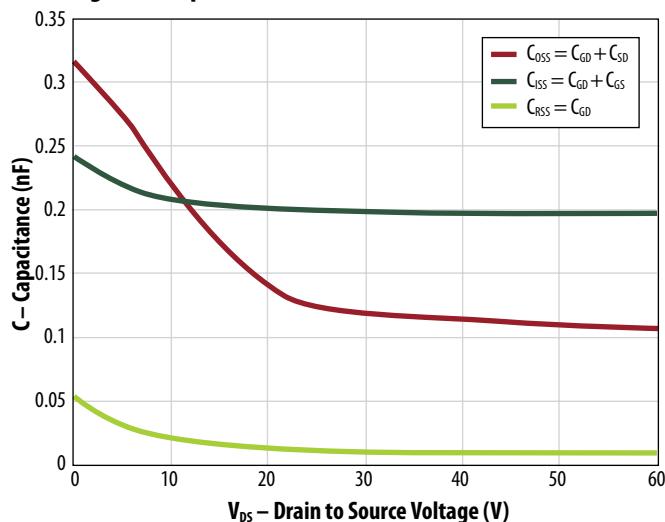
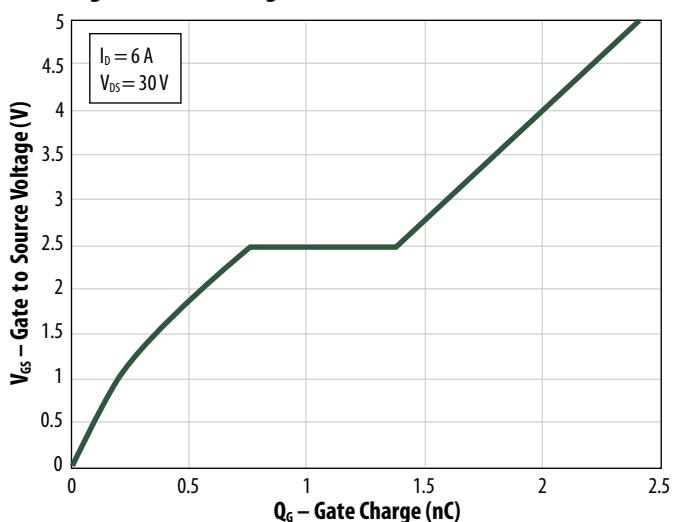
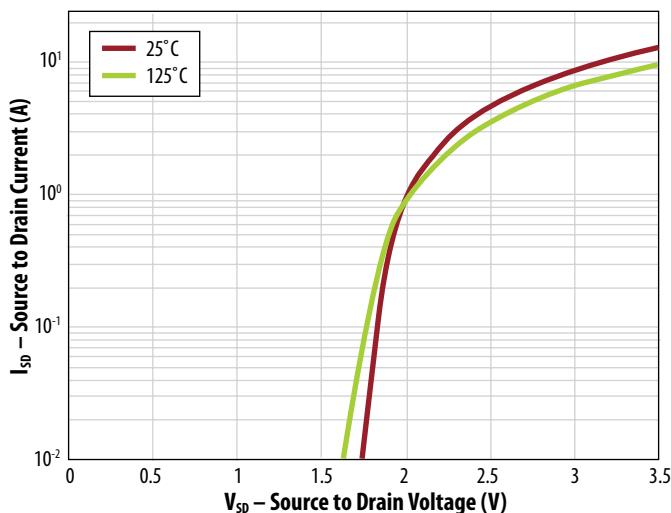
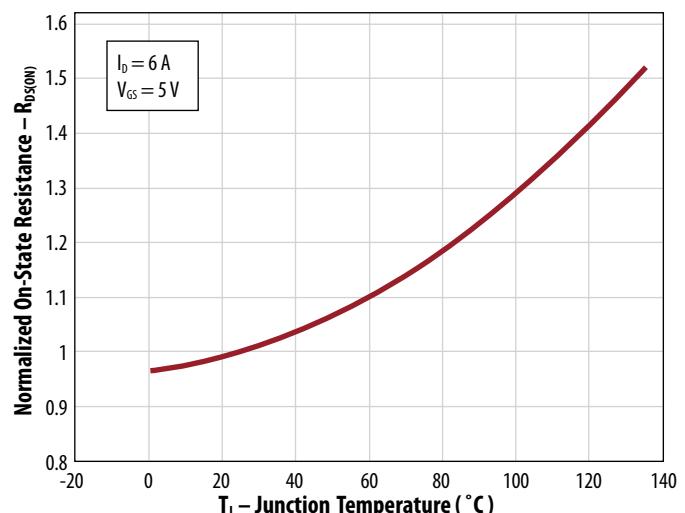
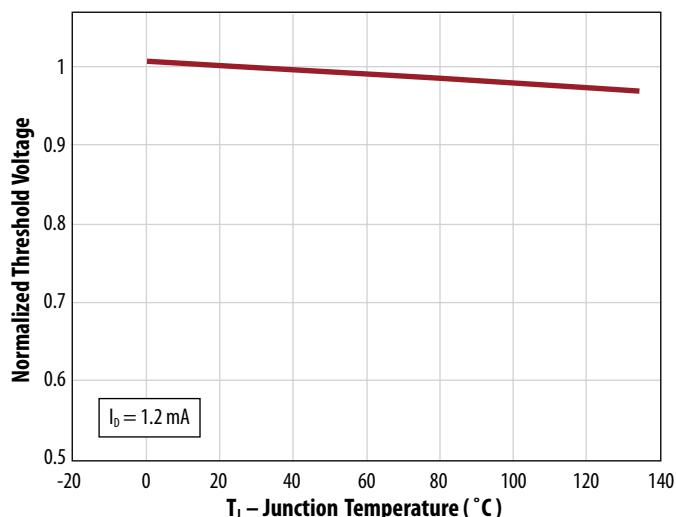
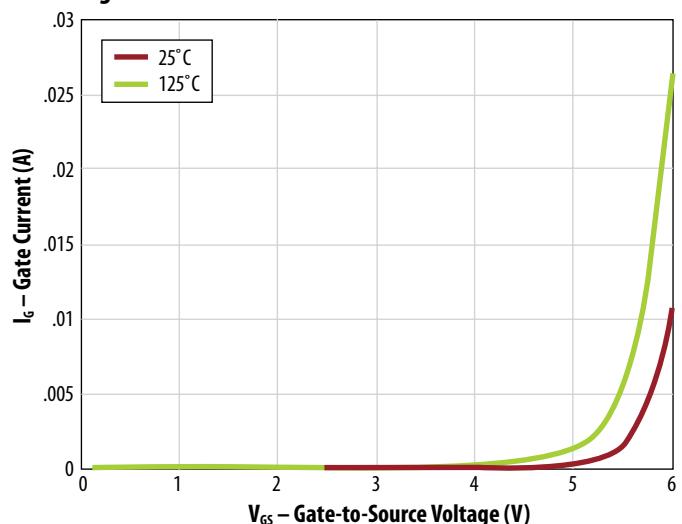
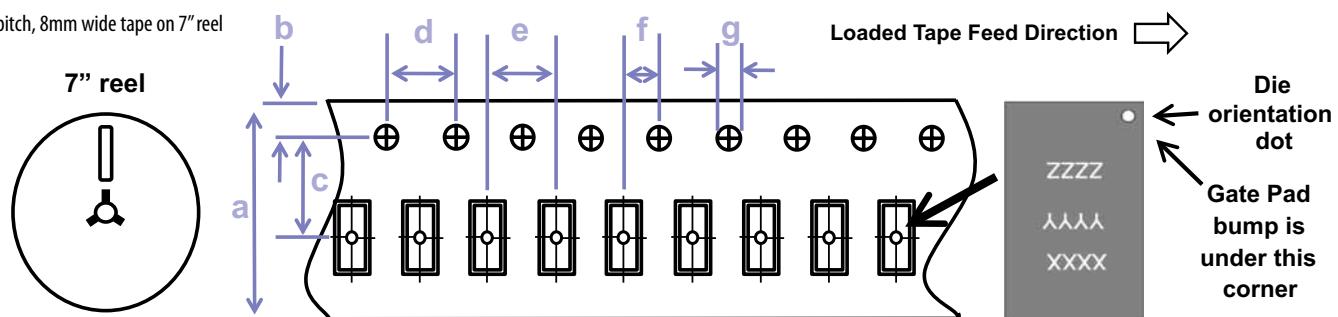
Figure 1: Typical Output Characteristics**Figure 2: Transfer Characteristics****Figure 3: $R_{DS(ON)}$ vs V_G for Various Current****Figure 4: $R_{DS(ON)}$ vs V_G for Various Temperature****Figure 5: Capacitance****Figure 6: Gate Charge**

Figure 7: Reverse Drain-Source Characteristics**Figure 8: Normalized On Resistance Vs Temperature****Figure 9: Normalized Threshold Voltage****Figure 10: Gate Current****TAPE AND REEL CONFIGURATION**

4mm pitch, 8mm wide tape on 7" reel

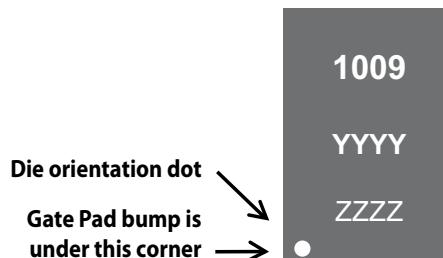


Dimension (mm)	EPC1009		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Die is placed into pocket
bump side down
(face side down)

Note: Pocket position is relative to the sprocket hole
measured as true position of the pocket, not the pocket hole

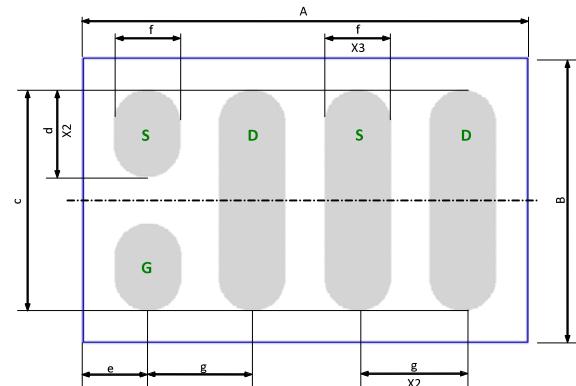
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC1009	1009	YYYY	ZZZZ

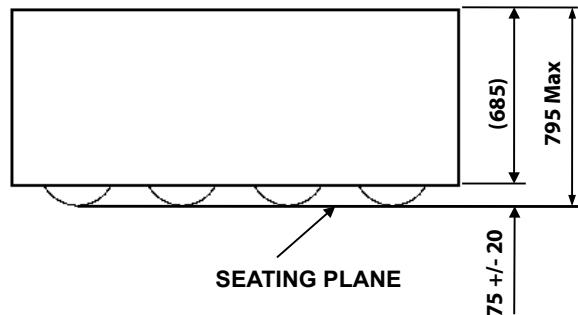
DIE OUTLINE

Bottom View

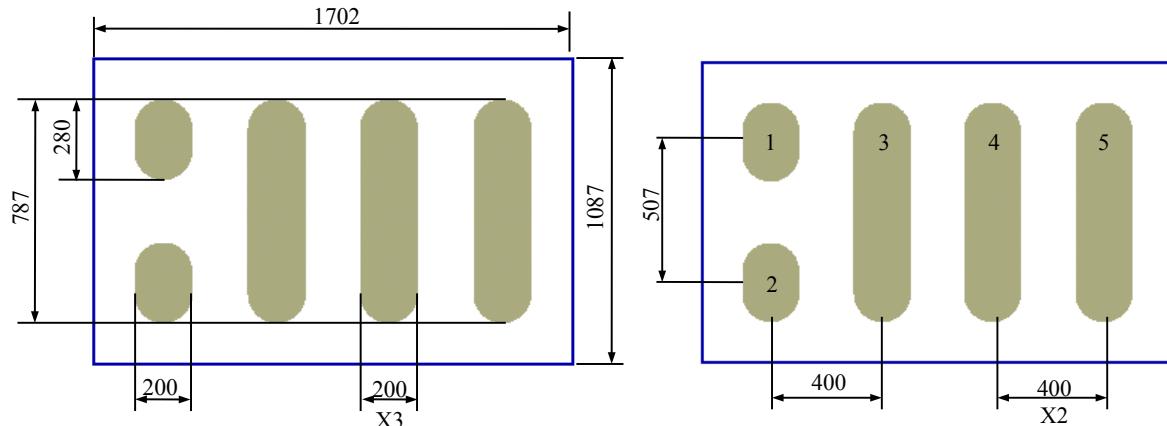


DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1672	1702	1732
B	1057	1087	1117
c	834	837	840
d	327	330	333
e	235	250	265
f	248	250	252
g	400	400	400

Side View



RECOMMENDED LAND PATTERN

(measurements in μm)

Pad no. 1 is Gate;
Pads no. 3 and 5 are Drain;
Pads no. 2 and 4 are Source.

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Revised April, 2010