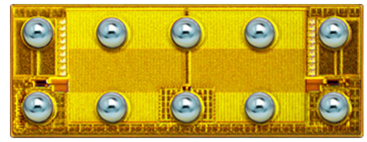
Preliminary Datasheet

FEATURES:

- Integrated Gate Driver
  - – Low Propagation Delay
  - – Up to 7 MHz Operation
  - – Operates from 5 V Supply
- Dual 88-mΩ, 150-V eGaN FET
- Low Inductance 2.9 mm x 1.1 mm BGA



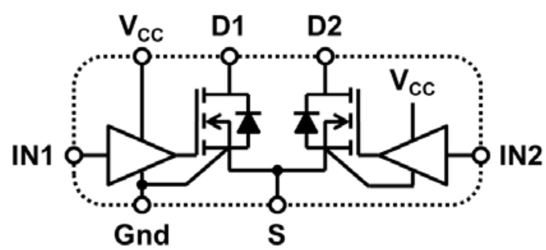
EPC2115 devices are supplied only in passivated die form with solder balls

Die Size: 2.9 mm x 1.1 mm

APPLICATIONS:

- Wireless Power (Highly Resonant and Inductive)
- High Frequency DC-DC Conversion

Schematic Diagram



DESCRIPTION

The EPC2115 enhancement-mode gallium-nitride (eGaN®) monolithic IC contains two monolithic 88-mΩ, 150-V GaN power transistors, each with an optimized gate driver, in a low inductance 2.9 mm by 1.1 mm BGA package.

The EPC2115 enables designers to improve efficiency, save space, and lower costs compared to silicon-based solutions. The ultra-low capacitance and zero reverse recovery of the eGaN FETs enable efficient operation in many topologies. The integrated drivers are specifically matched to the GaN device to yield optimal performance under various operating conditions that is further enhanced due to the small, low inductance footprint. Monolithic integration eliminates interconnect inductances for higher efficiency at high frequency. This is especially important for high frequency applications such as resonant wireless power.

ABSOLUTE MAXIMUM RATINGS

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	150	V
I_D	Continuous (T_A = 25˚C, $R_{θJA}$= 32 ˚C/W)	5	A
	Pulsed (25˚C, T_{PULSE} 300 µs)	18	
V_{IN}	Input Signal Voltage	6	V
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	
V_{CC}	Supply Voltage	6	V

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions					
PARAMETER	**Description**	**MIN**	**TYP**	**MAX**	**UNIT**
V_{DS}	Drain-Source voltage			120	V
V_{CC}	Driver Supply voltage	4.5	5	5.5	V
I_{CC}	External driver supply current[1]			60	mA
$V_{IN,Off}$	Input signal for turn-off			0.5	V
$V_{IN,On}$	Input signal for turn-on	4.5			V
$V_{IN,slew}$	Input signal slew rate	0.25			V/ns
T_J	Operating Temperature	-40		150	°C

[1] For up to maximum operating frequency and to power both FETs

THERMAL INFORMATION

Thermal Characteristics			
		TYP	**Unit**
$R_{θJC}$	Thermal Resistance, Junction to Case	2.1	˚C/W
$R_{θJB}$	Thermal Resistance, Junction to Board	21	˚C/W
$R_{θJA}$	Thermal Resistance, Junction to Ambient[2]	66	˚C/W

[2] $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

Thermal models for EPC devices available at http://epc-co.com/epc/DesignSupport/DeviceModels.aspx

ELECTRICAL CHARACTERSITCS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	Unit
eGaN POWER TRANSISTOR						
BV_{DSS}	Drain-to-Source Voltage	V_{CC} = 0 V, V_{IN} = 0 V, I_D = 125 µA	150			V
I_{DSS}	Drain -Source Leakage	V_{DS} = 120 V, T_J = 25 °C		10	100	µA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{CC} = 5 V, T_J = 25 °C		70	88	mΩ
V_{SD}	Source-Drain Forward Voltage	V_{CC} = 5 V, V_{IN} = 0 V, I_{SD} = 0.5 A		2		V
C_{OSS}	Output Capacitance	V_{IN} = 0 V, V_{CC} = 5 V, V_{DS} = 75 V, f = 1 MHz		57		pF
$C_{OSS(ER)}$	Energy Output Capacitance, Energy Related [3]	V_{IN} = 0 V, V_{CC} = 5 V, V_{DS} = 0 to 75 V		111		pF
$C_{OSS(TR)}$	Energy Output Capacitance, Energy Related [4]	V_{IN} = 0 V, V_{CC} = 5 V, V_{DS} = 0 to 75 V		108		pF
Q_{OSS}	Output Charge	V_{IN} = 0 V, V_{CC} = 5 V, V_{DS} = 75 V, V_{GS} = 0 V		6.7		nC
Q_{RR}	Source-Drain Recovery Charge			0		nC

[3] $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}

[4] $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}

ELECTRICAL CHARACTERSITCS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	Unit
DRIVER SUPPLY						
$I_{VCC, ON}$	Quiescent current (average)	V_{IN} = 5 V, V_{CC} = 5 V, V_{DS} = 0 V, each FET-driver		4.4		mA
$I_{VCC, OFF}$	Quiescent current (average)	V_{IN} = 0 V, V_{CC} = 5 V, V_{DS} = 0 V, each FET-driver		4.4		mA
$I_{VCC, OP}$	Operating Current	50% duty cycle, V_{CC} = 5 V, f_{SW} = 1 MHz, each FET-driver		6.5		mA
V_{IH}	Turn-on Input pin, logic high	V_{CC} = 5 V, each FET-driver	4.0			V
V_{IL}	Turn-off Input pin, logic low	V_{CC} = 5 V			0.7	V

SWITCHING CHARACTERISTICS

Switching Characteristics						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER[5]						
$t_{pd,on}$	Propagation delay, turn on	V_{CC} = 5 V, V_{DS} = 120 V, I_L = 2 A		2.6		ns
t_{rise}	Rise Time	V_{CC} = 5 V, V_{DS} = 120 V, I_L = 2 A		2.3		ns
t_{on}	Total turn-on time	V_{CC} = 5 V, V_{DS} = 120 V, I_L = 2 A		6.8		ns
$t_{pd,off}$	Propagation delay, turn off	V_{CC} = 5 V, V_{DS} = 120 V, I_L = 2 A		10.1		ns
t_{fall}	Fall Time	V_{CC} = 5 V, V_{DS} = 120 V, I_L = 2 A		3.7		ns
t_{off}	Total turn-off time	V_{CC} = 5 V, V_{DS} = 120 V, I_L = 2 A		16.4		ns
t_{MIN}	Minimum on-time	V_{CC} = 5 V, V_{BUS} = 120 V		9.2		ns
t_{MAX}	Maximum on-time	V_{CC} = 5 V, I_{DS} = 0.5 A		40		ms

[5]See application circuit, Figure 4 & 5

TYPICAL CHARACTERSITCS

Figure 1: Normalized On-State Resistance vs Temperature

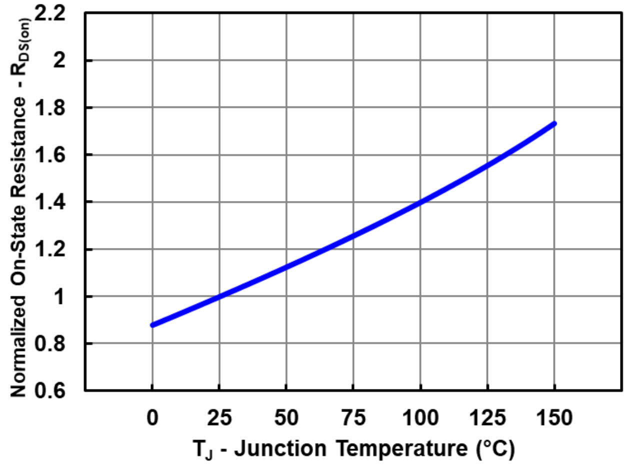


Figure 2: Capacitance (Linear Scale)

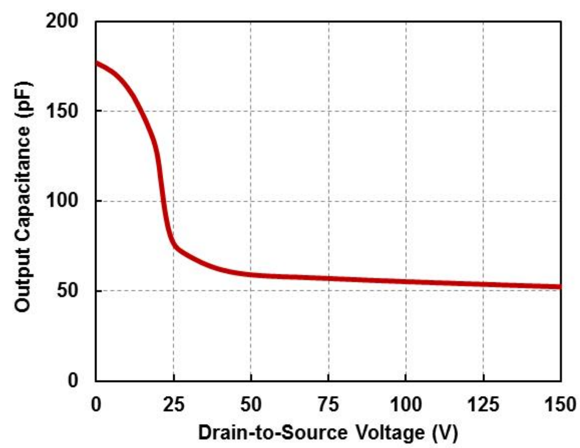


Figure 3: Output Charge and C_{OSS} Stored Energy

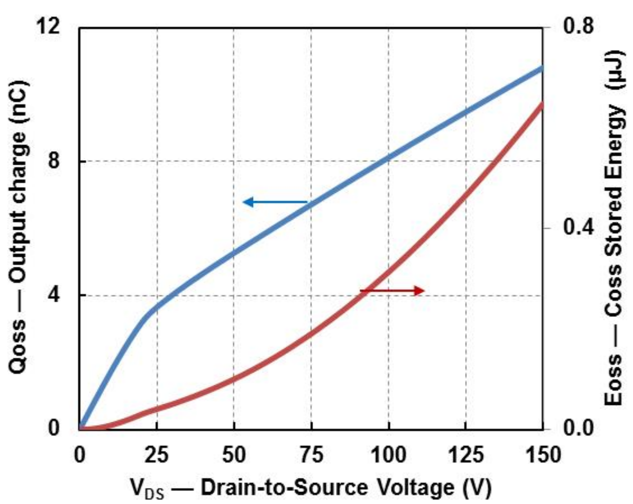


Figure 4: Double pulse Test Definitions

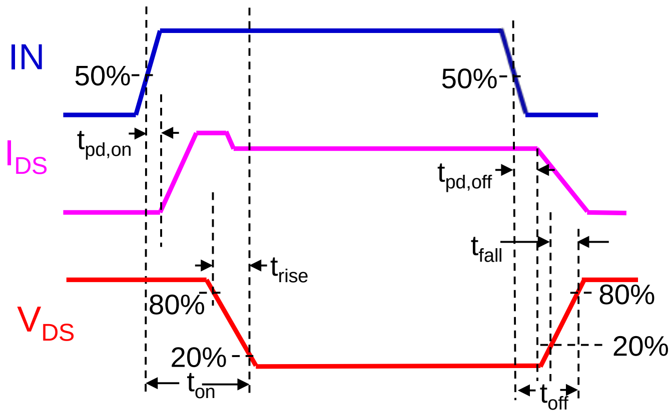


Figure 5: Double pulse Test Circuit

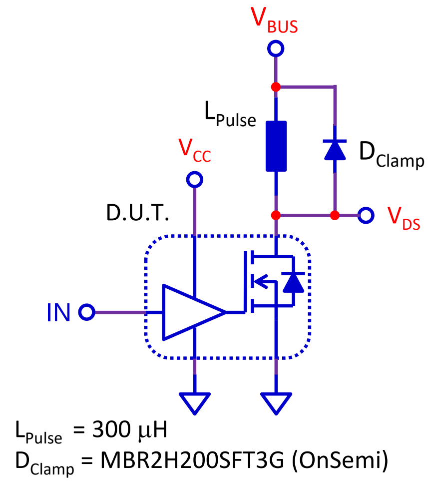
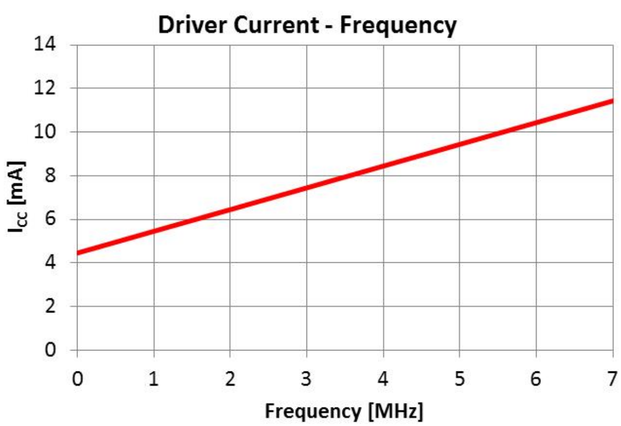
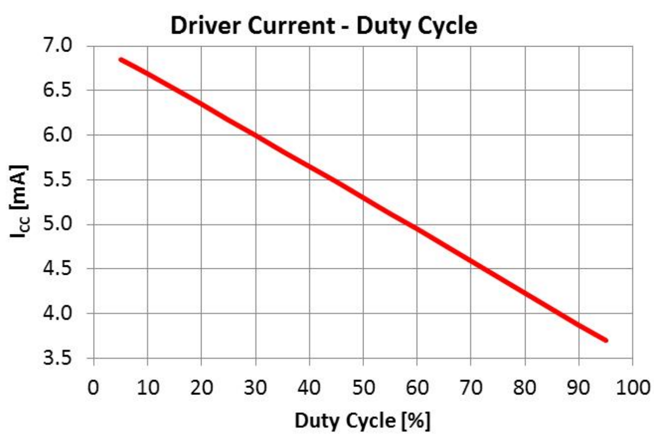


Figure 6: Driver quiescent current as function of frequency



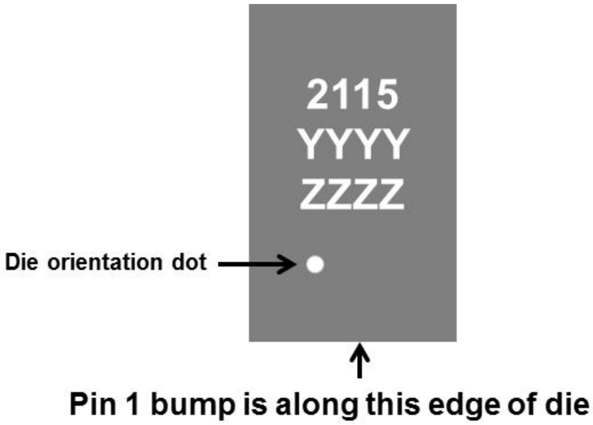
(50% duty cycle, V_{cc}= 5 V, V_{DS} = 0 V, each FET-driver)

Figure 7: Driver quiescent current as function of duty cycle



(1 MHz, V_{CC}= 5 V, V_{DS} = 0 V, each FET-driver)

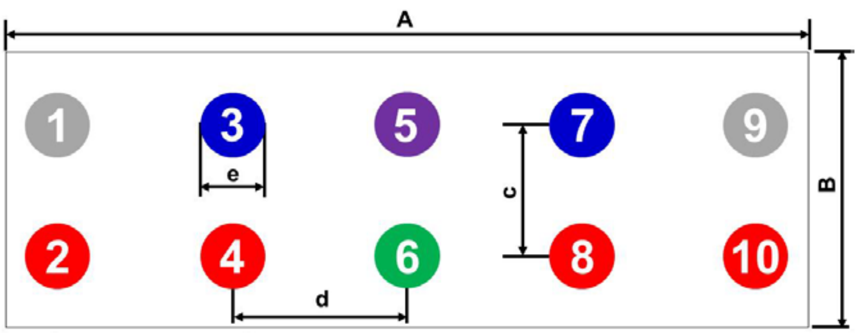
DIE MARKINGS



Part Number	Laser Marking		
	Part # Marking Line 1	Lot Date Code Marking Line 2	Lot Date Code Marking Line 3
EPC2115ENGRT	2115	YYYY	ZZZZ

DIE OUTLINE

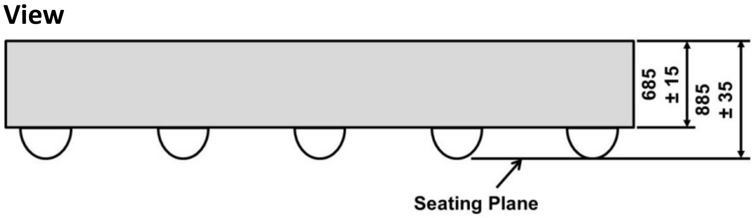
Solder Bump View



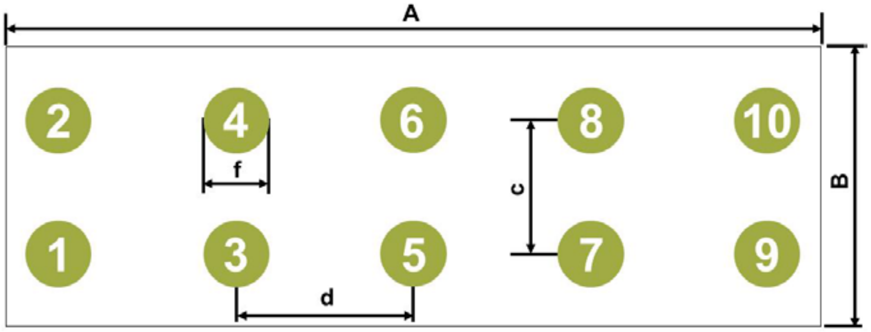
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2870	2900	2930
B	1070	1100	1130
c		600	
d		600	
e	238	264	290

Pad 1 is Input 1;
Pad 9 is Input 2;
Pad 6 is V_{CC};
Pad 5 is Gnd;
Pads 2, 4 are Drain 1;
Pads 8, 10 are Drain 2;
Pads 3, 7 are Source

Side View



RECOMMENDED LAND PATTERN
(*Units in µm)*

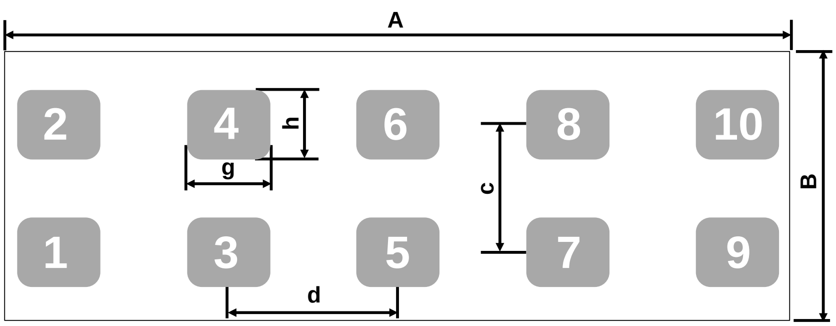


DIM	MICROMETERS
A	2900
B	1100
c	600
d	600
f	230

The land pattern is solder mask defined. Copper is larger than the solder mask opening.

RECOMMENDED STENCIL DESIGN
(*Units in µm)*

Back Side View (Bump on Bottom)



DIM	MICROMETERS
A	2900
B	1100
c	600
d	600
g	300
h	250

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Recommended stencil should be 4mil (100µm) thick, laser cut. The corner has a radius of R60.

Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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