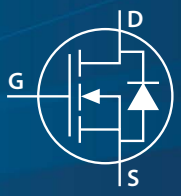
EPC2214 – Automotive 80 V (D-S) Enhancement Mode Power Transistor

V_{DS}, 80 V
$R_{DS(on)}$, 20 mΩ
I_D, 10 A,
AEC-Q101

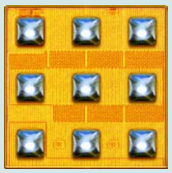


EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 60 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	96	
I_D	Continuous (T_A = 25°C)	10	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	47	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	



EPC2214 eGaN® FETs are supplied only in passivated die form with solder bumps
Die Size: 1.35 mm x 1.35 mm

Applications
- Lidar/Pulsed Power Applications
- DC-DC Conversion
- Wireless Power Transfer

Benefits
- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low Q_G
- Ultra Small Footprint

www.epc-co.com/epc/Products/eGaNFETs/EPC2214.aspx

Static Characteristics (T_J= 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.2 mA	80			V
I_{DSS}	Drain-Source Leakage	V_{DS} = 64 V, V_{GS} = 0 V, T_J = 25°C		0.003	0.15	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V, T_J = 25°C		0.003	1.1	mA
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.01	2.5	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V, T_J = 25°C		0.003	0.15	mA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 2 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 6 A		15	20	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.9		V

Defined by design. Not subject to production test.

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.6	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	7.4	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	81	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

Dynamic Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance#	V_{DS} = 40 V, V_{GS} = 0 V		198	238	pF
C_{RSS}	Reverse Transfer Capacitance			1.8		
C_{OSS}	Output Capacitance#			129	194	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 40 V, V_{GS} = 0 V		171		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			211		
R_G	Gate Resistance			0.65		Ω
Q_G	Total Gate Charge#	V_{DS} = 40 V, V_{GS} = 5 V, I_D = 6 A		1.8	2.2	nC
Q_{GS}	Gate to Source Charge	V_{DS} = 40 V, I_D = 6 A		0.5		
Q_{GD}	Gate to Drain Charge			0.3		
$Q_{G(TH)}$	Gate Charge at Threshold			0.4		
Q_{OSS}	Output Charge#	V_{DS} = 40 V, V_{GS} = 0 V		8	12	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

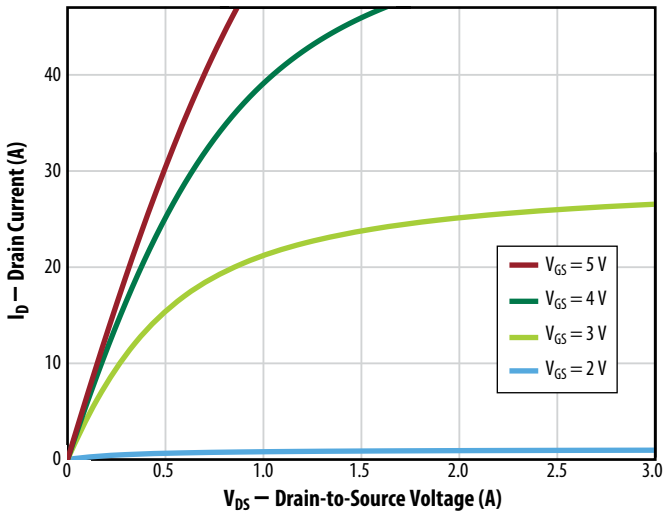


Figure 2: Transfer Characteristics

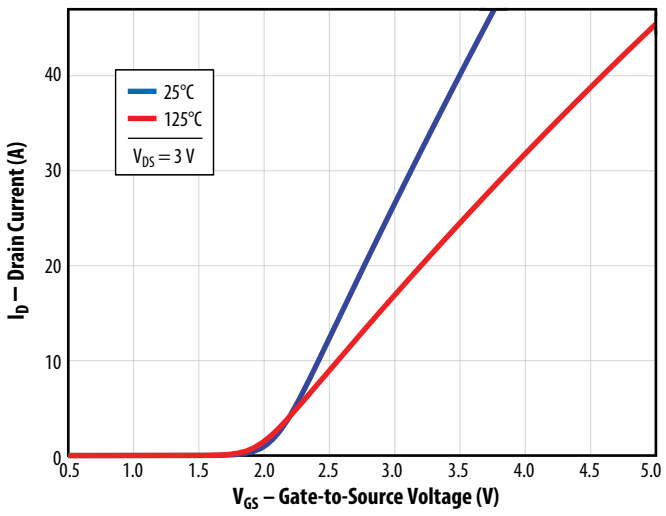


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

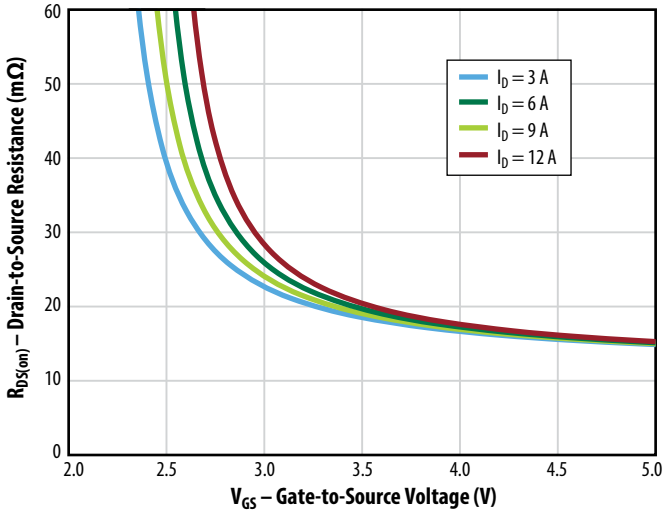


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

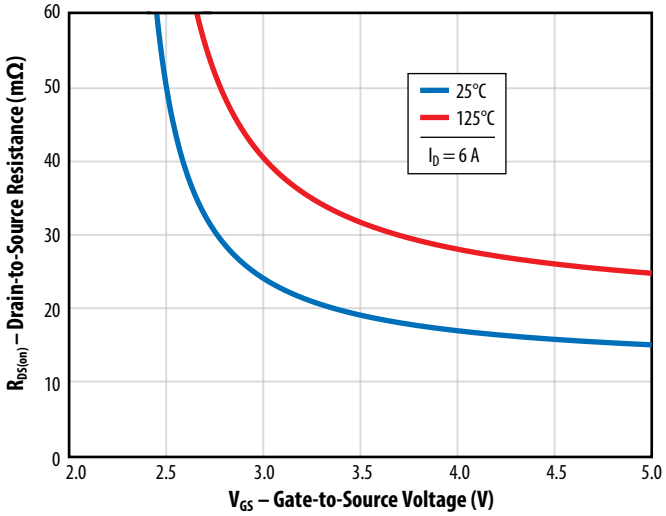


Figure 5a: Capacitance (Linear Scale)

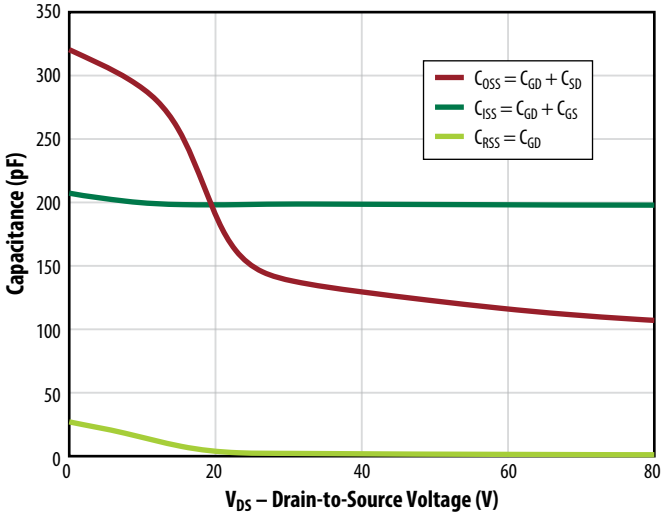


Figure 5b: Capacitance (Log Scale)

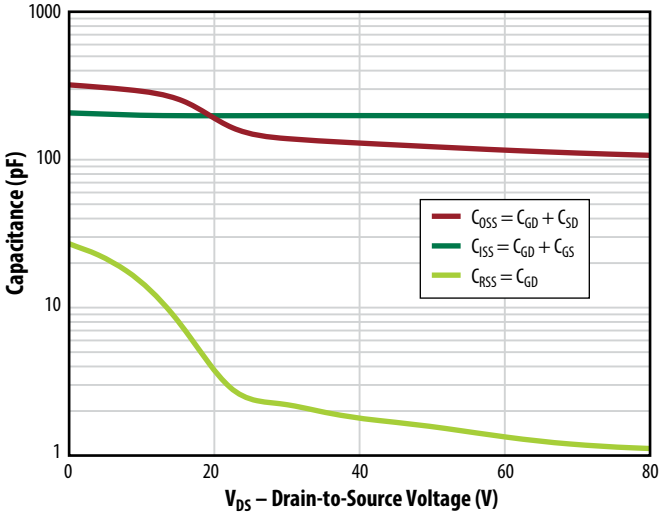


Figure 6: Output Charge and C_{OSS} Stored Energy

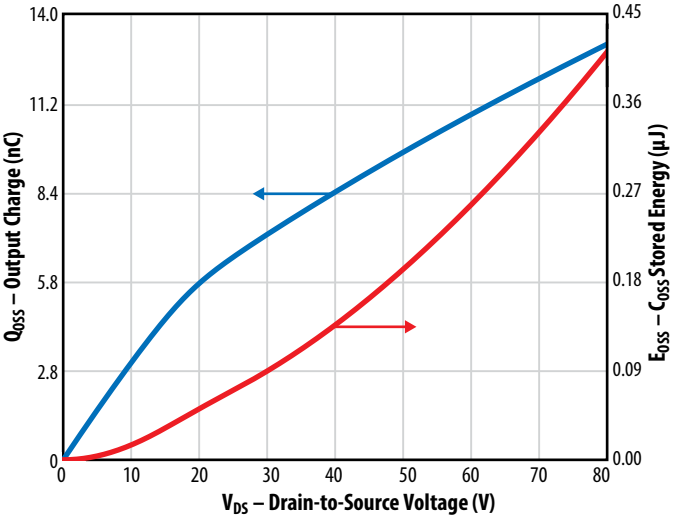


Figure 7: Gate Charge

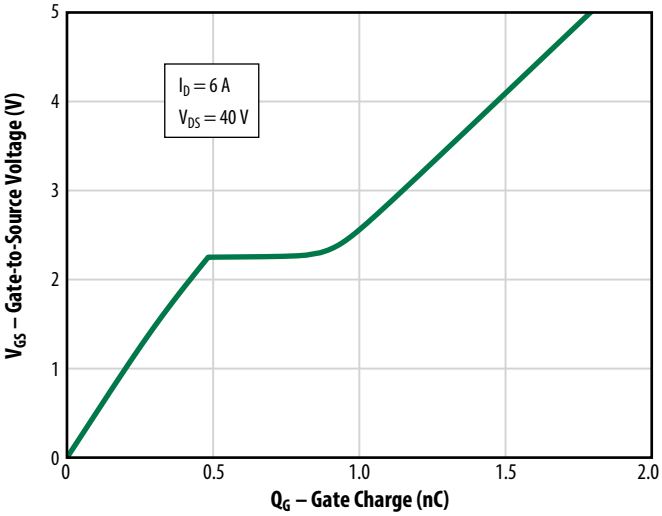


Figure 8: Reverse Drain-Source Characteristics

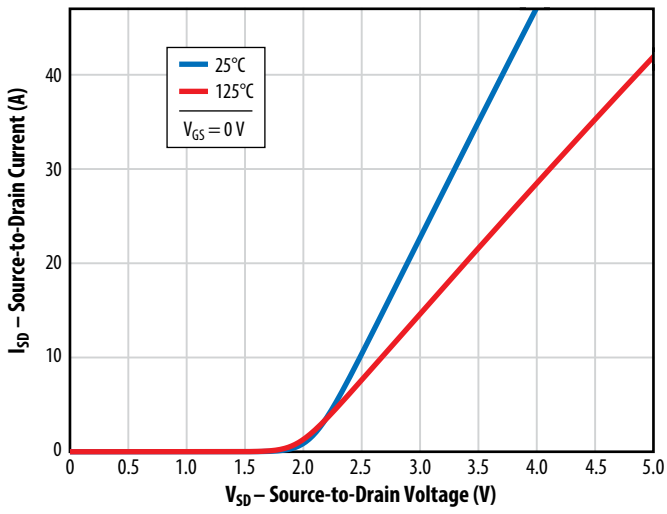
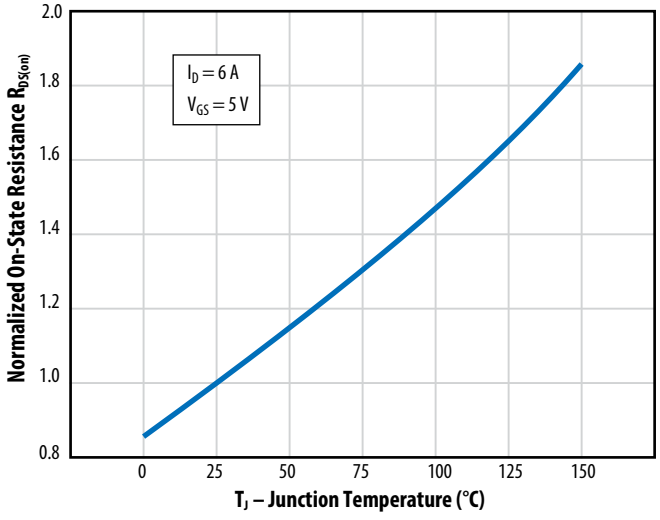


Figure 9: Normalized On-State Resistance vs. Temperature



All measurements were done with substrate shortened to source.

Figure 10: Normalized Threshold Voltage vs. Temperature

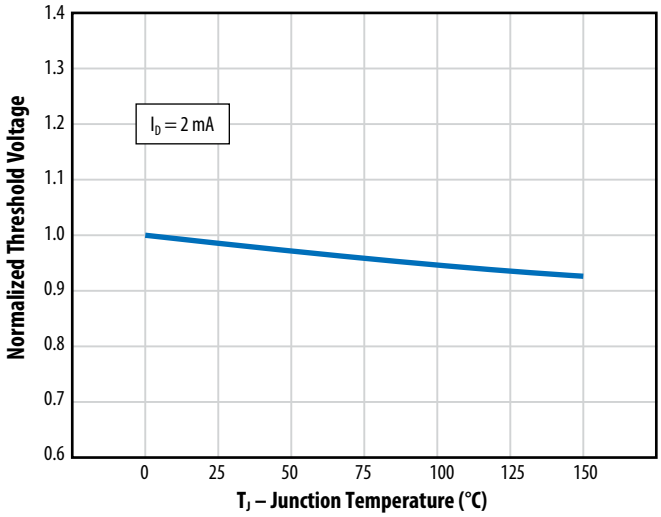
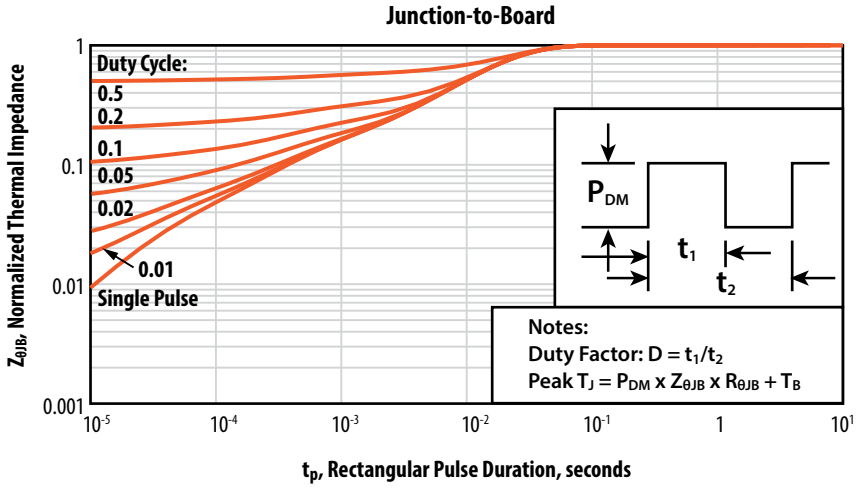


Figure 11: Transient Thermal Response Curves



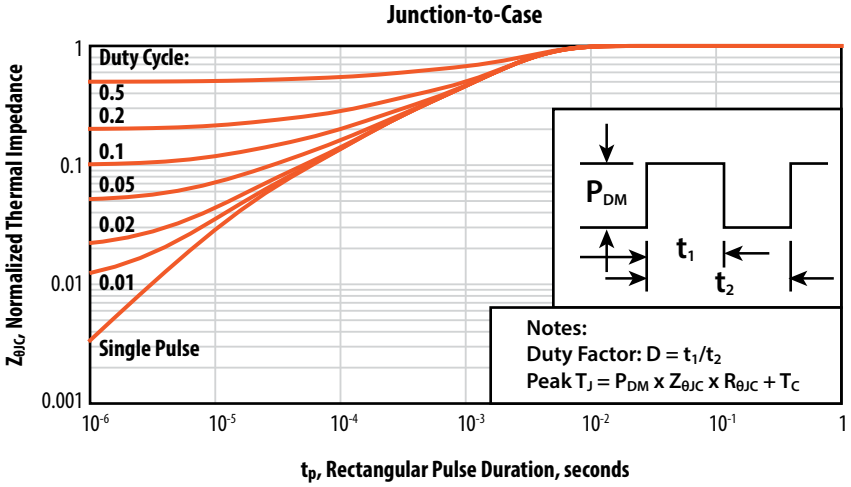
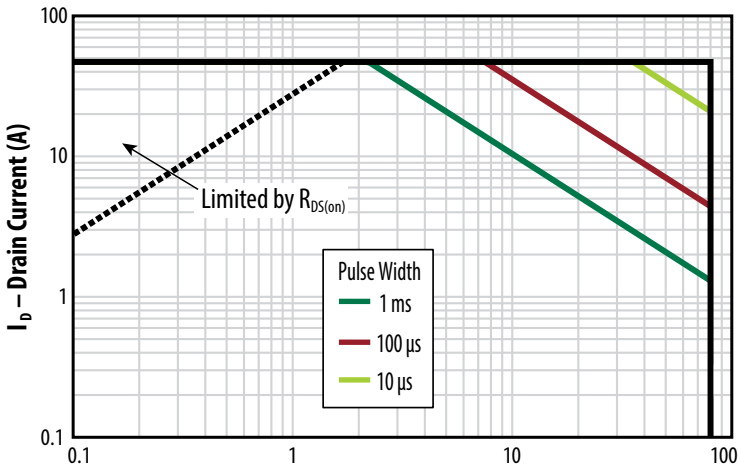


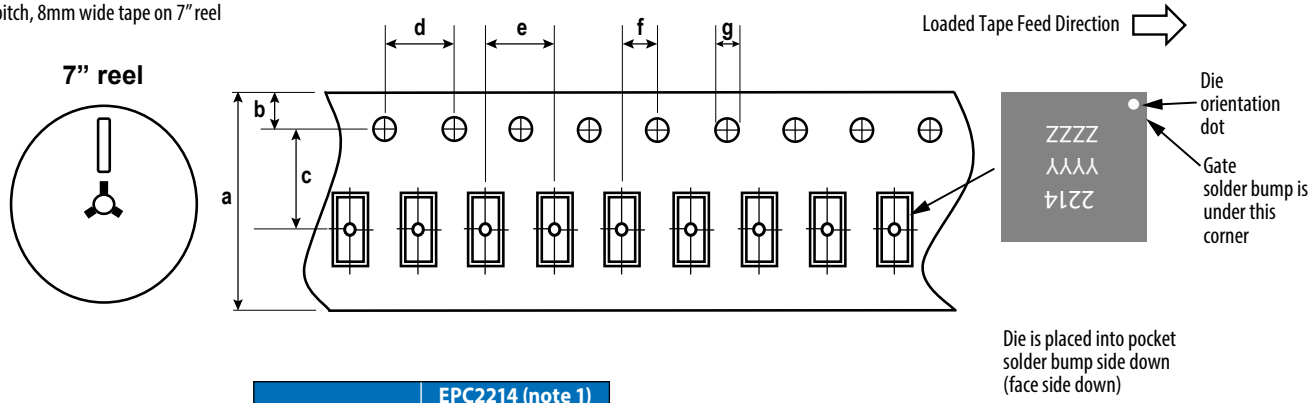
Figure 12: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

TAPE AND REEL CONFIGURATION

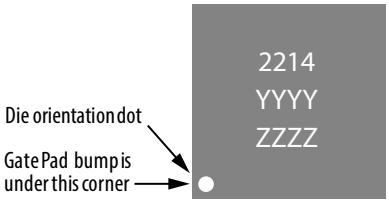
4mm pitch, 8mm wide tape on 7" reel



	EPC2214 (note 1)		
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (note 2)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

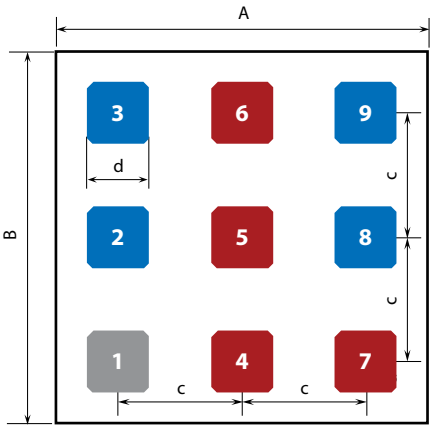
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2214	2214	YYYY	ZZZZ

DIE OUTLINE

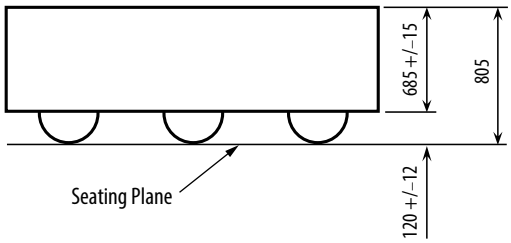
Pad View



DIM	Micrometers		
	MIN	Nominal	MAX
A	1320	1350	1380
B	1320	1350	1380
c		450	
d		225	

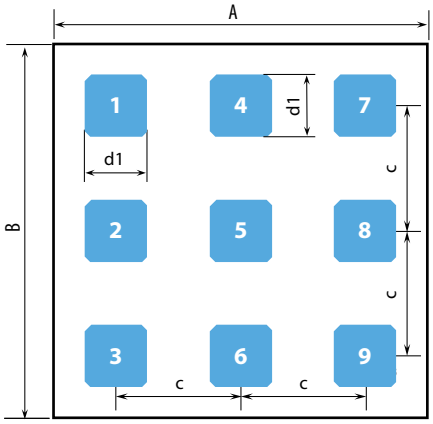
Pad 1 is Gate;
Pads 4, 5, 6, 7 are Drain;
Pads 2, 3, 8, 9 are Source.

Side View



RECOMMENDED LAND PATTERN

(measurements in µm)



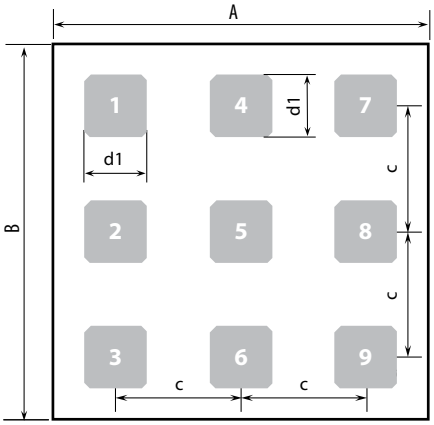
DIM	Micrometers
A	1350
B	1350
c	450
d1	205

The land pattern is solder mask defined
Solder mask is 10 µm smaller per side than bump

Pad 1 is Gate;
Pads 4, 5, 6, 7 are Drain;
Pads 2, 3, 8, 9 are Source.

RECOMMENDED STENCIL DRAWING

(measurements in µm)



DIM	Micrometers
A	1350
B	1350
c	450
d1	225

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.
The corner has a radius of R60.
Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at
http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx