

Preliminary Information

This errata sheet provides updated information for Revision A and Revision B EPF10K100B devices. The die revision is indicated by the third digit of the nine-digit code on the top side of the device. Revision C and higher EPF10K100B devices do not exhibit the conditions described in this document.

Under certain voltage conditions, the output buffer delay for Revision A and Revision B EPF10K100B devices is slower than the reported value for I/O pins with the Slow Slew Rate option turned on in the MAX+PLUS® II software. The MAX+PLUS II version 9.0 Timing Analyzer and Simulator report an added output delay of 4.5 ns when the Slow Slew Rate option is turned on. When the Slow Slew Rate option is turned on and the VCCINT and VCCIO pins are powered at 2.3 V and 3.6 V, respectively, the change in the measured output buffer delay due to the Slow Slew Rate option may be as high as 7.5 ns.

This condition in which the VCCINT and VCCIO pins are powered to the opposite extremes is rare. For designs where this increased delay is a problem, you should either turn off the Slow Slew Rate option or adjust the circuit's power supply to provide a 2.5-V V_{CCINT}.

With the Slow Slew Rate option turned off, the device functions as reported in the MAX+PLUS II version 9.0 Timing Analyzer and Simulator.



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