EPM7160 EPLD

High-Performance 160-Macrocell Device

September 1992, ver. 2

Data Sheet

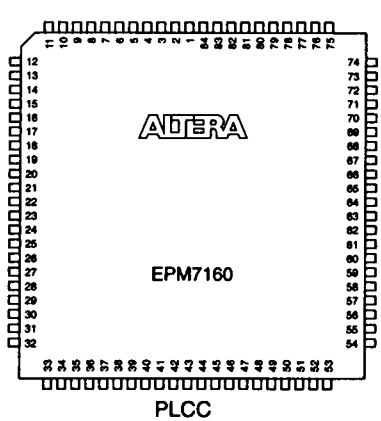
Features

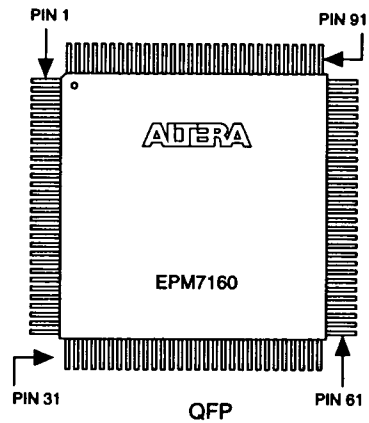
Preliminary Information

- High-density, erasable CMOS EPLD based on second-generation Multiple Array MatriX (MAX) architecture
  - 3,200 usable gates
  - Combinatorial speeds with t_{PD} = 12 ns
  - Clock frequencies up to 90.9 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 104 inputs or 100 outputs
- 160 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Programmable registers configurable as D, T, JK, or SR flipflops with individual Clock Enable and asynchronous Clear and Preset controls
- Independent clocking of registers from array or global Clock signals
- Programmable power-saver mode for 50% or more power reduction in each macrocell
- Available in 84-pin PLCC and 120-pin QFP packages. 120-pin PGA package under development. See Figure 1.
- Software design support with Altera's MAX+PLUS II development system for PC, Sun SPARCstation, and HP 9000 Series 700 platforms
- Programming support from Altera's Master Programming Unit (MPU) and other programming hardware manufacturers

Figure 1. EPM7160 84-Pin PLCC and 120-Pin Plastic QFP Package Pin-Out Diagrams

See Table 1 in this data sheet for 84-pin PLCC pin-outs and Table 2 for 120-pin QFP pin-outs. Package outlines not drawn to scale.





General Description

The Altera EPM7160 is a high-density, high-performance CMOS device based on Altera's second-generation MAX 7000 architecture. Fabricated on a 0.8-micron EEPROM technology, the EPM7160 provides 3,200 usable gates, in-system speeds of 90.9 MHz, and propagation delays of 12 ns. The EPM7160 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 160 macrocells, the EPM7160 implements complete system-level designs. It easily integrates multiple programmable logic devices such as PALs, GALs, and 22V10s. With its high performance and density, the EPM7160 provides FPGA density with PAL performance. The high density and high I/O pin count also make the EPM7160 appropriate for prototyping gate arrays. Available in 84-pin plastic J-lead chip carrier (PLCC) package, with 120-pin pin-grid array (PGA) and 120-pin plastic quad flat pack (QFP) packages under development, the EPM7160 accommodates logic- and I/O-intensive designs.

The EPM7160 uses CMOS EEPROM cells to configure logic functions within the device. EPM7160 architecture is user-configurable to accommodate a variety of independent logic functions, and the device can be reprogrammed for multiple design cycles. Each device is guaranteed for 100 program and erase cycles.

The EPM7160 consists of 160 macrocells organized into 10 Logic Array Blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register that provides D, T, JK, or SR operation with independent programmable Clock, Clock Enable, Clear, and Preset functions. For building complex logic functions, each macrocell can be supplemented with both shared expanders and high-speed parallel logic expanders to allow up to 32 product terms per macrocell.

The EPM7160 provides programmable speed/power optimization. Speed-critical portions of the design can run at high speed/full power, while the remainder runs at reduced speed/low power. This feature allows you to specify one or more macrocells to operate at 50% or less power while adding only a nominal timing delay.

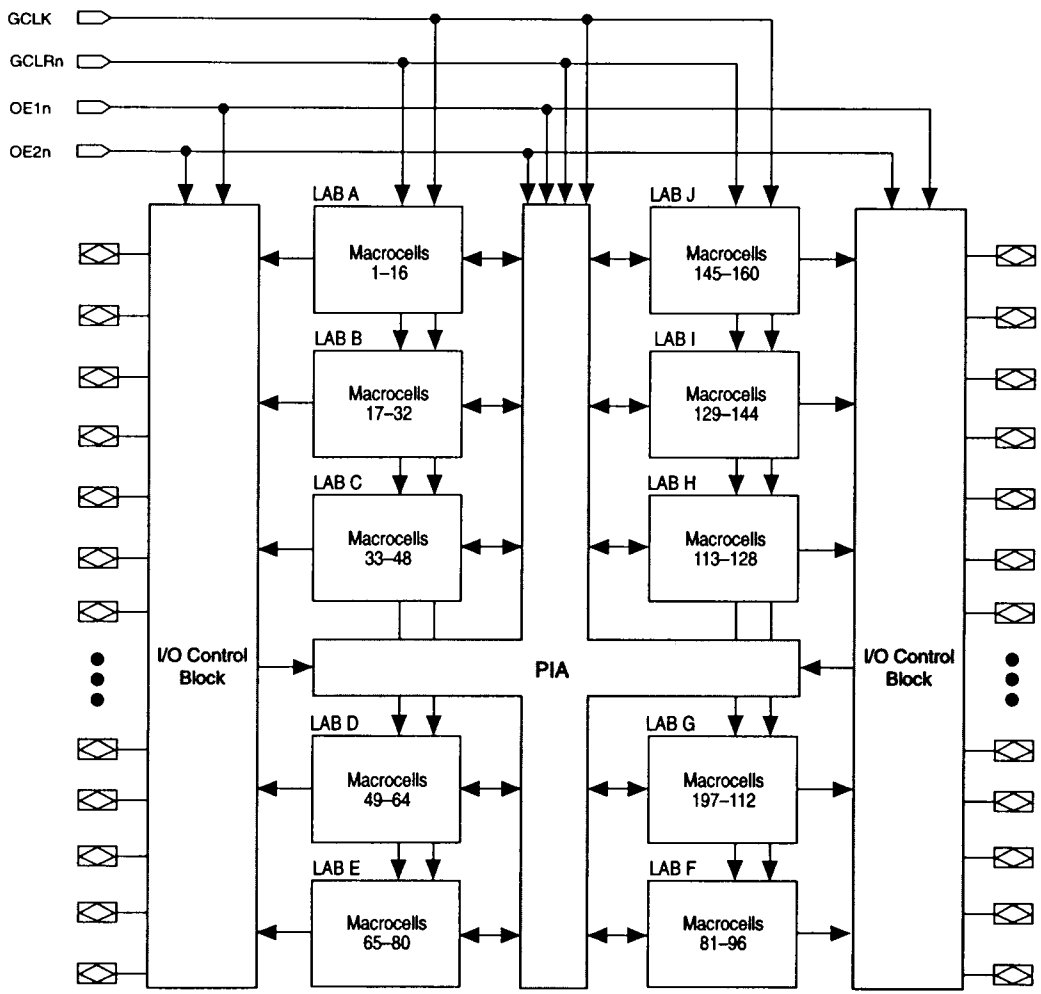
The EPM7160 is supported by the MAX+PLUS II development system, which provides a completely integrated design entry, compilation, verification, and programming environment. MAX+PLUS II software is available for 386- and 486-based PC, Sun SPARCstation, and HP 9000 Series 700 platforms. The Windows-based graphical interface supports hierarchical graphic, text, and waveform design entry with over 300 74-series macrofunctions. MAX+PLUS II includes the Altera Hardware Description Language (AHDL), which supports state machine, Boolean equation, conditional logic, and truth table entry methods. In addition, MAX+PLUS II provides highly automated compilation, automatic multi-device partitioning, timing simulation and analysis, automatic error location, device programming and verification, and a comprehensive on-line help

system. MAX+PLUS II imports and exports standard EDIF 2 0 0 netlist files for a convenient interface to popular PC- and workstation-based CAE tools.

Functional Description

The EPM7160 is a 160-macrocell EPLD that has been optimized for VLSI designs (see Figure 2). It has up to 100 I/O pins that can be individually configured for input, output, or bidirectional operation. It also has four dedicated input pins that can be programmed as general-purpose inputs

Figure 2. EPM7160 Block Diagram



or high-speed, global control signals (Clock, Clear, and two Output Enable signals) for each macrocell and I/O pin.

The EPM7160 contains the following architectural building blocks:

- Logic Array Blocks
- Macrocells
- Logic expanders (shared and parallel)
- Programmable Interconnect Array
- I/O control blocks

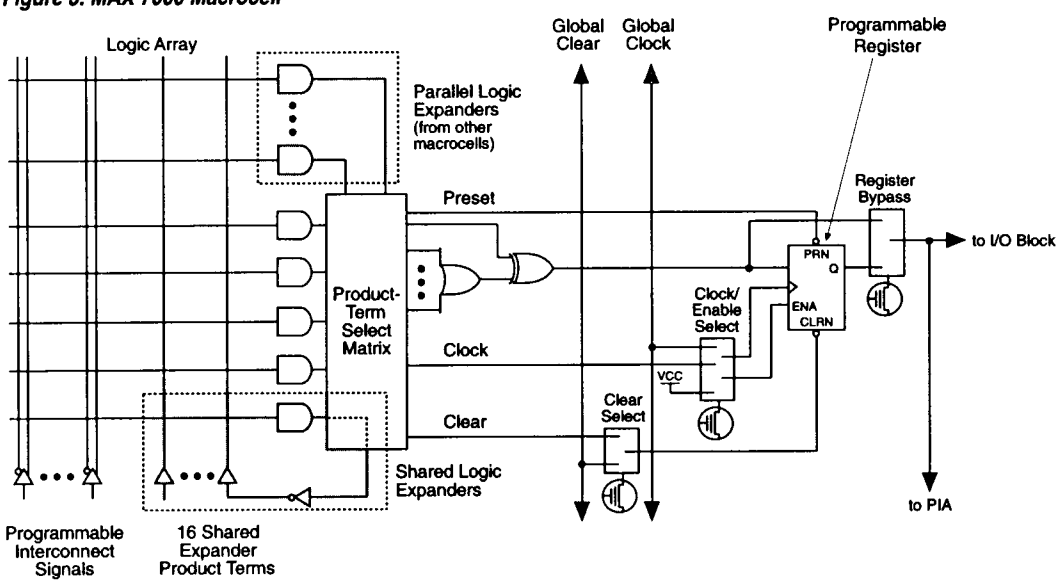
Logic Array Blocks

MAX 7000 architecture is based on the concept of linking small, high-performance, flexible logic array modules called Logic Array Blocks (LABs). Multiple LABs are linked together via a global bus called the Programmable Interconnect Array (PIA), which is fed by all EPM7160 dedicated inputs, I/O pins, and macrocells. The PIA routes only the signals required to implement logic in each LAB. The EPM7160 has 10 LABs, each of which contains 16 macrocells.

Macrocells

The MAX 7000 macrocell, shown in Figure 3, provides both sequential and combinatorial logic capabilities. It can be individually configured for

Figure 3. MAX 7000 Macrocell



registered or combinatorial operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the logic array, which contains five product terms. These product terms are allocated by the product-term select matrix for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs for the macrocell's register Clear, Preset, Clock, and Clock Enable control functions. One product term per macrocell can be used as a shared logic expander if it is fed back into the logic array. Based on the logic requirements of the design, the product-term select matrix automatically optimizes product-term allocation.

In registered functions, each macrocell flipflop can be individually programmed for D, T, JK, or SR operation with programmable Clock control. If necessary, the flipflop can be bypassed for combinatorial operation. During design entry, the user can specify the desired flipflop type or allow MAX+PLUS II to select the most efficient flipflop operation for each registered logic function to minimize the resources needed by the design.

The programmable register can be configured in three clocking modes:

- It can be clocked from the dedicated global Clock pin (GCLK). In this mode, the flipflop is positive-edge-triggered, and the fastest Clock-to-output performance is achieved.
- It can be clocked with the array Clock using a product term. In this mode, the flipflop can be configured for positive- or negative-edge-triggered operation. Array Clocks allow any signal source or gated logic function to clock the flipflop.
- It can be clocked from the global Clock pin and enabled by a product term. The register is enabled when the flipflop ENA input is high. Each flipflop can be activated individually while taking advantage of the fast Clock-to-output delay of the global Clock pin.

Each register also supports asynchronous Preset and Clear functions. As shown in Figure 3, the product-term select matrix allocates product terms to control these operations. Although the register is designed for active-low Preset and Clear, active-high control is also provided when the signal is inverted within the logic array. In addition, each register Clear function can be individually connected to the EPM7160 dedicated global Clear pin (GCLRn). In this mode, the Clear function is active low.

Logic Expanders

Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Instead of using another macrocell to supply the needed logic resources, the MAX 7000 architecture has both shared and parallel logic expanders that provide additional product terms directly to any macrocell.

Shared Logic Expanders

Each LAB has up to 16 shared expanders, which can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverting outputs that feed back into the logic array. Each shared logic expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. Shared logic expanders can also be cross-coupled to build additional buried flipflops, latches, or input registers. A small delay (t_{SEXP}) is incurred when shared logic expanders are used.

Parallel Logic Expanders

Parallel logic expanders are unused product terms from macrocells in the LAB that can be allocated to any macrocell by the product-term select matrix to implement fast, complex logic functions. With parallel logic expanders, up to 20 product terms can directly feed the macrocell OR logic (5 product terms from the macrocell and 15 parallel logic expanders provided by other macrocells in the LAB).

The MAX+PLUS II Compiler can automatically route parallel logic expanders to the necessary macrocells in sets of 1 to 5. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler will allocate 2 sets of parallel logic expanders (the first set equals 5 product terms, the second set equals 4 product terms, increasing the total delay by $2 \times t_{PEXP}$), in addition to the 5 product terms already in the macrocell.

The EPM7160 can use shared and parallel logic expanders to allocate additional product terms to any macrocell, ensuring that logic is synthesized with the fewest logic resources to obtain the fastest possible speed.

Programmable Interconnect Array

Logic is routed between the EPM7160 LABs on the Programmable Interconnect Array (PIA). This global bus is a programmable path that allows any signal source to reach any destination on the device. Although EPM7160 dedicated inputs, I/O pin feedbacks, and macrocell feedbacks all feed the PIA, the PIA routes only the required signals needed by each macrocell back into each LAB.

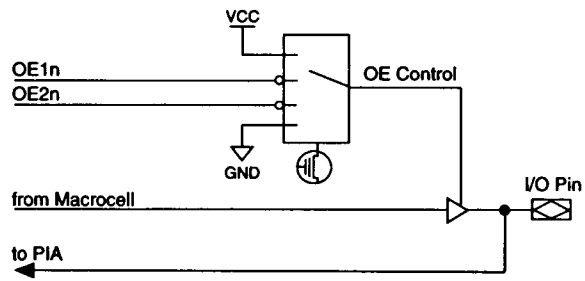
While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA eliminates skew between signals, making timing performance easy to predict.

I/O Control Blocks

The I/O control block, shown in Figure 4, allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is connected to one of two global active-low Output Enable pins (OE1n and OE2n) or directly to GND or VCC. When the I/O tri-state buffer is connected to GND, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the I/O tri-state buffer is connected to VCC, the output is enabled.

The EPM7160 EPLD provides dual feedback. The macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Figure 4. MAX 7000 I/O Control Block



Programmable Speed/Power Control

The EPM7160 offers a power-saver mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, since only a small number of all gates operates at maximum frequency in most logic applications.

Each macrocell in the EPM7160 can be individually programmed by the designer for either high-speed (Turbo = on) or low-power (Turbo = off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters.

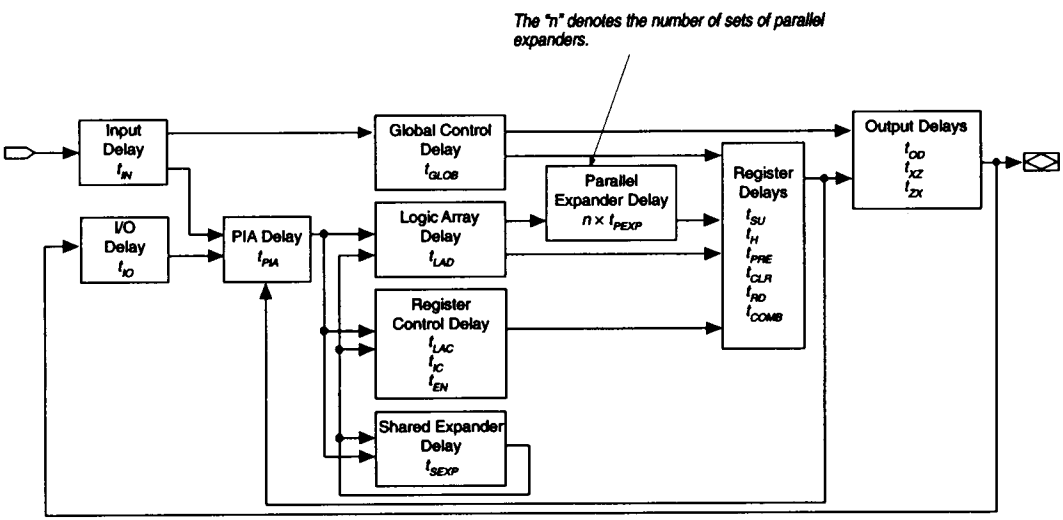
Design Security

The EPM7160 contains a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EEPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset when the EPLD is erased.

Timing Model

Timing within the EPM7160 can be analyzed with the MAX+PLUS II software, with a variety of popular CAE simulators and timing analyzers, or with the timing model shown in Figure 5. The EPM7160 has fixed internal delays that allow the user to determine the worst-case timing for any design. For complete timing information, MAX+PLUS II software provides complete timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

Figure 5. MAX 7000 Timing Model



Timing information can be calculated with the timing model and the timing parameters for a particular EPLD. External timing parameters are derived from the sum of internal parameters and represent pin-to-pin timing delays. Figure 6 shows the internal timing relationship for internal and external delay parameters. Actual worst-case timing can be calculated in a timing simulation with the MAX+PLUS II Simulator, in a timing analysis with the MAX+PLUS II Timing Analyzer, or with other supported CAE simulators.

Figure 6. Switching Waveforms (Part 1 of 2)

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

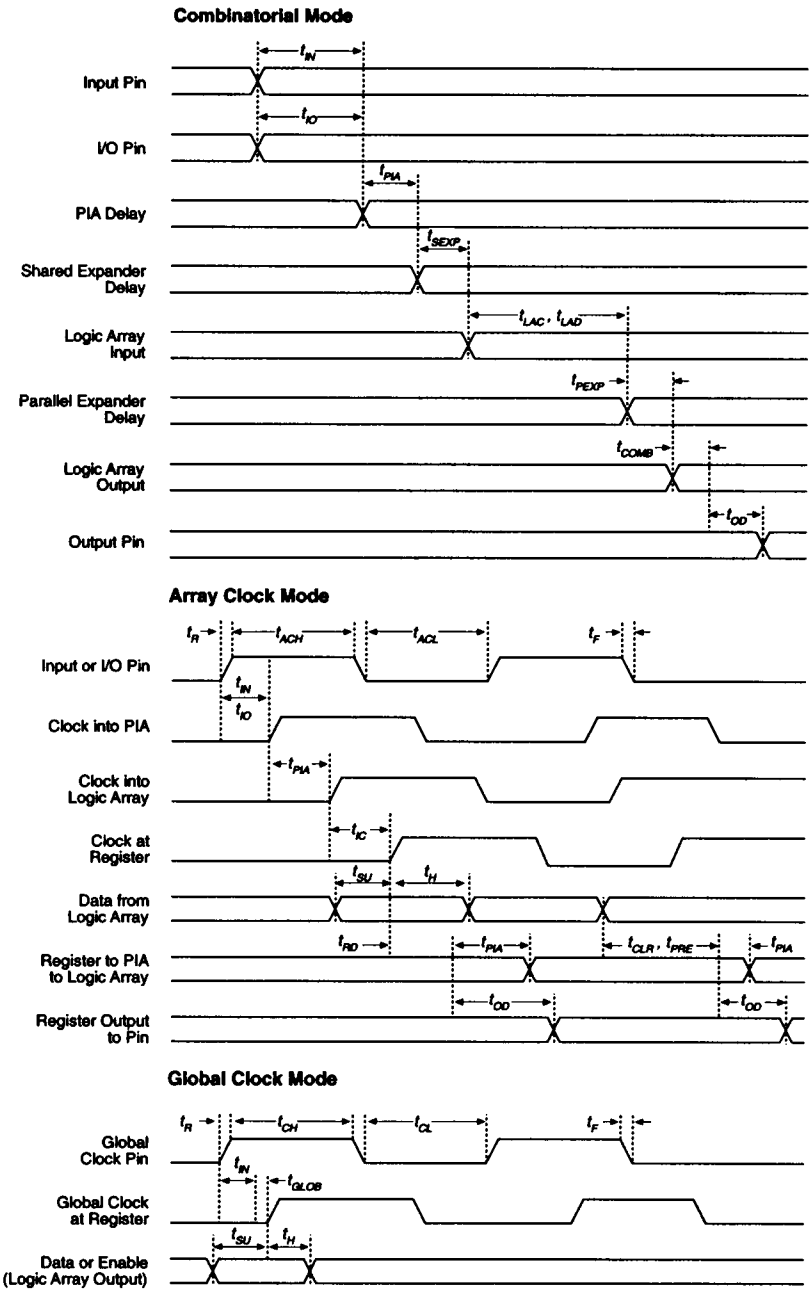
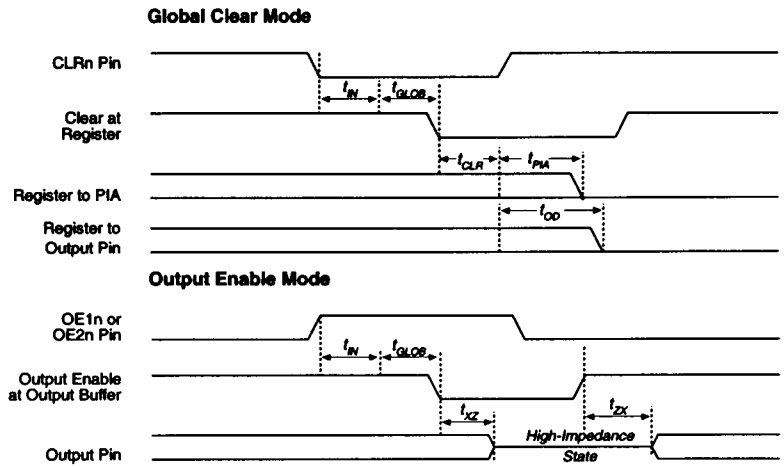


Figure 6. Switching Waveforms (Part 2 of 2)



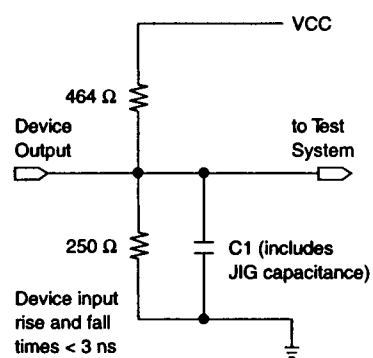
Generic Testing

The EPM7160 is functionally tested and guaranteed. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are made under the conditions shown in Figure 7.

Test patterns can be used and then erased during early stages of the production flow. This facility to use application-independent, general-purpose tests, called generic testing, is unique among user-configurable logic devices.

Figure 7. EPM7160 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, it can create significant reductions in observable noise immunity.



MAX+PLUS II Development System

The EPM7160 is supported by Altera's MAX+PLUS II development system. MAX+PLUS II also supports Altera Classic, MAX 5000/EPS464, and FLEX 8000 device families.

Designs can be entered as logic schematics with the Graphic Editor; as state machines, truth tables, and Boolean equations with the Altera Hardware Description Language (AHDL); or as waveforms with the Waveform Editor. Logic synthesis and minimization automatically optimize the logic of a design. MAX+PLUS II also provides automatic design partitioning into multiple devices from the same family. Design verification and timing analysis are performed with the built-in Simulator and Timing Analyzer. Errors in a design are automatically located and highlighted in the original design files.

MAX+PLUS II runs on IBM PC-AT, PS/2, and compatible computers, as well as Sun SPARCstations and HP 9000 Series 700 workstations. The software gives designers the tools to quickly and efficiently create complex logic designs. MAX+PLUS II also provides an EDIF netlist interface for additional design entry and simulation support with popular CAE tools from Cadence, DAZIX, Logic Modeling, Mentor Graphics, Synopsys, Viewlogic, and others. Further details about the MAX+PLUS II development system are available in the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

Device Programming

The EPM7160 can be programmed on an IBM PC-AT, PS/2, or compatible computer with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the PLMJ7160-84 or PLMQ7160-120 device adapter. The MPU supports device open- and short-circuit testing and performs continuity checking to ensure adequate electrical contact between the programming adapter and the device.

MAX+PLUS II software uses test vectors developed with the Waveform Editor to functionally test the programmed device. For added design verification, designers can compare the functional behavior of the EPM7160 with the results of timing simulation.

In addition, Data I/O and a variety of third-party manufacturers provide programming support for Altera devices.

Absolute Maximum Ratings See *Note (1)* and *Operating Requirements for EPLDs* in the 1992 ***Data Book***.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*See Note (2)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			800	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			4000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *See Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, No load *See Note (5)*		110		mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, No load, f = 1.0 MHz, *See Note (5)*		115		mA

Capacitance *See Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

AC Operating Conditions *See Note (3)*

External Timing Parameters			EPM7160-1		EPM7160-2		EPM7160-3		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{PD2}	I/O input to non-registered output			12		15		20	ns
t_{SU}	Global clock setup time		9		10		12		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		7		10		13	ns
t_{CH}	Global clock high time		4		5		6		ns
t_{CL}	Global clock low time		4		5		6		ns
t_{ASU}	Array clock setup time		4		5		5		ns
t_{AH}	Array clock hold time		4		5		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		12		15		20	ns
t_{ACH}	Array clock high time		5		7		8		ns
t_{ACL}	Array clock low time		5		7		8		ns
t_{CNT}	Minimum global clock period			11		13		15	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	90.9		76.9		66.6		MHz
t_{ACNT}	Minimum array clock period			11		14		15	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	90.9		71.4		66.6		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	125		100		83.3		MHz

Internal Timing Parameters			EPM7160-1		EPM7160-2		EPM7160-3		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			2		3		5	ns
t_{IO}	I/O input pad and buffer delay			2		3		5	ns
t_{SEXP}	Shared expander delay			7		8		10	ns
t_{PEXP}	Parallel expander delay			1		2		3	ns
t_{LAD}	Logic array delay			5		5		6	ns
t_{LAC}	Logic control array delay			5		5		6	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		4		5	ns
t_{ZX}	Output buffer enable delay			6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6		9	ns
t_{SU}	Register setup time		4		5		5		ns
t_{H}	Register hold time		4		5		5		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			5		5		6	ns
t_{EN}	Register enable time			5		5		6	ns
t_{GLOB}	Global control delay			1		2		2	ns
t_{PRE}	Register preset time			3		4		4	ns
t_{CLR}	Register clear time			3		5		6	ns
t_{PIA}	Prog. Interconnect Array delay			1		2		3	ns
t_{LPA}	Low power adder	*See Note (8)*		12		13		15	ns

Notes to tables:

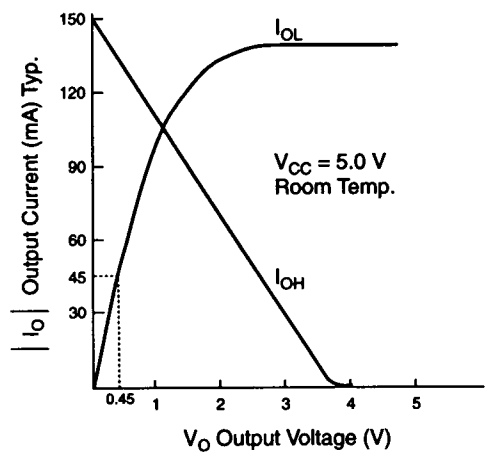
(1) Operation outside the absolute maximum ratings may permanently damage the device. Extended operation at absolute maximum ratings may impair device reliability.
(2) Minimum DC input is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(4) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
(5) Measured with a device programmed as a 16-bit loadable, enabled up/down counter in each LAB.
(6) Capacitance measured at 25° C. Sample tested only. `OE1n` (high-voltage pin during programming) has a capacitance of 25 pF.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{EN}, t_{SEXP} and t_{ACL} parameters for macrocells running in low-power mode.

Product Availability

Grade		Availability
Commercial	(0° C to 70° C)	EPM7160-1, EPM7160-2, EPM7160-3
Industrial	(–40° C to 85° C)	Consult factory
Military	(–55° C to 125° C)	Consult factory

Figure 8 shows output drive characteristics of EPM7160 I/O pins.

Figure 8. EPM7160 Output Drive Characteristics



Tables 1 and 2 show the pin-outs for the EPM7160 84-pin PLCC and 120-pin QFP packages, respectively.

Table 1. EPM7160 84-Pin PLCC Pin-Outs *Note (1)*

LAB	MC	Pin	LAB	MC	Pin	LAB	MC	Pin	LAB	MC	Pin	LAB	MC	Pin
A	1	11	B	17	18	C	33	–	D	49	–	E	65	–
A	2	–	B	18	–	C	34	–	D	50	–	E	66	–
A	3	10	B	19	17	C	35	25	D	51	33	E	67	41
A	4	–	B	20	–	C	36	–	D	52	–	E	68	–
A	5	–	B	21	–	C	37	–	D	53	–	E	69	–
A	6	–	B	22	–	C	38	24	D	54	31	E	70	40
A	7	–	B	23	–	C	39	–	D	55	–	E	71	–
A	8	9	B	24	16	C	40	23	D	56	30	E	72	37
A	9	8	B	25	15	C	41	–	D	57	–	E	73	–
A	10	–	B	26	–	C	42	–	D	58	–	E	74	–
A	11	5	B	27	14	C	43	20	D	59	29	E	75	36
A	12	–	B	28	–	C	44	–	D	60	–	E	76	–
A	13	–	B	29	–	C	45	–	D	61	–	E	77	–
A	14	–	B	30	–	C	46	21	D	62	28	E	78	35
A	15	–	B	31	–	C	31	–	D	47	–	E	63	–
A	16	4	B	32	12	C	32	22	D	48	27	E	64	34
F	81	–	G	97	–	H	113	–	I	129	67	J	145	74
F	82	–	G	98	–	H	114	–	I	130	–	J	146	–
F	83	44	G	99	52	H	115	60	I	131	68	J	147	75
F	84	–	G	100	–	H	116	–	I	132	–	J	148	–
F	85	–	G	101	–	H	117	–	I	133	–	J	149	–
F	86	45	G	102	54	H	118	61	I	134	–	J	150	–
F	87	–	G	103	–	H	119	–	I	135	–	J	151	–
F	88	48	G	104	55	H	120	62	I	136	69	J	152	76
F	89	–	G	105	–	H	121	–	I	137	70	J	153	77
F	90	–	G	106	–	H	122	–	I	138	–	J	154	–
F	91	49	G	107	56	H	123	65	I	139	71	J	155	80
F	92	–	G	108	–	H	124	–	I	140	–	J	156	–
F	93	–	G	109	–	H	125	–	I	141	–	J	157	–
F	94	50	G	110	57	H	126	64	I	142	–	J	158	–
F	95	–	G	111	–	H	127	–	I	143	–	J	159	–
F	96	51	G	112	58	H	128	63	I	144	73	J	160	81

EPM7160 84-pin PLCC dedicated inputs, VCC, GND, and Not Connected (NC) pin-outs:

VCC: 3, 13, 26, 38, 43, 53, 66, 78

GND: 7, 19, 32, 42, 47, 59, 72, 82

GCLK: 83; **OE1n:** 84; **OE2n:** 2; **GCLRn:** 1

NC: 6, 39, 46, 79

Note:

(1) A dash indicates a buried macrocell.

Table 2. EPM7160 120-Pin QFP Pin-Outs *Note (1)*

LAB	MC	Pin	LAB	MC	Pin	LAB	MC	Pin	LAB	MC	Pin	LAB	MC	Pin
A	1	119	B	17	10	C	33	22	D	49	33	E	65	44
A	2	–	B	18	–	C	34	–	D	50	–	E	66	–
A	3	118	B	19	9	C	35	20	D	51	32	E	67	43
A	4	–	B	20	–	C	36	–	D	52	–	E	68	–
A	5	117	B	21	8	C	37	19	D	53	31	E	69	42
A	6	116	B	22	7	C	38	18	D	54	29	E	70	41
A	7	–	B	23	–	C	39	–	D	55	–	E	71	–
A	8	115	B	24	6	C	40	17	D	56	28	E	72	39
A	9	114	B	25	5	C	41	11	D	57	27	E	73	38
A	10	–	B	26	–	C	42	–	D	58	–	E	74	–
A	11	112	B	27	4	C	43	13	D	59	26	E	75	37
A	12	–	B	28	–	C	44	–	D	60	–	E	76	–
A	13	111	B	29	2	C	45	14	D	61	25	E	77	36
A	14	110	B	30	1	C	46	15	D	62	24	E	78	35
A	15	–	B	31	–	C	47	–	D	63	–	E	79	–
A	16	109	B	32	120	C	48	16	D	64	23	E	80	34
F	81	47	G	97	58	H	113	69	I	129	81	J	145	92
F	82	–	G	98	–	H	114	–	I	130	–	J	146	–
F	83	48	G	99	59	H	115	71	I	131	82	J	147	93
F	84	–	G	100	–	H	116	–	I	132	–	J	148	–
F	85	49	G	101	60	H	117	72	I	133	83	J	149	94
F	86	50	G	102	62	H	118	73	I	134	84	J	150	95
F	87	–	G	103	–	H	119	–	I	135	–	J	151	–
F	88	52	G	104	63	H	120	74	I	136	85	J	152	96
F	89	53	G	105	64	H	121	80	I	137	86	J	153	97
F	90	–	G	106	–	H	122	–	I	138	–	J	154	–
F	91	54	G	107	65	H	123	78	I	139	87	J	155	99
F	92	–	G	108	–	H	124	–	I	140	–	J	156	–
F	93	55	G	109	66	H	125	77	I	141	89	J	157	100
F	94	56	G	110	67	H	126	76	I	142	90	J	158	101
F	95	–	G	111	–	H	127	–	I	143	–	J	159	–
F	96	57	G	112	68	H	128	75	I	144	91	J	160	102

EPM7160 120-pin QFP dedicated inputs, VCC, and GND:

VCC: 3, 21, 40, 46, 61, 79, 98, 108

GND: 12, 30, 45, 51, 70, 88, 103, 113

GCLK: 104; **OE1n:** 105; **OE2n:** 107; **GCLRn:** 106

Note:

(1) A dash indicates a buried macrocell.

Package Outlines

Figure 9 shows the package outline for the 84-pin PLCC package.

Figure 9. EPM7160 84-Pin Plastic J-Lead Chip Carrier (PLCC)

Dimensions are shown in inches/(millimeters).

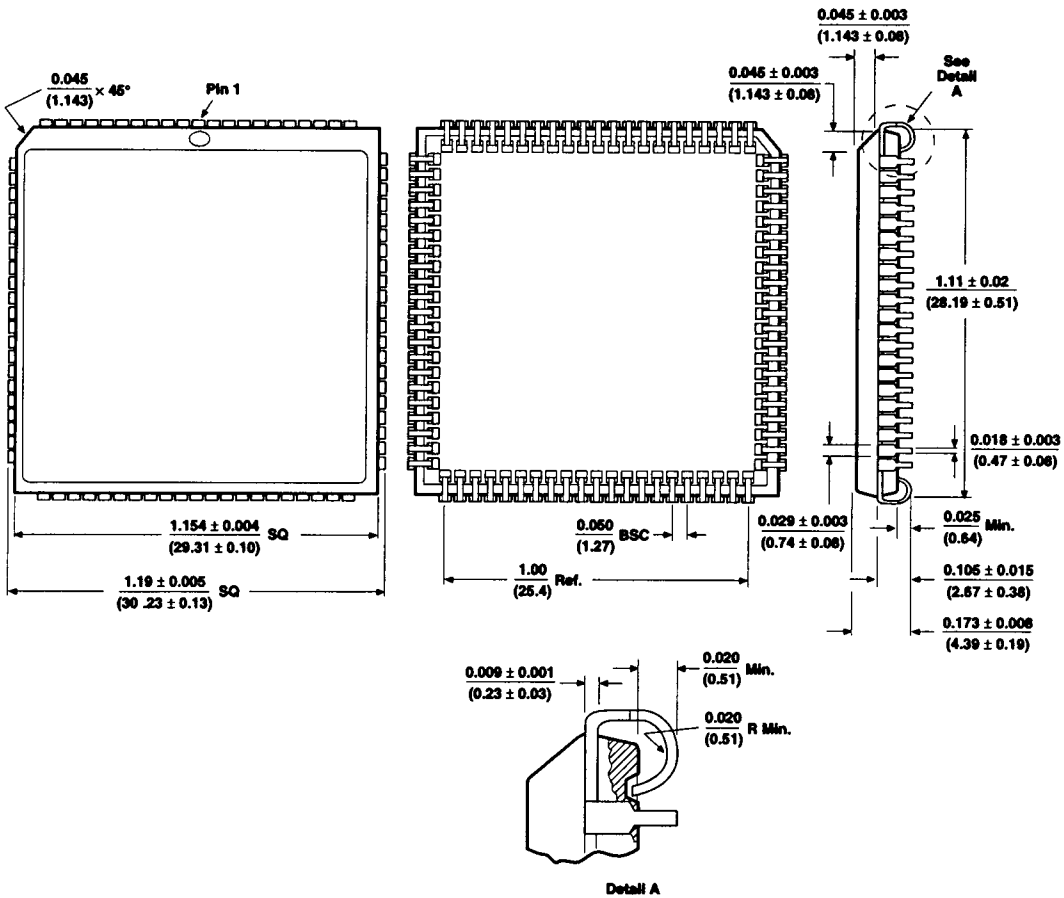
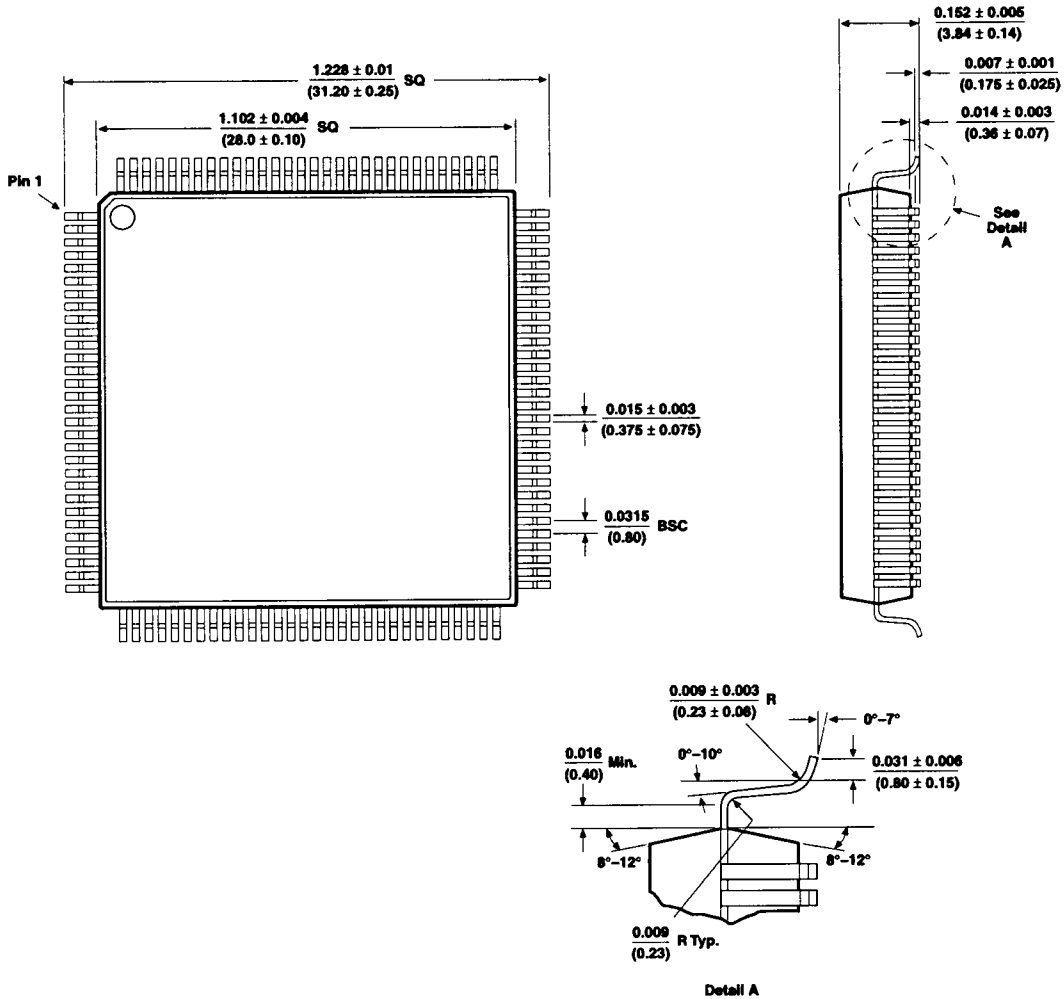


Figure 10 shows the package outline for the 120-pin plastic QFP package.

Figure 10. EPM7160 120-Pin Plastic Quad Flat Pack (QFP)

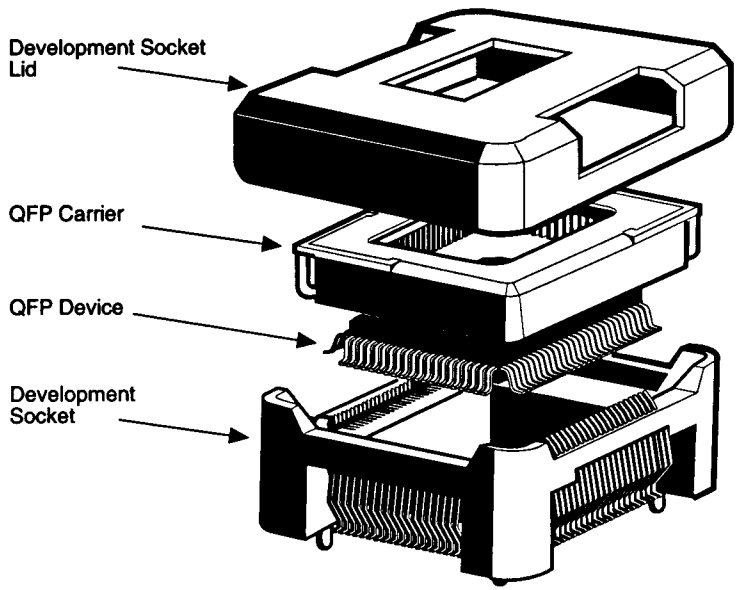
Dimensions are shown in inches/(millimeters).



QFP Carrier & Development Socket

The EPM7160 devices in QFP packages are shipped in special plastic carriers to protect the leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. Using this carrier technology, the EPLD may be programmed, tested, erased, and reprogrammed without exposing the leads to mechanical stress (see Figure 11). Refer to the *QFP Carrier & Development Socket Data Sheet* for more information and carrier dimensions.

Figure 11. QFP Carrier and Development Socket



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