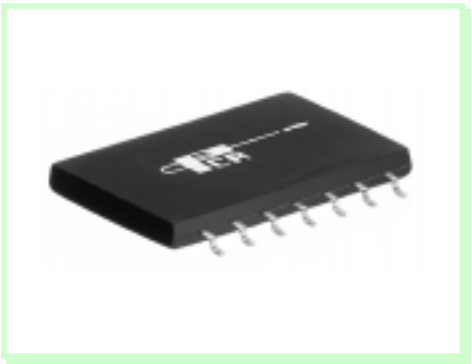
PCA ELECTRONICS INC.

120Ω Token Ring Front End Filter Module

EPT7069G

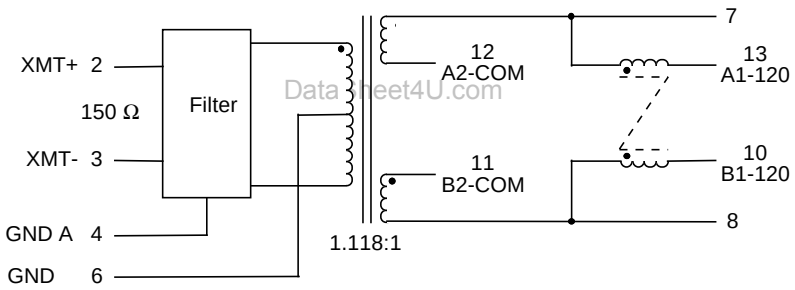


- Recommended for use in both UTP and STP
- Enhanced Common Mode Rejection Capability
- Robust construction in low profile allows for severe soldering processes
- Complies with or exceeds IEEE 802.5 Requirements

Electrical Parameters @ 25° C

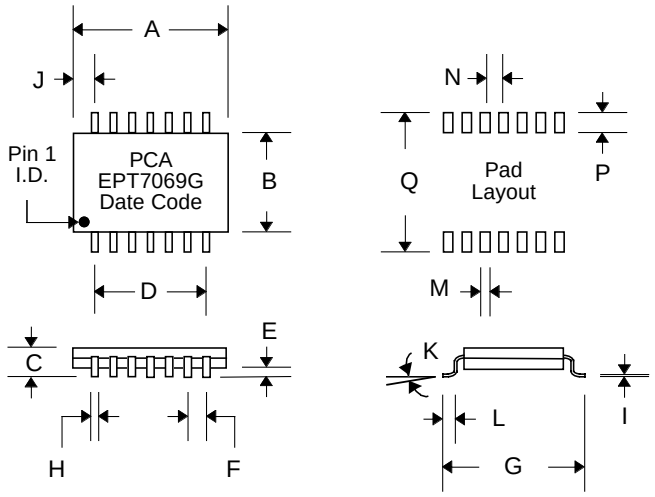
Impedance (Ω) [Xmit/Rcv]	Insertion Loss (dB)				Return Loss (dB Min.)			Common Mode Rejection (dB Min.)			
Media Side 150	1-16 MHz (Max.)	32 MHz (Min.)	36 MHz (Min.)	44 MHz (Min.)	1-6 MHz	6-17 MHz	17-25 MHz	1-30 MHz	30-100 MHz	100-200 MHz	200-300 MHz
Cable Side 120	-.8	-7	-18	-30	-18	-12	-8	-40	-20	-15	-10

Schematic



Pins 1, 5, 9 & 14 are not connected.

Package



Dimensions

Dim.	(Inches) Min.	Max.	Nom.	(millimeters) Min.	Max.	Nom.
A	.780	.800	.790	19.81	20.32	20.07
B	.510	.530	.520	12.95	13.46	13.21
C	.090	.100	.095	2.29	2.54	2.41
D	.595	.605	.600	15.11	15.37	15.24
E	.003	.010	.005	.076	.254	.127
F	.097	.103	.100	2.46	2.62	2.54
G	.660	.680	.670	16.76	17.27	17.02
H	.017	.022	.020	.432	.559	.508
I	.008	.013	.011	.203	.330	2.79
J	.090	.100	.095	2.29	2.54	2.41
K	0°	8°	4°	0°	8°	4°
L	.025	.045	.040	.635	1.14	1.02
M			.030			.762
N			.100			2.54
P			.085			2.16
Q			.700			17.78

PCA ELECTRONICS, INC.
16799 SCHOENBORN ST.
NORTH HILLS, CA 91343

TEL: (818) 892-0761
FAX: (818) 894-5791
http://www.pca.com

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The circuit below is a guideline for interconnecting PCA's EPT7069G with a typical Token Ring PHY chip for 4 Mb/16Mb applications over STP or UTP cable. Further details of system design should be obtained from the specific chip manufacturer. Note that this module is optimized for a "voltage source" driver such as TI380C series. Only one type of cable should be driven by the module: either UTP or STP. This module is ideally suited for applications with only one RJ45 connector installed. Changing to STP is accomplished by using an adaptor without any need for additional impedance transforming device embedded in it. The same approach is usable if one were to drive the European standard 120Ω cable, which poses no problems.

Note that the receiver side filtering is identical, thus making it possible for use in a DTR application as well. Consider this a cost effective solution for almost all Token Ring applications using this chip or similar chips.

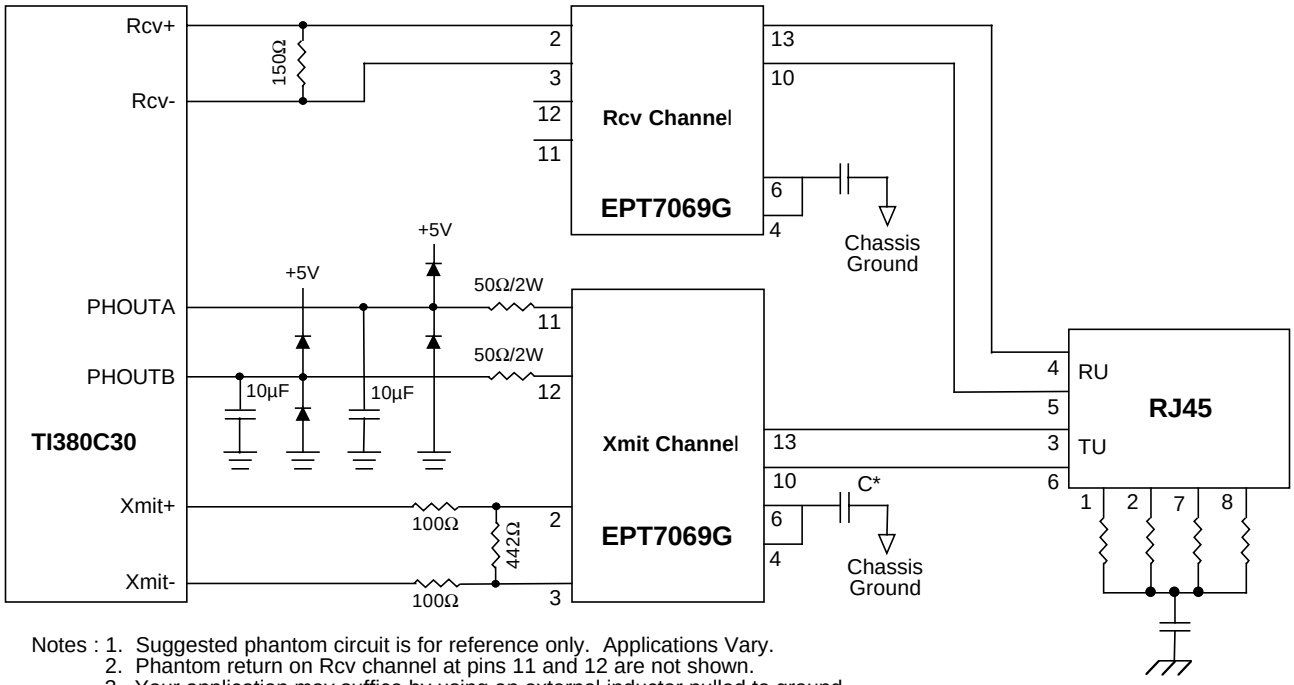
The pull down resistors to chassis via a cap shown around the RJ45 connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. This is specially true if driving UTP cable. Their placement and use are to be considered carefully before a design is finalized.

No specific recommendation is made here for phantom circuitry, implementation varies. Please note that additional emission control has been observed if both nodes of the phantom bypass capacitor on the transmit channel are pulled to the chassis ground via suitable capacitors.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPT7069G. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 75Ω/50Ω, balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit Connection to TI380C30 (or Equivalent)



Notes : 1. Suggested phantom circuit is for reference only. Applications Vary.
2. Phantom return on Rcv channel at pins 11 and 12 are not shown.
3. Your application may suffice by using an external inductor pulled to ground.
4. C* : Primary center taps may be pulled to ground by Caps to enhance common mode attenuation.

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