# ER-OLED0.95-2C

## OLED Display Datasheet

## EastRising Technology Co., Limited

Attention:

A. Some specifications of IC are not listed in this datasheet. Please refer to the IC datasheet for more details.

B. The related documents for interfacing, demo code, ic datasheet are all available, please download from www.buydisplay.com.

C. Please pay more attention to “Quality Control” in this Datasheet. We assume you already agree with these criterions when you place an order with us. No more recommendations.

| REV | DESCRIPTION | RELEASE DATE |
|---|---|---|
| 1.0 | Preliminary Release | Nov-28-2014 |
| | | |
| | | |

## ORDERING INFORMATION

Order Number

| Part Number(Order Number) | Description |
|---|---|
| ER-OLED0.95-2C | 0.95”OLED Display Module in 65,536 Colors |
| ER-DBO0.95-2C | Testing or Demo Board for ER-OLED0.95-2C Products |

Image


↑ ER-OLED0.95-2C

# Contents

# 1. Basic Specifications

## 1.1 Display Specifications

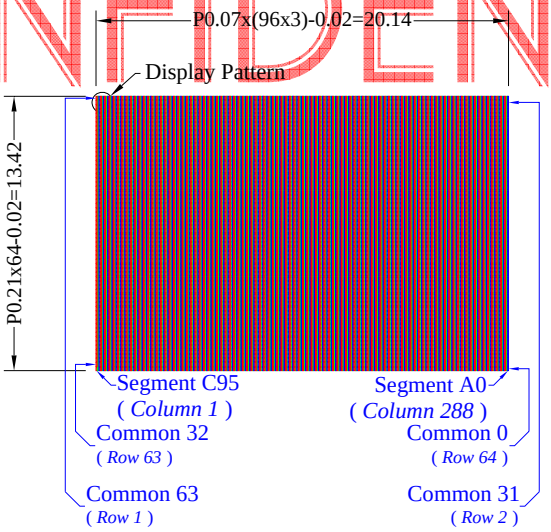
1) Display Mode: Passive Matrix
2) Display Color: 65,536 Colors (Maximum)
3) Drive Duty: 1/64 Duty

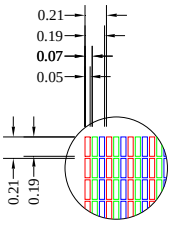
## 1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing number
2) Number of Pixels: 96 (RGB) × 64
3) Panel Size: 25.70 × 22.20 × 1.50 (mm)
4) Active Area: 20.14 × 13.42 (mm)
5) Pixel Pitch: 0.07 × 0.21 (mm)
6) Pixel Size: 0.05 × 0.19 (mm)
7) Weight: 1.8 (g)

## 1.3 Active Area & Pixel Construction

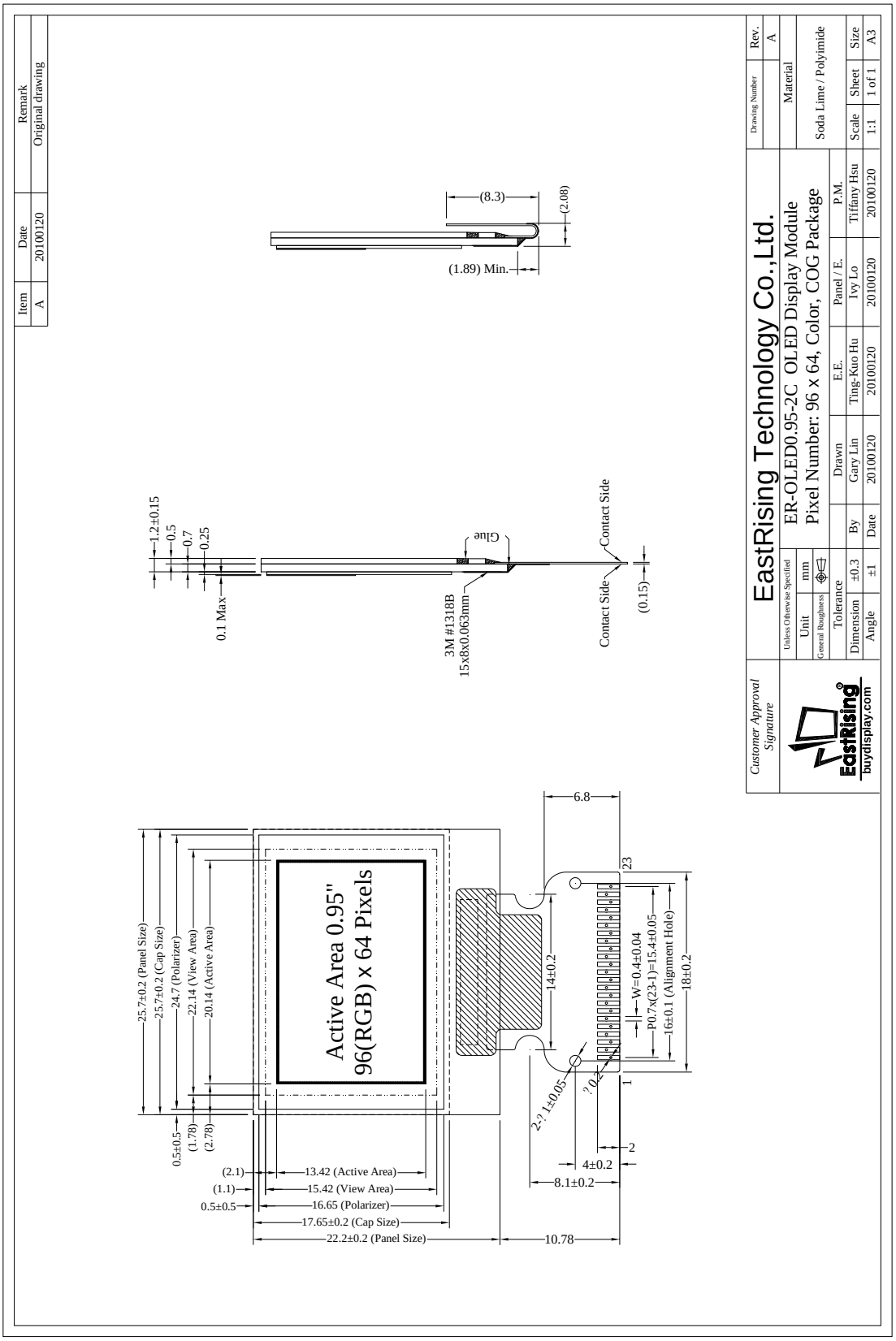





Display Pattern
Scale (5:1)

### 1.4 Mechanical Drawing



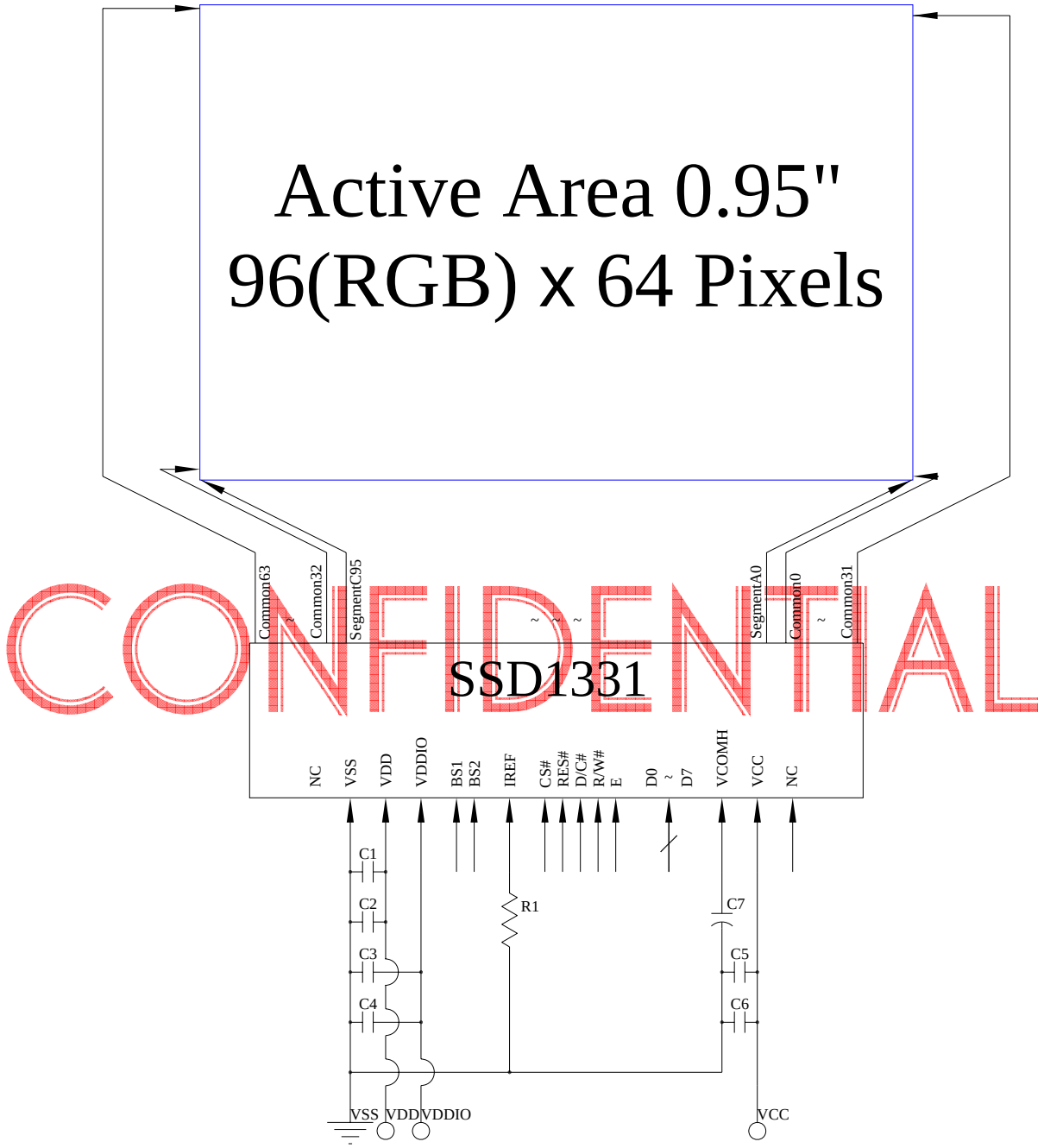
### 1.5 Pin Definition

| Pin Number | Symbol | Type | Function |
|---|---|---|---|
| *Power Supply Pins* | | | |
| 2 | VSS | P | *Ground of OEL System*<br>This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground. |
| 3 | VDD | P | *Power Supply Pins for Core $V_{DD}$*<br>This is a voltage supply pin. It must be connected to external source. |
| 4 | VDDIO | P | *Power Supply for Interface Logic Level*<br>It should be match with the MCU interface voltage level. $V_{DDIO}$ must always be equal or lower than $V_{DD}$. |
| 22 | VCC | P | *Power Supply for OEL Panel*<br>This is the most positive voltage supply pin of the chip. It should be supplied externally. |
| *MPU Interface Pins* | | | |
| 8 | CS# | I | *Chip Select*<br>This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low. |
| 9 | RES# | I | *Power Reset for Controller and Driver*<br>This pin is reset signal input. When the pin is low, initialization of the chip is executed. |
| 10 | D/C# | I | *Data/Command Control*<br>This pin is Data/Command control pin. When the pin is pulled high, the input at D0~D7 is treated as display data. When the pin is pulled low, the input at D0~D7 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams. |
| 11 | R/W# (WR#) | I | *Read/Write Select or Write*<br>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode.<br>When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. |
| 12 | E (RD#) | I | *Read/Write Enable or Read*<br>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.<br>When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. |
| 13~20 | D0~D7 | I/O | *Host Data Input/Output Bus*<br>These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. |

## 1.5 Pin Definition (Continued)

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">System Control Pins</td></tr>
<tr><td>5<br>6</td><td>BS1<br>BS2</td><td>I</td><td>Communicating Protocol Select<br>These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>68XX-parallel</td><td>80XX-parallel</td><td>Serial</td></tr>
<tr><td>BS1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>7</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment<br>This pin is segment current reference pin. A resistor should be connected between this pin and $V_{SS}$. Set the current at 10uA.</td></tr>
<tr><td>21</td><td>VCOMH</td><td>O</td><td>Voltage Output High Level for COM Signal<br>The COM signal deselected voltage level. A tantalum capacitor should be connected between this pin and $V_{SS}$.</td></tr>
<tr><td colspan="4">Reserved Pins</td></tr>
<tr><td>1, 23</td><td>NC</td><td>-</td><td>Reserved Pin (Supporting Pin)<br>The supporting pins can reduce the influences from stresses on the function pins.</td></tr>
</table>

### 1.6 Block Diagram






MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, CS#, D/C#, and RES#

C1, C3, C5: 10μF
C2, C4, C6: 0.1μF
C7: 4.7uF/20V Tantalum CAP
R1: 1.2MΩ, R1 = (Voltage at IREF – VSS) / IREF

## 2. Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.3 | 4 | V | 1, 2 |
| Driver Supply Voltage | $V_{CC}$ | 0 | 15 | V | 1, 2 |
| $V_{CC}$ Supply Current | $I_{CC}$ | - | 25 | mA | 1, 2 |
| Operating Temperature | $T_{OP}$ | -30 | 70 | °C | - |
| Storage Temperature | $T_{STG}$ | -40 | 80 | °C | - |

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

# 3. Electrical Characteristics

## 3.1 DC Characteristics

| Characteristics | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 2.4 | 2.8 | 3.5 | V |
| Supply Voltage for I/O Pins | $V_{DDIO}$ | | 1.6 | 2.8 | 3.5 | V |
| Driver Supply Voltage | $V_{CC}$ | | - | 14.0 | - | V |
| High Level Input | $V_{IH}$ | $I_{out}$ = 100μA, 3.3MHz | $0.8 \times V_{DDIO}$ | - | $V_{DDIO}$ | V |
| Low Level Input | $V_{IL}$ | $I_{out}$ = 100μA, 3.3MHz | 0 | - | $0.2 \times V_{DDIO}$ | V |
| High Level Output | $V_{OH}$ | $I_{out}$ = 100μA, 3.3MHz | $0.9 \times V_{DDIO}$ | - | $V_{DDIO}$ | V |
| Low Level Output | $V_{OL}$ | $I_{out}$ = 100μA, 3.3MHz | 0 | - | $0.1 \times V_{DDIO}$ | V |

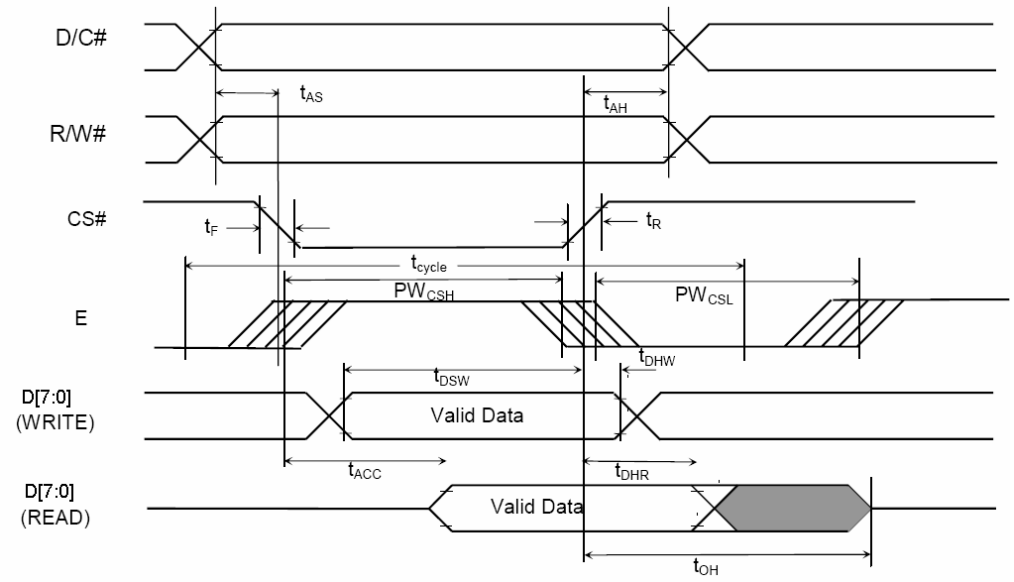
## 3.2 AC Characteristics

### 3.2.1 68XX-Series MPU Parallel Interface Timing Characteristics:

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time (write cycle) | 130 | - | ns |
| $PW_{CSL}$ | Control Pulse Low Width (write cycle) | 60 | - | ns |
| $PW_{CSH}$ | Control Pulse High Width (write cycle) | 60 | - | ns |
| $t_{cycle}$ | Clock Cycle Time (read cycle) | 200 | - | ns |
| $PW_{CSL}$ | Control Pulse Low Width (read cycle) | 100 | - | ns |
| $PW_{CSH}$ | Control Pulse High Width (read cycle) | 100 | - | ns |
| $t_{AS}$ | Address Setup Time | 0 | - | ns |
| $t_{AH}$ | Address Hold Time | 10 | - | ns |
| $t_{DSW}$ | Data Setup Time | 40 | - | ns |
| $t_{DHW}$ | Data Hold Time | 10 | - | ns |
| $t_{ACC}$ | Access Time | - | 140 | ns |
| $t_{OH}$ | Output Disable Time | - | 70 | ns |
| $t_R$ | Rise Time | - | 15 | ns |
| $t_F$ | Fall Time | - | 15 | ns |



* ($V_{DD}$ - $V_{SS}$ = 2.4V to 3.5V, $V_{DDIO}$ = 2.4V to $V_{DD}$, $T_A$ = -40 to +85°C)

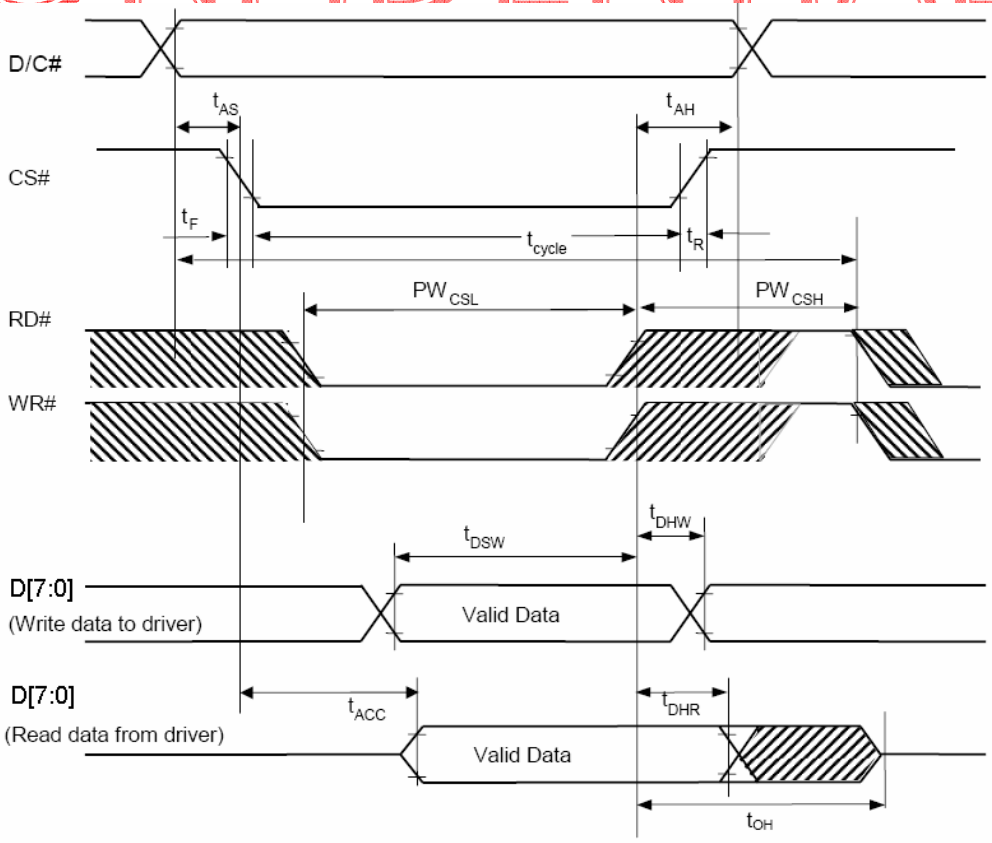


3.2.2 80XX-Series MPU Parallel Interface Timing Characteristics:

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 130 | - | ns |
| $t_{AS}$ | Address Setup Time | 0 | - | ns |
| $t_{AH}$ | Address Hold Time | 10 | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 40 | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 10 | - | ns |
| $t_{DHR}$ | Read Data Hold Time | 20 | - | ns |
| $t_{OH}$ | Output Disable Time | - | 70 | ns |
| $t_{ACC}$ | Access Time | - | 140 | ns |
| $PW_{CSL}$ | Chip Select Low Pulse Width (Read)<br>Chip Select Low Pulse Width (Write) | 120<br>60 | - | ns |
| $PW_{CSH}$ | Chip Select High Pulse Width (Read)<br>Chip Select High Pulse Width (Write) | 60<br>60 | - | ns |
| $t_R$ | Rise Time | - | 15 | ns |
| $t_F$ | Fall Time | - | 15 | ns |

* ($V_{DD}$ - $V_{SS}$ = 2.4V to 3.5V, $V_{DDIO}$ = 2.4V to $V_{DD}$, $T_A$ = -40 to +85°C)

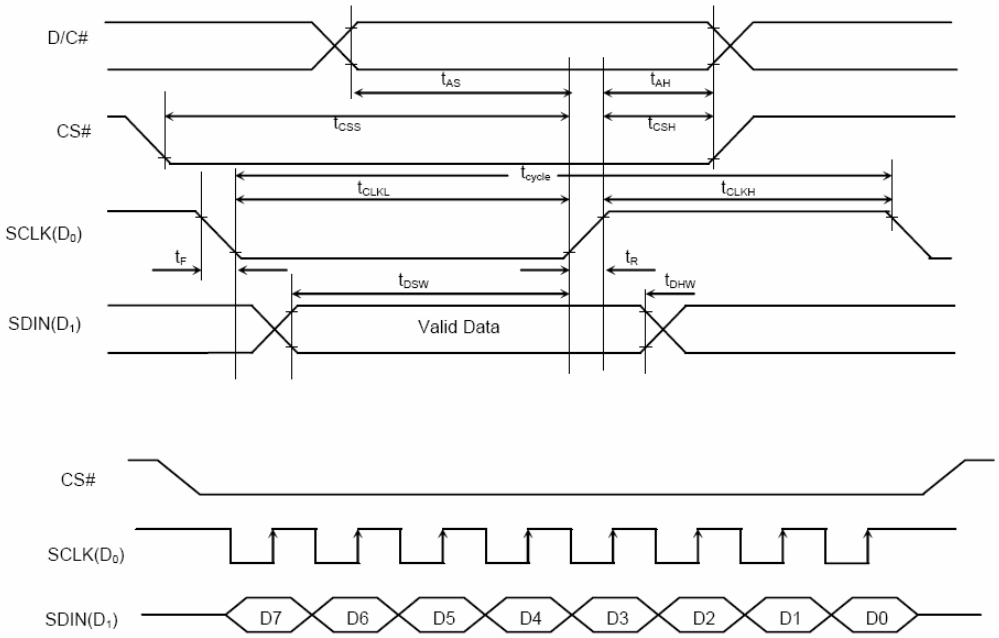




3.2.3 Serial Interface Timing Characteristics:

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{cycle}$ | Clock Cycle Time | 150 | - | ns |
| $t_{AS}$ | Address Setup Time | 40 | - | ns |
| $t_{AH}$ | Address Hold Time | 40 | - | ns |
| $t_{CSS}$ | Chip Select Setup Time | 75 | - | ns |
| $t_{CSH}$ | Chip Select Hold Time | 60 | - | ns |
| $t_{DSW}$ | Write Data Setup Time | 40 | - | ns |
| $t_{DHW}$ | Write Data Hold Time | 40 | - | ns |
| $t_{CLKL}$ | Clock Low Time | 75 | - | ns |
| $t_{CLKH}$ | Clock High Time | 75 | - | ns |
| $t_R$ | Rise Time | - | 15 | ns |
| $t_F$ | Fall Time | - | 15 | ns |

* ($V_{DD}$ - $V_{SS}$ = 2.4V to 3.5V, $V_{DDIO}$ = 2.4V to $V_{DD}$, $T_A$ = -40 to +85°C)



### 3.3 Optics & Electrical Characteristics

| Characteristics | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Brightness (White) | $L_{br}$ | With Polarizer (Note 3) | 80 | 100 | - | cd/m$^2$ |
| C.I.E. (White) | (x)<br>(y) | With Polarizer | 0.26<br>0.30 | 0.30<br>0.33 | 0.34<br>0.36 | |
| C.I.E. (Red) | (x)<br>(y) | With Polarizer | 0.57<br>0.30 | 0.61<br>0.34 | 0.65<br>0.38 | |
| C.I.E. (Green) | (x)<br>(y) | With Polarizer | 0.26<br>0.58 | 0.30<br>0.62 | 0.34<br>0.66 | |
| C.I.E. (Blue) | (x)<br>(y) | With Polarizer | 0.10<br>0.14 | 0.14<br>0.18 | 0.18<br>0.22 | |
| Dark Room Contrast | CR | | - | >1000:1 | - | |
| View Angle | | | >160 | - | - | degree |

* Optical measurement taken at $V_{DD}$ = 2.8V, $V_{CC}$ = 14V, and software configuration follows Sec. 9.1 “Software Initial Setting”.



### 3.4 General Electrical Specification

| Characteristics | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 2.4 | 2.8 | 3.5 | V |
| Supply Voltage for I/O Pins | $V_{DDIO}$ | | 1.6 | 2.8 | 3.5 | V |
| Driver Supply Voltage | $V_{CC}$ | Note 3 | - | 14.0 | - | V |
| Operating Current for $V_{DD}$ | $I_{DD}$ | Note 4 | - | 0.2 | 0.6 | mA |
| | | Note 5 | - | 0.2 | 0.6 | mA |
| Operating Current for $V_{CC}$ | $I_{CC}$ | Note 4 | - | 8 | 11 | mA |
| | | Note 5 | - | 13.5 | 18 | mA |
| Sleep Mode Current for $V_{DD}$ | $I_{DD, SLEEP}$ | | - | 1 | 2 | $\mu$A |
| Sleep Mode Current for $V_{CC}$ | $I_{CC, SLEEP}$ | | - | <2 | 2 | $\mu$A |

Note 3: Brightness ($L_{br}$) and Driver Supply Voltage ($V_{CC}$) are subject to the change of the panel characteristics and the customer’s request.

Note 4: $V_{DD}$ = 2.8V, $V_{CC}$ = 14V, Software Initial Setting follow Chapter 9.1 “Software Initial Setting”, 50% Display Area Turn on.

Note 5: $V_{DD}$ = 2.8V, $V_{CC}$ = 14V, Software Initial Setting follow Chapter 9.1 “Software Initial Setting”, 100% Display Area Turn on.

# 4. Functional Specification

## 4.1. Commands

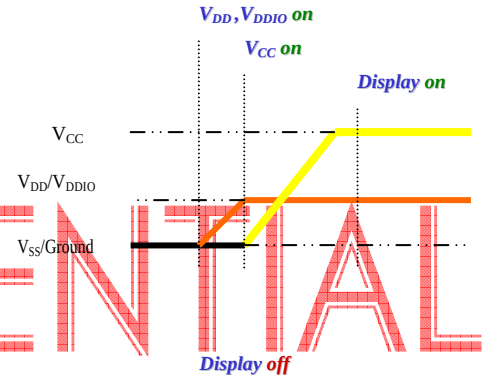
Refer to the Technical Manual for the SSD1331

## 4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

4.2.1 Power up Sequence:

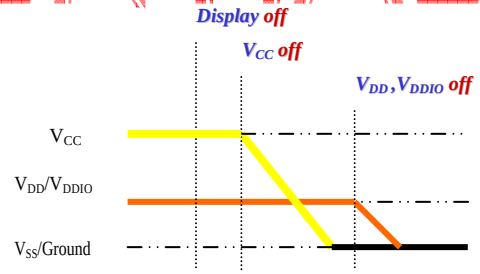
1. Power up $V_{DD}$ & $V_{DDIO}$
2. Send Display off command
3. Driver IC initial setting
4. Clear Screen
5. Power up $V_{CC}$
6. Delay 100ms
   (when $V_{DD}$ & $V_{DDIO}$ is stable)
7. Send Display on command






4.2.2 Power down Sequence:

1. Send Display off command
2. Power down $V_{CC}$
3. Delay 100ms
   (when $V_{CC}$ is reach 0 and panel is completely discharges)
4. Power down $V_{DD}$ & $V_{DDIO}$




## 4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 64 MUX Display Mode
3. Display start line is set at display RAM address 0
4. Display offset set to 0
5. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00H and COM0 mapped to address 00H)
6. Column address counter is set at 0
7. Master contrast control register is set at 0FH
8. Individual contrast control registers of color A, B, and C are set at 80H
9. Shift register data clear in serial interface
10. Normal display mode (Equivalent to A4 command)

### 4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization Setting>
Set Display On/Off (1010111X)
10101110 => 0xAE (Display Off)

Set Display Mode (101001XX)
10100100 => 0xA4 (Normal Display Mode)

Set Display Clock Divide Ratio / Oscillator Frequency
(10110011 with XXXXXXXX)

Set Display Offset
(10100010 with XXXXXXXX)

Set Multiplex Ratio
(11001000 with XXXXXXXX)

Set Master Configuration
(10101101 with 1000111X)
10001110 => 0x8E (External VCC Supply Selected)



Set Display Start Line
(10100001 with XXXXXXXX)
Set Segment Re-map & Data Format
(10100000 with XXXXXXXX)

Set Master Current Control
(10000111 with ****XXXX)
Set Contrast Control for Color “A”
(10000001 with XXXXXXXX)
Set Contrast Control for Color “B”
(10000010 with XXXXXXXX)
Set Contrast Control for Color “C”
(10000011 with XXXXXXXX)

Set Pre-charge Level
(10111011 with **XXXXXX)
Set Second Pre-charge Speed of Color A
(10001010 with XXXXXXXX)
Set Second Pre-charge Speed of Color B
(10001011 with XXXXXXXX)
Set Second Pre-charge Speed of Color C
(10001100 with XXXXXXXX)
Set VCOMH
(10111110 with 00XXXXX0)

Set Phase 1 & 2 Period Adjustment
(10110001 with XXXXXXXX)

Set Power Saving Mode
(10110000 with 000XXXXX)

Set Display On/Off (1010111X)
10101111 => 0xAF (Display On)

<Display Boundary Setting>
Set Column Address
(00010101 with XXXXXXXX for Start & XXXXXXXX for End)
Set Row Address
(01110101 with XXXXXXXX for Start & XXXXXXXX for End)

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

# 5. Reliability

## 5.1 Contents of Reliability Tests

| Item | Conditions | Criteria |
|---|---|---|
| High Temperature Operation | 70°C, 240 hrs | The operational functions work. |
| Low Temperature Operation | -30°C, 240 hrs | |
| High Temperature Storage | 80°C, 240 hrs | |
| Low Temperature Storage | -40°C, 240 hrs | |
| High Temperature/Humidity Operation | 60°C, 90% RH, 120 hrs | |
| Thermal Shock | -40°C ⇔ 85°C, 24 cycles 1 hr dwell | |

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

## 5.2 Lifetime



End of lifetime is specified as 50% of initial brightness.

| Parameter | Min | Max | Unit | Condition | Notes |
|---|---|---|---|---|---|
| Operating Life Time | 10,000 | - | Hrs | 80 cd/m$^2$, 50%checkerboard | 6 |
| Storage Life Time | 20,000 | - | Hrs | Ta=25°C, 50%RH | - |

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

## 5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

# 6. QUALITY CONTROL

6.1 EastRising Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature: 23±5℃

Humidity: 55±15% RH

Fluorescent Lamp: 30W

Distance between the Panel & Lamp: ≥50cm

Distance between the Panel & Eyes of the Inspector: ≥30cm

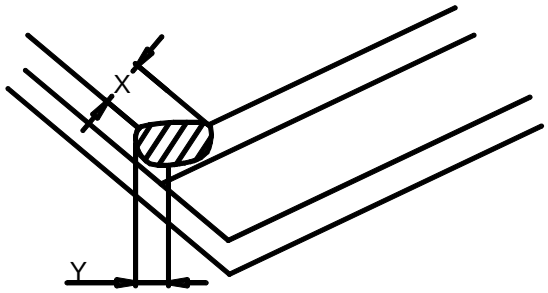
Finger glove (or finger cover) must be worn by the inspector.

Inspection table of jig must be anti-electrostatic.

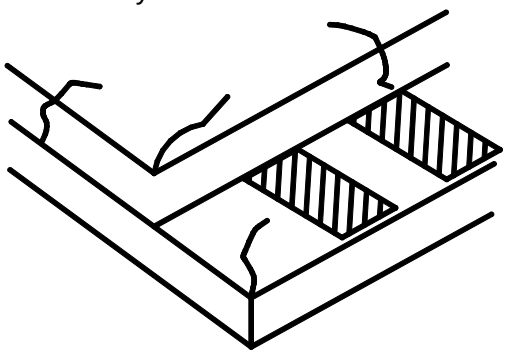
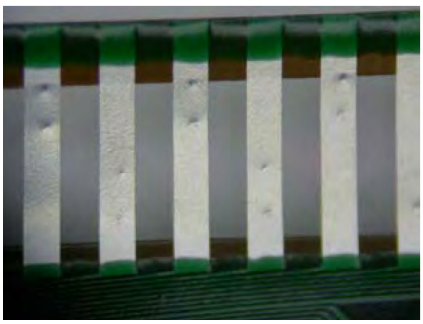
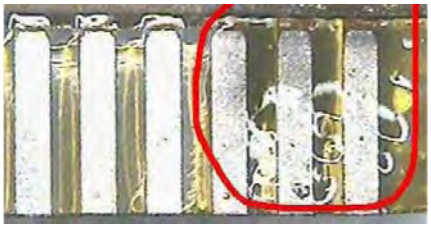
6.2 EastRising OLED Display Criteria & Acceptable Quality Level

| Partition | AQL | Definition |
|---|---|---|
| Major | 0.65 | Defects in Pattern Check (Display On) |
| Minor | 1.0 | Defects in Cosmetic Check (Display Off) |

6.2.1 EastRising Cosmetic Check (Display Off) in Non-Active Area

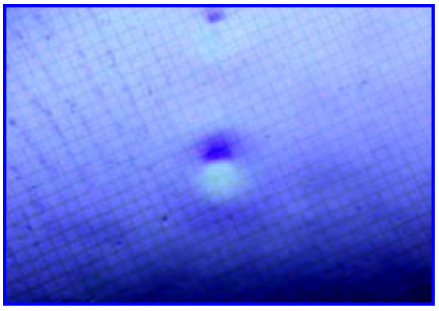
| Check Item | Classification | Criteria |
|---|---|---|
| Panel General Chipping | Minor | X>6mm (Along with Edge)<br>Y>1mm (Perpendicular to edge)<br>  |

6.2.2 EastRising Cosmetic Check (Display Off)in Non-Active Area (Continued)

| Check Item | Classification | Criteria |
|---|---|---|
| Panel Crack | Minor | Any crack is not allowable  |
| Copper Exposed (Even Pin or Film) | Minor | Not Allowable by Naked Eye Inspection |
| Film or Trace Damage | Minor |  |
| Termial Lead Prober Mark | Acceptable |  |
| Glue or Contamination on Pin | Minor |  |
| Ink marking on Back Side of Panel (Exclude on Film) | Acceptable | Ignore for Any |

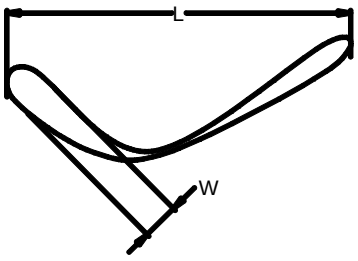
6.2.3 EastRising Cosmetic Check (Display Off) in Active Area

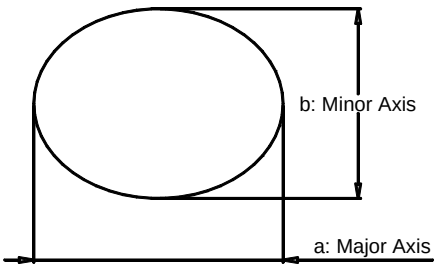
EastRising recommends to execute in clear environment (class 10k) if actual in necessary.

| Check Item | Classification | Criteria |
|---|---|---|
| Any Dirt & Scratch on Polarizer's Protective Film | Acceptable | Ignore for not Affect the Polarizer |
| Scratches,Fiber,Line-Shape Defect (On Polarizer) | Minor | W≤0.1 Ignore<br>W>0.1<br>L≤2 n≤1<br>L>2 n=0 |
| Dirt, Black Spot, Foreign Material (On Polarizer) | Minor | Φ≤0.1 Ignore<br>0.1<Φ≤0.25 n≤1<br>0.25<Φ n=0 |
| Dent,Bubbles,White Spot (Any Transparent Spot on Polarizer) | Minor | Φ≤0.5<br>Ignore if no Influence on Display<br>0.5<Φ n=0<br>  |
| Fingerpint ,Flow Mark (On Polarizer) | Minor | Not Allowable |

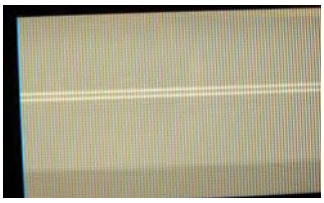
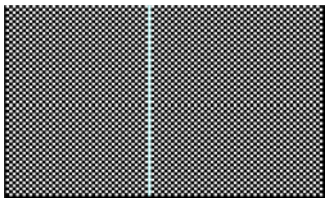
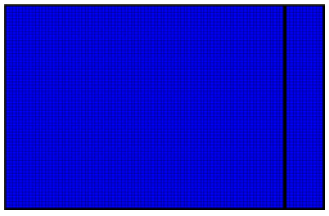
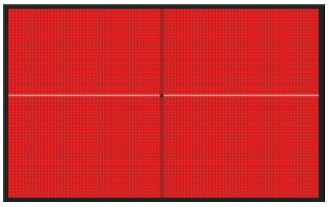
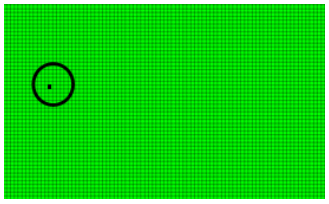
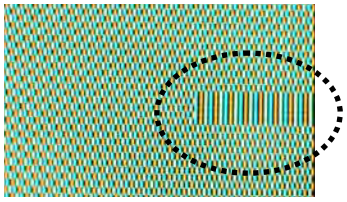
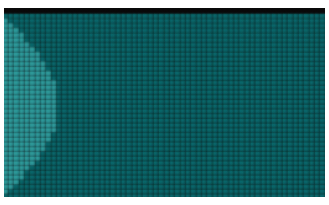
* Protective film should not be tear off when cosmetic check.

* Definition of W & L &Φ(Unit:mm): Φ=(a+b)/2



6.2.4 EastRising Pattern Check (Display On) in Active Area

| Check Item | Classification | Criteria |
|---|---|---|
| No Display | Major | Not allowable |
| Bright Line | Major |  |
| Missed Line | Major |   |
| Pixel Short | Major |  |
| Darker Pixel | Major |  |
| Wrong Display | Major |  |
| Un-Uniform (Luminance Variation within a Display) | Major |  |

## 7.PRECAUTIONS for USING

7.1 Handling Precautions

1) Since the EastRiisng OLED display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.

2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.

3) If pressure is applied to the display surface or its neighborhood of the EastRising OLED display module, the cell structure may be damaged and be careful not to apply pressure to these sections.

4) The polarizer covering the surface of the OLED display module is soft and easily scratched. Please be careful when handling the OLED display module.

5) When the surface of the polarizer of the OLED display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
* Scotch Mending Tape No. 810 or an equivalent
Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy. Also, pay attention that the following liquid and solvent may spoil the polarizer:
* Water
* Ketone
* Aromatic Solvents

6) Hold EastRising OLED display module very carefully when placing OLED display module into the system housing. Do not apply excessive stress or pressure to OLED display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.

7) Do not apply stress to the driver IC and the surrounding molded sections.

8) Do not disassemble nor modify the OLED display module.

9) Do not apply input signals while the logic power is off.

10) Pay sufficient attention to the working environments when handing EastRising OLED display modules to prevent occurrence of element breakage accidents by static electricity.
* Be sure to make human body grounding when handling OLED display modules.
* Be sure to ground tools to use or assembly such as soldering irons.
* To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

* Protective film is being applied to the surface of the display panel of the OLED display module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the EastRising OLED display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

12) If electric current is applied when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

7.2 Storage Precautions

1) When storing EastRising OLED display modules, put them in static electricity preventive bags avoiding exposure neither to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high
humidity environment or low temperature (less than 0℃) environments. (We recommend you to store these modules in the packaged state when they were shipped from EastRising.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OLED display module, when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

7.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OLED display module, and if these values are exceeded, panel damage may be happen.

2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.

3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)

4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.

5) As for EMI, take necessary measures on the equipment side basically.

6) When fastening the OLED display module, fasten the external plastic housing section.

7) If power supply to the EastRising OLED display module is forcibly shut down by such errors as taking out the main battery while the OLED display panel is in operation, we cannot guarantee the quality of this OLED display module.

7.4 Precautions when disposing of the EastRising OLED display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OLED display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

7.5 Other Precautions

1) When an OLED display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

2) To protect OLED display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OLED display modules.
   * Pins and electrodes
   * Pattern layouts such as the FPC

3) With this OLED display module, the OLED driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OLED driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OLED driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OLED driver may be shielded from light during the inspection processes.

4) Although this OLED display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

**That's the end of the datasheet.**