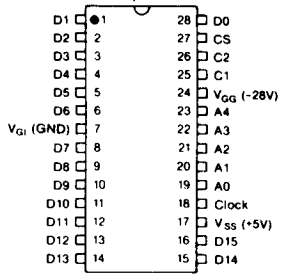
512 Bit Electrically Alterable Read Only Memory

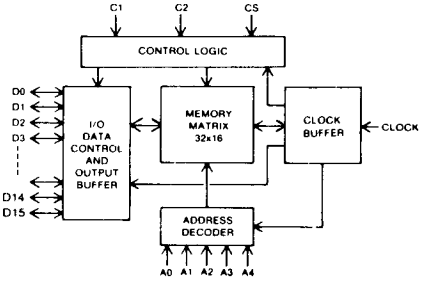
- 32 Word x 16 Bit Organization
- 5 Bit Binary Addressing
- +5, −28 V Power Supplies
- Word Alterable
- 10 Year Data Storage for ER2051 (at −70°C)
- 1 Year Data Storage for ER2051IR (at +85°C) and ER2051HR (at +125°C)
- TTL Compatibility with Pull-Up Resistors on Inputs
- Tri-State Outputs
- Read Time: 1μs (ER2051), 2μs (ER2051IR and ER2051HR)
- Write/Erase Time: 50ms (ER2051), 100ms (ER2051HR)
- No Voltage Switching Required
- Chip Select
- Two Extended Temperature Ranges;
  −40°C to +85°C ER2051IR
  −55°C to +125°C ER2051HR

PIN CONFIGURATION

28 LEAD DUAL IN LINE Top View



BLOCK DIAGRAM



DESCRIPTION

The ER2051, ER2051IR and ER2051HR are fully decoded 32 x 16 electrically erasable and reprogramable ROMs. Write, erase, and read voltages are switched internally via a 2-bit code applied to C1 and C2.

Data is stored by applying negative writing pulses that selectively tunnel charge into the oxide-nitride interface of the gate insulator of the 512 MNOS memory transistors. When the writing voltage is removed the charge trapped at the interface is manifested as a negative shift in the threshold voltage of the selected memory transistors.

The EAROM may be operated with the V_{SS} power supply between +5V and +10Volts, as long as the $V_{SS}-V_{GG}$ always equals 33 Volts. Thus, V_{SS} can be +5Volts for TTL compatibility or up to +10Volts for CMOS compatibility, if V_{GG} is appropriately adjusted.

The ER2051IR and ER2051HR are screened to Mil Std. 883B/method 5004.1/level B, pre-cap visual inspection, environmental testing, burn-in and external visual. They are available in 28 lead ceramic dual in line packages.

OPERATION

Data is stored in a two transistor memory cell. After the cell is preconditioned by an erase signal (which causes a positive shift in the threshold of both transistors), data is written into one of the transistors making its threshold more negative. A sensing flip flop is used to read the memory cell and presents a logic high or low to the output depending upon which transistor is written.

It is important to note two things: first, that an erase is required before a wire to precondition the cell, and second, that after an erase, both transistors will have the same threshold voltage and valid data will not be present at the output.

The ER2051, ER2051IR and ER2051HR EAROM's use internal dynamic, edge triggered circuits. This requires either a mode change, a clock, or a transition of the chip select between successive operations. Thus successive operations in the same mode must be separated by transitions of one of these four lines. Clock pulses are not normally required during erase or write operations, but are needed for successive operations if the chip select is held high, i.e., applications where one EAROM is used.

PIN FUNCTIONS

Pin No	Name	Function
19, 20, 21, 22	A_0-A_4	5-Bit Word Address.
1-6, 8-14, 28	D_0-D_{15}	Data input and output pins.
27	CS	Chip Select. Chip selected at logic "1". When chip select is at logic "0", outputs are open circuit, read, write and erase are disabled. Power is reduced.
25, 26	C1, C2	Mode Control Inputs. C1 C2 0 1 Erase Mode: stored data is erased at addressed location. 1 Don't Care Read Mode: addressed data read after clock pulse. Output data retained at output pins until chip deselected or control lines switched. 0 0 Write Mode: input data written at addressed location. Clock not required.
18	CLK	Clock input. Pulse to logic "1" for read operation.
17	V_{SS}	Substrate supply. Normally at +5 volts.
7	V_{GI}	Ground Input.
24	V_{GG}	Power Supply Input. Normally at −28 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All Inputs and Outputs (with Respect to V_{SS}) ..... −35V to +0.3V
Storage Temperature ..... −65°C to +150°C
Soldering Temperature of Leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (for TTL compatibility)

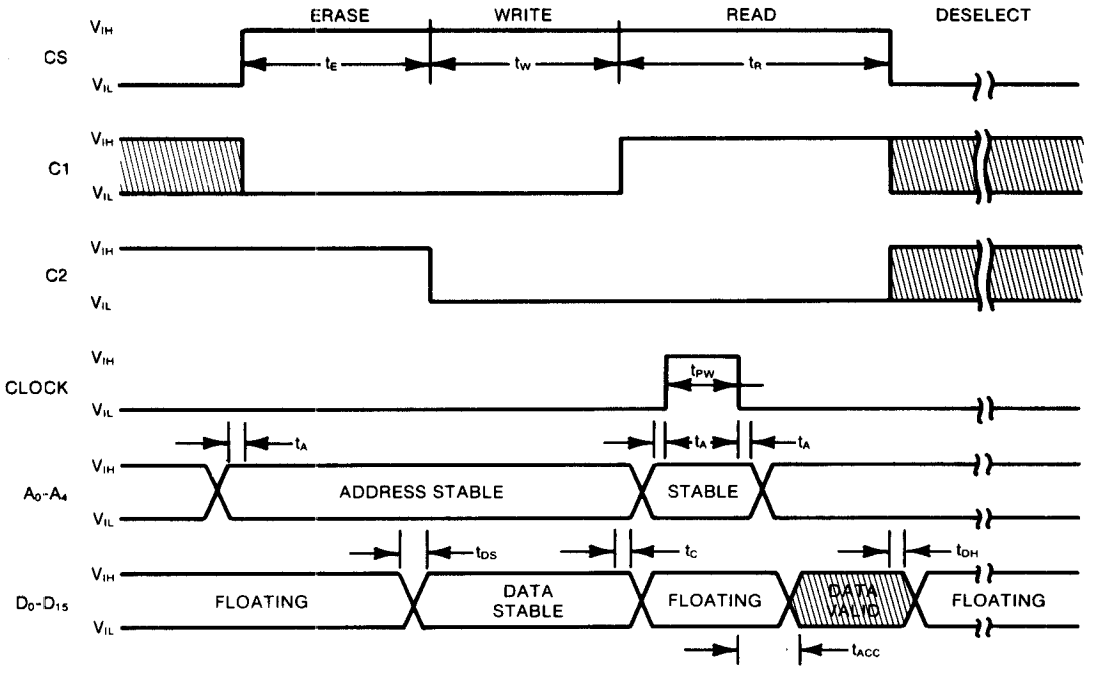
V_{SS} = +5V ±5%
V_{GG} = −28V ±5%
V_{GI} = GND
Operating Temperature T_A = 0°C to −70°C for ER2051
T_A = −40°C to +85°C for ER2051 IR
T_A = −55°C to +125°C for ER2051 HR
Output Load = 100pf, 1 TTL load

		ER2051			ER2051 IR/ER2051 HR				
Characteristics	**Sym**	**Min.**	**Typ.****	**Max.**	**Min.**	**Typ.****	**Max.**	**Units**	**Conditions**
DC CHARACTERISTICS									
Input Logic "1"	V_{IH}	V_{SS} −1.5	—	V_{SS} +0.3	V_{SS}−1.5	—	V_{SS} +0.3	V	
Input Logic "0"	V_{IL}	V_{SS} −15	—	0.8	V_{SS}−10	—	0.6	V	
Output Logic "1"	V_{OH}	V_{SS} −1.5	—	—	V_{SS}−1.5	—	—	V	I_{OH} = 100μA
Output Logic "0"	V_{OL}	—	—	0.6	—	—	0.6	V	I_{OL} = 1.6mA for V_{SS} = +5V
Input Leakage	I_L	—	2	10	—	2	10	μA	V_{IN} = V_{SS} −15
Output Leakage	I_O	—	2	10	—	2	10	μA	Chip deselected
Power Supply Current									
Read	I_{GG}	—	—	14	—	—	18	mA	I_{GG} returned through V_{SS}
Write	I_{GG}	—	—	11	—	—	15	mA	
Erase	I_{GG}	—	—	11	—	—	15	mA	
Deselected	I_{GG}	—	—	9	—	—	12	mA	
AC CHARACTERISTICS									
Access Time	t_{ACC}	—	—	1	—	—	2	μs	
Clock Pulse Width	t_{PW}	2	—	20	2	—	20	μs	
Erase Cycle Time	t_E	50	—	200	100	—	200	ms	
Write Cycle Time	t_W	50	—	200	100	—	200	ms	
Read Cycle Time	t_R	3.5	—	24	4.5	—	25	μs	
Address to Clock Time	t_A	50	—	—	50	—	—	ns	
Data Set Up Time	t_{DS}	50	—	—	50	—	—	ns	
Data Hold Time	t_{DH}	50	—	—	50	—	—	ns	
Control to Address & Data Change	t_C	0	—	—	0	—	—	ns	
Number of Reads/Word Refresh	N_{RA}	10^{11}	—	—	10^{11}	—	—		
Number of Erase/Write Cycles	N_W	10^6	—	—	10^5	—	—	—	
Input Capacitance (all pins)	C_{IO}	—	8	15	—	8	15	pf	
Unpowered Data Storage Time	t_S	10	—	—	1	—	—	Years	at max temperature
Power Dissipation Read Cycle	P_D	—	450	500	—	450	500	mW	at 25°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	500	mW	at 125°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	600	mW	at −55°C V_{SS} = +5, V_{GG} = −29
Pulse Rise, Fall Time	t_{rl}, t_f	10	—	100	10	—	100	ns	

**Typical values are at +25°C and nominal voltages.

TUNING

TIMING DIAGRAM



TUNING

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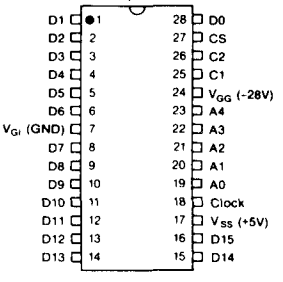
- 32 word x 16 bit organization
- 5 bit binary addressing
- +5, −28 V power supplies
- Word Alterable
- 10 year data storage for ER2051 (at +70°C)
- 1 year data storage for ER2051 IR (at +85°C) and ER2051 HR (at +125°C)
- TTL compatibility with pull-up resistors on inputs
- Tri-state outputs
- Read Time: 1μs (ER2051), 2μs (ER2051 IR and ER2051 HR)
- Write/Erase Time: 50ms (ER2051), 100ms (ER2051 HR)
- No Voltage switching required
- Chip select
- Two extended temperature ranges:
  −40°C to +85°C (Industrial) Part # ER2051 IR
  −55°C to +125°C (Hi-Rel) Part # ER2051 HR

PIN CONFIGURATION

28 LEAD DUAL IN LINE Top View



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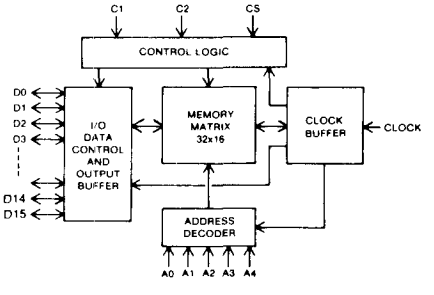

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CLK	Clock input. Pulse to logic "1" for read operation.
V_{SS}	Substrate supply. Normally at +5 volts.
V_{GI}	Ground Input.
V_{GG}	Power Supply Input. Normally at −28 volts.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All input and outputs (with respect to V_{SS}) ..... −35V to +0.3V
Storage temperature ..... −65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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T_A = −40°C to +85°C for ER2051 IR
T_A = −55°C to +125°C for ER2051 HR
Output Load = 100pf, 1 TTL load

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Input Logic "0"	V_{IL}	V_{SS} −15	—	0.8	V_{SS} −10	—	0.6	V	
Output Logic "1"	V_{OH}	V_{SS} −1.5	—	—	V_{SS} −1.5	—	—	V	I_{OH} = 100μA
Output Logic "0"	V_{OL}	—	—	0.6	—	—	0.6	V	I_{OL} = 1.6mA for V_{SS} = 5V
Input Leakage	I_L	—	2	10	—	2	10	μA	V_{IN} = V_{SS} −15
Output Leakage	I_O	—	2	10	—	2	10	μA	Chip deselected
Power Supply Current									
Read	I_{GG}	—	—	14	—	—	18	mA	I_{GG} returned through V_{SS}
Write	I_{GG}	—	—	11	—	—	15	mA	
Erase	I_{GG}	—	—	11	—	—	15	mA	
Deselected	I_{GG}	—	—	9	—	—	12	mA	
AC CHARACTERISTICS									
Access Time	t_{ACC}	—	—	1.0	—	—	2.0	μs	
Clock Pulse width	t_{PW}	2.0	—	20.0	2.0	—	20.0	μs	
Erase Cycle Time	t_E	50	—	200.0	100	—	200.0	ms	
Write Cycle Time	t_W	50	—	200.0	100	—	200.0	ms	
Read Cycle Time	t_R	3.5	—	24.0	4.5	—	25	μs	
Address to Clock Time	t_A	50	—	—	50	—	—	ns	
Data Set Up Time	t_{DS}	50	—	—	50	—	—	ns	
Data Hold Time	t_{DH}	50	—	—	50	—	—	ns	
Control to Address & Data Change	t_C	0	—	—	0	—	—	ns	
Number of Reads/Word Refresh	N_{RA}	10^{11}	—	—	10^{11}	—	—		
Number of Erase/Write Cycles	N_W	10^6	—	—	10^5	—	—	—	
Input Capacitance, all pins	C_{IN}	—	8	15	—	8	15	pF	
Unpowered Data Storage Time	t_S	10	—	—	1	—	—	Years	at max. temperature
Power Dissipation Read Cycle	P_D	—	450	500	—	450	500	mW	at 25°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	500	mW	at 125°C V_{SS} = +5, V_{GG} = −29
	P_D	not applicable			—	—	600	mW	at −55°C V_{SS} = +5, V_{GG} = −29
Pulse Rise, fall time	t_R, t_F	10	—	100	10	—	100	ns	

**Typical values are at +25°C and nominal voltages.

TIMING DIAGRAM