

ES29LV160E

16Mbit(2M x 8/1M x 16)

CMOS 3.0 Volt-only, Boot Sector Flash Memory

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GENERAL FEATURES

- **Single power supply operation**
 - 2.7V -3.6V for read, program and erase operations
- **Sector Structure**
 - 16Kbyte x 1, 8Kbyte x 2, 32Kbyte x 1 boot sectors
 - 64Kbyte x 31 sectors
- **Top or Bottom boot block**
 - ES29LV160ET for Top boot block device
 - ES29LV160EB for Bottom boot block device
- **Package Options**
 - 48-pin TSOP
 - 48-ball FBGA (6 x 8 mm)
 - Pb-free packages
 - All Pb-free products are RoHS-Compliant
- **Low Vcc write inhibit**
- **Manufactured on 0.18um process technology**
- **Compatible with JEDEC standards**
 - Pinout and software compatible with single-power supply flash standard

DEVICE PERFORMANCE

- **Read access time**
 - 70ns / 90ns
- **Program and erase time**
 - Program time : 6us/byte, 8us/word (typical)
 - Sector erase time : 0.7sec/sector (typical)
- **Power consumption (typical values)**
 - 200nA in standby or automatic sleep mode
 - 9mA active read current at 5 MHz
 - 15mA active write current during program or erase

- **Minimum 100,000 program/erase cycles per sector**
- **20 Year data retention at 125°C**

SOFTWARE FEATURES

- **Erase Suspend / Erase Resume**
- **Data# poll and toggle for Program/erase status**
- **CFI (Common Flash Interface) supported**
- **Unlock Bypass program**
- **Autoselect mode**
- **Auto-sleep mode after $t_{ACC} + 30ns$**

HARDWARE FEATURES

- **Hardware reset input pin (RESET#)**
 - Provides a hardware reset to device
 - Any internal device operation is terminated and the device returns to read mode by the reset
- **Ready/Busy# output pin (RY/BY#)**
 - Provides a program or erase operational status about whether it is finished for read or still being progressed
- **Sector protection / unprotection (RESET# , A9)**
 - Hardware method of locking a sector to prevent any program or erase operation within that sector
 - Two methods are provided :
 - In-system method by RESET# pin
 - A9 high-voltage method for PROM programmers
- **Temporary Sector Unprotection (RESET#)**
 - Allows temporary unprotection of previously protected sectors to change data in-system



GENERAL PRODUCT DESCRIPTION

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The ES29LV160 is a 16 megabit, 3.0 volt-only flash memory device, organized as 2M x 8 bits (Byte mode) or 1M x 16 bits (Word mode) which is configurable by BYTE#. Four boot sectors and thirty one main sectors are provided : 16Kbytes x 1, 8Kbytes x 2, 32Kbytes x 1 and 64Kbytes x 31. The device is manufactured with ESI's proprietary, high performance and highly reliable 0.18um CMOS flash technology. The device can be programmed or erased in-system with standard 3.0 Volt Vcc supply (2.7V-3.6V) and can also be programmed in standard EPROM programmers. The device offers minimum endurance of 100,000 program/erase cycles and more than 10 years of data retention.

The ES29LV160 offers access time as fast as 70ns or 90ns, allowing operation of high-speed microprocessors without wait states. Three separate control pins are provided to eliminate bus contention : chip enable (CE#), write enable (WE#) and output enable (OE#).

All program and erase operation are automatically and internally performed and controlled by embedded program/erase algorithms built in the device. The device automatically generates and times the necessary high-voltage pulses to be applied to the cells, performs the verification, and counts the number of sequences. Some status bits (DQ7, DQ6 and DQ5) read by data# polling or toggling between consecutive read cycles provide to the users the internal status of program/erase operation: whether it is successfully done or still being progressed.

The ES29LV160 is completely compatible with the JEDEC standard command set of single power supply Flash. Commands are written to the internal command register using standard write timings of microprocessor and data can be read out from the cell array in the device with the same way as used in other EPROM or flash devices.

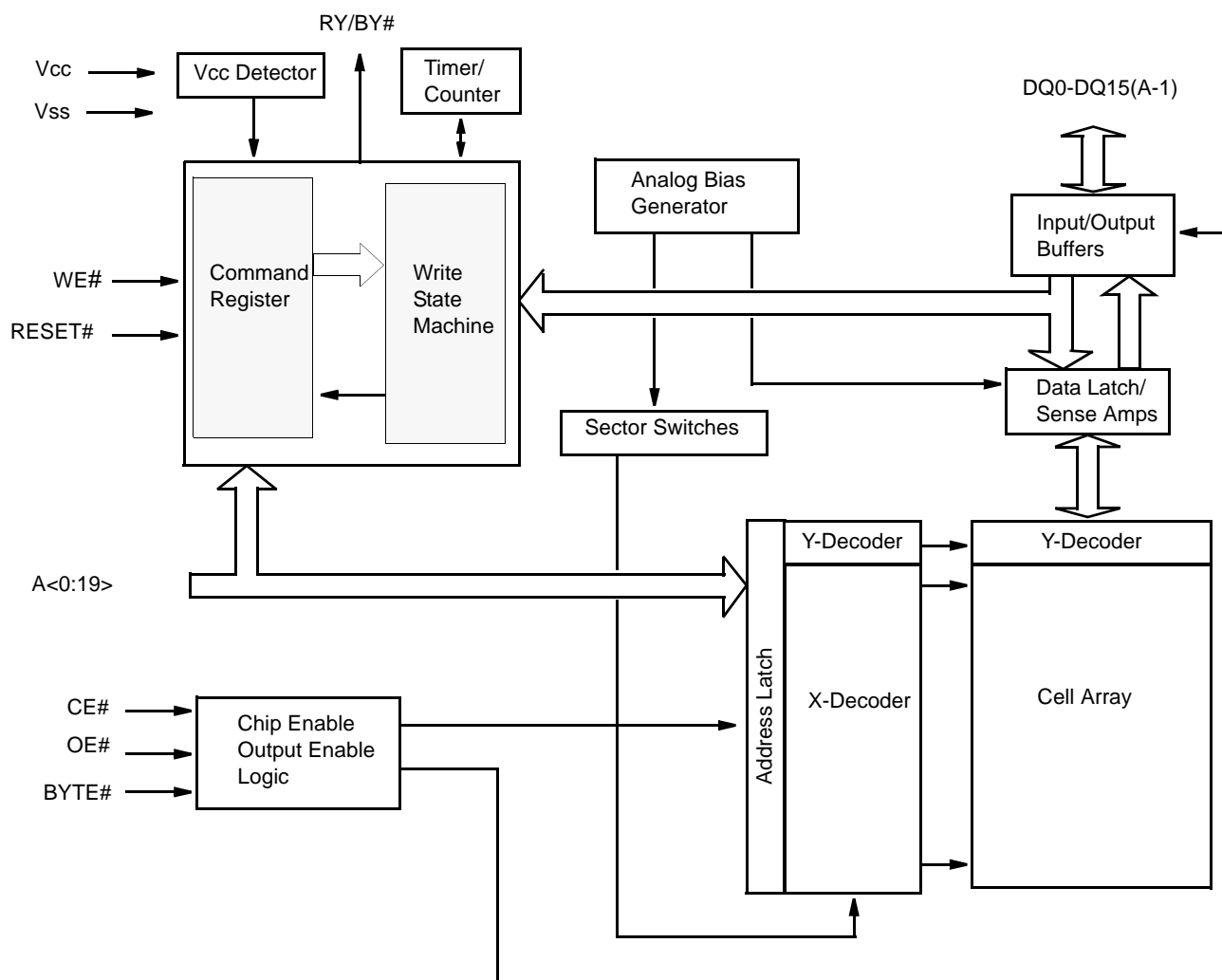


PRODUCT SELECTOR GUIDE

| Family Part Number | ES29LV160E | |
|----------------------|------------|-----------|
| Voltage Range | 2.7 ~ 3.6V | |
| Speed Option | 70 | 90 |
| Max Access Time (ns) | 70 | 90 |
| CE# Access (ns) | 70 | 90 |
| OE# Access (ns) | 35 | 40 |

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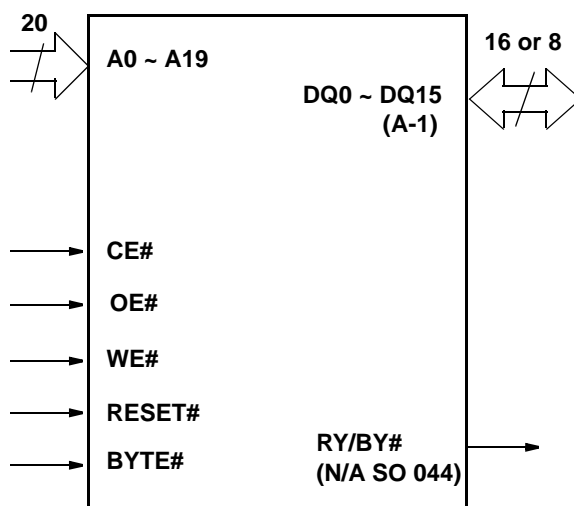
FUNCTION BLOCK DIAGRAM



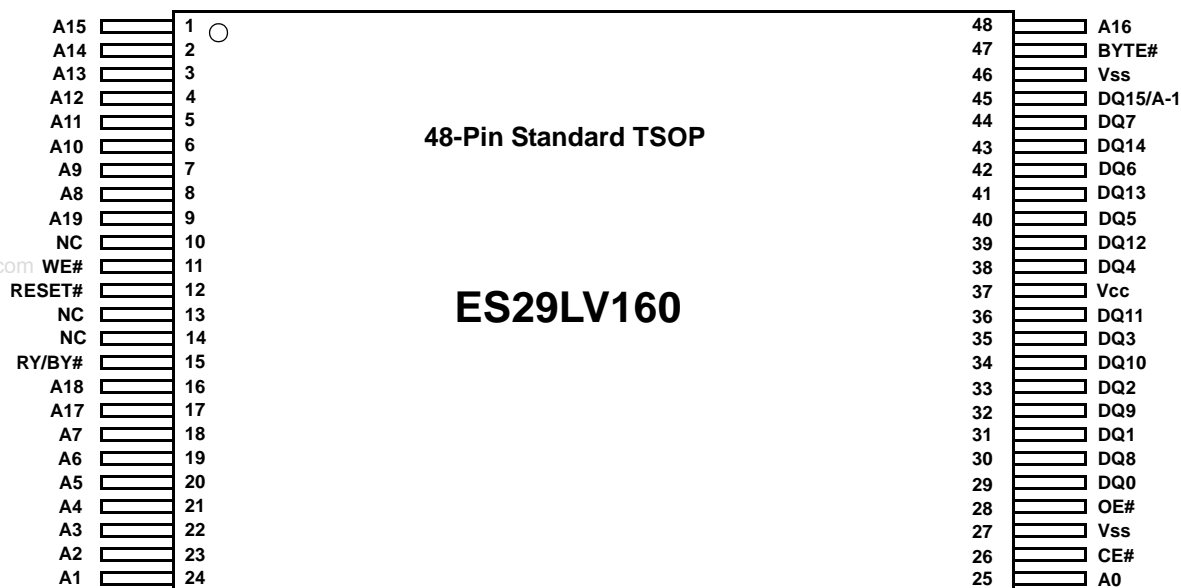
PIN DESCRIPTION

| Pin | Description |
|-----------------|---|
| A0-A19 | 20 Addresses |
| DQ0-DQ14 | 15 Data Inputs/Outputs |
| DQ15/A-1 | DQ15 (Data Input/Output, Word Mode) A-1 (LSB Address Input, Byte Mode) |
| CE# | Chip Enable |
| OE# | Output Enable |
| WE# | Write Enable |
| RESET# | Hardware Reset Pin, Active Low |
| BYTE# | Selects 8-bit or 16-bit mode |
| RY/BY# | Ready/Busy Output (N/A SO 044) |
| V _{cc} | 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances) |
| V _{ss} | Device Ground |
| NC | Pin Not Connected Internally |

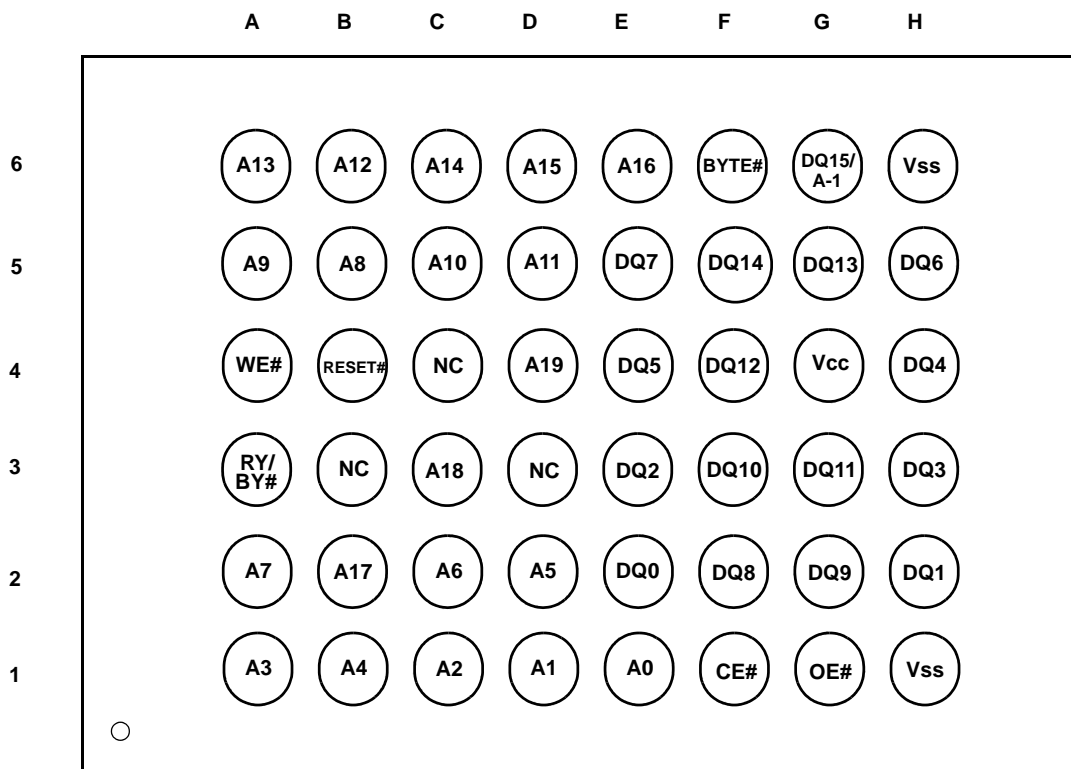
LOGIC SYMBOL



CONNECTION DIAGRAM



48-Ball FBGA (6 x 8 mm) (Top View, Balls Facing Down)



DEVICE BUS OPERATIONS

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Several device operational modes are provided in the ES29LV160 device. Commands are used to initiate the device operations. They are latched and stored into internal registers with the address and data information needed to execute the device operation.

The available device operational modes are listed in Table 1 with the required inputs, controls, and the resulting outputs. Each operational mode is described in further detail in the following subsections.

Read

The internal state of the device is set for the read mode and the device is ready for reading array data upon device power-up, or after a hardware reset. To read the stored data from the cell array of the device, CE# and OE# pins should be driven to V_{IL} while WE# pin remains at V_{IH} . CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins.

Word or byte mode of output data is determined by the BYTE# pin. No additional command is needed in this mode to obtain array data. Standard micro-processor read cycles that assert valid addresses

on the device address inputs produce valid data on the device data outputs. The device stays at the read mode until another operation is activated by writing commands into the internal command register. Refer to the AC read cycle timing diagrams for further details (Fig. 16).

Word/Byte Mode Configuration (BYTE#)

The device data output can be configured by BYTE# into one of two modes : word and byte modes. If the BYTE# pin is set at logic '1', the device is configured in word mode, DQ0 - DQ15 are active and controlled by CE# and OE#. If the BYTE# pin is set at logic '0', the device is configured in byte mode, and only data I/O pins DQ0 - DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8 - DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address.

Standby Mode

When the device is not selected or activated in a system, it needs to stay at the standby mode, in which current consumption is greatly reduced with outputs in the high impedance state.

The device enters the CMOS standby mode when CE# and RESET# pins are both held at $V_{CC} \pm 0.3V$. (Note that this is a more restricted voltage range than V_{IH} .) If CE# and RESET# are held at V_{IH} , but not within $V_{CC} \pm 0.3V$, the device will be still in the standby mode, but the standby current will be greater than the CMOS standby current (0.2uA typically). When the device is in the standby mode, only standard access time (t_{CE}) is required for read access, before it is ready for read data. And even if the device is deselected by CE# pin during erase or programming operation, the device draws active current until the operation is completely done. While the device stays in the standby mode, the output is placed in the high impedance state, independent of the OE# input.

The device can enter the deep power-down mode where current consumption is greatly reduced down to less than 0.2uA typically by the following three ways:

- **CMOS standby** (CE#, RESET# = $V_{CC} \pm 0.3V$)
- **During the device reset** (RESET# = $V_{SS} \pm 0.3V$)
- **In Autosleep Mode** (after $t_{ACC} + 30ns$)

Refer to the CMOS DC characteristics Table11 for further current specification.

Autosleep Mode

The device automatically enters a deep power-down mode called the autosleep mode when addresses remain stable for $t_{ACC} + 30ns$. In this mode, current consumption is greatly reduced (less than 0.2uA typical), regardless of CE#, WE# and OE# control signals.

Writing Commands

To write a command or command sequences to initiate some operations such as program or erase, the system must drive WE# and CE# to V_{IL} , and OE# to V_{IH} . For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to "BYTE# timings for Write Operations" in the Fig. 19 for more information.

Unlock Bypass Mode

To reduce more the programming time, an unlock-bypass mode is provided. Once the device enters this mode, only two write cycles are required to initiate the programming operation instead of four cycles in the normal program command sequences which are composed of two unlock cycles, program

set-up cycle and the last cycle with the program data and addresses. In this mode, two unlock cycles are saved (or bypassed).

Sector Addresses

The entire memory space of cell array is divided into a many of small sectors: 16Kbytes x 1, 8Kbytes x 2, 32Kbytes x 1 and 64Kbytes x 31 main sectors. In erase operation, a single sector, multiple sectors, or the entire device (chip erase) can be selected for erase. The address space that each sector occupies is shown in detail in the Table 3-4.

Autoselect Mode

Flash memories are intended for use in applications where the local CPU alters memory contents. In such applications, manufacturer and device identification (ID) codes must be accessible while the device resides in the target system (the so called "in-system program"). On the other hand, signature codes have been typically accessed by raising A9 pin to a high voltage in PROM programmers. However, multiplexing high voltage onto address lines is not the generally desired system design practice. Therefore, in the ES29LV160 device an **autoselect command** is provided to allow the system to access the signature codes without any high voltage. The conventional **A9 high-voltage method** used in the PROM programers for signature codes are still supported in this device.

If the system writes the autoselect command sequence, the device enters the Autoselect mode. The system can then read some useful codes such as manufacturer and device ID from the internal registers on DQ7 - DQ0. Standard read cycle timings apply in this mode. In the Autoselect mode, the following three informations can be accessed through either autoselect command method or A9 high-voltage autoselect method. Refer to the Table 2.

- **Manufacturer ID**
- **Device ID**
- **Sector protection verify**

Hardware Device Reset (RESET#)

The RESET# pin provides a hardware method of resetting the device to read array data. When the RESET# pin is driven low for at least a period of t_{RP} ,

the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once after the device is ready to accept another command sequence, to ensure data integrity.

CMOS Standby during Device Reset

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3V$, the device draws the greatly reduced CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within $V_{SS} \pm 0.3V$, the standby current will be greater.

RY/BY# and Terminating Operations

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is completed, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is completed. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data after the RESET# pin returns to V_{IH} , which requires a time of t_{RH} .

RESET# tied to the System Reset

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory. Refer to the AC Characteristics tables for RESET# parameters and to Fig. 17 for the timing diagram.

SECTOR PROTECTION

The ES29LV160 features hardware sector protection. In the device, sector protection is performed on the sector previously defined in the Table 3-4. Once after a sector is protected, any program or erase operation is not allowed in the protected sector. The previously protected sectors must be unprotected by one of the unprotect methods provided here before changing data in those sectors.

Sector protection can be implemented via two methods.

- In-system protection
- A9 High-voltage protection

To check whether the sector protection was successfully executed or not, another operation called "protect verification" needs to be performed after the protection operation on a sector. All protection and protect verifications provided in the device are summarized in detail at the Table 1.

In-System Protection

"In-system protection", the primary method, requires V_{ID} (11.5V~12.5V) on the RESET# with $A6=0$, $A1=1$, and $A0=0$. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing. Refer to Fig. 26 for timing diagram and Fig. 2 for the protection algorithm.

A9 High-Voltage Protection

"High-voltage protection", the alternate method intended only for programming equipment, must force V_{ID} (11.5~12.5V) on address pin A9 and control pin OE# with $A6=0$, $A1=1$ and $A0=0$. Refer to Fig. 28 for timing diagram and Fig. 4 for the protection algorithm.

SECTOR UNPROTECTION

The previously protected sectors must be unprotected before modifying any data in the sectors. The sector unprotection algorithm unprotects all sectors in parallel. All unprotected sectors must first be protected prior to the first sector unprotection write cycle to avoid any over-erase due to the intrinsic erase characteristics of the protection cell. After the unprotection operation, all previously protected sectors will need to be individually re-protected. Standard microprocessor bus cycle timings are used in the unprotection and unprotect verification operations. Three unprotect methods are provided in the ES29LV160 device. All unprotection and unprotect verification cycles are summarized in detail at the Table 1.

- In-system unprotection
- A9 High-voltage unprotection
- Temporary sector unprotection

In-System Unprotection

“In-system unprotection”, the primary method, requires V_{ID} (11.5V~12.5V) on the **RESET#** with $A6=1$, $A1=1$, and $A0=0$. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing. Refer to Fig. 26 for timing diagram and Fig. 3 for the unprotection algorithm.

A9 High-Voltage Unprotection

“High-voltage unprotection”, the alternate method intended only for programming equipment, must force V_{ID} (11.5~12.5V) on address pin **A9** and control pin **OE#** with $A6=1$, $A1=1$ and $A0=0$. Refer to Fig. 29 for timing diagram and Fig. 5 for the unprotection algorithm.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the **RESET#** pin to V_{ID} (11.5V-12.5V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the **RESET#** pin, all the previously protected sectors are protected again. Fig. 1 shows the algorithm, and Fig. 25 shows the timing diagrams for this feature.

HARDWARE DATA PROTECTION

The ES29LV160 device provides some protection measures against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power-up, all internal registers and latches in the device are cleared and the device automatically resets to the read mode. In addition, with its internal state machine built-in the device, any alteration of the memory contents or any initiation of new operation can only occur after successful completion of specific command sequences. And several features are incorporated to prevent inadvertent write cycles resulting from V_{cc} power-up and power-down transition or system noise.

Low V_{cc} Write inhibit

When V_{cc} is less than V_{LKO} , the device does not accept any write cycles. This protects data during V_{cc} power-up and power-down.

The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{cc} is greater than V_{LKO} . The system must provide proper signals to the control pins to prevent unintentional writes when V_{cc} is greater than V_{LKO} .

Write Pulse “Glitch” Protection

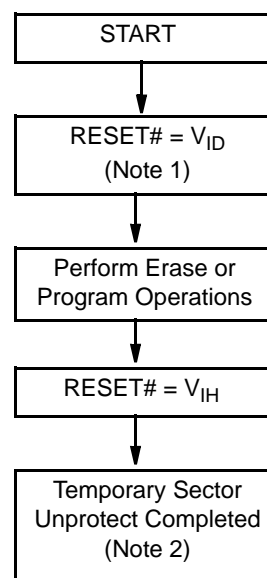
Noise pulses of less than 5ns (typical) on **OE#**, **CE#** or **WE#** do not initiate a write cycle.

Logical inhibit

Write cycles are inhibited by holding any one of $OE#=V_{IL}$, $CE#=V_{IH}$ or $WE#=V_{IH}$. To initiate a write cycle, **CE#** and **WE#** must be a logical zero while **OE#** is a logical one.

Power-up Write Inhibit

If $WE#=CE#=V_{IL}$ and $OE#=V_{IH}$ during power up, the device does not accept any commands on the rising edge of **WE#**. The internal state machine is automatically reset to the read mode on power-up.



Notes:

1. All protected sectors are unprotected .
2. All previously protected sectors are protected once again.

Figure 1. Temporary Sector Unprotect Operation

Table 1. ES29LV160 Device Bus Operations

| Operation | | CE# | OE# | WE# | RESET# | Addresses (Note 1) | DQ0 ~ DQ7 | DQ8~DQ15 | |
|-----------------------------|-------------------------------|---------------------------|-----------------|-----|---------------------------|---|------------------|----------------------------|----------------------------------|
| | | | | | | | | BYTE# = V _{IH} | BYTE# = V _{IL} |
| Read | | L | L | H | H | A _{IN} | D _{OUT} | D _{OUT} | DQ8~DQ14 = High-Z, DQ15 = A-1 |
| Write | | L | H | L | H | A _{IN} | (Note 3) | (Note 3) | |
| Standby | | V _{CC} ± 0.3V | X | X | V _{CC} ± 0.3V | X | High-Z | High-Z | High-Z |
| Output Disable Reset | | L | H | H | H | X | High-Z | High-Z | |
| | | X | X | X | L | X | High-Z | High-Z | |
| In-system | Sector Protect (Note 2) | L | H | L | V _{ID} | SA,A6=L, A1=H,A0=L | (Note 3) | X | X |
| | Sector Unprotect (Note 2) | L | H | L | V _{ID} | SA,A6=H, A1=H,A0=L | (Note 3) | X | X |
| | Temporary Sector Unprotect | X | X | X | V _{ID} | A _{IN} | (Note 3) | (Note 3) | High-Z |
| A9 High-Volt- age Method | Sector protect | L | V _{ID} | L | H | SA,A9=V _{ID} , A6=L, A1=H,A0=L | (Note 3) | (Note 3) | High-Z |
| | Sector unprotect | L | V _{ID} | L | H | SA,A9=V _{ID} , A6=H, A1=H,A0=L | | | |

Legend: L=Logic Low=V_{IL}, H=Logic High=V_{IH}, V_{ID}=11.5-12.5V, X=Don't Care, SA=Sector Address, A_{IN}=Address In, D_{IN}=Data In, D_{OUT}=Data Out

Notes:

- Addresses are A19:A0 in word mode (BYTE#=V_{IH}), A19:A-1 in byte mode (BYTE#=V_{IL}).
- The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector Protection and Unprotection" section.
- D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protection algorithm.

Table 2. Autoselect Codes (A9 High-Voltage Method)

| Description | CE# | OE# | WE# | A19 to A12 | A11 to A10 | A9 | A8 to A7 | A6 | A5 to A2 | A1 | A0 | DQ8~DQ15 | | DQ7~DQ0 |
|-----------------------------------|-----|-----|-----|------------------|------------------|-----------------|----------------|----|----------------|----|----|----------------------------|----------------------------|------------------------------------|
| | | | | | | | | | | | | BYTE# = V _{IH} | BYTE# = V _{IL} | |
| ManufactureID:ESI | L | L | H | X | X | V _{ID} | X | L | X | L | L | X | X | 4Ah |
| Device ID: ES29LV160 | L | L | H | X | X | V _{ID} | X | L | X | L | H | 22h | X | C4h(T),49h(B) |
| Sector Protection Verification | L | L | H | SA | X | V _{ID} | X | L | X | H | L | X | X | 01h(protected) 00h(unprotected) |

Legend: T= Top Boot Block, B = Bottom Boot Block, L=Logic Low=V_{IL}, H=Logic High=V_{IH}, SA=Sector Address, X = Don't care

Table 3. Top Boot Sector Addresses (ES29LV160ET)

| Sector | Sector address A19~A12 | Sector Size (Kbytes/Kwords) | (X8) Address Range | (X16) Address Range | Remark |
|--------|------------------------|-----------------------------|--------------------|---------------------|-------------|
| SA0 | 00000XXX | 64/32 | 000000h~00FFFFh | 00000h~07FFFh | Main Sector |
| SA1 | 00001XXX | 64/32 | 010000h~01FFFFh | 08000h~0FFFFh | |
| SA2 | 00010XXX | 64/32 | 020000h~02FFFFh | 10000h~17FFFh | |
| SA3 | 00011XXX | 64/32 | 030000h~03FFFFh | 18000h~1FFFFh | |
| SA4 | 00100XXX | 64/32 | 040000h~04FFFFh | 20000h~27FFFh | |
| SA5 | 00101XXX | 64/32 | 050000h~05FFFFh | 28000h~2FFFFh | |
| SA6 | 00110XXX | 64/32 | 060000h~06FFFFh | 30000h~37FFFh | |
| SA7 | 00111XXX | 64/32 | 070000h~07FFFFh | 38000h~3FFFFh | |
| SA8 | 01000XXX | 64/32 | 080000h~08FFFFh | 40000h~47FFFh | |
| SA9 | 01001XXX | 64/32 | 090000h~09FFFFh | 48000h~4FFFFh | |
| SA10 | 01010XXX | 64/32 | 0A0000h~0AFFFFh | 50000h~57FFFh | |
| SA11 | 01011XXX | 64/32 | 0B0000h~0BFFFFh | 58000h~5FFFFh | |
| SA12 | 01100XXX | 64/32 | 0C0000h~0CFFFFh | 60000h~67FFFh | |
| SA13 | 01101XXX | 64/32 | 0D0000h~0DFFFFh | 68000h~6FFFFh | |
| SA14 | 01110XXX | 64/32 | 0E0000h~0EFFFFh | 70000h~77FFFh | |
| SA15 | 01111XXX | 64/32 | 0F0000h~0FFFFFh | 78000h~7FFFFh | |
| SA16 | 10000XXX | 64/32 | 100000h~10FFFFh | 80000h~87FFFh | |
| SA17 | 10001XXX | 64/32 | 110000h~11FFFFh | 88000h~8FFFFh | |
| SA18 | 10010XXX | 64/32 | 120000h~12FFFFh | 90000h~97FFFh | |
| SA19 | 10011XXX | 64/32 | 130000h~13FFFFh | 98000h~9FFFFh | |
| SA20 | 10100XXX | 64/32 | 140000h~14FFFFh | A0000h~A7FFFh | |
| SA21 | 10101XXX | 64/32 | 150000h~15FFFFh | A8000h~AFFFFh | |
| SA22 | 10110XXX | 64/32 | 160000h~16FFFFh | B0000h~B7FFFh | |
| SA23 | 10111XXX | 64/32 | 170000h~17FFFFh | B8000h~BFFFFh | |
| SA24 | 11000XXX | 64/32 | 180000h~18FFFFh | C0000h~C7FFFh | |
| SA25 | 11001XXX | 64/32 | 190000h~19FFFFh | C8000h~CFFFFh | |
| SA26 | 11010XXX | 64/32 | 1A0000h~1AFFFFh | D0000h~D7FFFh | |
| SA27 | 11011XXX | 64/32 | 1B0000h~1BFFFFh | D8000h~DFFFFh | |
| SA28 | 11100XXX | 64/32 | 1C0000h~1CFFFFh | E0000h~E7FFFh | |
| SA29 | 11101XXX | 64/32 | 1D0000h~1DFFFFh | E8000h~EFFFFh | |
| SA30 | 11110XXX | 64/32 | 1E0000h~1EFFFFh | F0000h~F7FFFh | |
| SA31 | 11110XX | 32/16 | 1F0000h~1F7FFFh | F8000h~FBFFFh | Boot Sector |
| SA32 | 1111100 | 8/4 | 1F8000h~1F9FFFh | FC000h~FCFFFh | |
| SA33 | 1111101 | 8/4 | 1FA000h~1FBFFFh | FD000h~FDFFFh | |
| SA34 | 111111X | 16/8 | 1FC000h~1FFFFFh | FE000h~FFFFFh | |

Note:

The addresses range is A19:A-1 in byte mode (BYTE#=V_{IL}) or A19:A0 in word mode (BYTE#=V_{IH}).

Table 4. Bottom Boot Sector Addresses (ES29LV160EB)

| Sector | Sector address A19-A12 | Sector Size (Kbytes/Kwords) | (X8) Address Range | (X16) Address Range | Remark |
|--------|---------------------------|--------------------------------|-----------------------|------------------------|-------------|
| SA0 | 0000000X | 16/8 | 000000h~003FFFh | 00000h~01FFFh | Boot Sector |
| SA1 | 00000010 | 8/4 | 004000h~005FFFh | 02000h~02FFFh | |
| SA2 | 00000011 | 8/4 | 006000h~007FFFh | 03000h~03FFFh | |
| SA3 | 000001XX | 32/16 | 008000h~00FFFFh | 04000h~07FFFh | |
| SA4 | 00001XXX | 64/32 | 010000h~01FFFFh | 08000h~0FFFFh | Main Sector |
| SA5 | 00010XXX | 64/32 | 020000h~02FFFFh | 10000h~17FFFh | |
| SA6 | 00011XXX | 64/32 | 030000h~03FFFFh | 18000h~1FFFFh | |
| SA7 | 00100XXX | 64/32 | 040000h~04FFFFh | 20000h~27FFFh | |
| SA8 | 00101XXX | 64/32 | 050000h~05FFFFh | 28000h~2FFFFh | |
| SA9 | 00110XXX | 64/32 | 060000h~06FFFFh | 30000h~37FFFh | |
| SA10 | 00111XXX | 64/32 | 070000h~07FFFFh | 38000h~3FFFFh | |
| SA11 | 01000XXX | 64/32 | 080000h~08FFFFh | 40000h~47FFFh | |
| SA12 | 01001XXX | 64/32 | 090000h~09FFFFh | 48000h~4FFFFh | |
| SA13 | 01010XXX | 64/32 | 0A0000h~0AFFFFh | 50000h~57FFFh | |
| SA14 | 01011XXX | 64/32 | 0B0000h~0BFFFFh | 58000h~5FFFFh | |
| SA15 | 01100XXX | 64/32 | 0C0000h~0CFFFFh | 60000h~67FFFh | |
| SA16 | 01101XXX | 64/32 | 0D0000h~0DFFFFh | 68000h~6FFFFh | |
| SA17 | 01110XXX | 64/32 | 0E0000h~0EFFFFh | 70000h~77FFFh | |
| SA18 | 01111XXX | 64/32 | 0F0000h~0FFFFh | 78000h~7FFFFh | |
| SA19 | 10000XXX | 64/32 | 100000h~10FFFFh | 80000h~87FFFh | |
| SA20 | 10001XXX | 64/32 | 110000h~11FFFFh | 88000h~8FFFFh | |
| SA21 | 10010XXX | 64/32 | 120000h~12FFFFh | 90000h~97FFFh | |
| SA22 | 10011XXX | 64/32 | 130000h~13FFFFh | 98000h~9FFFFh | |
| SA23 | 10100XXX | 64/32 | 140000h~14FFFFh | A0000h~A7FFFh | |
| SA24 | 10101XXX | 64/32 | 150000h~15FFFFh | A8000h~AFFFFh | |
| SA25 | 10110XXX | 64/32 | 160000h~16FFFFh | B0000h~B7FFFh | |
| SA26 | 10111XXX | 64/32 | 170000h~17FFFFh | B8000h~BFFFFh | |
| SA27 | 11000XXX | 64/32 | 180000h~18FFFFh | C0000h~C7FFFh | |
| SA28 | 11001XXX | 64/32 | 190000h~19FFFFh | C8000h~CFFFFh | |
| SA29 | 11010XXX | 64/32 | 1A0000h~1AFFFFh | D0000h~D7FFFh | |
| SA30 | 11011XXX | 64/32 | 1B0000h~1BFFFFh | D8000h~DFFFFh | |
| SA31 | 11100XXX | 64/32 | 1C0000h~1CFFFFh | E0000h~E7FFFh | |
| SA32 | 11101XXX | 64/32 | 1D0000h~1DFFFFh | E8000h~EFFFFh | |
| SA33 | 11110XXX | 64/32 | 1E0000h~1EFFFFh | F0000h~F7FFFh | |
| SA34 | 11111XXX | 64/32 | 1F0000h~1FFFFh | F8000h~FFFFh | |

Note:

The addresses range is A19:A-1 in byte mode (BYTE#=V_{IL}) or A19:A0 in word mode (BYTE#=V_{IH}).

In-System Protection / Unprotection Method

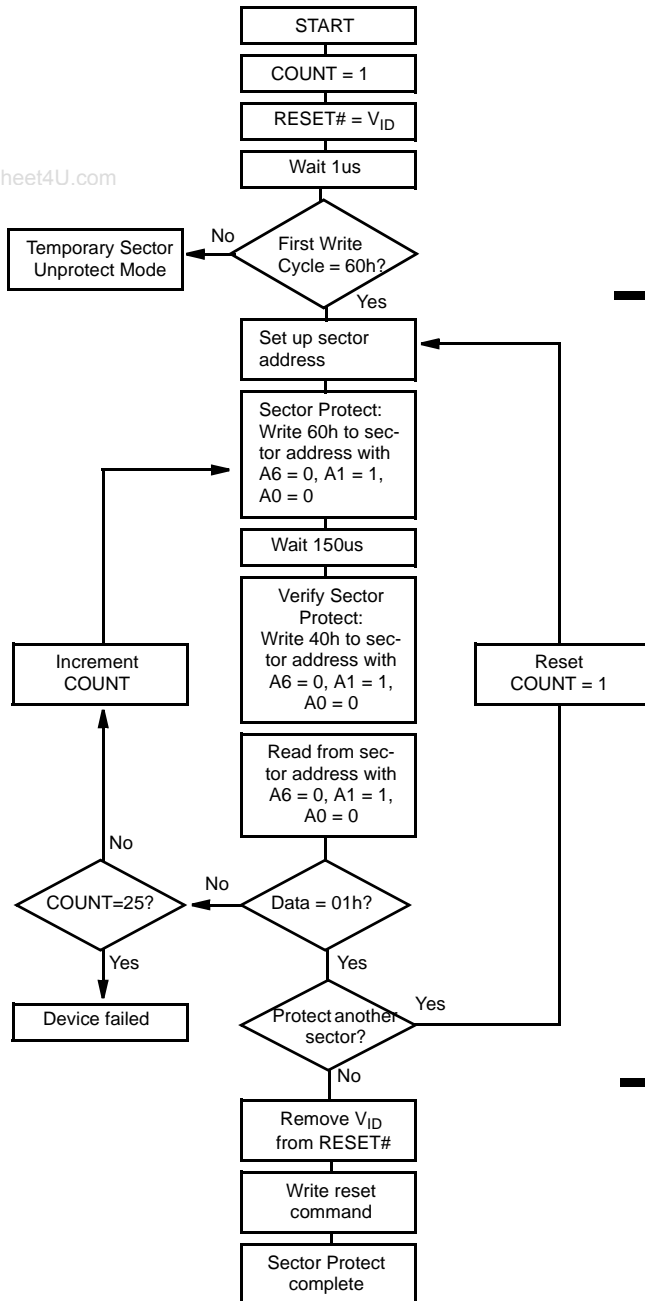


Figure 2. In-System Sector Protect Algorithm

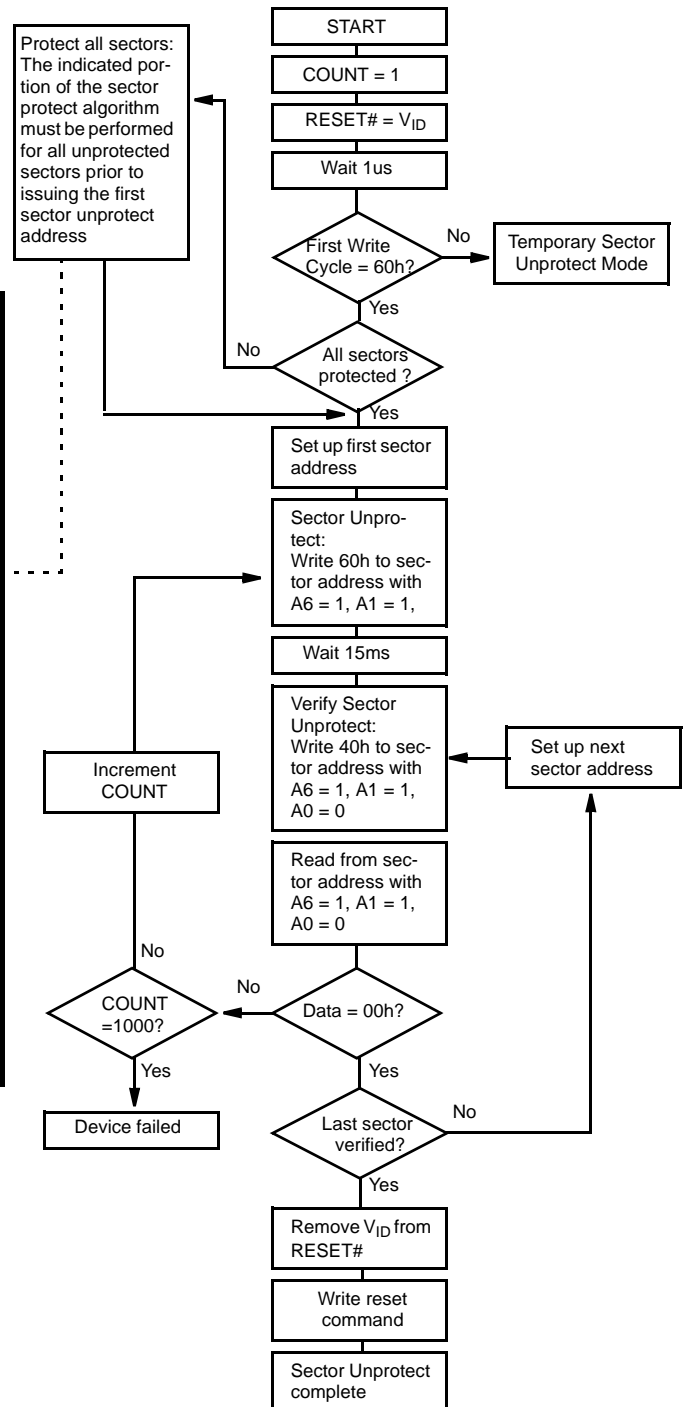


Figure 3. In-System Sector Unprotect Algorithm

A9 High-Voltage Method

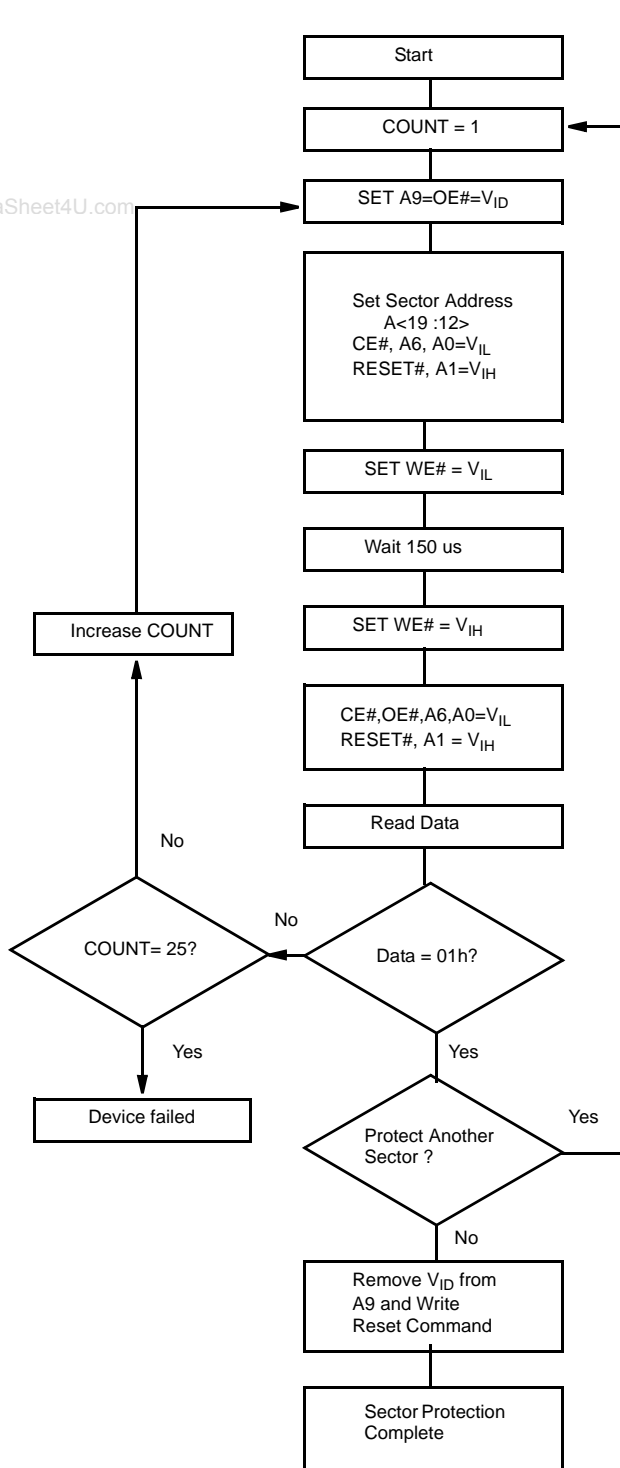


Figure 4. Sector Protection Algorithm
(A9 High-Voltage Method)

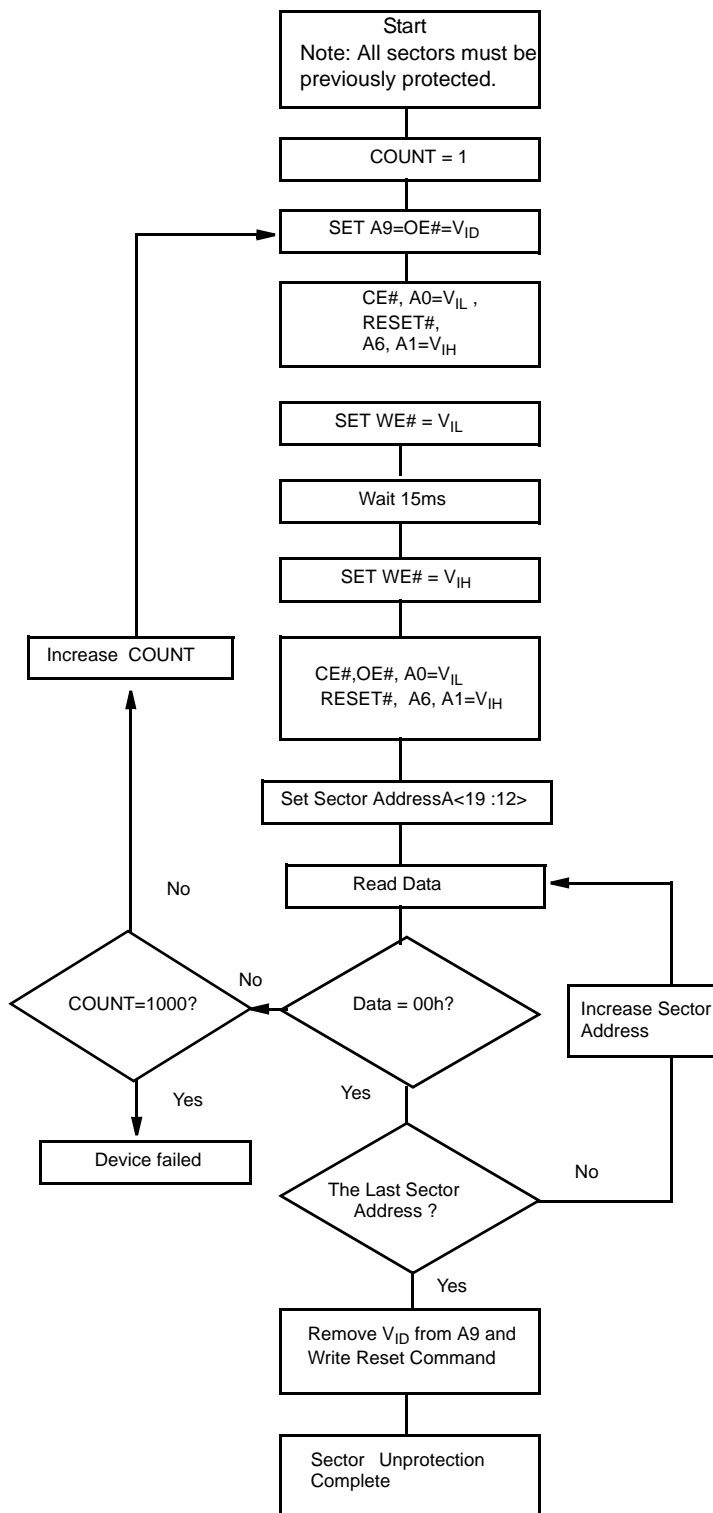


Figure 5. Sector Un-Protection Algorithm
(A9 High-Voltage Method)

Common Flash Memory Interface (CFI)

CFI is supported in the ES29LV160 device. The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the **CFI query command**, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 5-8. To terminate reading CFI data, the system must write the **reset command**. The CFI query command can be written to the system when the device is in the **autoselect mode** or the **erase-suspend-read** mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 5-8. When the reset command is written, the device returns respectively to the read mode or erase-suspend-read mode.

Table 5. CFI Query Identification String

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|-----------------------|-----------------------|-------------------------|--|
| 10h 11h 12h | 20h 22h 24h | 0051h 0052h 0059h | Query Unique ASCII string "QRY" |
| 13h 14h | 26h 28h | 0002h 0000h | Primary OEM Command Set |
| 15h 16h | 2Ah 2Ch | 0040h 0000h | Address for Primary Extended Table |
| 17h 18h | 2Eh 30h | 0000h 0000h | Alternate OEM Command Set(00h = none exists) |
| 19h 1Ah | 32h 34h | 0000h 0000h | Address for Alternate OEM Extended Table (00h = none exists) |

Table 6. System Interface String

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|-----------------------|-----------------------|-------|--|
| 1Bh | 36h | 0027h | Vcc Min. (write/erase) D7-D4: volt, D3-D0: 100 millivolt |
| 1Ch | 38h | 0036h | Vcc Max. (write/erase) D7-D4: volt, D3-D0: 100 millivolt |
| 1Dh | 3Ah | 0000h | Vpp Min. voltage (00h = no Vpp pin present) |
| 1Eh | 3Ch | 0000h | Vpp Max. voltage (00h = no Vpp pin present) |
| 1Fh | 3Eh | 0004h | Typical timeout per single byte/word write 2^N us |
| 20h | 40h | 0000h | Typical timeout for Min. size buffer write 2^N us (00h = not supported) |
| 21h | 42h | 000Ah | Typical timeout per individual block erase 2^N ms |
| 22h | 44h | 0000h | Typical timeout for full chip erase 2^N ms (00h = not supported) |
| 23h | 46h | 0005h | Max. timeout for byte/word write 2^N times typical |
| 24h | 48h | 0000h | Max. timeout for buffer write 2^N times typical |
| 25h | 4Ah | 0004h | Max. timeout per individual block erase 2^N times typical |
| 26h | 4Ch | 0000h | Max. timeout for full chip erase 2^N times typical (00h = not supported) |

Table 7. Device Geometry Definition

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|--------------------------|--------------------------|----------------|--|
| 27h | 4Eh | 0015h | Device Size = 2^N byte |
| 28h 29h | 50h 52h | 0002h 0000h | Flash Device Interface description 02 = x8, x16 Asynchronous |
| 2Ah 2Bh | 54h 56h | 0000h 0000h | Max. number of bytes multi-byte write = 2^N (00h = not supported) |
| 2Ch | 58h | 0004h | Number of Erase Block Regions within device |
| 2Dh 2Eh | 5Ah 5Ch | 0000h 0000h | Erase Block Region 1 Information Number of identical size erase block = $0000h+1 = 1$ |
| 2Fh 30h | 5Eh 60h | 0040h 0000h | Erase Block Region 1 Information Block size in Region 1 = $0040h * 256 \text{ byte} = 16 \text{ Kbyte}$ |
| 31h 32h | 62h 64h | 0001h 0000h | Erase Block Region 2 Information Number of identical size erase block = $0001h+1 = 2$ |
| 33h 34h | 66h 68h | 0020h 0000h | Erase Block Region 2 Information Block size in Region 2 = $0020h * 256 \text{ byte} = 8 \text{ Kbyte}$ |
| 35h 36h | 6Ah 6Ch | 0000h 0000h | Erase Block Region 3 Information Number of identical size erase block = $0000h+1 = 1$ |
| 37h 38h | 6Eh 70h | 0080h 0000h | Erase Block Region 3 Information Block size in Region 3 = $0080h * 256 \text{ byte} = 32 \text{ Kbyte}$ |
| 39h 3Ah | 72h 74h | 001Eh 0000h | Erase Block Region 4 Information Number of identical size erase block = $001Eh+1 = 31$ |
| 3Bh 3Ch | 76h 78h | 0000h 0001h | Erase Block Region 4 Information Block size in Region 4 = $0100h * 256 \text{ byte} = 64 \text{ Kbyte}$ |

Table 8. Primary Vendor-Specific Extended Query

| Addresses (Word Mode) | Addresses (Byte Mode) | Data | Description |
|--------------------------|--------------------------|-------------------------|---|
| 40h 41h 42h | 80h 82h 84h | 0050h 0052h 0049h | Query-unique ASCII string "PRI" |
| 43h | 86h | 0031h | Major version number, ASCII |
| 44h | 88h | 0030h | Minor version number, ASCII |
| 45h | 8Ah | 0000h | Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not required Silicon Revision Number (Bits 7-2) |
| 46h | 8Ch | 0002h | Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write |
| 47h | 8Eh | 0001h | Sector Protect 0 = Not Supported, X = Number of sectors in per group |
| 48h | 90h | 0001h | Sector Temporary Unprotect 00 = Not Supported, 01 = Supported |
| 49h | 92h | 0004h | Sector Protect/Unprotect scheme 04 = In-System Method and A9 High-Voltage Method |
| 4Ah | 94h | 0000h | Simultaneous Operation 00 = Not Supported |
| 4Bh | 96h | 0000h | Burst Mode Type 00 = Not Supported, 01 = Supported |
| 4Ch | 98h | 0000h | Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page |

COMMAND DEFINITIONS

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Writing specific address and data commands or sequences into the command register initiates device operations. Table 9 defines the valid register command sequences. Note that writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. A reset command is required to return the device to normal operation.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

READING ARRAY DATA

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erased Resume Commands section for more information.

The system must issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in

the Device Bus Operations section for more information. The Read-Only Operations table provides the read parameters, and Fig. 16 shows the timing diagram

RESET COMMAND

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to which the system was writing to the read mode. If the program command sequence is written to a sector that is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase-Suspend).

Command Definitions

Table 9. ES29LV160 Command Definitions

| Command Sequence (Note 1) | | Cycles | Bus Cycles (Notes 2-5) | | | | | | | | | | | | | |
|---------------------------------|--------------------------------|--------|------------------------|------|--------|------|-------|------|---------|-------|-------|------|-------|------|--|--|
| | | | First | | Second | | Third | | Fourth | | Fifth | | Sixth | | | |
| | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | | |
| Read (Note 6) | | 1 | RA | RD | | | | | | | | | | | | |
| Reset (Note 7) | | 1 | XXX | F0 | | | | | | | | | | | | |
| Autoselect (Note 8) | Manufacturer ID | Word | 555 | AA | 2AA | 55 | 555 | 90 | X00 | 4A | | | | | | |
| | | Byte | AAA | | 555 | | AAA | | | | | | | | | |
| | Device ID (Top) | Word | 555 | AA | 2AA | 55 | 555 | 90 | X01 | C4 | | | | | | |
| | | Byte | AAA | | 555 | | AAA | | X02 | | | | | | | |
| | Device ID (Bottom) | Word | 555 | AA | 2AA | 55 | 555 | 90 | X01 | 49 | | | | | | |
| | | Byte | AAA | | 555 | | AAA | | X02 | | | | | | | |
| | Sector Protect Verify (Note 9) | Word | 555 | AA | 2AA | 55 | 555 | 90 | (SA)X02 | 00/01 | | | | | | |
| | | Byte | AAA | | 555 | | AAA | | (SA)X04 | | | | | | | |
| Program | Word | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | | | | |
| | Byte | AAA | | 555 | | AAA | | | | | | | | | | |
| Unlock Bypass | Word | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | | | | |
| | Byte | AAA | | 555 | | AAA | | | | | | | | | | |
| Unlock Bypass Program (Note 10) | | 2 | XXX | A0 | PA | PD | | | | | | | | | | |
| Unlock Bypass Reset (Note 11) | | 2 | XXX | 90 | XXX | 00 | | | | | | | | | | |
| Chip Erase | Word | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 | | | |
| | Byte | AAA | | 555 | | AAA | | AAA | | 555 | | AAA | | | | |
| Sector Erase | Word | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | SA | 30 | | | |
| | Byte | AAA | | 555 | | AAA | | AAA | | 555 | | | | | | |
| Erase Suspend (Note 12) | | 1 | XXX | B0 | | | | | | | | | | | | |
| Erase Resume (Note 13) | | 1 | XXX | 30 | | | | | | | | | | | | |
| CFI Query (Note 14) | Word | 55 | | | | | | | | | | | | | | |
| | Byte | AA | 98 | | | | | | | | | | | | | |

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation

PA = Address of the memory location to be programmed.

Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A19-A12 uniquely select any sector.

Notes:

- See Table 1 for description of bus operations.
- All values are in hexadecimal.
- Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.
- Data bits DQ15-DQ8 are don't care in command sequences, except for RD and PD
- Unless otherwise noted, address bits A19-A11 are don't cares.
- No unlock or command cycles required when device is in read mode.
- The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when a device is in the autoselect mode, or if DQ5 goes high (while the device is providing status information).
- The fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15-DQ8 are don't care. See the Autoselect Command Sequence section for more information.
- The data is 00h for an unprotected sector and 01h for a protected sector.
- The Unlock Bypass command is required prior to the Unlock Bypass Program command.
- The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.
- The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
- The Erase Resume command is valid only during the Erase Suspend mode.
- Command is valid when device is ready to read array data or when device is in autoselect mode.

AUTOSELECT COMMAND

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected, including information about factory-locked or customer lockable version.

| Identifier Code | Address | Data |
|-----------------------|---------|-------------------|
| Manufacturer ID | 00h | 4Ah |
| Device ID | 01h | C4h(T), 49h(B) |
| Sector Protect Verify | (SA)02h | 00 / 01 |

Table 9 shows the address and data requirements. This method is an alternative to "A9 high-voltage method" shown in Table 2, which is intended for PROM programmers and requires V_{ID} on address pin A9. The autoselect command sequence may be written to an address within sector that is either in the read mode or erase-suspend-read mode. The auto-select command may not be written while the device is actively programming or erasing. The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence.

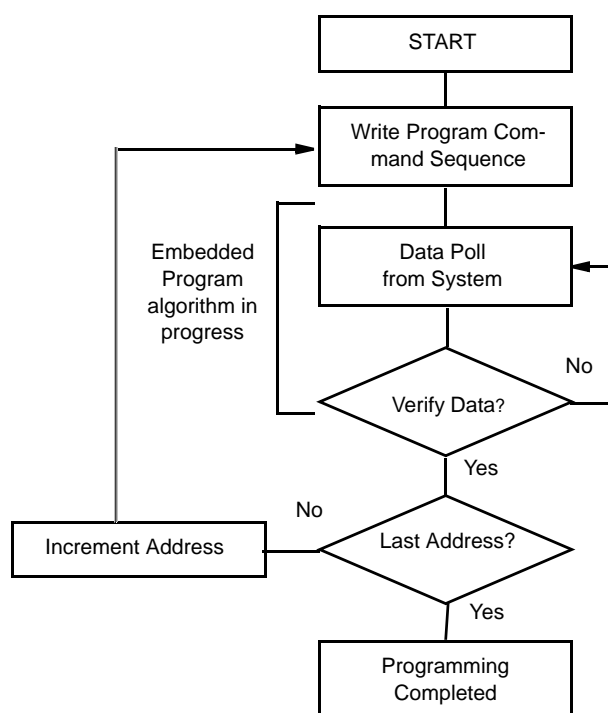
Once after the device enters the auto-select mode, the manufacture ID code (4Ah) can be accessed by one of two ways. Just one read cycle (with A6, A1 and A0 = 0) can be used. Or four consecutive read cycles (with A6 = 1 and A1, A0 = 0) for continuation codes (7Fh) and then another last cycle for the code (4Ah) (with A6, A1 and A0 = 0) can be used for reading the manufacturer code.

- 4Ah (one-cycle read)
- 7Fh 7Fh 7Fh 7Fh 4Ah (Five-cycle read)

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

BYTE / WORD PROGRAM

The system may program the device by word or byte, depending on the state of the **BYTE# pin**. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 9 shows the address and data requirements for the byte program command sequence. Note that the autoselect and CFI modes are unavailable while a programming operation is in progress.



Note: See Table 9 for program command sequence

Figure 6. Program Operation

Program Status Bits : DQ7, DQ6 or RY/BY#

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Write Operation Status section Table 10 for information on these status bits.

Any Commands Ignored during Programming Operation

Any commands written to the device during the Embedded Program algorithm are ignored. Note that a hardware reset can immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming from “0” back to “1”

Programming is allowed in any sequence and across sector boundaries. But a bit cannot be programmed from “0” back to a “1”. Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still “0”. Only erase operations can convert a “0” to a “1”

Unlock Bypass

In the ES29LV160 device, an unlock bypass program mode is provided for faster programming operation. In this mode, two cycles of program command sequences can be saved. To enter this mode, an unlock bypass enter command should be first written to the system. The unlock bypass enter command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock-bypass program mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program set-up command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 9 shows the requirements for the command sequence.

During the unlock-bypass mode, only the unlock-bypass program and unlock-bypass reset commands are valid. To exit the unlock-bypass mode, the system must issue the two-cycle unlock-bypass reset command sequence. The first cycle must contain the data 90h. The second cycle need to only contain the data 00h. The device then returns to the read mode.

- Unlock Bypass Enter Command
- Unlock Bypass Reset Command
- Unlock Bypass Program Command

CHIP ERASE COMMAND

To erase the entire memory, a chip erase command is used. This command is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The chip erase command erases the entire memory including all other sectors except the protected sectors, but the internal erase operation is performed on a single sector base.

Embedded Erase Algorithm

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 9 shows the address and data requirements for the chip erase command sequence. Note that the autoselect, and CFI modes are unavailable while an erase operation is in progress

Erase Status Bits : DQ7, DQ6, DQ2, or RY/BY#

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Write Operation Status section Table 10 for information on these status bits.

Commands Ignored during Erase Operation

Any command written during the chip erase operation are ignored. However, note that a hardware

reset immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity. Fig. 7 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Fig. 21 section for timing diagrams.

SECTOR ERASE COMMAND

By using a sector erase command, a single sector or multiple sectors can be erased. The sector erase command is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 9 shows the address and data requirements for the sector erase command sequence. Note that the autoselect, and CFI modes are unavailable while an erase operation is in progress.

Embedded Sector Erase Algorithm

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings these operations.

Sector Erase Time-out Window and DQ3

After the command sequence is written, a sector erase time-out of **50us** occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 us, otherwise the last address and command may not be accepted, and erasure may begin. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. The system can monitor **DQ3** to determine if the sector erase timer has timed out (See the section on DQ3:Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

Any command other than Sector Erase or Erase Suspend during the time-out period resets the device

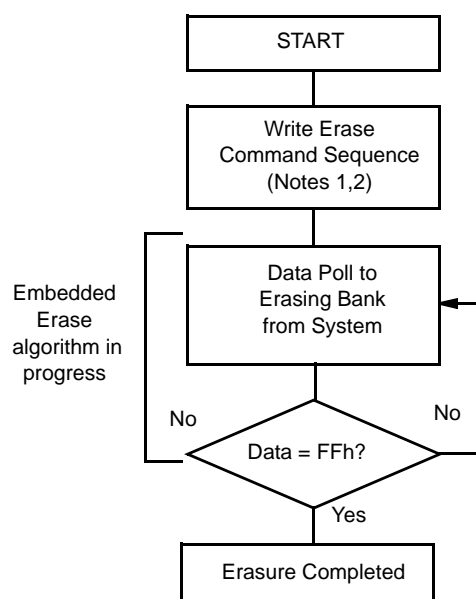
to the read mode. The system must rewrite the command sequence and any additional addresses and commands.

Status Bits : DQ7,DQ6,DQ2, or RY/BY#

When the Sector Erase Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing sector. The system can determine the status of the erase operation by reading DQ7,DQ6,DQ2, or RY/BY# in the erasing sector. Refer to the Write Operation Status section Table 10 for information on these status bits.

Valid Command during Sector Erase

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command



Notes:

1. See Table 9 for erase command sequence
2. See the section on DQ3 for information on the sector erase timer

Figure 7. Erase Operation

sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Fig. 7 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Fig. 21 section for timing diagrams.

ERASE SUSPEND/ERASE RESUME

An erase operation is a long-time operation so that two useful commands are provided in the ES29LV160 device Erase Suspend and Erase Resume Commands. Through the two commands, erase operation can be suspended for a while and the suspended operation can be resumed later when it is required. While the erase is suspended, read or program operations can be performed by the system.

Erase Suspend Command, (B0h)

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the **50us time-out** period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of **20us** to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

Read and Program during Erase-Suspend-Read Mode

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.)

Reading at any address within erase-suspended sectors produces status information on DQ7-DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits (Table 10).

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status for the program operation using the DQ7 or DQ6 status bits, just as in the standard Byte Program operation. Refer to the Write Operation Status section for more information.

Autoselect during Erase-Suspend- Read Mode

In the erase-suspend-read mode, the system can also issue the autoselected command sequence. Refer to the Autoselect Mode and Autoselect Command Sequence section for details (Table 9).

Erase Resume Command

To resume the sector erase operation, the system must write the Erase Resume command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

COMMAND DIAGRAM

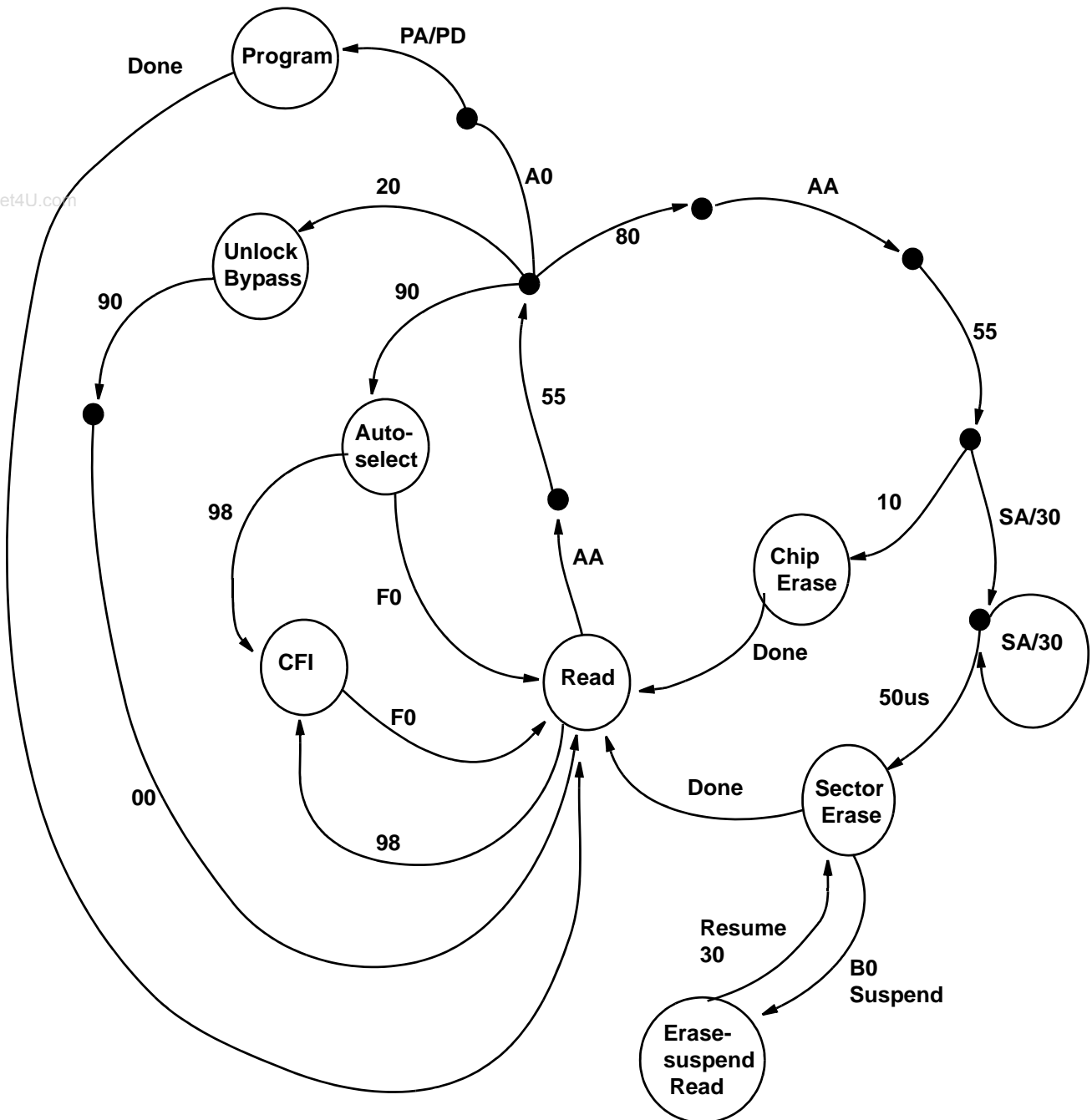


Figure 8. Command Diagram

WRITE OPERATION STATUS

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In the ES29LV160 device, several bits are provided to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, DQ7 and RY/BY#. Table 10 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7 (DATA# POLLING)

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During Programming

During the Embedded Program algorithm, the device outputs on DQ7 the **complement** of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a **protected sector**, Data# Polling on DQ7 is active for approximately **250ns**, then the device returns to the read mode.

During Erase

During the Embedded Erase algorithm, Data# Polling produces a **"0" on DQ7**. When the Embedded

Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# polling produces a **"1"** on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

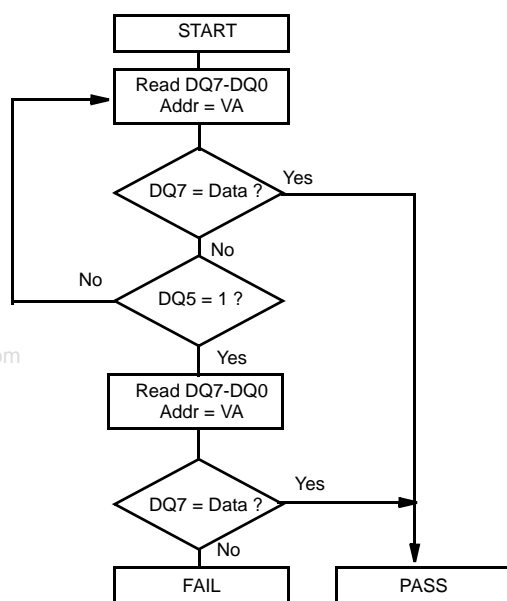
Erase on the Protected Sectors

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately **1.8us**, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Data# Polling Algorithm

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0-DQ6 while Output Enable(OE#) is asserted low. That is, this device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0-DQ7 will appear on successive read cycles.

Table 10 shows the outputs for Data# Polling on DQ7. Fig. 9 shows the Data# Polling algorithm. Fig. 22 in the AC Characteristics section shows the Data# Polling timing diagram.


Notes:

1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address in any non-protected sector address.
2. DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5

Figure 9. Data# Polling Algorithm
RY/BY# (READY/BUSY#)

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to Vcc. If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. Table 10 shows the outputs for RY/BY#.

DQ6 (TOGGLE BIT I)

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the

Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out. During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7(see the subsection on DQ7:Data# Polling). DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 10 shows the outputs for Toggle Bit I on DQ6. Fig. 10 shows the toggle bit algorithm. Fig. 23 in the "AC Characteristics" section shows the toggle bit timing diagrams. Fig. 24 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2 : (Toggle Bit II).

Toggling on the Protected Sectors

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately **1.8us**, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. If a program address falls within a protected sector, DQ6 toggles for approximately **250ns** after the program command sequence is written, then returns to reading array data.

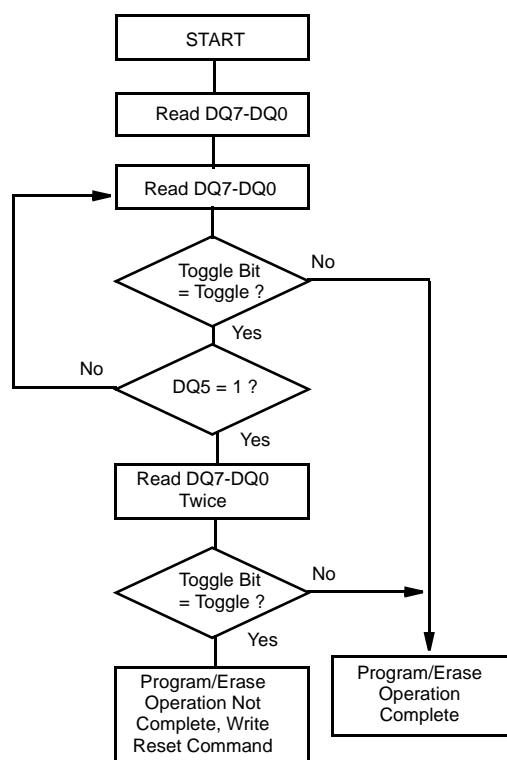
DQ2 (TOGGLE BIT II)

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence DQ2

toggles when the system reads at addresses within those sectors that have been **selected for erasure**. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 10 to compare outputs for DQ2 and DQ6. Fig. 10 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the DQ6: Toggle Bit I subsection. Fig. 23 shows the toggle bit timing diagram. Fig. 24 shows how differently DQ2 operates compared with DQ6.

Reading Toggle Bits DQ6/DQ2

Refer to Fig. 10 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7-DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7-DQ0 on the following read cycle. However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data. The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, this system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Fig. 10).



Note:

The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1". See the subsections on DQ6 and DQ2 for more information.

Figure 10. Toggle Bit Algorithm

DQ5 (EXCEEDED TIMING LIMITS)

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1", indicating that the program or erase cycle was not successfully completed. The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0". Only an erase operation can change a "0" back to a "1". Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1". Under both these conditions, the system must write the reset command to return to the read mode.

DQ3 (SECTOR ERASE TIMER)

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase time does not apply to the chip erase command.)

If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1". If the time between additional sector erase commands from the system can be assumed to be less than **50us**, the system need not monitor DQ3. See also the Sector Erase Command Sequence section. After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1", the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erasure operation is complete. If DQ3 is "0", the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. In Table 10, DQ3 status operation is well defined and summarized with other status bits, DQ7, DQ6, DQ5, and DQ2.

Table 10. Write Operation Status

| Status | | DQ7 (Note 2) | DQ6 | DQ5 (Note 1) | DQ3 | DQ2 (Note 2) | RY/ BY# | |
|--------------------|----------------------------|----------------------------|--------|-----------------|------|-----------------|------------|---|
| Standard Mode | Embedded Program Algorithm | DQ7# | Toggle | 0 | N/A | No toggle | 0 | |
| | Embedded Erase Algorithm | 0 | Toggle | 0 | 1 | Toggle | 0 | |
| Erase Suspend Mode | Erase-Suspend-Read | Erase Suspended Sector | 1 | No toggle | 0 | N/A | Toggle | 1 |
| | | Non-Erase Suspended Sector | Data | Data | Data | Data | Data | 1 |
| | Erase-Suspend-Program | DQ7# | Toggle | 0 | N/A | N/A | 0 | |

Notes :

1. DQ5 switches to "1" when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.

ABSOLUTE MAXIMUM RATINGS

| | |
|--------------------------|-----------------|
| Storage Temperature | |
| Plastic Packages | -65°C to +150°C |
| Ambient Temperature | |
| with Power Applied | -65°C to +125°C |

Voltage with Respect to Ground

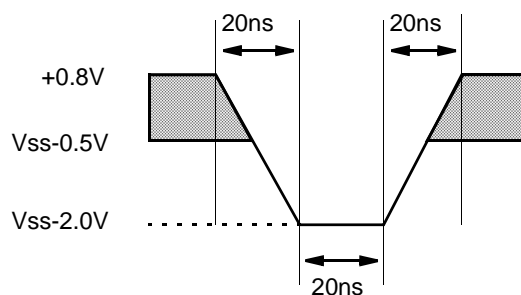
| | |
|-----------------------------------|---------------------------------|
| V _{CC} (Note 1) | -0.5V to +4.0V |
| A9, OE# and RESET# (Note 2) | -0.5V to +12.5V |
| All other pins (Note 1) | -0.5V to V _{CC} + 0.5V |

Output Short Circuit Current (Note 3) 200 mA

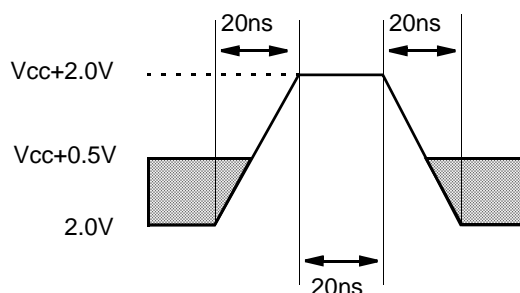
Notes:

1. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may overshoot V_{SS} to -2.0V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is V_{CC}+0.5V. See Fig. 11. During voltage transition, input or I/O pins may overshoot to V_{CC}+2.0V for periods up to 20ns. See Fig. 11.
2. Minimum DC input voltage on pins A9, OE# and RESET# is -0.5V . During voltage transitions, A9, OE# and RESET# may overshoot V_{SS} to -2.0V for periods of up to 20ns. See Fig. 11. Maximum DC input voltage on pin A9 is +12.5V which may overshoot to +14.0V for periods up to 20ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.



Negative Overshoot



Positive Overshoot

Figure 11. Maximum Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A).....-40°C to +85°C

Commercial Devices

Ambient Temperature (T_A).....0°C to +70°C

V_{CC} Supply Voltages

V_{CC} for all devices2.7V to 3.6V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

Table 11. CMOS Compatible

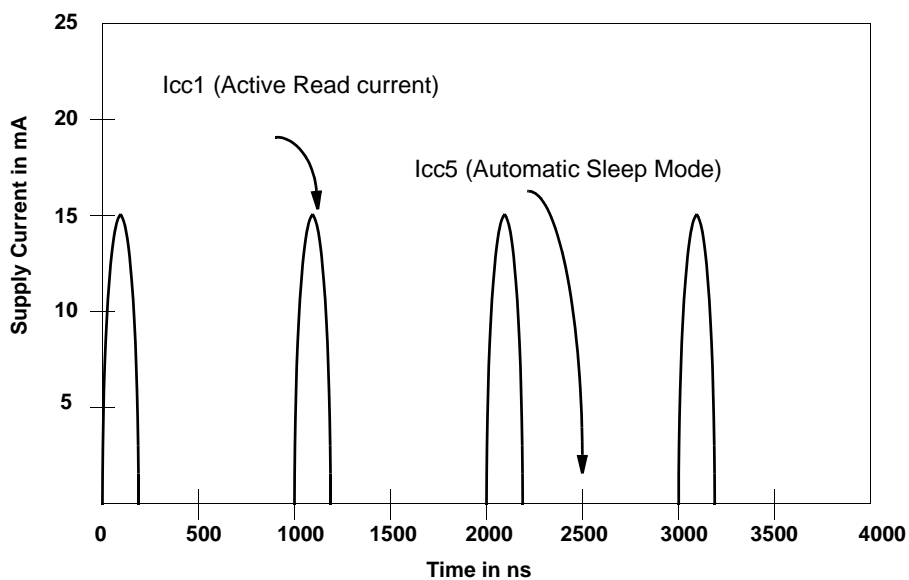
| Parameter Symbol | Parameter Description | Test Conditions | Min | Typ | Max | Unit |
|------------------|--|---|---------------------|-----|----------------|---------|
| I_{LI} | Input Load Current | $V_{IN}=V_{SS}$ to V_{CC} $V_{CC}=V_{CC}$ max | | | ± 1.0 | μA |
| I_{LIT} | A9 Input Load Current | $V_{CC}=V_{CC}$ max; A9=12.5V | | | 35 | μA |
| I_{LR} | RESET# Input Load Current | $V_{CC}=V_{CC}$ max; RESET#=12.5V | | | 35 | μA |
| I_{LO} | Output Leakage Current | $V_{out}=V_{SS}$ to V_{CC} , $V_{CC}=V_{CC}$ max | | | ± 1.0 | μA |
| I_{CC1} | Vcc Active Read Current (Notes 1,2) | CE#=V _{IL} , OE#=V _{IH} , Byte mode | 5MHz | 9 | 16 | mA |
| | | | 1MHz | 2 | 4 | |
| | | CE#=V _{IL} , OE#=V _{IH} , Word mode | 5MHz | 9 | 16 | |
| | | | 1MHz | 2 | 4 | |
| I_{CC2} | Vcc Active Write Current (Note 2,3) | CE#=V _{IL} , OE#=V _{IH} , WE#=V _{IL} | | 15 | 30 | mA |
| I_{CC3} | Vcc Standby Current (Note 2) | CE#, RESET#= $V_{CC}\pm 0.3V$ | | 0.2 | 10 | μA |
| I_{CC4} | Vcc Reset Current (Note 2) | RESET#=V _{SS} $\pm 0.3V$ | | 0.2 | 10 | μA |
| I_{CC5} | Automatic Sleep Mode (Notes 2,4) | $V_{IH} = V_{CC} \pm 0.3V$ $V_{IL} = V_{SS} \pm 0.3V$ | | 0.2 | 10 | μA |
| V_{IL} | Input Low Voltage | | -0.5 | | 0.8 | V |
| V_{IH} | Input High Voltage | | $0.7 \times V_{CC}$ | | $V_{CC} + 0.3$ | V |
| V_{ID} | Voltage for Autoselect and Temporary Sector Unprotect | $V_{CC} = 3.0V \pm 10\%$ | 11.5 | | 12.5 | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 4.0$ mA, $V_{CC} = V_{CC}$ min | | | 0.45 | V |
| V_{OH1} | Output High Voltage | $I_{OH} = -2.0$ mA, $V_{CC} = V_{CC}$ min | $0.85 V_{CC}$ | | | V |
| V_{OH2} | | $I_{OH} = -100$ μA , $V_{CC} = V_{CC}$ min | $V_{CC} - 0.4$ | | | |
| V_{LKO} | Low Vcc Lock-Out Voltage (Note 5) | | 2.3 | | 2.5 | V |

Notes:

1. The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH} , **Typical condition : 25°C, Vcc = 3V**
2. Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$ max.
3. I_{CC} active while Embedded Erase or Embedded Program is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for $t_{ACC} + 30ns$. Typical sleep mode current is 200 nA.
5. Not 100% tested.

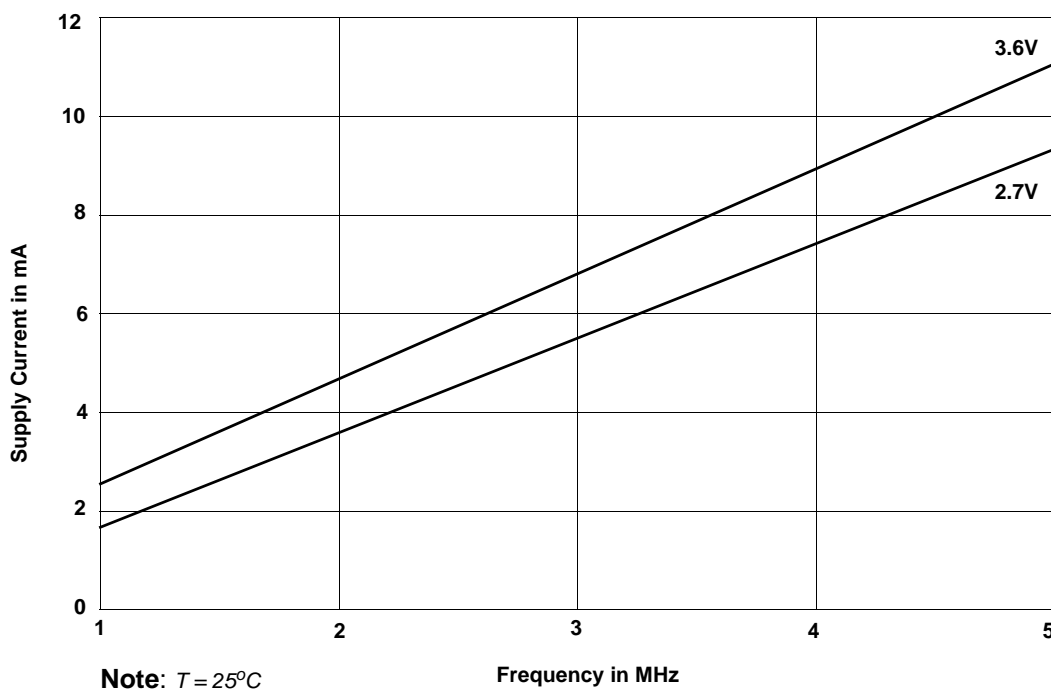
DC CHARACTERISTICS

Zero-Power Flash



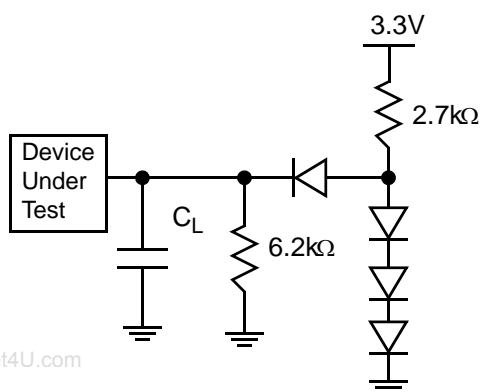
Note: Addresses are switching at 1 MHz

Figure 12. I_{cc1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: $T = 25^{\circ}C$

Figure 13. Typical I_{cc1} vs. Frequency


Figure 14. Test Setup

Note: Diodes are IN3064 or equivalent

Table 12. Test Specifications

| Test Condition | 70 | 90 |
|--|-------------|-------|
| Output Load | 1TTL gate | |
| Output Load Capacitance, C_L (including jig capacitance) | 30 pF | 30 pF |
| Input Rise and Fall Times | 5 ns | |
| Input Pulse Levels | 0.0 - 3.0 V | |
| Input timing measurement reference levels | 1.5 V | |
| Output timing measurement reference levels | 1.5 V | |

Key To Switching Waveforms

| WAVEFORM | INPUTS | OUTPUTS |
|----------|----------------------------------|--|
| | | Steady |
| | | Changing from H to L |
| | | Changing from L to H |
| | Don't Care, Any Change Permitted | Changing, State Unknown |
| | Does Not Apply | Center Line is High Impedance State (High Z) |


Figure 15. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Table 13. Read-Only Operations

| Parameter | | Description | Test Setup | | Speed Options | | Unit |
|------------|-----------|---|--------------------------|-----|---------------|----|------|
| JEDEC | Std. | | | | 70 | 90 | |
| t_{AVAV} | t_{RC} | Read Cycle Time(Note 1) | | Min | 70 | 90 | ns |
| t_{AVQV} | t_{ACC} | Address to Output Delay | CE#,OE#=V _{IL} | Max | 70 | 90 | ns |
| t_{ELQV} | t_{CE} | Chip Enable to Output Delay | OE#=V _{IL} | Max | 70 | 90 | ns |
| t_{GLQV} | t_{OE} | Output Enable to Output Delay | | Max | 35 | 40 | ns |
| t_{EHQZ} | t_{DF} | Chip Enable to Output High Z (Note 1) | | Max | 16 | | ns |
| t_{GHQZ} | t_{DF} | Output Enable to Output High Z (Note 1) | | Max | 16 | | ns |
| t_{AXQX} | t_{OH} | Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First | | Min | 0 | | ns |
| | t_{OEH} | Output Enable Hold Time (Note 1) | Read | Min | 0 | | ns |
| | | | Toggle and Data# Polling | Min | 10 | | ns |

Note 1. Not 100% tested

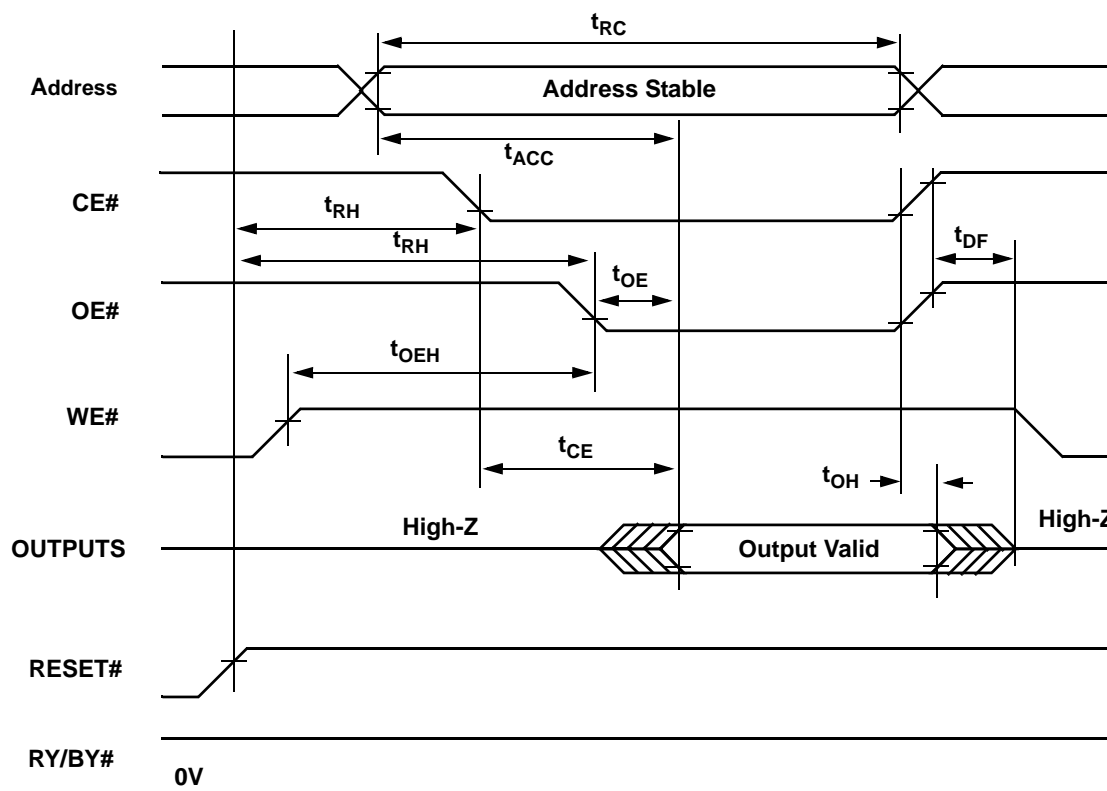


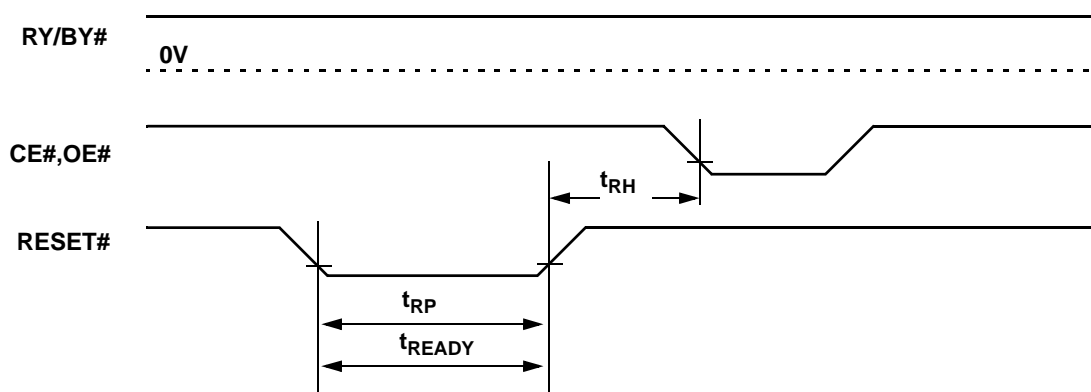
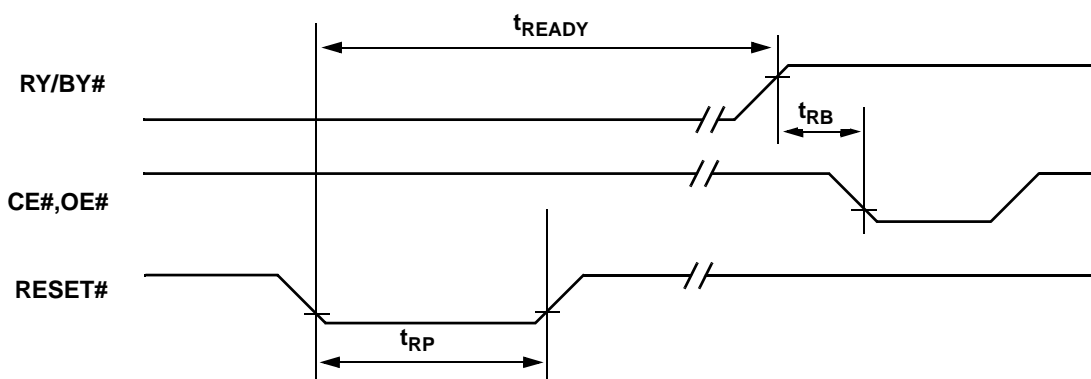
Figure 16. Read Operation Timings

AC CHARACTERISTICS

Table 14. Hardware Reset (RESET #)

| Parameter | | Description | | All Speed Options | Unit |
|-----------|-------------|---|-----|-------------------|------|
| JEDEC | Std. | | | | |
| | t_{Ready} | RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note) | Max | 20 | us |
| | t_{Ready} | RESET# Pin Low (Not During Embedded Algorithms) to Read Mode (See Note) | Max | 500 | ns |
| | t_{RP} | RESET# Pulse Width | Min | 500 | ns |
| | t_{RH} | RESET High Time Before Read (See Note) | Min | 50 | ns |
| | t_{RPD} | RESET# Low to Standby Mode | Min | 20 | us |
| | t_{RB} | RY/BY# Recovery Time | Min | 0 | ns |

Note : Not 100% tested

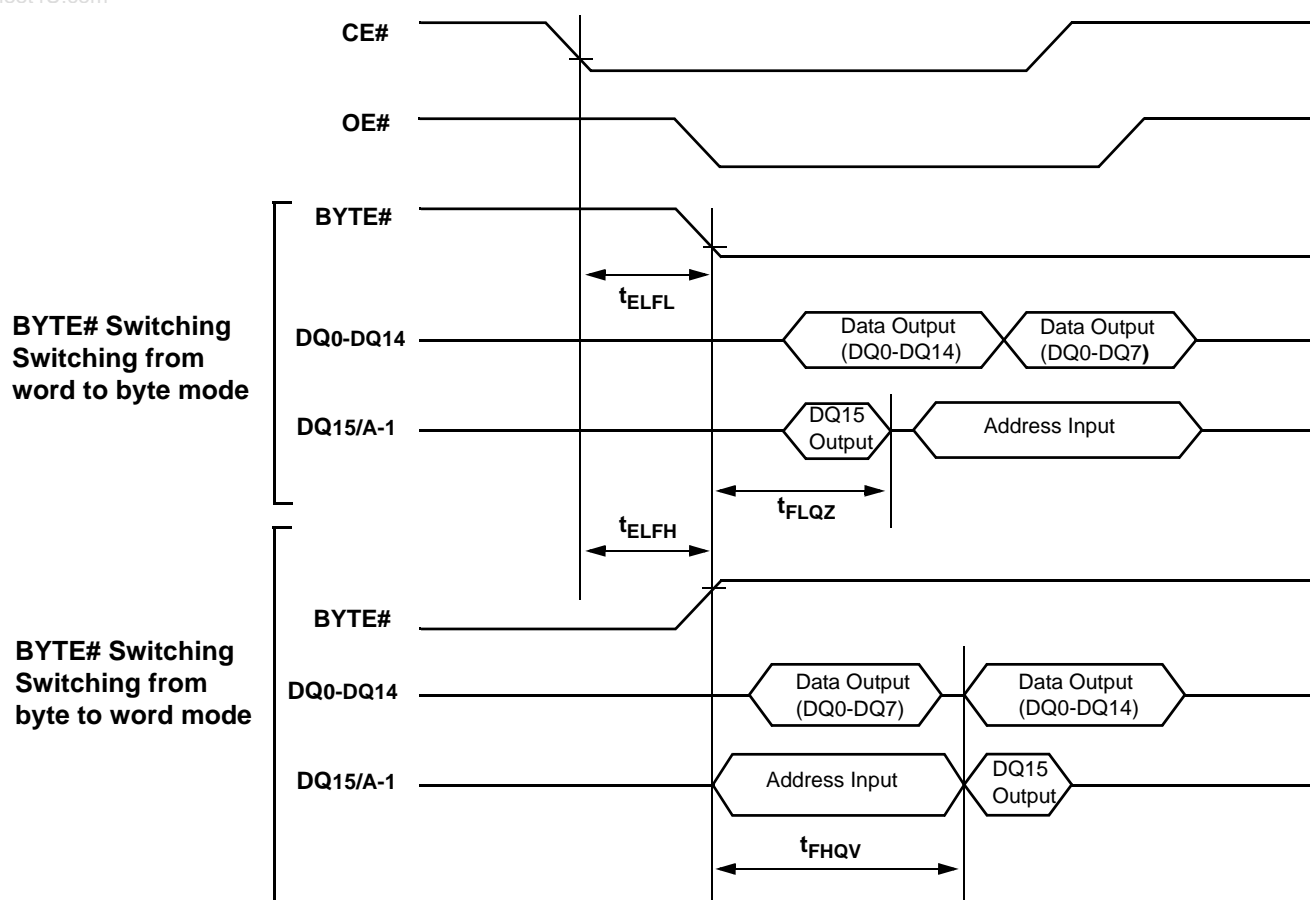
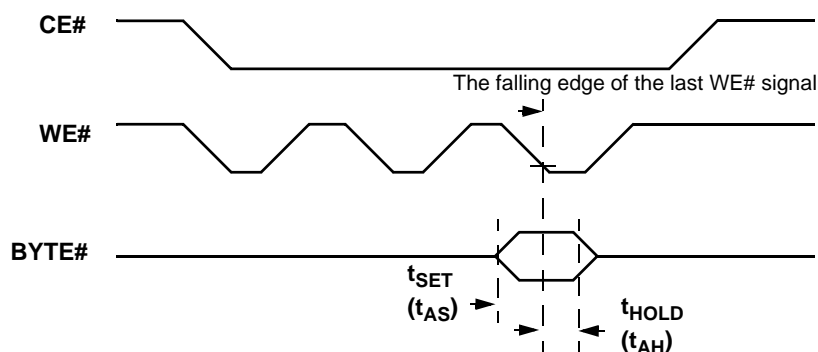

(A) Not During Embedded Algorithm

(B) During Embedded Algorithm
Figure 17. Reset Timings

AC CHARACTERISTICS

Table 15. Word/Byte Configuration (BYTE#)

| Parameter | | Description | | 70 | 90 | Unit |
|-----------|---------------------|---------------------------------------|-----|----|----|------|
| JEDEC | Std. | | | | | |
| | t_{ELFL}/t_{ELFH} | CE# to BYTE# Switching Low or High | Max | | 5 | ns |
| | t_{FLQZ} | BYTE# Switching Low to Output HIGH Z | Max | | 30 | ns |
| | t_{FHQV} | BYTE# Switching High to Output Active | Min | 70 | 90 | ns |

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Figure 18. BYTE# Timing for Read Operations


Note : Refer to the Erase/Program Operations table for t_{AS} and t_{AH} specifications.

Figure 19. BYTE# Timing for Write Operations

AC CHARACTERISTICS

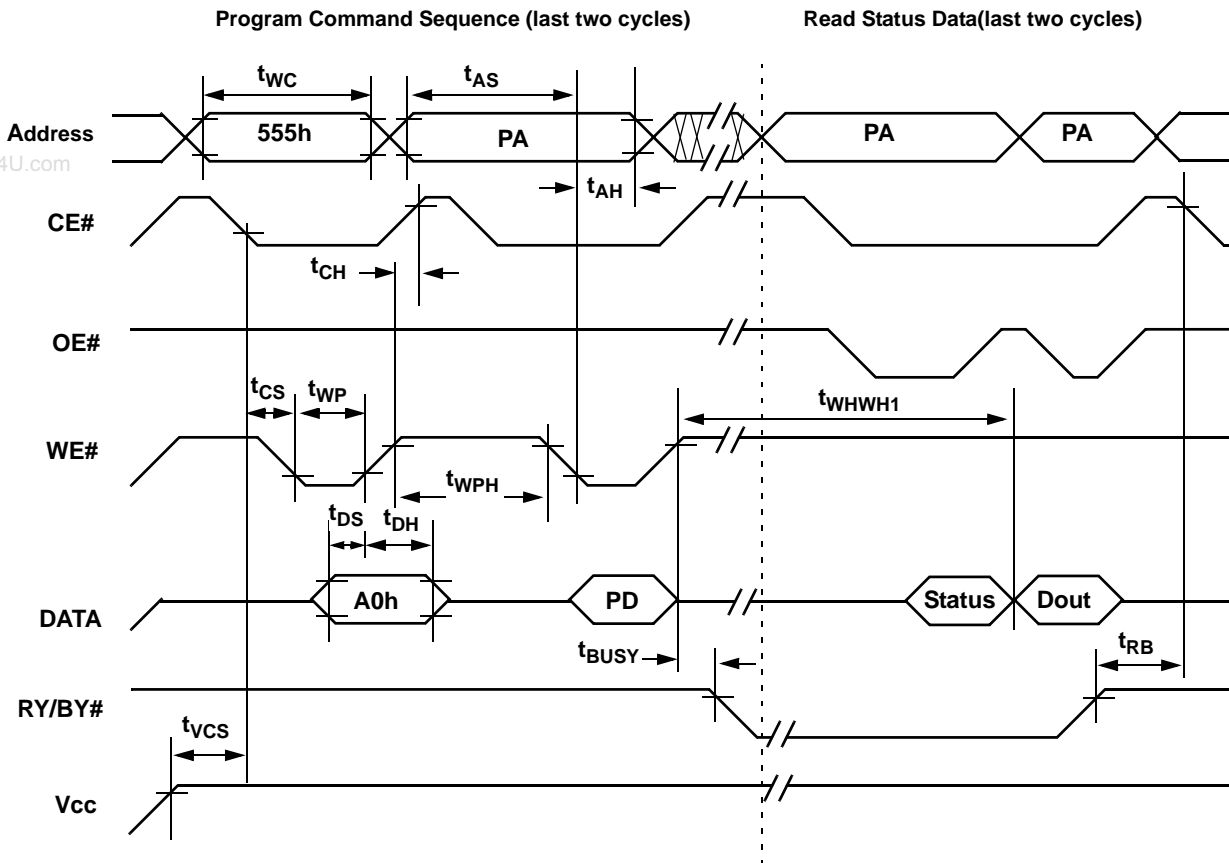
Table 16. Erase and Program Operations

| Parameter | | Description | | 70 | 90 | Unit |
|-------------|-------------|--|------|-----|----|------|
| JEDEC | Std. | | | 70 | 90 | |
| t_{AVAV} | t_{WC} | Write Cycle Time (Note 1) | Min | 70 | 90 | ns |
| t_{AVWL} | t_{AS} | Address Setup Time | Min | 0 | | ns |
| | t_{ASO} | Address Setup Time to OE# low during toggle bit polling | Min | 15 | | ns |
| t_{WLAX} | t_{AH} | Address Hold Time | Min | 45 | 45 | ns |
| | t_{AHT} | Address Hold Time From CE# or OE# high during toggle bit polling | Min | 0 | | ns |
| t_{DVWH} | t_{DS} | Data Setup Time | Min | 35 | 45 | ns |
| t_{WHDX} | t_{DH} | Data Hold Time | Min | 0 | | ns |
| | t_{OEPH} | Output Enable High during toggle bit polling | Min | 20 | | ns |
| t_{GHWL} | t_{GHWL} | Read Recovery Time Before Write (OE# High to WE# Low) | Min | 0 | | ns |
| t_{ELWL} | t_{CS} | CE# Setup Time | Min | 0 | | ns |
| t_{WHEH} | t_{CH} | CE# Hold Time | Min | 0 | | ns |
| t_{WLWH} | t_{WP} | Write Pulse Width | Min | 35 | 35 | ns |
| t_{WHDL} | t_{WPH} | Write Pulse Width High | Min | 30 | | ns |
| | $t_{SR/W}$ | Latency Between Read and Write Operations | Min | 0 | | ns |
| t_{WHWH1} | t_{WHWH1} | Programming Operation (Note 2) | Byte | Typ | 6 | us |
| | | | Word | Typ | 8 | |
| t_{WHWH2} | t_{WHWH2} | Sector Erase Operation (Note 2) | Typ | 0.7 | | sec |
| | t_{VCS} | Vcc Setup Time (Note 1) | Min | 50 | | us |
| | t_{RB} | Write Recovery Time from RY/BY# | Min | 0 | | ns |
| | t_{BUSY} | Program/Erase Valid to RY/BY# Delay | Max | 90 | | ns |

Notes:

1. Not 100% tested.
2. See the "Erase And Programming Performance" section for more information.

AC CHARACTERISTICS

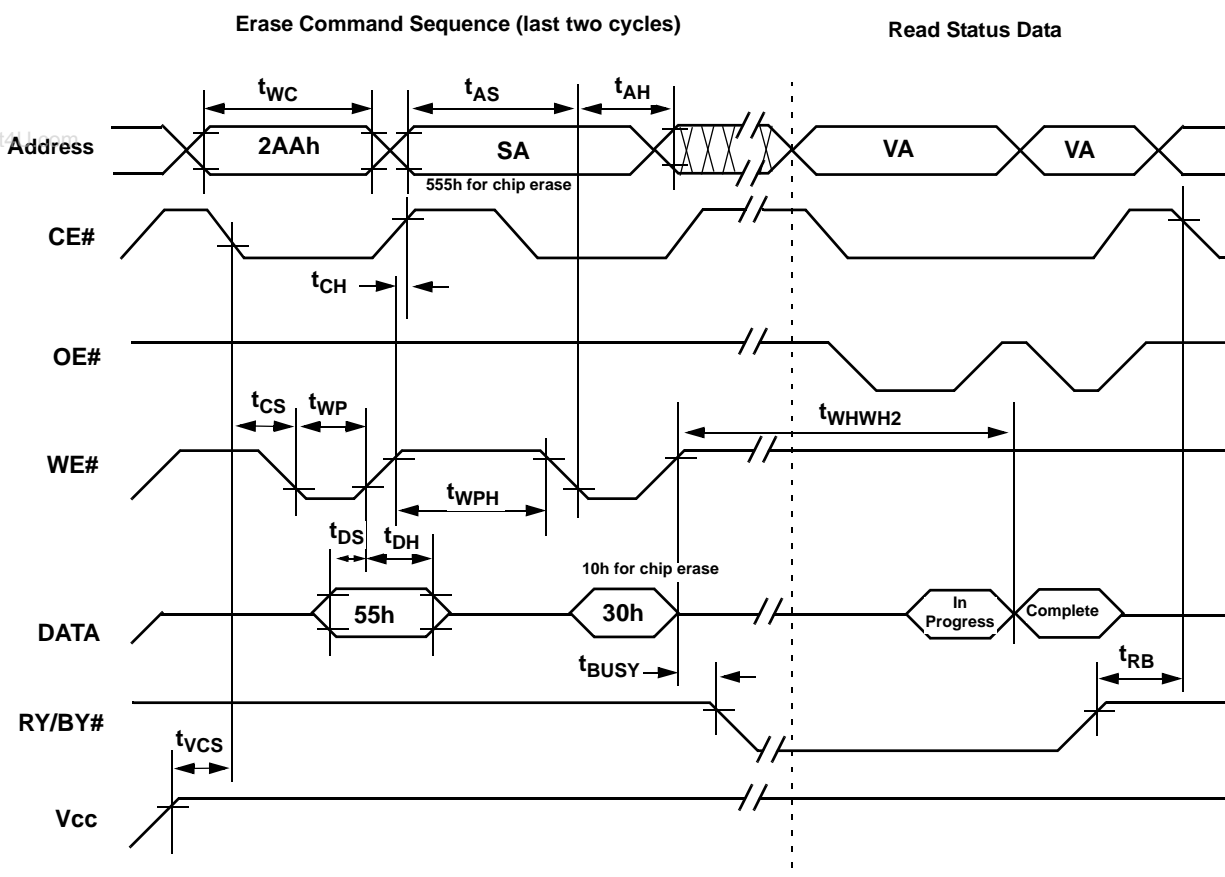


NOTES :

1. PA = program address, PD = program data, Dout is the true data at the program address.
2. Illustration shows device in word mode.

Figure 20. Program Operation Timings

AC CHARACTERISTICS

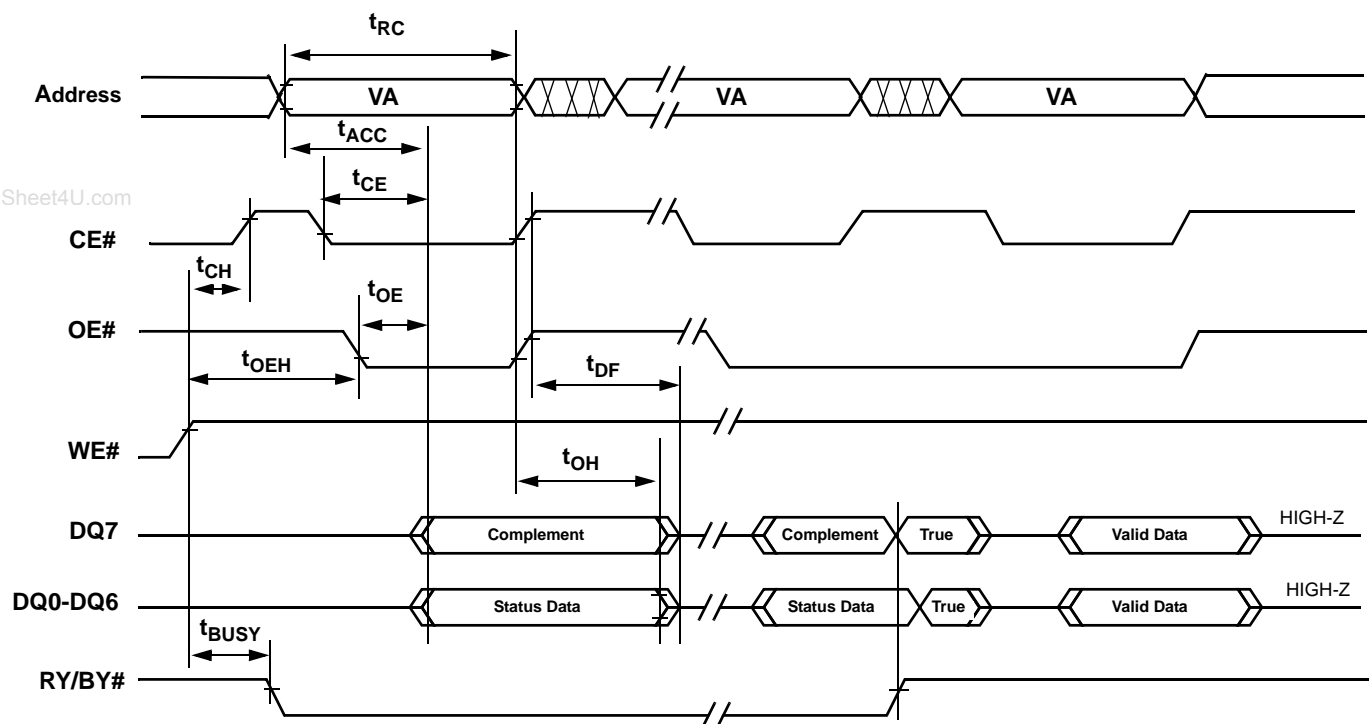


NOTES :

1. SA = sector address (for Sector Erase), VA = valid address for reading status data (see "Write Operation Status").
2. These waveforms are for the word mode.

Figure 21. Chip/Sector Erase Operation Timings

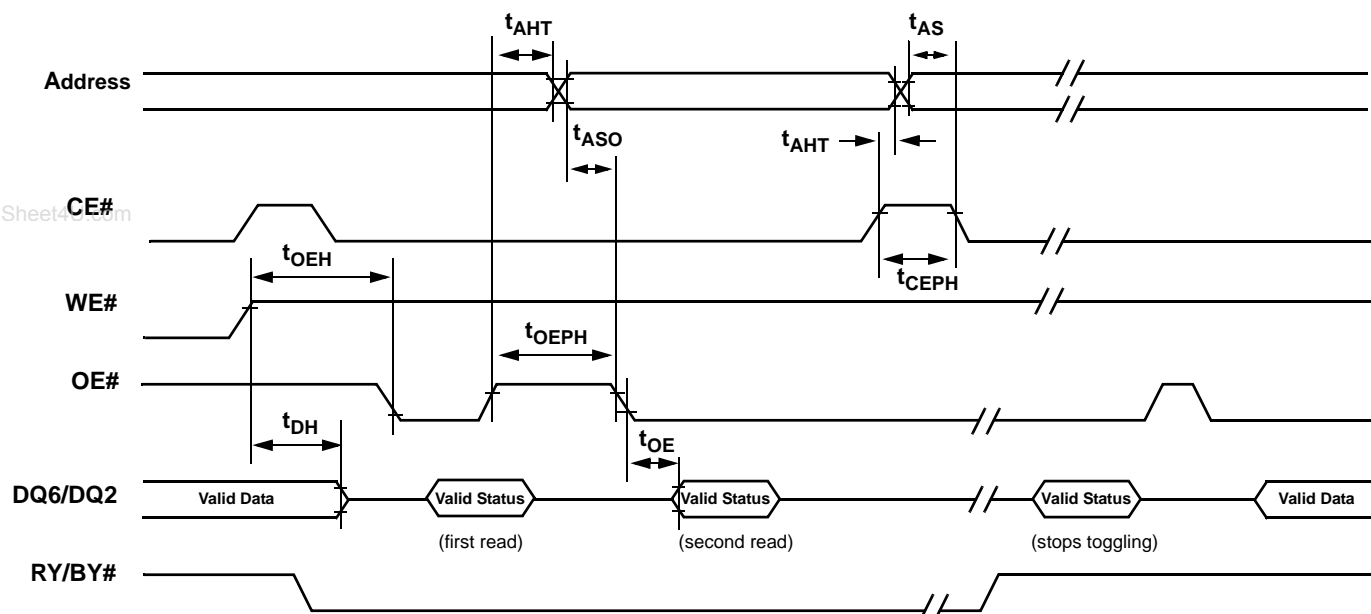
AC CHARACTERISTICS



NOTE : VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle

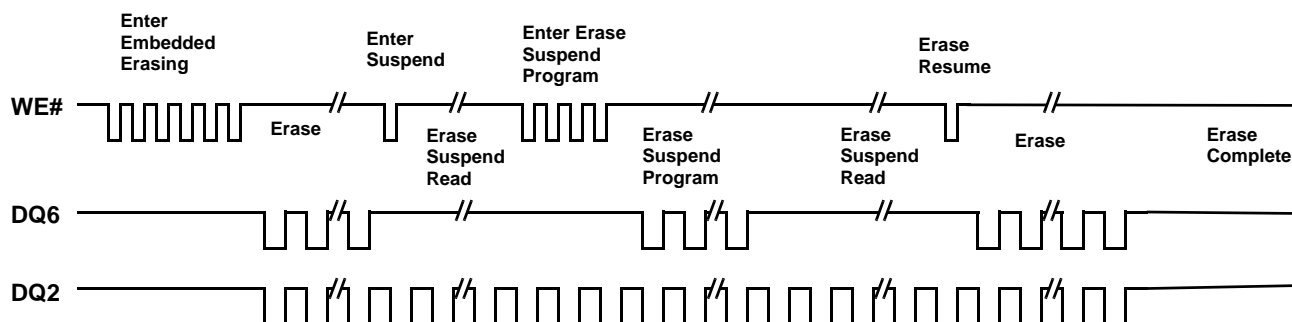
Figure 22. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS



NOTE : VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 23. Toggle Bit Timings (During Embedded Algorithms)



NOTE : DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.

Figure 24. DQ2 vs. DQ6

AC CHARACTERISTICS

Table 17. Temporary Sector Unprotect

| Parameter | | Description | | All Speed Options | Unit |
|-----------|------------|--|-----|-------------------|------|
| JEDEC | Std. | | | | |
| | t_{VIDR} | V_{ID} Rise and Fall Time (See Note) | Min | 500 | ns |
| | t_{RSP} | RESET# Setup Time for Temporary Sector Unprotect | Min | 4 | us |
| | t_{RRB} | RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect | Min | 4 | us |

Note: Not 100% tested.

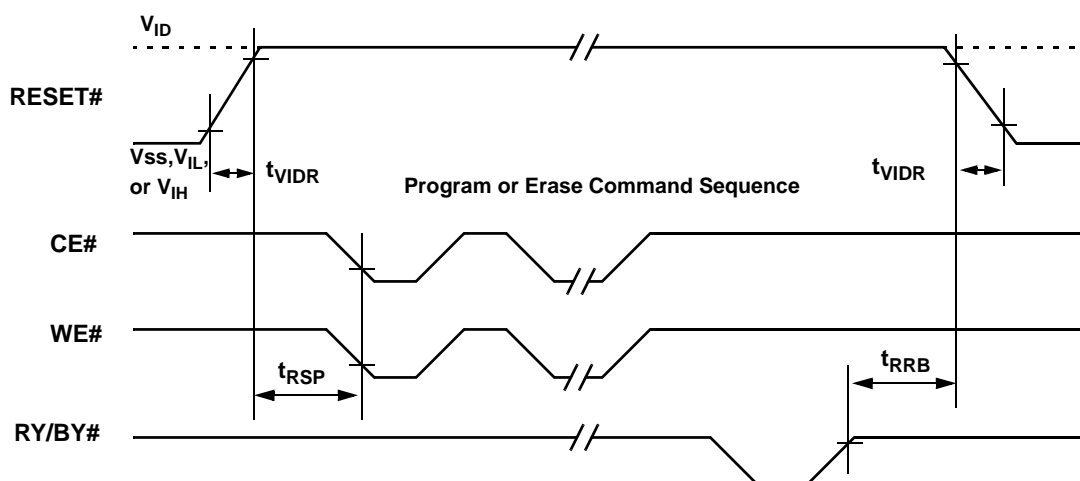
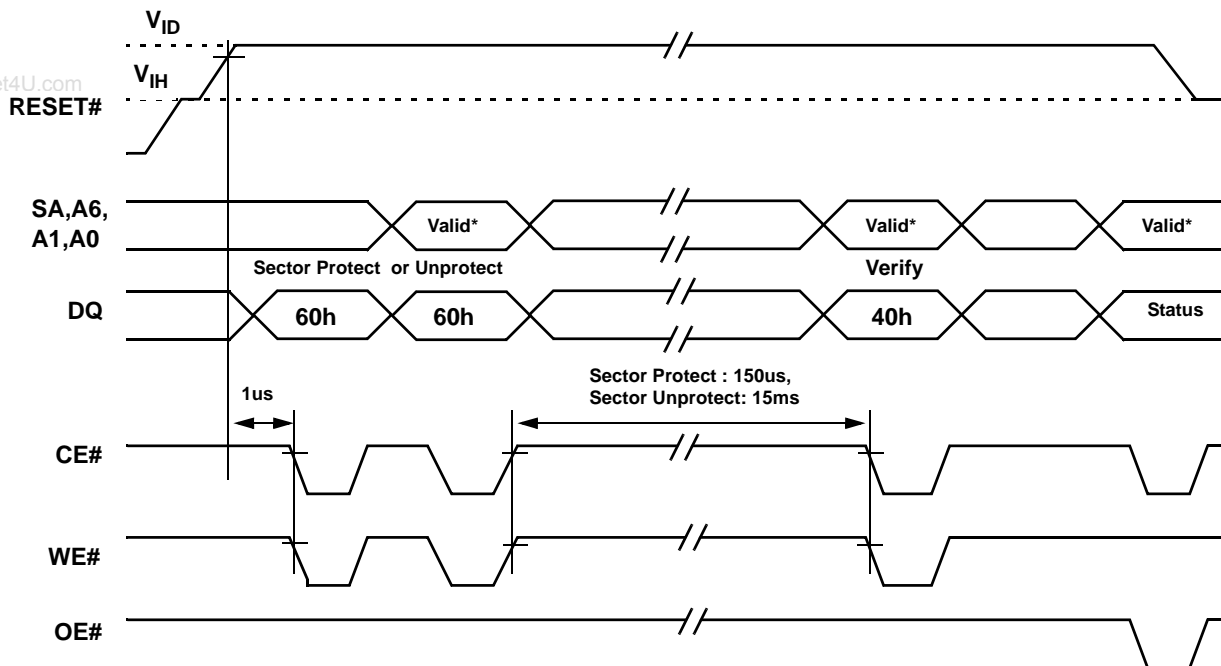


Figure 25. Temporary Sector Unprotect Timing Diagram

AC CHARACTERISTICS



* For sector protect, A6=0, A1=1, A0=0 For sector unprotect, A6=1, A1=1, A0=0

Figure 26. Sector Protect & Unprotect Timing Diagram

AC CHARACTERISTICS

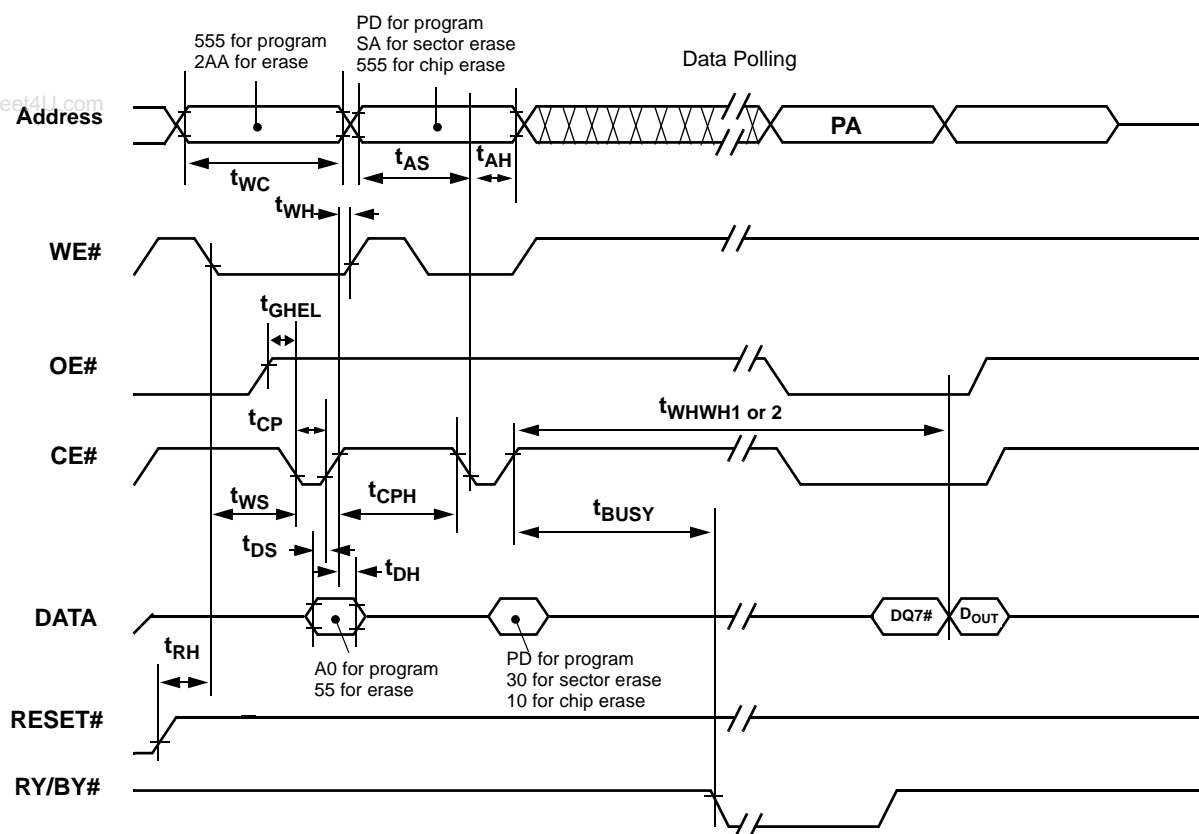
Table 18. Alternate CE# Controlled Erase and Program Operations

| Parameter | | Description | | 70 | 90 | Unit |
|--------------------|--------------------|---|------|-----|----|------|
| JEDEC | Std. | | | | | |
| t _{AVAV} | t _{WC} | Write Cycle Time(Note 1) | Min | 70 | 90 | ns |
| t _{AVWL} | t _{AS} | Address Setup Time | Min | 0 | | ns |
| t _{ELAX} | t _{AH} | Address Hold Time | Min | 45 | 45 | ns |
| t _{DVEH} | t _{DS} | Data Setup Time | Min | 35 | 45 | ns |
| t _{EHDX} | t _{DH} | Data Hold Time | Min | 0 | | ns |
| t _{GHEL} | t _{GHEL} | Read Recovery Time Before Write (OE# High to WE# Low) | Min | 0 | | ns |
| t _{WLEL} | t _{WS} | WE# Setup Time | Min | 0 | | ns |
| t _{EHWH} | t _{WH} | WE# Hold Time | Min | 0 | | ns |
| t _{ELEH} | t _{CP} | CE# Pulse Width | Min | 35 | 35 | ns |
| t _{ELEL} | t _{CPH} | CE# Pulse Width High | Min | 30 | | ns |
| t _{WHWH1} | t _{WHWH1} | Programming Operation (Note 2) | Byte | Typ | 6 | us |
| | | | Word | Typ | 8 | |
| t _{WHWH2} | t _{WHWH2} | Sector Erase Operation (Note 2) | Typ | 0.7 | | sec |

Notes :

1. Not 100% tested
2. See the "Erase And Programming Performance" section for more information.

AC CHARACTERISTICS



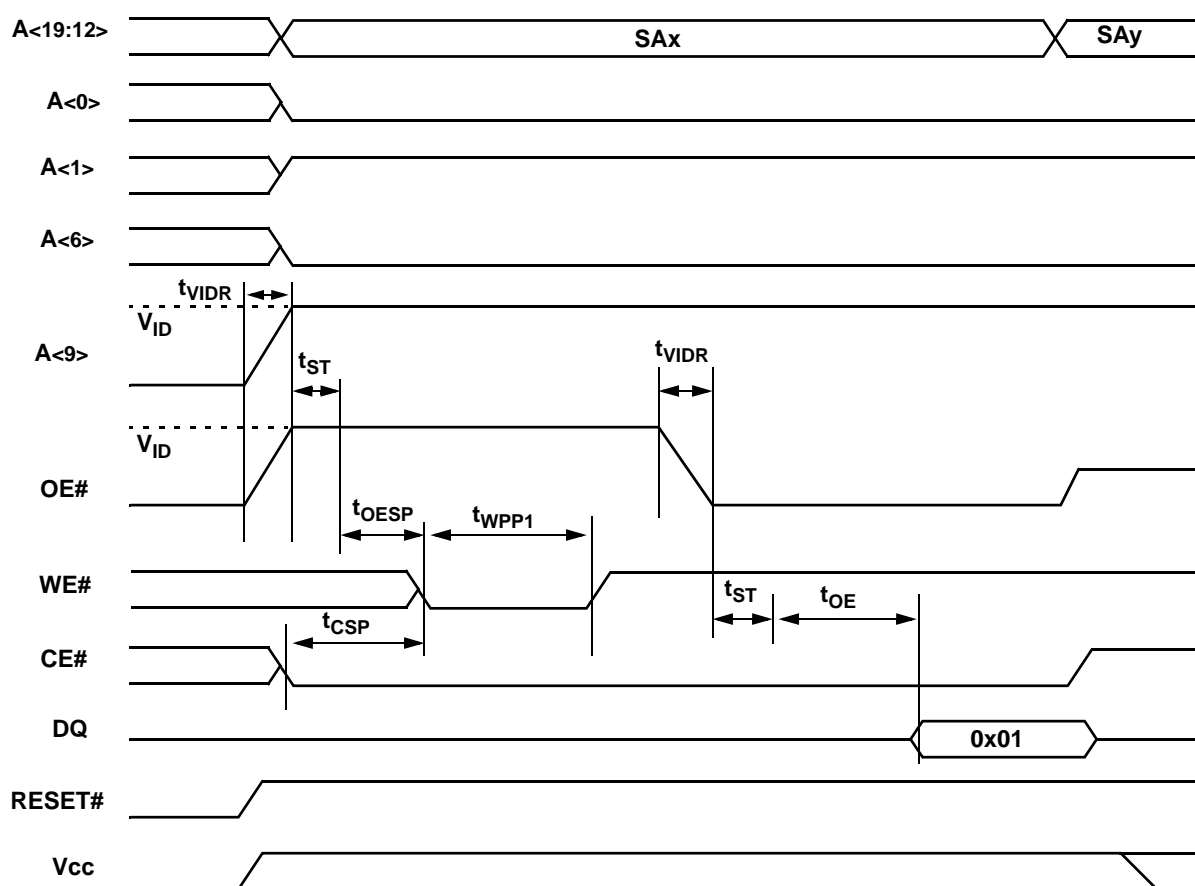
NOTES :

1. Figure indicates last two bus cycles of a program or erase operation.
2. PA = program address, SA = sector address, PD = program data
3. DQ7# is the complement of the data written to the device. DOUT is the data written to the device.
4. Waveforms are for the word mode.

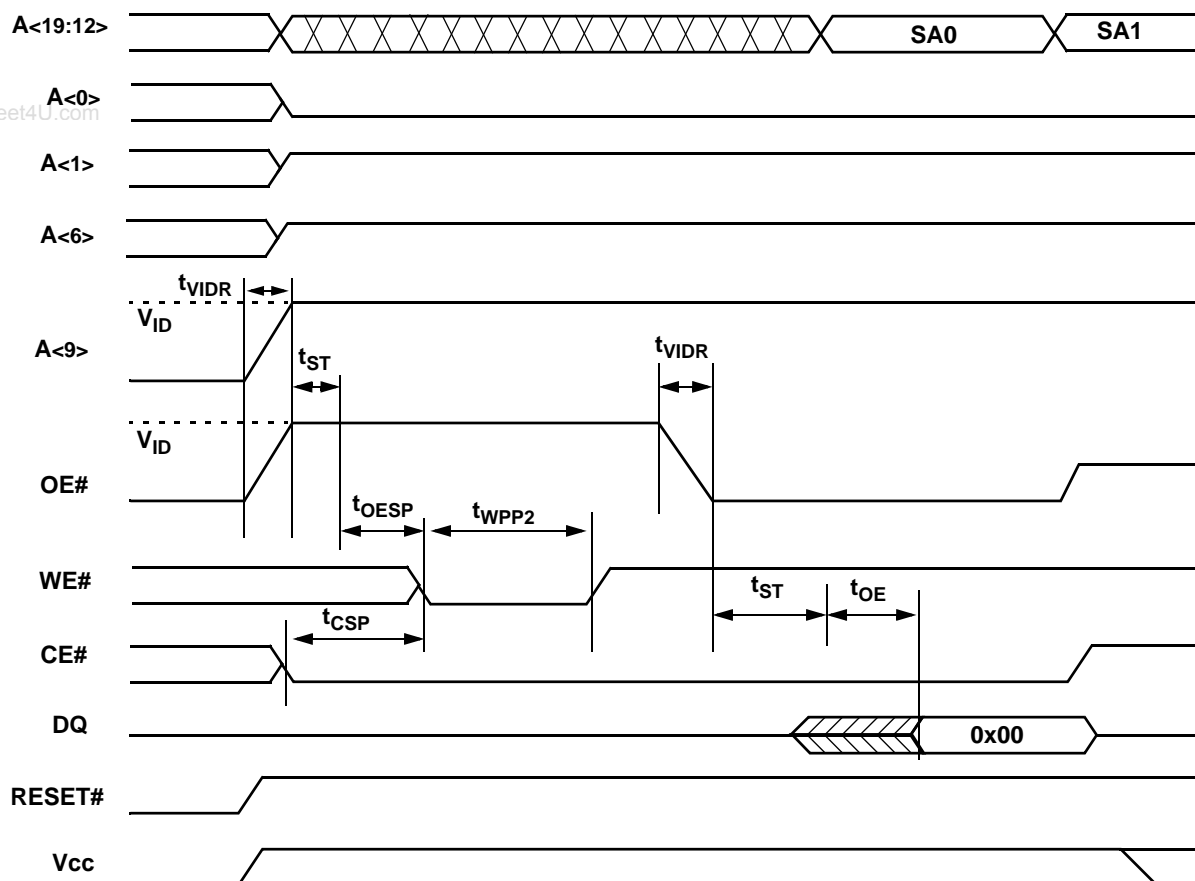
Figure 27. Alternate CE# Controlled Write(Erase/Program) Operation Timings

Table 19. AC CHARACTERISTICS

| Parameter | Description | | Value | Unit |
|------------|--|-----|-------|------|
| t_{OE} | Output Enable to Output Delay | Max | 35/40 | ns |
| t_{VIDR} | Voltage Transition Time | Min | 500 | ns |
| t_{WPP1} | Write Pulse Width for Protection Operation | Min | 150 | us |
| t_{WPP2} | Write Pulse Width for Unprotection Operation | Min | 15 | ms |
| t_{OESP} | OE# Setup Time to WE# Active | Min | 4 | us |
| t_{CSP} | CE# Setup Time to WE# Active | Min | 4 | us |
| t_{ST} | Voltage Setup Time | Min | 4 | us |


Figure 28. Sector Protection timings (A9 High-Voltage Method)

AC CHARACTERISTICS



NOTE : It is recommended to verify for all sectors.

Figure 29. Sector Unprotection timings (A9 High-Voltage Method)

Table 20. ERASE AND PROGRAMMING PERFORMANCE

| Parameter | | Typ (Note 1) | Max (Note 2) | Unit | Comments |
|----------------------------|-----------|--------------|--------------|------|--|
| Sector Erase Time | | 0.7 | 15 | sec | Excludes 00h programming prior to erasure (Note 4) |
| Chip Erase Time | | 25 | | sec | |
| Byte Program Time | | 6 | 150 | us | Exclude system level overhead (Note 5) |
| Word Program Time | | 8 | 210 | us | |
| Chip Program Time (Note 3) | Byte Mode | 12.6 | 37.8 | sec | |
| | Word Mode | 8.4 | 25.2 | | |

Notes:

1. Typical program and erase times assume the following conditions: 25°C, 3.0V Vcc, 10,000 cycles. Additionally, programming typicals assume checkerboard pattern.
2. Under worst case conditions of 90°C, Vcc = 2.7V, 100,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the two-or-four-bus-cycle sequence for the program command. See Table 9 for further information on command definitions.
6. The device has a minimum erase and program cycle endurance of 100,000 cycles.

Table 21. LATCHUP CHARACTERISTICS

| Description | Min | Max |
|---|----------|-------------|
| Input voltage with respect to Vss on all pins except I/O pins (including A9, OE#, and RESET#) | - 1.0V | 12.5 V |
| Input voltage with respect to Vss on all I/O pins | - 1.0V | Vcc + 1.0 V |
| Vcc Current | - 100 mA | +100 mA |

Note: Includes all pins except Vcc. Test conditions: Vcc = 3.0 V, one pin at a time

Table 22. TSOP, SO, AND BGA PACKAGE CAPACITANCE

| Parameter Symbol | Parameter Description | Test Setup | Typ | Max | Unit | |
|------------------|-------------------------|----------------------|------|-----|------|----|
| C _{IN} | Input Capacitance | V _{IN} = 0 | TSOP | 6 | 7.5 | pF |
| | | | FBGA | 4.2 | 5.0 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0 | TSOP | 8.5 | 12 | pF |
| | | | FBGA | 5.4 | 6.5 | pF |
| C _{IN2} | Control Pin Capacitance | V _{IN} = 0 | TSOP | 7.5 | 9 | pF |
| | | | FBGA | 3.9 | 4.7 | pF |

Notes:

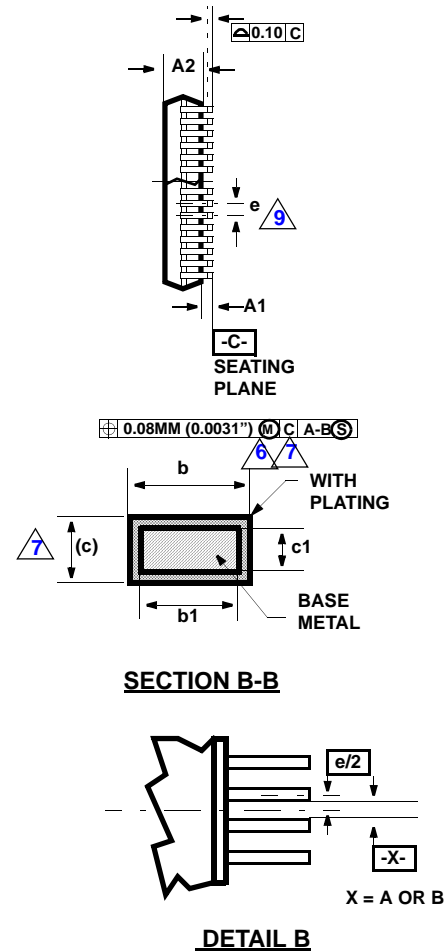
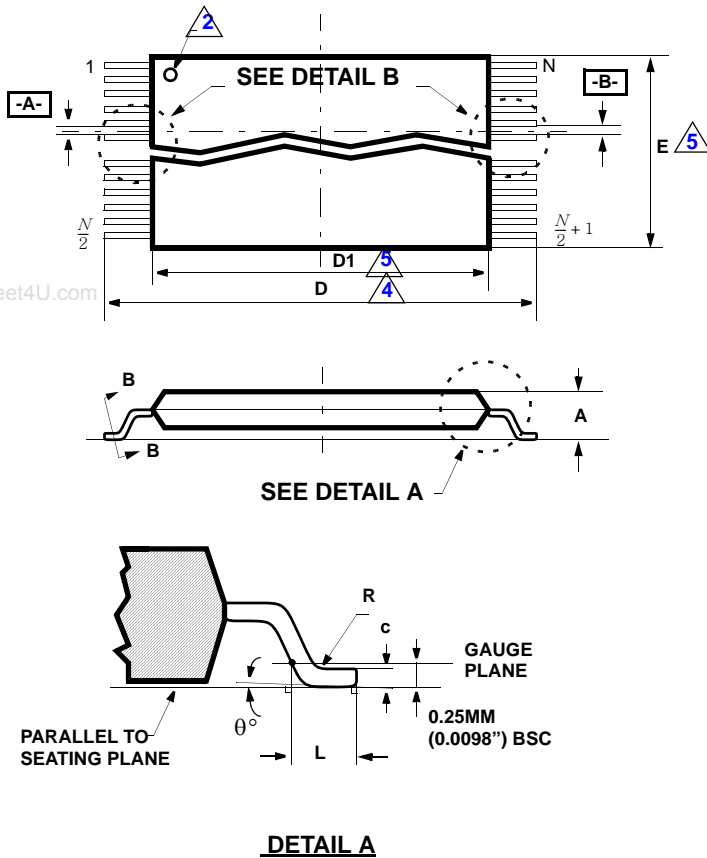
1. Sampled, not 100% tested.
2. Test conditions TA = 25°C, f=1.0MHz.

Table 23. DATA RETENTION

| Parameter Description | Test conditions | Min | Unit |
|-------------------------------------|-----------------|-----|-------|
| Minimum Pattern Data Retention Time | 150°C | 10 | Years |
| | 125°C | 20 | Years |

PHYSICAL DIMENSIONS

48-Pin Standard TSOP (measured in millimeters)



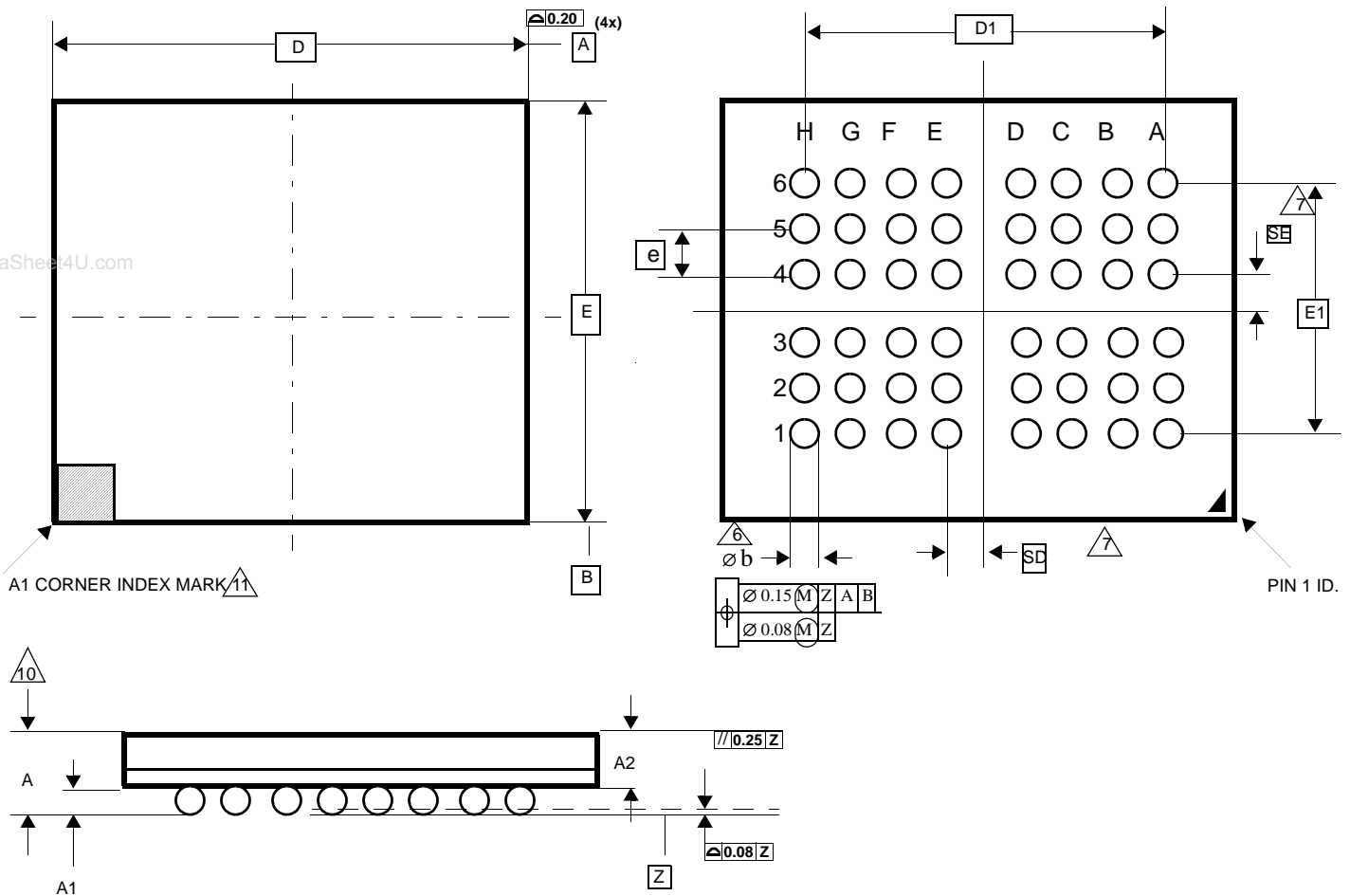
| Package | TS 48 | | |
|----------|---------------|-------|-------|
| JEDEC | MO-142 (B) DD | | |
| Symbol | MIN | NOM | MAX |
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b1 | 0.17 | 0.20 | 0.23 |
| b | 0.17 | 0.22 | 0.27 |
| c1 | 0.10 | - | 0.16 |
| c | 0.10 | - | 0.21 |
| D | 19.80 | 20.00 | 20.20 |
| D1 | 18.30 | 18.40 | 18.50 |
| E | 11.90 | 12.00 | 12.10 |
| e | 0.50 BASIC | | |
| L | 0.50 | 0.60 | 0.70 |
| θ | 0° | 3° | 5° |
| R | 0.08 | - | 0.20 |
| N | 48 | | |

NOTES:

1. Controlling dimensions are in millimeters(mm). (Dimensioning and tolerancing conforms to ANSI Y14.5M-1982)
2. Pin 1 identifier for standard pin out (Die up).
3. Pin 1 identifier for reverse pin out (Die down): Ink or Laser mark
4. To be determined at the seating plane. The seating plane is defined as the plane of contact that is made when the package leads are allowed to rest freely on a flat horizontal surface.
5. Dimension **D1** and **E** do not include mold protrusion. Allowable mold protrusion is 0.15mm (0.0059") per side.
6. Dimension **b** does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.0031") total in excess of **b** dimension at max. material condition. Minimum space between protrusion and an adjacent lead to be 0.07mm (0.0028").
7. These dimensions apply to the flat section of the lead between 0.10mm (0.0039") and 0.25mm (0.0098") from the lead tip.
8. Lead coplanarity shall be within 0.10mm (0.004") as measured from the seating plane.
9. Dimension "e" is measured at the centerline of the leads.

PHYSICAL DIMENSIONS

48-Ball FBGA (6 x 8 mm)



| PACKAGE | xFBD 048 | | | |
|---------|---------------------------|------|------|----------------------------|
| JEDEC | N/A | | | |
| | 6.00 mm x 8.00 mm PACKAGE | | | |
| SYMBOL | MIN | NOM | MAX | NOTE |
| A | | | 1.10 | OVERALL THICKNESS |
| A1 | 0.21 | 0.25 | 0.29 | BALL HEIGHT |
| A2 | 0.7 | 0.76 | 0.82 | BODY THICKNESS |
| D | 8.00 BSC | | | BODY SIZE |
| E | 6.00 BSC | | | BODY SIZE |
| D1 | 5.60 BSC | | | BALL FOOTPRINT |
| E1 | 4.00 BSC | | | BALL FOOTPRINT |
| MD | 8 | | | ROW MATRIX SIZED DIRECTION |
| ME | 6 | | | ROW MATRIX SIZED DIRECTION |
| N | 48 | | | TOTAL BALL COUNT |
| b | 0.30 | 0.35 | 0.40 | BALL DIAMETER |
| e | 0.80 BSC | | | BALL PITCH |
| SD / SE | 0.40 BSC | | | SOLDER BALL PLACEMENT |

NOTES:

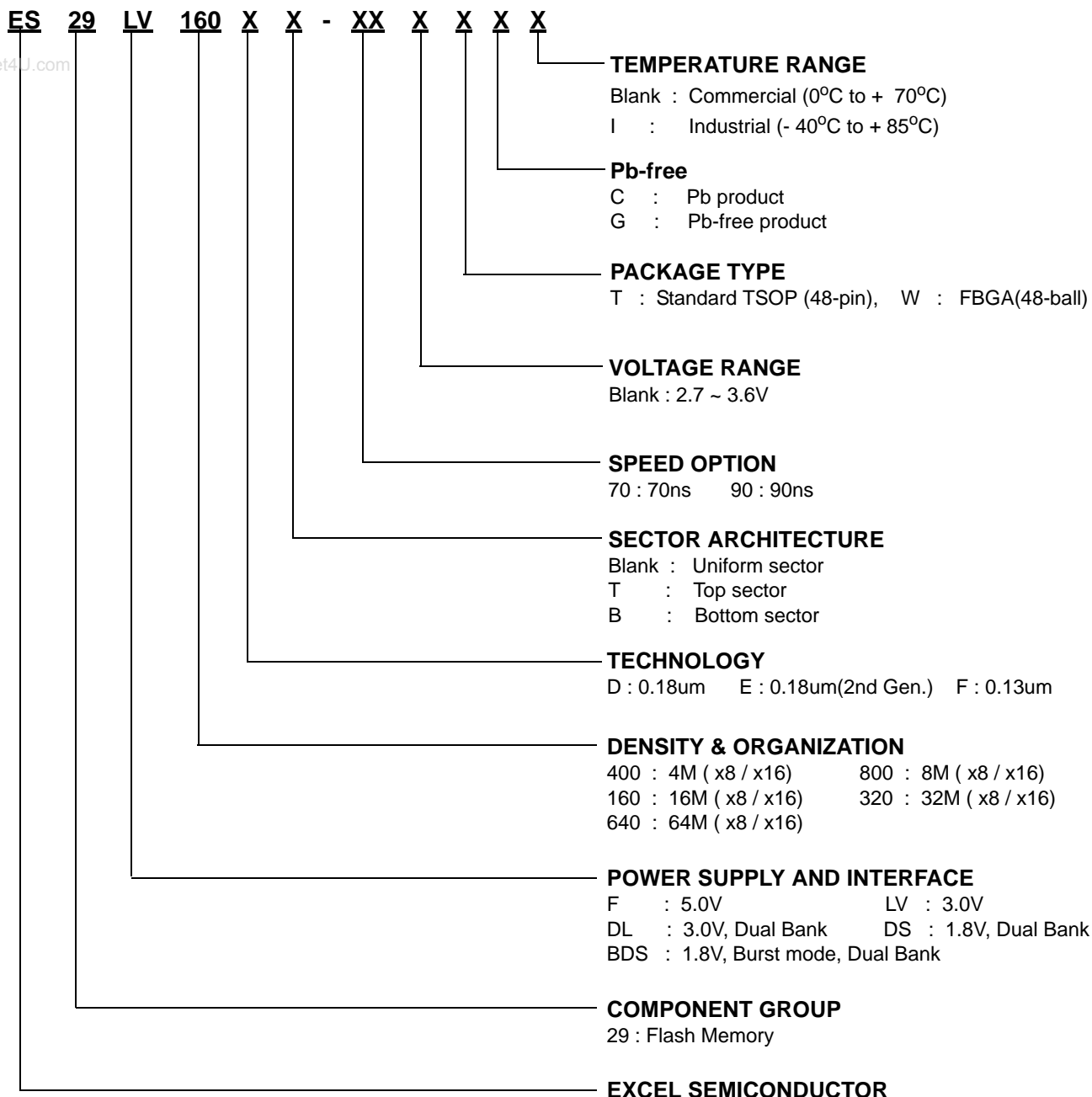
- Dimensioning and tolerancing per ASME Y14.5M-1994
- All dimensions are in millimeters.
- Ball position designation per JESD 95-1, SPP-010.
- \square represents the solder ball grid pitch.
- Symbol "MD" is the ball row matrix size in the "D" direction. Symbol "ME" is the ball column matrix size in the "E" direction. N is the maximum number of solder balls for matrix size MD X ME.
- \triangle Dimension "b" is measured at the maximum ball diameter in a plane parallel to datum Z.
- \triangle SD and SE are measured with respect to datums A and B and define the position of the center solder ball in the outer row. When there is an odd number of solder balls in the outer row parallel to the D or E dimension, respectively, SD or SE = 0.000 when there is an even number of solder balls in the outer row, SD or SE = $\lceil e/2 \rceil$
- "X" in the package variations denotes part is outer qualification.
- "+" in the package drawing indicate the theoretical center of depopulated balls.
- \triangle For package thickness A is the controlling dimension.
- \triangle A1 corner to be identified by chamfer, ink mark, metallized markings indentation or other means.



ORDERNG INFORMATION

Standard Products

ESI standard products are available in several package and operating ranges. The order number (Valid Combination) is formed by a combination of the following:





Product Selection Guide

Industrial Device

| Part No. | Speed | Vcc | Boot Sector | Package | Pb | Ball Pitch/Size | Body Size |
|-------------------|-------|------------|-------------|--------------|---------|-----------------|-----------|
| ES29LV160ET-70TGI | 70ns | 2.7 - 3.6V | Top | 48-pin TSOP | Pb-free | | |
| ES29LV160ET-70TCI | 70ns | 2.7 - 3.6V | Top | 48-pin TSOP | - | | |
| ES29LV160EB-70TGI | 70ns | 2.7 - 3.6V | Bottom | 48-pin TSOP | Pb-free | | |
| ES29LV160EB-70TCI | 70ns | 2.7 - 3.6V | Bottom | 48-pin TSOP | - | | |
| ES29LV160ET-90TGI | 90ns | 2.7 - 3.6V | Top | 48-pin TSOP | Pb-free | | |
| ES29LV160ET-90TCI | 90ns | 2.7 - 3.6V | Top | 48-pin TSOP | - | | |
| ES29LV160EB-90TGI | 90ns | 2.7 - 3.6V | Bottom | 48-pin TSOP | Pb-free | | |
| ES29LV160EB-90TCI | 90ns | 2.7 - 3.6V | Bottom | 48-pin TSOP | - | | |
| ES29LV160ET-70WGI | 70ns | 2.7 - 3.6V | Top | 48-Ball FBGA | Pb-free | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160ET-70WCI | 70ns | 2.7 - 3.6V | Top | 48-Ball FBGA | - | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160EB-70WGI | 70ns | 2.7 - 3.6V | Bottom | 48-Ball FBGA | Pb-free | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160EB-70WCI | 70ns | 2.7 - 3.6V | Bottom | 48-Ball FBGA | - | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160ET-90WGI | 90ns | 2.7 - 3.6V | Top | 48-Ball FBGA | Pb-free | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160ET-90WCI | 90ns | 2.7 - 3.6V | Top | 48-Ball FBGA | - | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160EB-90WGI | 90ns | 2.7 - 3.6V | Bottom | 48-Ball FBGA | Pb-free | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160EB-90WCI | 90ns | 2.7 - 3.6V | Bottom | 48-Ball FBGA | - | 0.8mm/0.3mm | 6mm x 8mm |



Product Selection Guide

Commercial Device

| Part No. | Speed | Vcc | Boot Sector | Package | Pb | Ball Pitch/Size | Body Size |
|------------------|-------|------------|-------------|--------------|---------|-----------------|-----------|
| ES29LV160ET-70TG | 70ns | 2.7 - 3.6V | Top | 48-pin TSOP | Pb-free | | |
| ES29LV160ET-70TC | 70ns | 2.7 - 3.6V | Top | 48-pin TSOP | - | | |
| ES29LV160EB-70TG | 70ns | 2.7 - 3.6V | Bottom | 48-pin TSOP | Pb-free | | |
| ES29LV160EB-70TC | 70ns | 2.7 - 3.6V | Bottom | 48-pin TSOP | - | | |
| ES29LV160ET-90TG | 90ns | 2.7 - 3.6V | Top | 48-pin TSOP | Pb-free | | |
| ES29LV160ET-90TC | 90ns | 2.7 - 3.6V | Top | 48-pin TSOP | - | | |
| ES29LV160EB-90TG | 90ns | 2.7 - 3.6V | Bottom | 48-pin TSOP | Pb-free | | |
| ES29LV160EB-90TC | 90ns | 2.7 - 3.6V | Bottom | 48-pin TSOP | - | | |
| ES29LV160ET-70WG | 70ns | 2.7 - 3.6V | Top | 48-Ball FBGA | Pb-free | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160ET-70WC | 70ns | 2.7 - 3.6V | Top | 48-Ball FBGA | - | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160EB-70WG | 70ns | 2.7 - 3.6V | Bottom | 48-Ball FBGA | Pb-free | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160EB-70WC | 70ns | 2.7 - 3.6V | Bottom | 48-Ball FBGA | - | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160ET-90WG | 90ns | 2.7 - 3.6V | Top | 48-Ball FBGA | Pb-free | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160ET-90WC | 90ns | 2.7 - 3.6V | Top | 48-Ball FBGA | - | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160EB-90WG | 90ns | 2.7 - 3.6V | Bottom | 48-Ball FBGA | Pb-free | 0.8mm/0.3mm | 6mm x 8mm |
| ES29LV160EB-90WC | 90ns | 2.7 - 3.6V | Bottom | 48-Ball FBGA | - | 0.8mm/0.3mm | 6mm x 8mm |



Document Title**16M Flash Memory****Revision History**

| Revision Number | Date | Items |
|-----------------|--------------|------------------------------------|
| Rev. 0A | Sep. 1, 2005 | Initial Release Version. |
| Rev. 0B | Jan. 5, 2006 | Add RoHS-Compliant Package Option. |

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