I、GENERAL DESCRIPTION

The ES5136 combines analog section and digital section on a single monolithic CMOS integrated circuit to provide a high performance, very low power 3 1/2 –digit A/D converter. Each device includes a dual slope converter, internal reference, seven segment decoders, display drivers, and clock. The ES5136 is designed to interface with a liquid crystal display and includes a back plane drive. The supply current is only 150μA, very suitable for 9V battery operation.

To built a high performance digital panel meter, ES5136 needs only few passive components and a LCD display. The true differential input and reference of ES5136 are versatile and useful in all systems, and these give the designers an uncommon advantage to make the measurement of load cells, train gauges and other bridge type transducers.

The ES5136 can be used as a plug-in replacement for the ES5106 in a wide variety of applications by changing only the passive components of the ES5106. The ES5136 differs from the ES5106 in that it includes lower power dissipation, improved temperature coefficient of analog common and scale factor, and the design of ZERO INTEGRATE phase to eliminate the overrange hangover and hysteresis.

II、FEATURES

*Pin compatible with ES5106.

*Internal reference with low temperature drift

*Direct LCD display drive

*No additional active components required

*Low input leakage current---1pA typical

*Guaranteed zero reading for 0 volts input on all scales

*Auto polarity indication

*True differential input and reference

*Internal clock circuit

*Low power consumption

III、APPLICATTONS

*Digital panel meters

*Digital multi-meters

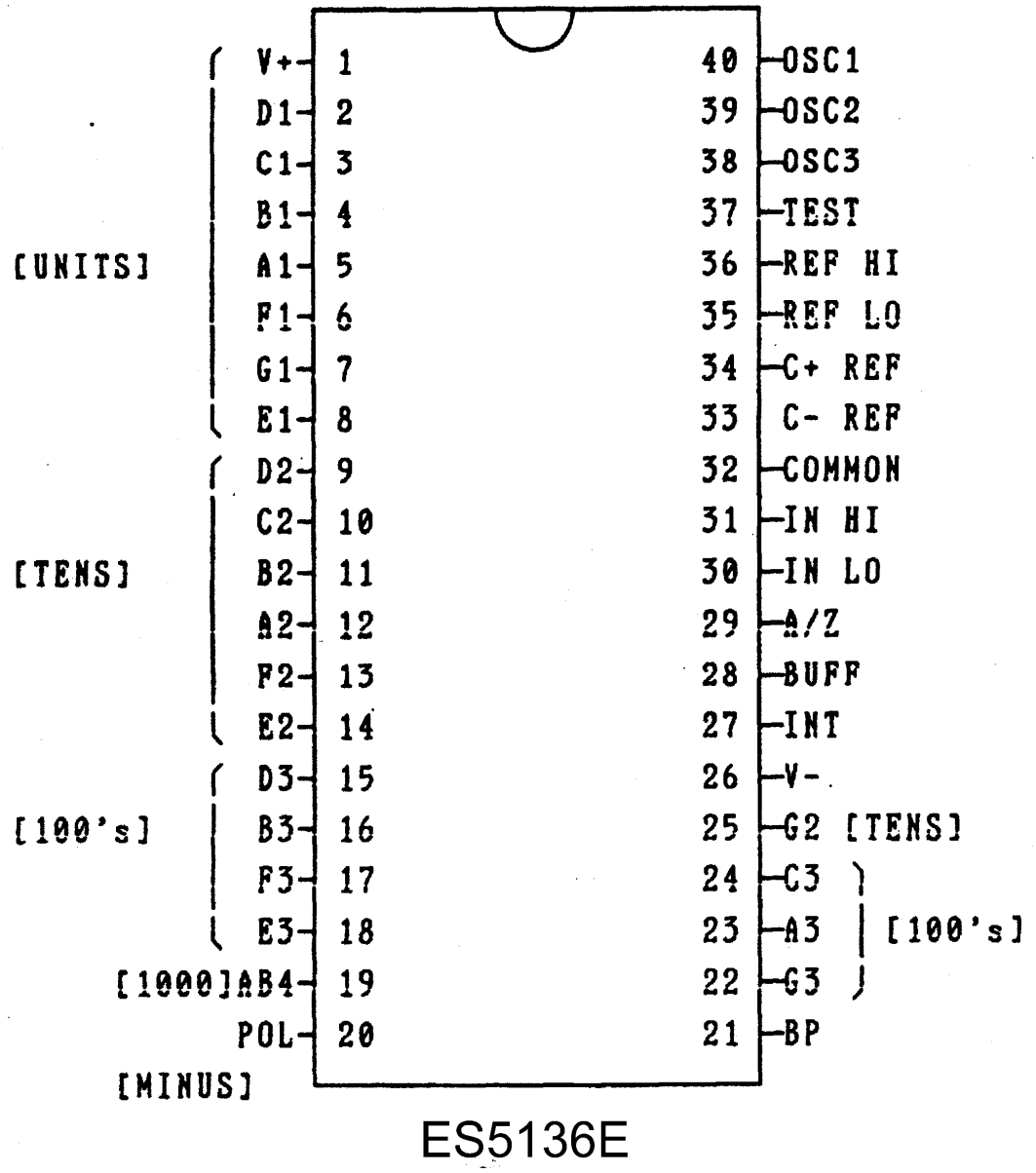
*Digital centigrade thermometer

*pH meters

*Capacitance meters

IV、PIN ASSIGNMENT

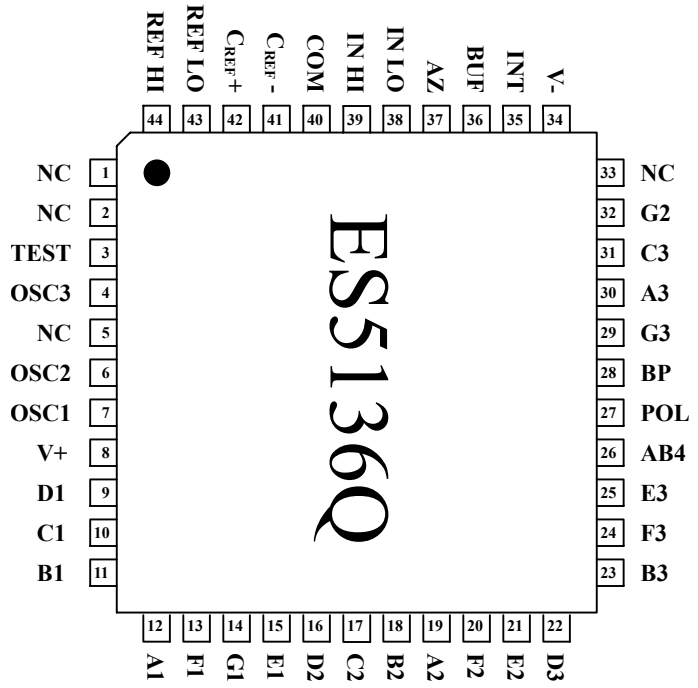
40 PIN DIP Package



ES5136E

44PIN QFP Package

PIN ASSIGNMENT



V、BLOCK DIAGRAM

V. BLOCK DIAGRAM

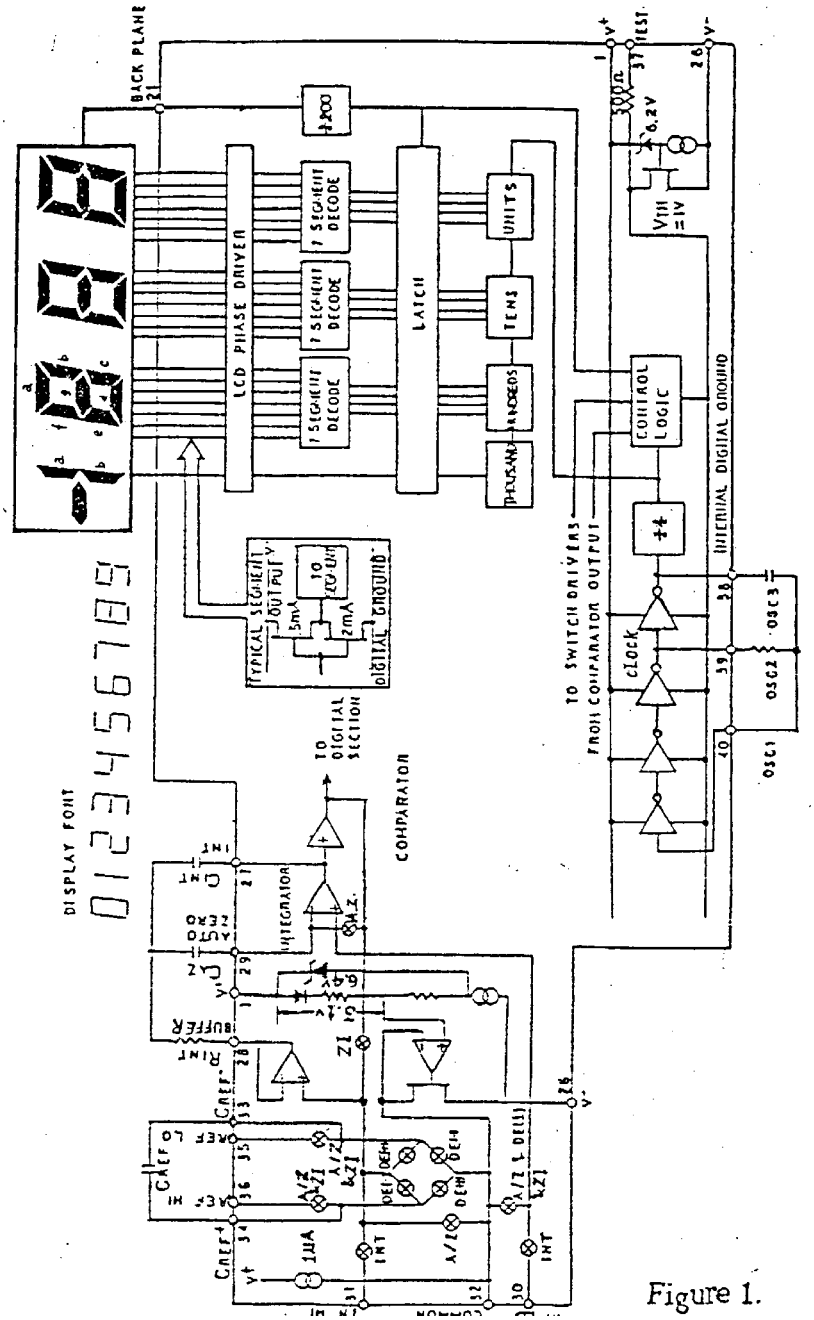


Figure 1.

VI、ABSOLUTE MAXIMUM RATING

DC Supply Voltage (between pin 1.V+ and pin 26.V-) ------ 12V

Analog Input Voltage (either input)---------- V+ to V-

Reference Input Voltage(either input) ---------- V+ to V-

Clock Input ---------- TEST to V+

Power Dissipation(plastic package) ---------- 800 mW

Operating Temperature ---------- 0℃ to + 70℃

Storage Temperature ---------- -65℃ to +150℃

Lead Temperature(during soldering):

At distance 1/16±1/32 inch(1.59±0.79mm)from case for 10S max +265℃

VII、ELECTRICAL CHARACTERISTICS

AT T_A = 25℃,V+ to V- = 9V , f_{colock} = 48Khz unless otherwise indicated. Refer to Fig.2.

CHARACTERISTIC	TEST CONDITIONS	LIMITS			
		MIN	TVP	MAX	UNITS
Zero Input Reading	V_{IN}=0.0V	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
$R_{OLLOVER}$ Error	-VIN = +VIN≅200.0mV	-1	±0.2	+1	Counts
Linearity	Full Scale = 200mV or 2V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ± 1V,V_{IN} = 0V Full Scale = 200.0mV	—	50	—	μV/V
Input Leakage Current	V_{IN} = 0V	—	1	10	pA

ELECTRICAL CHARACTERISTICS(Contd.)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			Units
		Min	Typ	Max	
Noise (P_K-P_K value not exceeded 95% of time)	V_{IN} = OV Full Scale = 200mV	—	15	—	μV
Zero Reading Drift	V_{IN} = 0V 0℃<T_A<70℃	—	0.2	—	μV/℃
Scale Factor Temperature Coefficient	VIN = 199.0mV 0℃<TA<70℃ (Ext. Ref.0 ppm/℃)	—	1	5	ppm/℃
Supply Current (Does not include COMMON current)	VIN = 0V (not 1)	—	150	180	μA
Analog COOMON Voltage (with respect to V+)	250 KΩ between COMMON & V+	2.8	3.0	3.2	V
Temp. Coeff. of Analog COMMON (with respect to V+)	250 KΩ between COMMON & V+	—	50	75	ppm/℃
P_K-P_K Segment Drive Voltage	V+ to V- = 9V	4	5	6	V
P_K-P_K Backplane Drive Voltage	V+ to V- = 9V	4	5	6	V
Power Dissipation Capacitance	VS. Clock Freq	—	40	—	pF

Note 1:During auto zero phase, current is 10-20μA higher.

VIII、TEST CIRCUIT

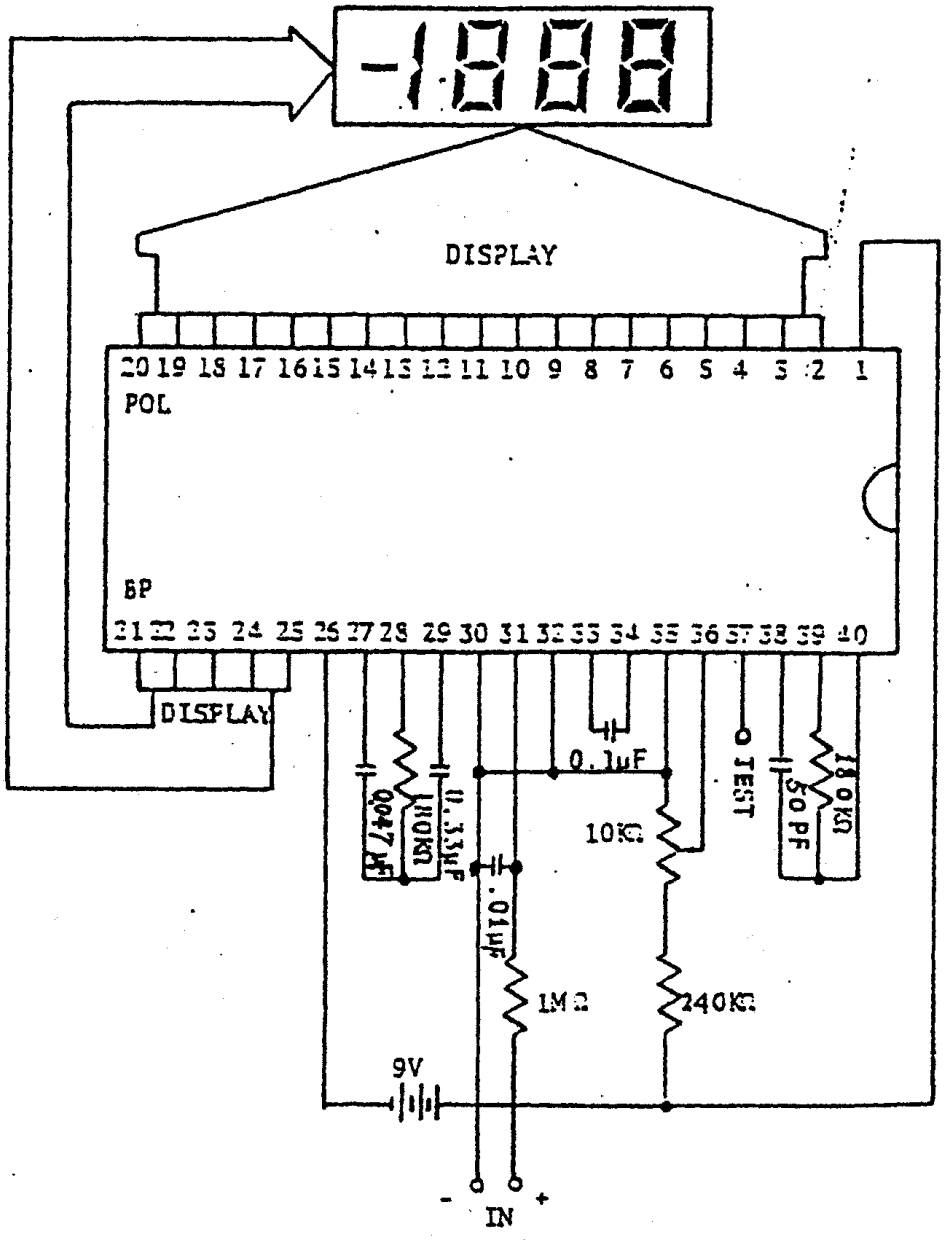


Figure 2 : ES5136 Clock Frequency 48 KHz,
200mV Full scale.

DX、FUNCTION DESCRIPTION

A、Analog Section

The Analog Section of the ES5136 is a dual slope converter, which is shown in Figure 1. The conversion takes place in four distinct phases.

1.Phase 1, Auto Zero (A/Z)

During auto zero processing, the internal A/Z switches are turned on. The errors in the analog components(offset voltage of buffer, integrator and comparator)will be automatically nulled out by shorting the input internally to COMMON and closing a feed back loop such that error information is stored on the auto-zero capacitor C_{AZ} At the same time. the reference capacitor is charged to the reference voltage V_{REF}.

2.Phase 2, Signal Integrate(INT)

During signal integrating, the A/Z switches are opened and the INT switches are closed for 1,000 system clock pulses. The integrating capacitor will ramp up at a rate that is proportional to input voltage V_{IN}. At the end of this phase the polarity of the integrated signal is determined.

3.Phase 3, Reference Deintegrate(DE)

At the beginning of this phase, the input low is internally connected to COMMON and input high is switched from V_{IN} to. V_{REF} According to the polarity, the integrator will discharge back toward zero. The nuber of system clock pulses counted between the beginning of this cycle and the time when the integrator output passes through zero is a digital measure of the magnitude of input voltage. Specifically the digital reading displayed is $1000(V_{IN}/V_{REF})$.

4.Phase 4, Zero Integrate (ZI)

During zero integrating, the reference capacitor is charged to the reference voltage and input low is shorted to analog common. At the same time, a feedback loop is closed around the system to input high to cause the integrator output to return to zero so that the overrange hangover of the integral capacitor can be eliminated.

5.Differential Input

The input voltage can be any differential voltages, but must be within the common mode range of the input amplifier(buffer). The voltage range is from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the CMRR of the system is 86dB typical. Since the integrator swings with the common mode voltage, it must be assured that the integrator output does not saturate.

6.Differential Reference

The reference inputs are floating, and the only restriction on the applied voltage is that it should lie in the range of the owner supply voltage of the converter. The roll- over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes is the main source of common mode error. In a large common mode condition, the reference capacitor will gain extral charge(increase voltage)when deintegrates a positive signal but lose charge(decrease voltage)when deintegrates a negative input signal. The difference in reference for positive or negative input signal will give a roll-over error. By selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition.

7. Analog COMMON

The voltage between V+ and COMMON is internally regulated at about 3.1 volts. Thus the COMMON pin can set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. As a reference, the common voltage is adequate for many applications.

When the total supply voltage is large enough to cause the zener to regulate(6.4V typical), the common voltage will have a low voltage coefficient(0.001%/%), low output impedance (≅10Ω), and a temperature coefficient typically less than 75ppm/℃.

The on-chip reference has some limitations. If there is a large temperature variation, the reference temperature coefficient may not take over and cause some errors. The other limitation is when the total supply voltage is less than that which will cause the zener to regulate, the common voltage will have a poor voltage coefficient. The problems are of course eliminated if an external reference is used, as shown in Figure 3.

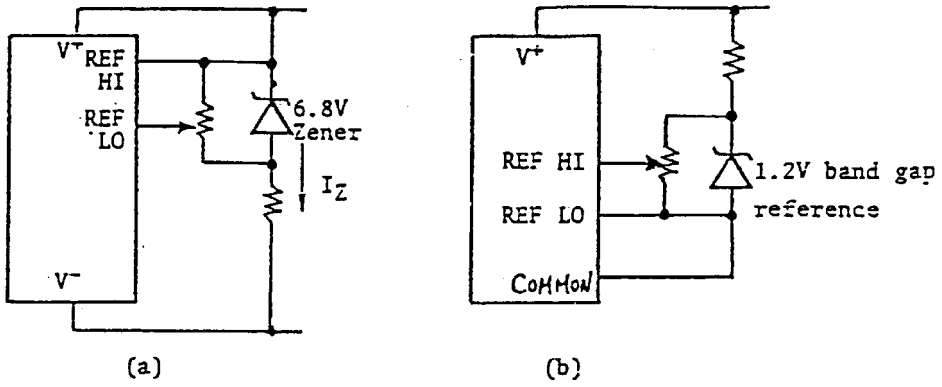


Figure 3:Using External reference

During auto-zero and deintegrating, analog COMMON is used as the return of input low. If IN LO and COMMON are not connected to the same node, a common mode voltage may exist in the system and is taken care of by the excellent CMRR of the ES5136.

When IN LO is set at a fixed known voltage, COMMON should be tied to the same point of IN LO, thus the common mode voltage can be removed from the converter. The same holds true for the reference voltage. If reference can be referenced to analog COMMON, it should be since this removes the common mode voltage from output stage of analog COMMON includes an N channel FET that can sink 30mA or more of current to hold the voltage 3.1 volts below the positive supply . And there is only 1μA of source current, so the COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

8. Digital Section

The digital section of the ES5136 is shown in Figure 1. A large P channel source follower and a 6 volts zener diode form the internal digital ground of ES5136. This formation is strong enough to absorb large capacitive currents when the back plane (BP) voltage is switched.

1. Test

The TEST pin is connected to the internal digital ground by a 500Ω resistor. It has two functions. First, it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation on the LCD display. Figures 4(a) and (b) show such an application. The applied load current should not be more than 1mA. Second, it is used as "lamp test". When TEST is connected to V+(pull high)all segments will be turned on and the display should read-1888. The TEST pin will sink about 10mA under this cibdutuib.

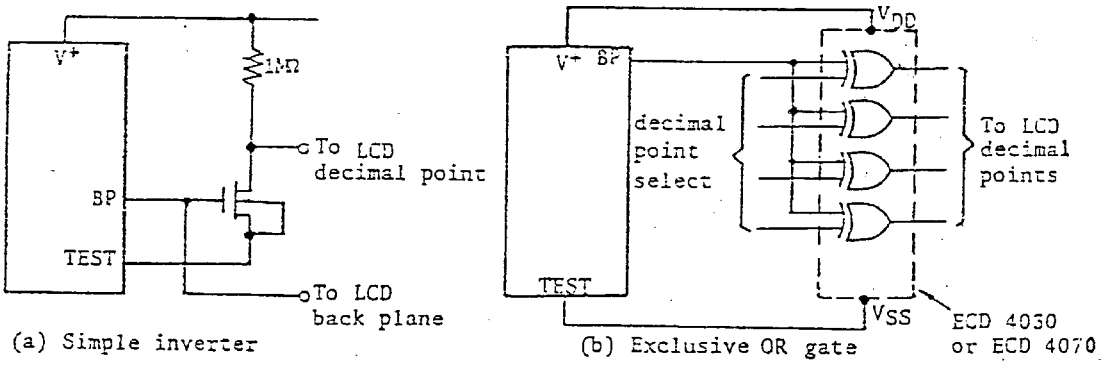


Figure4: Decimal point drivers

Coution:In the lamp test mode, the segments output are no longer a square-wave but a constant DC voltage which may destroy the LCD display if left in this mode for extended periods.

2. System Clock

Following three basic clocking arrangements can be used in the ES5136.

a. An external oscillator connected to pin 40

b. A crystal between pins 39 and 40

c. An R-C oscillator using all three pins

These arrangements are shown in Figure 5.

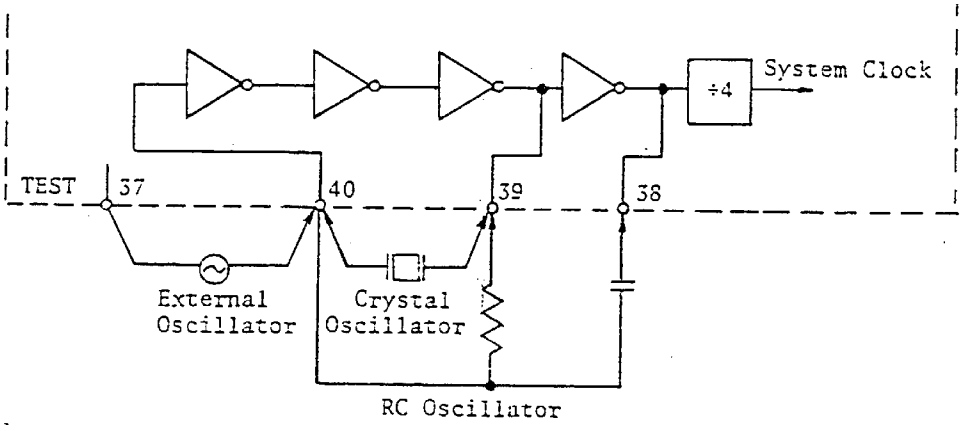


Figure 5: Clock Circuits

The clock frequency is divided by 4 prior to being used as the system clock. The system clock is then divided to form the four convert-cycle phases. They are signal integrate(1000 counts), reference deintegrate(0 to 2000 counts), zero integrator(11 counts to 140 counts) and auto-zero(910 to 2900 counts). When input signals are less than full scale, the unused portion of reference deintegrate and zero integrator is occupied by auto-zero.

Thus a complete measure cycle is 4,000 cunts and is independent of input voltage. When the clock frequency is 48Khz , the conversion tate is 3 readings per second.

To achieve maximum line frequency(60Hz) noise rejection, the signal integrate period should be an integral number of line frequency period. For 60Hz noise rejection, clock frequency should be one of 24KHz, 120KHz, 80KHz, 60KHz, 48KHz, 34 2/7KHz, etc. For 50Hz rejection, clock frequencies of 2000Khz, 100KHz, 66 2/3KHz, etc. would be suitable. Note that 40Khz will reject both 50 and 60Hz.

3. Back Plane and Polarity

The back plane(BP)frequency is the system clock frequency divided by 200. For 3 readings/sec conversion rate, the BP frequency is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude of BP, but out of phase when ON and in phase when OFF. In all cases negligible dc voltage exists across the segments. The polarity (POL) indication is “ON” for negative input signals.

X、COMPONENT VALUE SELECTION

1. Oscillator Components

For all ranges of clock frequency a 50PF or 47PF capacitor is recommended and the approximate resistor values are given in the Table 1.

2. Reference Voltage

The relation ship between the full-scale input voltage and the reference voltage is :V_{IN} (full-scale) = $2V_{REF}$,for 200mV full scale, the voltage applied between REF HI and REF LO should be set at 100/0mV. For 2V full scale, set reference voltage at 1.000V.

3. Integrating Resistor

The output stage of the buffer amplifier and the integrator have a quiescent current of 6μA. They can supply drive current around 1μA with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full scale, 1.8MΩ is near optimum and similarly 180KΩ for a 200mV scale.

4.Integrating Capacitor

The value of integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing(approx. 0.3V from either supply). When the analog COMMON is used as reference, a nominal ±2V full scale integrator swing is recommended.

The value of C_{INT} is 0.047 μF for 48Khz clock frequency , and is 0.15μF for 16Khz clock frequency. If different clock frequencies are used, the value of C_{INT} should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should be a low dielectric-loss type to prevent roll-over errors. Long term stability and temperature coefficient are unimportant since the dual slope technique cancels the effect of these variations. Polypropylene capacitors have been found to work well; they have low dielectric loss characteristics and are inexpensive.

5.Auto-Zero Capacitor

Since much of the noise originates in the auto-zero loop, the size of the auto-zero capacitor has some influence on the noise of the converter, For 200mV full scale where noise is very important, a 0.33μF capacitor is recommended. For 2V full scale, a 0.033μF capacitor can increase the speed of recovery from overload and is adequate for noise on this scale.

6.Reference Capacitor

A 0.1μF reference capacitor is large enough to work well in most applications. When a large common mode voltage exists and a 200mV full scale is used, capacitor of large value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

CLOCK Freq. / RC value	34 2/7Khz	40KHz	48KHz	50KHz	60KHz	66 2/3KHz
R(C = 47PF)	280KΩ	240KΩ	200KΩ	190KΩ	160KΩ	140KΩ
R(C = 47PF)	250KΩ	220KΩ	180KΩ	170KΩ	140KΩ	120KΩ

Table 1: Resistor value VS. Clock Frequency

XI、APPLICATION CIRCUITS

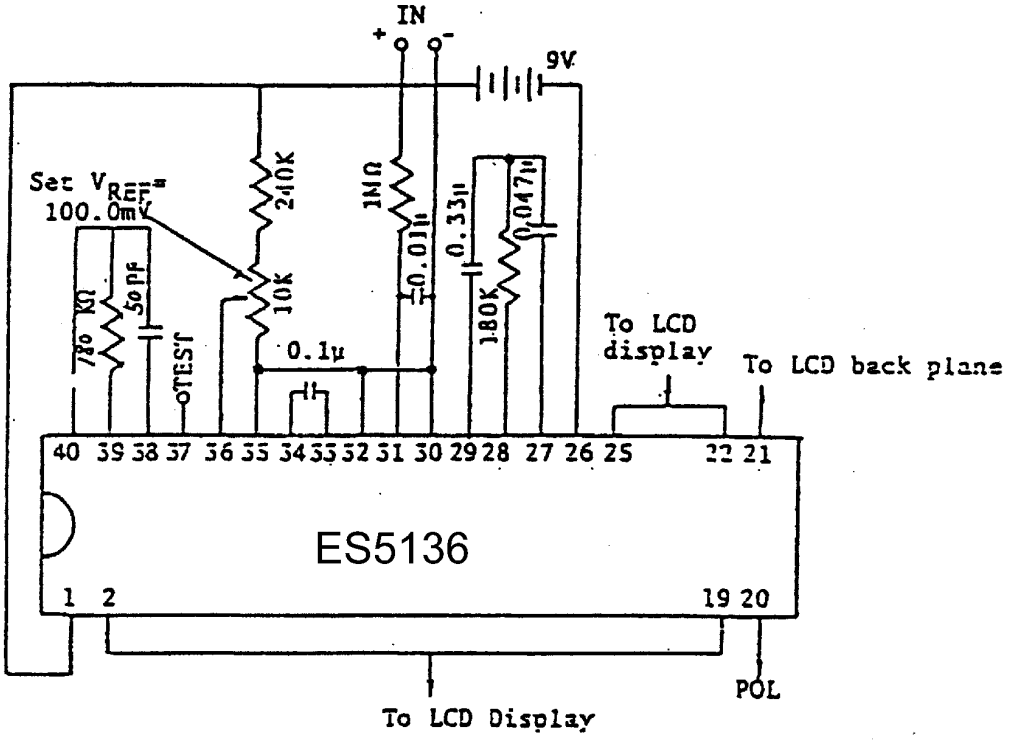


Figure 6: Typical DPM circuit, 200mV full-scale, 3 readings/sec, using internal reference.

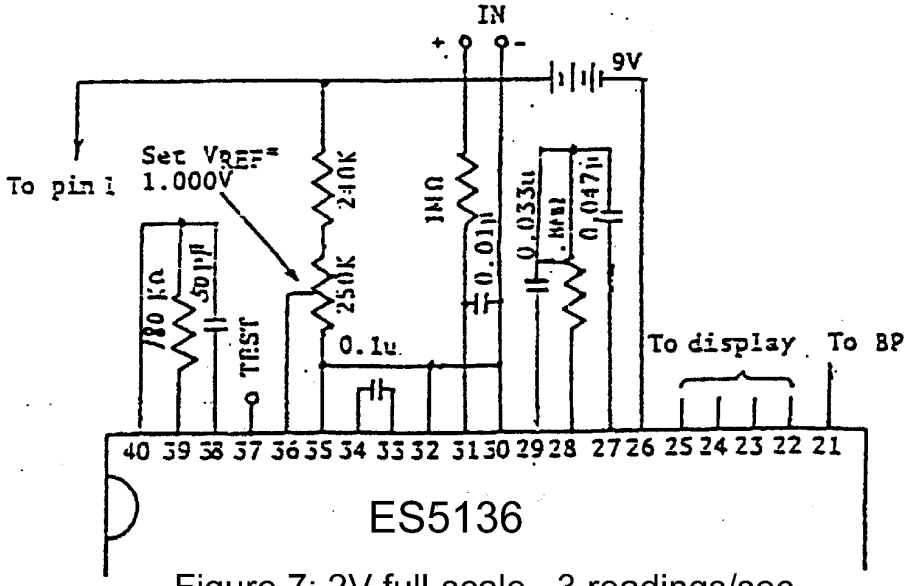


Figure 7: 2V full-scale , 3 readings/sec

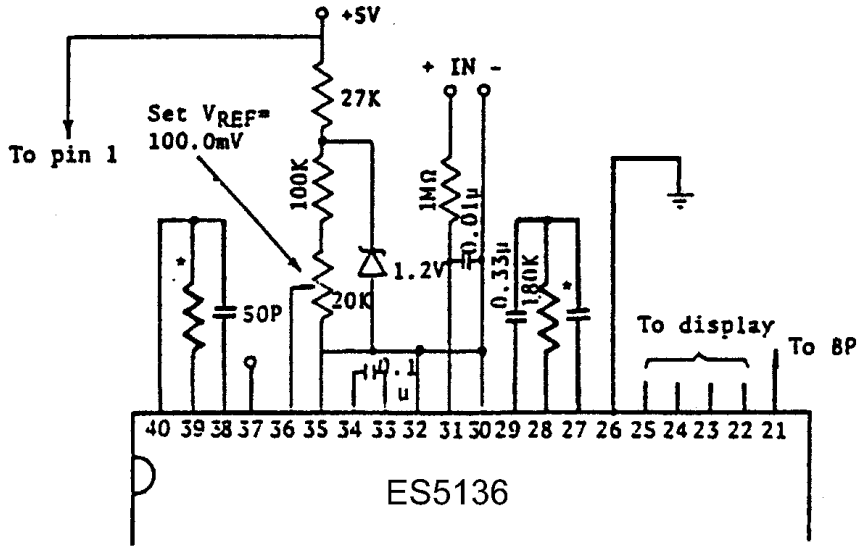


Figure 8 : Single +5V power supply, using 1.2V band gap external reference.

* : Values depend on clock frequency.

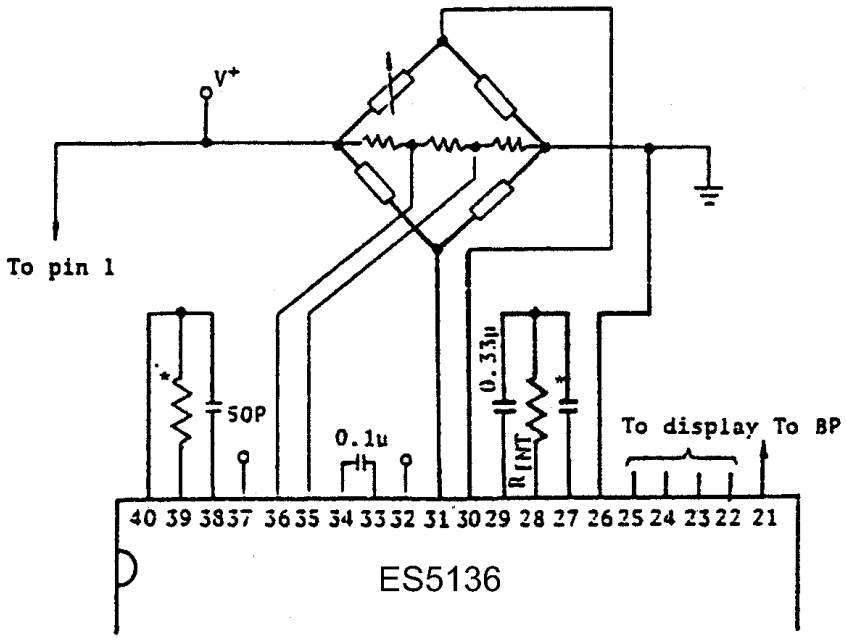


Figure 9 : Ratiometric values of Quad Load Cell measurement The resistors within the bridge are determined by the desired sensitivity.

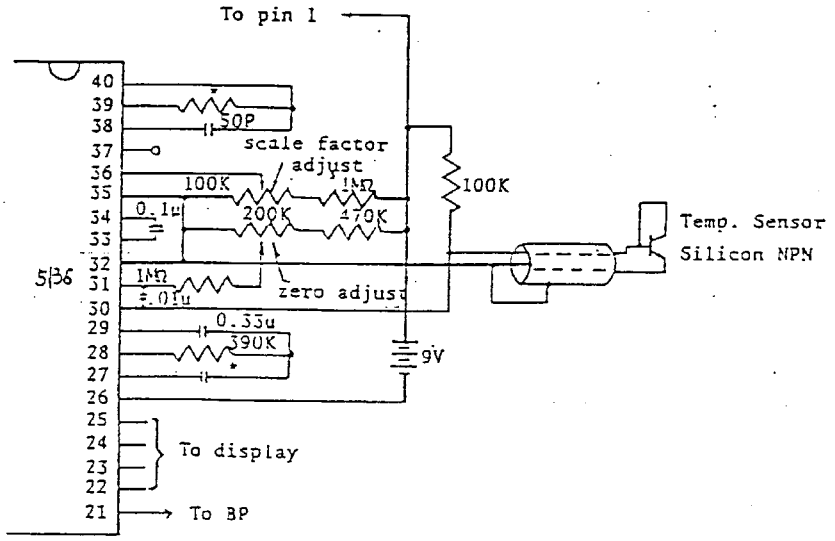


Figure 10 : Digital centigrade thermometer

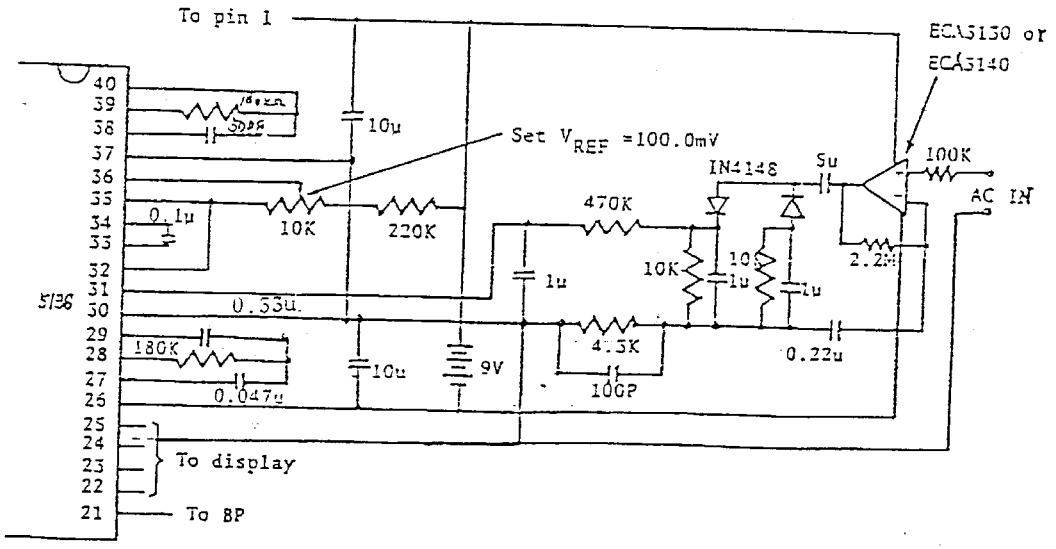
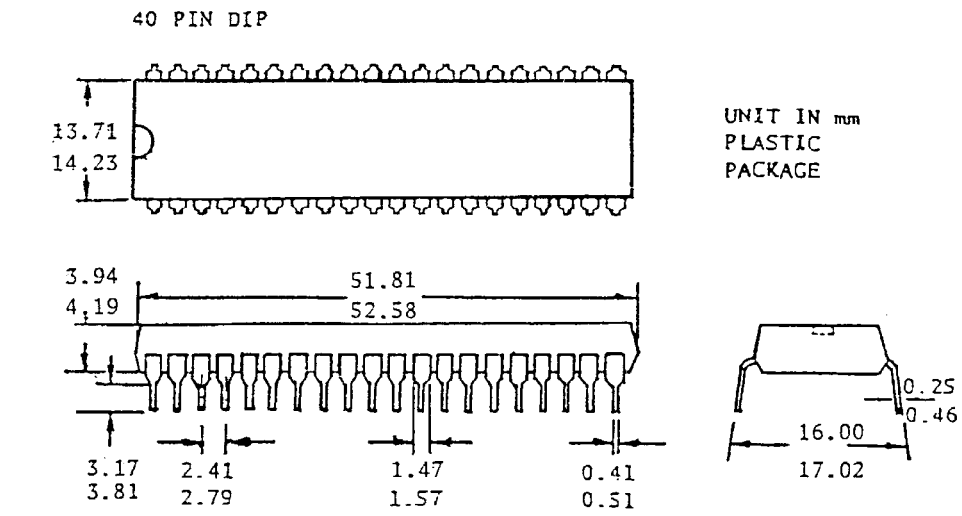


Figure 11 : AC to DC Converter.
TEST is used as a common mode reference level.

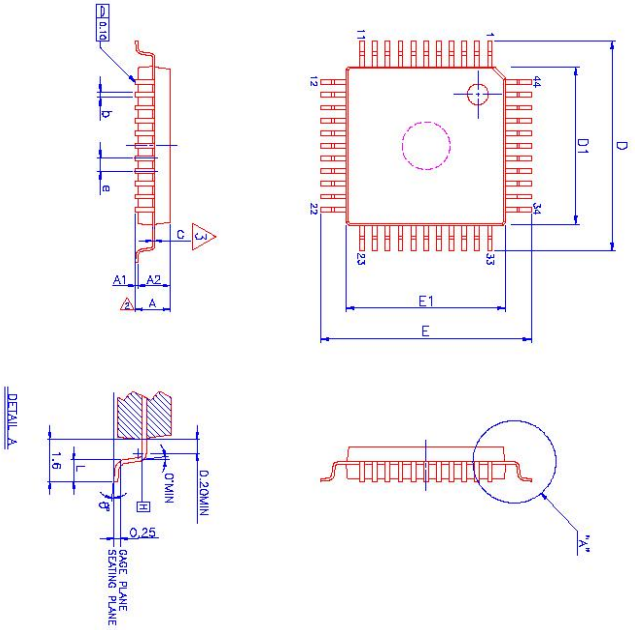
XII、PHYSICAL DIMENSION

XII. PHYSICAL DIMENSION



XII、PHYSICAL DIMENSION

44 pins QFP package size



SYMBOLS	MIN.	NOM	MAX.
A	–	–	2.7
A1	0.25	0.30	0.35
3 A2	1.9	2.0	2.2
b		0.3 (TYP.)	
D	13.00	13.20	13.40
D1	9.9	10.00	10.10
E	13.00	13.20	13.40
E1	9.9	10.00	10.10
L	0.73	0.88	0.93
e		0.80 (TYP.)	
θ°	0	–	7
3 C	0.1	0.15	0.2

UNIT : mm

NOTES:

1.JEDEC OUTLINE:MO-108 AA-1

2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.