ESS Technology, Inc.

ES6461 / ES6460
DMPX Digital Media Processor
Datasheet

OVERVIEW

The ***DMPX*** series is a 4th generation Digital Picture Frame and HDD Media Player solution built upon ESS's highly popular DMP3 (ES6430), DMP2 (ES6425) and DMP1 (ES6420) processors.

P/N	Description	Package	Core Function	HS USB 2.0 OTG	Digital TCON / HDMI	CF / IDE / MPEG1/2	AC3
ES6460SAA	*DMPX Premier*	128-LQFP	Analog TCON RTC MPEG4 / JPEG MP3 Card Reader	1	NA	NA	NA
ES6461SAA	*DMPX Reference*	176-LPFP		2	24-bit TCON or 1080p upscaler with HDMI (ES7108)	√	
ES6461SAB	*DMPX Reference w/ Dolby*						√

The ***DMPX*** has a versatile card reader interface for direct connection to CF/MicroDrive, SD, MMC, MS/MS Pro, xD, SM, and IDE hard drives. In addition, HS USB 2.0 host/device interfaces are included for connection to PC, thumb drive, USB hard drives and cameras. The built-in A/V decoder supports MPEG 1/2/4, JPEG and MP3 formats with numerous other options including Dolby AC3 and WMA.

The ***DMPX*** further integrates the TCON, RTC, DC/DC PWM and NAND Flash controllers to make it the most integrated solution for Digital Picture Frame products. In addition, the boot from NAND Flash feature allows additional system cost savings by eliminating the SPI flash.

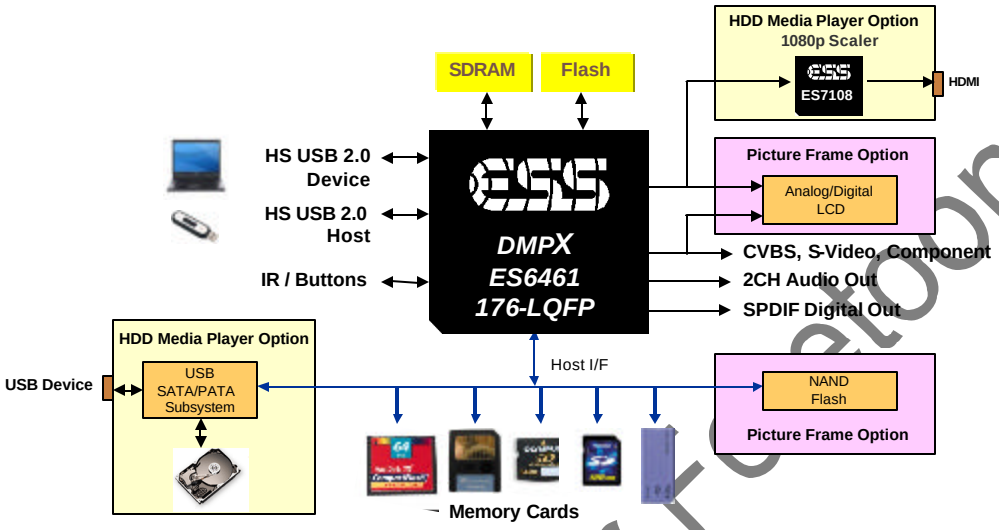
The ***DMPX*** ES6461 can work with the companion ES7108 Video Scaler/HDMI transmitter to upscale any standard definition (480i/p) video to full 1080p high definition output needed for the emerging HDD Media Player products.

KEY FEATURES

Feature	Benefit
Audio/Video	
• 4ch Video DAC	• Analog LCD or CVBS / S / Component / VGA / SCART
• 8/12-bit Digital Video Out	• Digital LCD or HDMI (with ES7108) output
• Stereo Audio DAC	• Eliminate external audio DAC
System & Peripheral	
• 32kB RISC cache	• Increase JPEG decoding speed
• TCON	• Eliminate external TCON for LCD control
• RTC	• Eliminate external RTC for clock / calendar
• NAND Flash Boot	• Reduce cost by eliminating SPI flash
• DC/DC PWM	• Reduce cost for LCD VGH/VGL and backlight generation
• HS USB 2.0 OTG	• Connect USB thumb-drives, cameras or PC
• Card Reader	• Read/write SM, xD, SD, MMC, MS/MS Pro
• IDE port	• Connect to CF / MD / hard drives or network controllers
Media Playback	
• MPEG 1/2/4 decoder	• Display MPEG-4 AVI, DVD or VCD video files
• JPEG/MP3 decoder	• Display pictures and music slideshows
• WMA/AC3 option	• Playback WMA/AC3 audio

APPLICATIONS

- Digital Picture Frames
- HDD Media Player
- Digital Signage Media Player
- Embedded TV Media Player



DEVELOPMENT KIT

Two development kits are available

- ***DMPX*** ES6461 HDD Media Player or Digital Picture Frame reference design
- ***DMPX*** ES6460 Digital Picture Frame reference design

Each development kit comes with a complete set of tools:

- Data sheet and schematics
- User Interface software source code
- ROM emulator for code development

Additionally ESS provides FAE support for:

- Customer prototype design
- Firmware customization

LICENSING REQUIREMENTS

Depending on the features desired, you may be required to apply and obtain a license with the organizations shown below. Per-chip royalties may be required and are to be paid by the purchaser with the respective organizations.

WMA:

Details on licensing or membership can be obtained at http://www.microsoft.com

MPEG-2/MPEG-4:

Details on licensing or membership can be obtained at http://www.mpegla.com

Dolby:

Details on licensing or membership can be obtained at http://www.dolby.com

AAC MPEG-2/MPEG-4:

Details on licensing or membership can be obtained at http://www.vialicensing.com

MP3:

Details on licensing or membership can be obtained at http://www.mp3licensing.com

SD:

Details on licensing or membership can be obtained at http://www.sdcard.org

Memory Stick:

Details on licensing or membership can be obtained at http://www.memorystick.org

MultiMediaCard:

Details on licensing or membership can be obtained at http://www.mmca.org

Compact Flash:

Details on licensing or membership can be obtained at http://www.compactflash.org

xD-Picture Card:

Details on licensing or membership can be obtained at http://www.xd-picture.com

SmartMedia:

Details on licensing or membership can be obtained at http://www.ssfdc.or.jp

ADDITIONAL LICENSING REQUIREMENTS

Dolby Digital Licensing

Dolby Digital audio enabling software is provided with the DMPX series of DMP processors. Dolby is a trademark of the Dolby Laboratories. Supply of this implementation of Dolby Technology does not convey a license or imply a right under any patent, or any other Industrial or Intellectual Property Right of Dolby Laboratories, to use this implementation in any end-user or ready-to-use final product. Companies planning to use this implementation in products must obtain a license from Dolby Laboratories Licensing Corporation before designing such products. Additional per-chip royalties may be required and are to be paid by the purchaser to Dolby Laboratories, Inc. Details of the OEM Dolby Digital license may be obtained by writing to:

Dolby Laboratories, Inc.
Dolby Laboratories Licensing Corporation
Attn.: Intellectual Property Manager
100 Potrero Avenue
San Francisco, CA 94103-4813
http://www.dolby.com

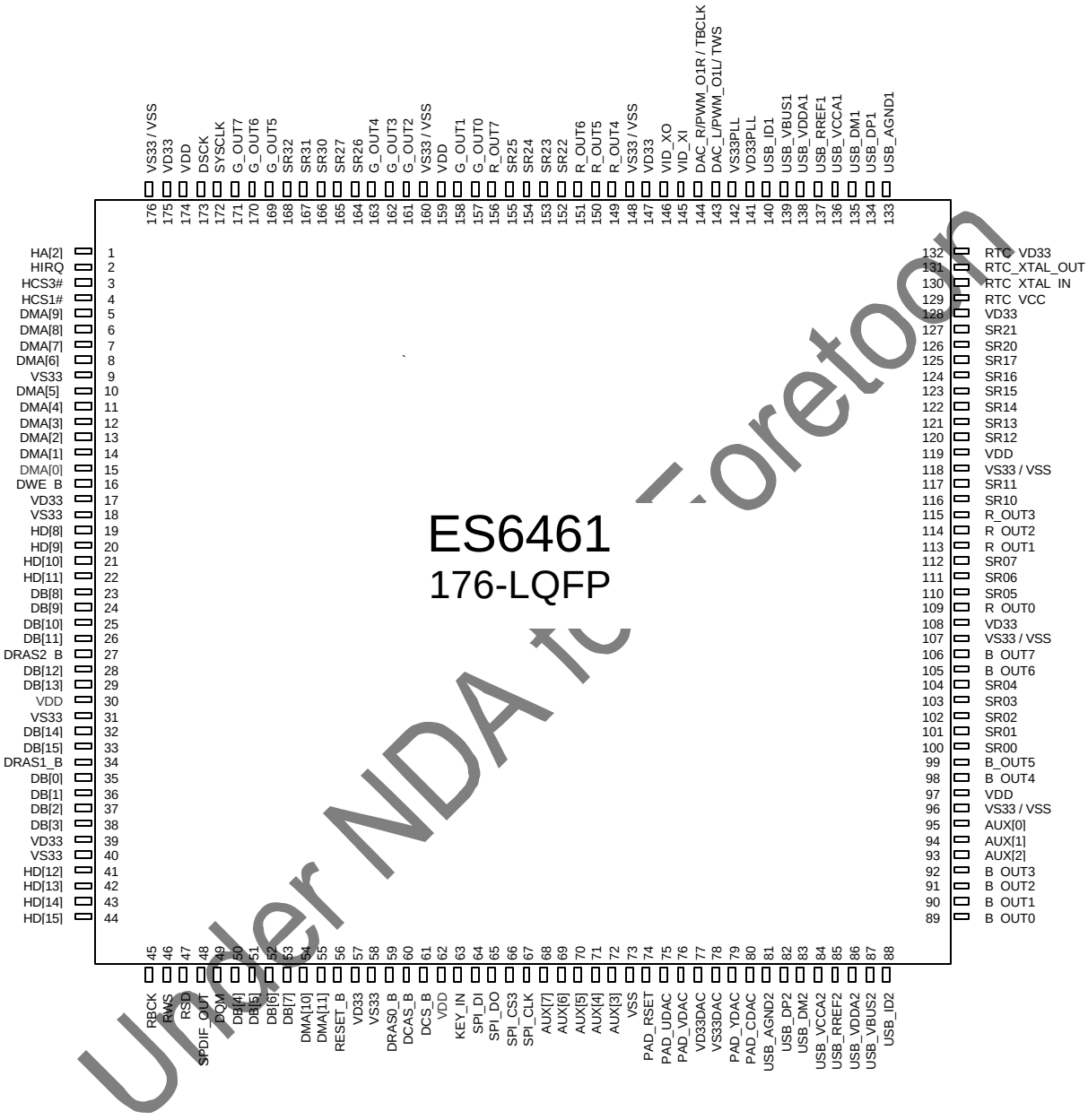
MPEG-4 and WMA Notification

System manufacturers need to obtain a license for MPEG-4 decode from MPEG-LA for MPEG-4 parts. Optionally, this device requires system manufacturers to obtain a license for Windows Media Audio from Microsoft in order to support the decoding of WMA content.

MPEG-LA
4601 Willard Avenue, Suite 200
Chevy Chase, MD 20815
http://www.mpegla.com

Microsoft Corporation
Digital Media Division
One Microsoft Way
Redmond, WA 98052-6399
http://www.microsoft.com

ES6461 PIN-OUT



ES6461 PIN DESCRIPTION

ES6461 PIN #	NAME	Pin Description	Type
1	HA[2]	Host control / GPIO101	HOST
2	HIRQ	Host control / GPIO102	HOST
3	HCS3#	Host control / GPIO103	HOST
4	HCS1#	Host control / GPIO104	HOST
5	DMA[9]	DRAM address bus / VDACTEST_IN	DRAM
6	DMA[8]	DRAM address bus / VDACTEST_IN	DRAM
7	DMA[7]	DRAM address bus / VDACTEST_IN	DRAM
8	DMA[6]	DRAM address bus / VDACTEST_IN	DRAM
9	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
10	DMA[5]	DRAM address bus / VDACTEST_IN	DRAM
11	DMA[4]	DRAM address bus / VDACTEST_IN	DRAM
12	DMA[3]	DRAM address bus / VDACTEST_IN	DRAM
13	DMA[2]	DRAM address bus / VDACTEST_IN	DRAM
14	DMA[1]	DRAM address bus / VDACTEST_IN	DRAM
15	DMA[0]	DRAM address bus / VDACTEST_IN	DRAM
16	DWE_B	DRAM Write Enable; For External Bonding / PLL_SEL[1]	DRAM
17	VD33	3.3V power supply	P3.3V
18	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
19	HD[8]	Host data / GPIO70	HOST
20	HD[9]	Host data / GPIO71	HOST
21	HD[10]	Host data /GPIO72	HOST
22	HD[11]	Host data / GPIO73	HOST
23	DB[8]	DRAM data bus	DRAM
24	DB[9]	DRAM data bus	DRAM
25	DB[10]	DRAM data bus	DRAM
26	DB[11]	DRAM data bus	DRAM
27	DRAS2_B	SDRAM Bank Select 1 / GPIO83 / Debug Mode (strap)	DRAM
28	DB[12]	DRAM data bus	DRAM
29	DB[13]	DRAM data bus	DRAM
30	VDD	1.2V power supply	P1.2V
31	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
32	DB[14]	DRAM data bus	DRAM
33	DB[15]	DRAM data bus	DRAM
34	DRAS1_B	SDRAM Bank Select 0 / GPIO84 /Booting (strap)	DRAM
35	DB[0]	DRAM data bus	DRAM
36	DB[1]	DRAM data bus	DRAM
37	DB[2]	DRAM data bus	DRAM
38	DB[3]	DRAM data bus	DRAM
39	VD33	3.3V power supply	P3.3V
40	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
41	HD[12]	Host data / GPIO74	HOST

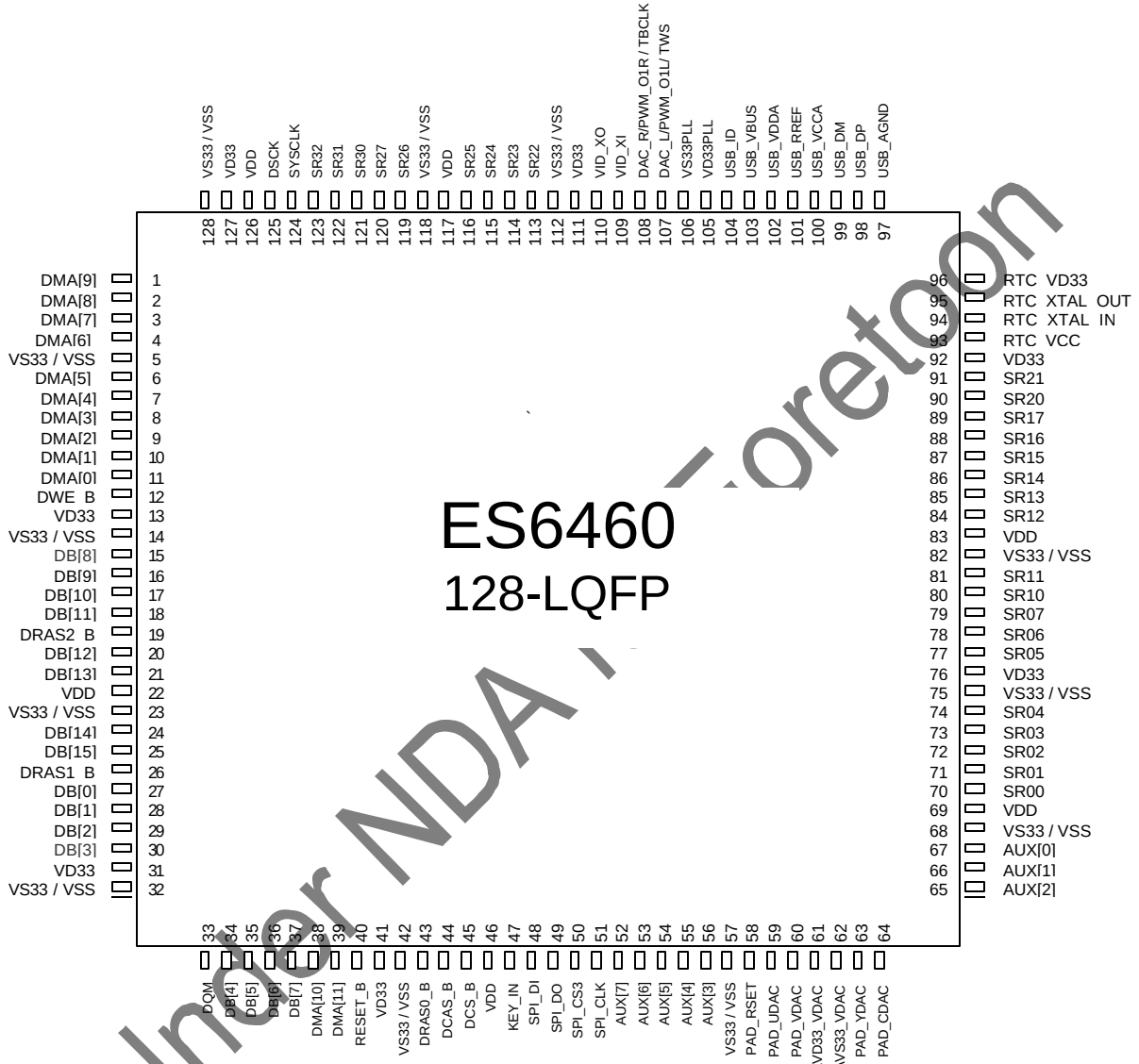
ES6461 PIN #	NAME	Pin Description	Type
42	HD[13]	Host data / GPIO75	HOST
43	HD[14]	Host data / GPIO76	HOST
44	HD[15]	Host data / GPIO77	HOST
45	RBCK	Digital audio / TDMCLK / GPI80	AUDIO
46	RWS	Digital audio / TDMFS / GPI81	AUDIO
47	RSD	Digital audio / TDMDR / GPI82	AUDIO
48	SPDIF_OUT	SPDIF OUT / D-REV	AUDIO
49	DQM	DRAM write control / PLL_SEL[0]	DRAM
50	DB[4]	DRAM data bus	DRAM
51	DB[5]	DRAM data bus	DRAM
52	DB[6]	DRAM data bus	DRAM
53	DB[7]	DRAM data bus	DRAM
54	DMA[10]	DRAM address bus / VDACTEST_IN	DRAM
55	DMA[11]	DRAM address bus / VDACTEST_IN	DRAM
56	RESET_B	Chip Reset (active low)	SYS
57	VD33	3.3V power supply	P3.3V
58	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
59	DRAS0_B	DRAM address bus / PLL_SEL[2]	DRAM
60	DCAS_B	DRAM address bus / PLL_SEL[3]	DRAM
61	DCS_B	DRAM chip select / GPIO85	DRAM
62	VDD	1.2V power supply	P1.2V
63	KEY_IN	Digital key input	SYS
64	SPI_DI	SPI_DI	SRAM
65	SPI_DO	SPI_DO	SRAM
66	SPI_CS3	SPI_CS3 / Bank3_Sel (strap)	SRAM
67	SPI_CLK	SPI_CLK / Bank3_Serial (strap)	SRAM
68	AUX[7]	Original AUX[7] / XD_CS# / SM_CS# / GPIO105	AUX
69	AUX[6]	Original AUX[6] / GPIO106 / HRST#	AUX
70	AUX[5]	Original AUX[5] / SPI_CS2/ MUTE / GPIO37 / NAND_CS#	AUX
71	AUX[4]	Original AUX[4] / IR	AUX
72	AUX[3]	Original AUX[3] / SM_CD# / SOUT / GPIO34 / DrvVbus1	AUX
73	VSS	1.2V Ground supply	G1.2V
	VSS3	3.3V Ground supply	G3.3V
74	PAD_RSET	VDAC Current Adjustment Resistor Input/ GPIO 94	VDAC
75	PAD_UDAC	UDAC / A-VB / GPIO90 / A-VR	VDAC
76	PAD_VDAC	VDAC / CVBS / GPIO96 / CVBS	VDAC
77	VD33DAC	3.3V power supply (for VDAC)	PA3.3V
78	VS33DAC	Ground (for VDAC)	GA3.3V
79	PAD_YDAC	YDAC / A-VG / GPIO95 / A-VG	VDAC
80	PAD_CDAC	CDAC / A-VR / GPIO92 / A-VB	VDAC
81	USB_AGND2	Analog ground for USB 2	USB
82	USB_DP2	Analog USB 2 signal 0 (plus)	USB
83	USB_DM2	Analog USB 2 signal 0 (minus)	USB
84	USB_VCCA2	Analog power +3.3V for USB 2	USB
85	USB_RREF2	Analog USB 2 external reference	USB
86	USB_VDDA2	Analog USB 2 power for regulator	USB
87	USB_VBUS2	Analog USB 2 VBUS pin	USB

ES6461 PIN #	NAME	Pin Description	Type
88	USB_ID2	Analog USB 2 ID pin	USB
89	B_OUT0	Blu panel data (8ma) /GPIO50 /YUV0 /HDMI_D[0]	TCON
90	B_OUT1	Blu panel data (8ma) /GPIO51 /YUV1 /HDMI_D[1]	TCON
91	B_OUT2	Blu panel data (8ma) /GPIO52 /YUV2/ HDMI_D[2]	TCON
92	B_OUT3	Blu panel data (8ma) /GPIO53 /YUV3 / HDMI_D[3]	TCON
93	AUX[2]	Original AUX[2] / XD_CD# / SIN / GPIO33 / DrvVbus2	AUX
94	AUX[1]	Original AUX[1] / I2C-CLK	AUX
95	AUX[0]	Original AUX[0] / I2C-DATA	AUX
96	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
97	VDD	1.2V power supply	P1.2V
98	B_OUT4	Blu panel data (8ma) /GPIO54 /YUV4 / HDMI_D[4]	TCON
99	B_OUT5	Blu panel data (8ma) /GPIO55 /YUV5/ HDMI_D[5]	TCON
100	SR00	GPIO00 / HD[0] / MS_D[0] / SD_D[0] / XD_D[0] / SM_D[0] / NAND_D[0]	GPIO
101	SR01	GPIO01 / HD[1] / MS_D[1] / SD_D[1] / XD_D[1] / SM_D[1] / NAND_D[1]	GPIO
102	SR02	GPIO02 / HD[2] / MS_D[2] / SD_D[2] / XD_D[2] / SM_D[2] / NAND_D[2]	GPIO
103	SR03	GPIO03 / HD[3] / MS_D[3] / SD_D[3] / XD_D[3] / SM_D[3] / NAND_D[3]	GPIO
104	SR04	GPIO04 / HD[4] / XD_D[4] / SM_D[4] / NAND_D[4]	GPIO
105	B_OUT6	Blu panel data (8ma) /GPIO56 /YUV6 / HDMI_D[6]	TCON
106	B_OUT7	Blu panel data (8ma) /GPIO57 /YUV7 / HDMI_D[7]	TCON
107	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
108	VD33	3.3V power supply	P3.3V
109	R_OUT0	Red panel data (8ma) /GPIO40 /CAMIN0 /HDMI_D[8]	TCON
110	SR05	GPIO05 / HD[5] / XD_D[5] / SM_D[5] / NAND_D[5]	GPIO
111	SR06	GPIO06 / HD[6] / XD_D[6] / SM_D[6] / NAND_D[6]	GPIO
112	SR07	GPIO07 / HD[7] / XD_D[7] / SM_D[7] / NAND_D[7]	GPIO
113	R_OUT1	Red panel data (8ma) /GPIO41 /CAMIN1 / HDMI_D[9]	TCON
114	R_OUT2	Red panel data (8ma) /GPIO42 /CAMIN2 / HDMI_D[10]	TCON
115	R_OUT3	Red panel data (8ma) /GPIO43 /CAMIN3 /HDMI_D[11]	TCON
116	SR10	GPIO10 / HD[8] / MSBS / SDCMD	GPIO
117	SR11	GPIO11 / HD[9] / MSCLK / SDCLK	GPIO

ES6461 PIN #	NAME	Pin Description	Type
118	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
119	VDD	1.2V power supply	P1.2V
120	SR12	GPIO12 / HD[10] / SD_CD# / PWM_VGL (8ma)	GPIO
121	SR13	GPIO13 / HD[11] / MS_CD# / PWM_VGH (8ma)	GPIO
122	SR14	GPIO14 / HD[12] / A-CPH2 / D-LD (8ma)	GPIO
123	SR15	GPIO15 / HD[13] / A-CPH3 / D-POL (8ma)	GPIO
124	SR16	GPIO16 / HD[14] / A-VCOM / D-CKH (8ma)	GPIO
125	SR17	GPIO17 / HD[15] / A-CKV / D-CKV (8ma)	GPIO
126	SR20	GPIO20 / HIOCS16# / PWM_VLED (8ma)	GPIO
127	SR21	GPIO21 / HIORDY / NAND_RDY / XD_RDY / SM_RDY	GPIO
128	VD33	3.3V power supply	P3.3V
129	RTC_VCC	RTC 1.2V	RTC
130	RTC_XTAL_IN	RTC 32KHz crystal osc in	RTC
131	RTC_XTAL_OUT	RTC 32KHz crystal osc out	RTC
132	RTC_VD33	RTC battery in	RTC
133	USB_AGND1	Analog ground for USB 1	USB
134	USB_DP1	Analog USB 1 signal 0 (plus)	USB
135	USB_DM1	Analog USB 1 signal 0 (minus)	USB
136	USB_VCCA1	Analog power +3.3V for USB 1	USB
137	USB_RREF1	Analog USB 1 external reference	USB
138	USB_VDDA1	Analog USB 1 power for regulator	USB
139	USB_VBUS1	Analog USB 1 VBUS pin	USB
140	USB_ID1	Analog USB 1 ID pin	USB
141	VD33PLL	3.3V power supply (for PLL)	PA3.3V
142	VS33PLL	3.3V ground supply (for PLL)	GA3.3V
143	DAC_L/PWM_O1L/ TWS	Audio Transmit Frame Sync / Audio hyperstream out / GPIO35	AUDOUT
144	DAC_R/PWM_O1R / TBCLK	Audio Transmit Bit Clock/ Audio hyperstream out / GPIO36	AUDOUT
145	VID_XI	Crystal input	CLK
146	VID_XO	Crystal output	CLK
147	VD33	3.3V power supply	P3.3V
148	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
149	R_OUT4	Red panel data (8ma) / GPIO44 / CAMIN4 / HDMI_ACTIVE	TCON
150	R_OUT5	Red panel data (8ma) / GPIO45 / CAMIN5 / HDMI_HSYNC	TCON
151	R_OUT6	Red panel data (8ma) / GPIO46 / CAMIN6 / HDMI_VSYNC	TCON
152	SR22	GPIO22 / HWR# / XD_WR# / SM_WR# / NAND_WR#	GPIO
153	SR23	GPIO23 / HRD# / XD_RD# / SM_RD# / NAND_RD#	GPIO
154	SR24	GPIO24 / HA[0] / XD_CLE / SM_CLE / NAND_CLE	GPIO
155	SR25	GPIO25 / HA[1] / XD_ALE / SM_ALE / NAND_ALE	GPIO
156	R_OUT7	Red panel data (8ma) / GPIO47 / CAMIN7 /	TCON

ES6461 PIN #	NAME	Pin Description	Type
		TSD3	
157	G_OUT0	Grn panel data (8ma) / GPIO60 / TSD0	TCON
158	G_OUT1	Grn panel data (8ma) / GPIO61 / TSD1	TCON
159	VDD	1.2V power supply	P1.2V
160	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
161	G_OUT2	Grn panel data (8ma) / GPIO62 / TSD2	TCON
162	G_OUT3	Grn panel data (8ma) / GPIO63 / MCLK	TCON
163	G_OUT4	Grn panel data (8ma) / GPIO64 / TBCK	TCON
164	SR26	GPIO26 / HA[2] / A-CPH1 / D-PCLK0 (8ma)	GPIO
165	SR27	GPIO27 / HIRQ / A-STH / D-STH (8ma)	GPIO
166	SR30	GPIO30 / HCS3# / A-STV / D-STV (8ma)	GPIO
167	SR31	GPIO31 / HCS1# / A-OEH / D-OEH (8ma)	GPIO
168	SR32	GPIO32 / HRST# / A-OEV / D-OEV (8ma)	GPIO
169	G_OUT5	Grn panel data (8ma) / GPIO65 / TWS	TCON
170	G_OUT6	Grn panel data (8ma) / GPIO66 / YUV_CLK	TCON
171	G_OUT7	Grn panel data (8ma) / GPIO67 / CAM_CLK	TCON
172	SYSCLK	System PLL bypass clock	AUX
173	DSCK	DRAM Clock	DRAM
174	VDD	1.2V power supply	P1.2V
175	VD33	3.3V power supply	P3.3V
176	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V

ES6460 PIN-OUT



ES6460 PIN DESCRIPTION

ES6460 PIN #	NAME	Pin Description	Type
1	DMA[9]	DRAM address bus / VDACTEST_IN	DRAM
2	DMA[8]	DRAM address bus / VDACTEST_IN	DRAM
3	DMA[7]	DRAM address bus / VDACTEST_IN	DRAM
4	DMA[6]	DRAM address bus / VDACTEST_IN	DRAM
5	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
6	DMA[5]	DRAM address bus / VDACTEST_IN	DRAM
7	DMA[4]	DRAM address bus / VDACTEST_IN	DRAM
8	DMA[3]	DRAM address bus / VDACTEST_IN	DRAM
9	DMA[2]	DRAM address bus / VDACTEST_IN	DRAM
10	DMA[1]	DRAM address bus / VDACTEST_IN	DRAM
11	DMA[0]	DRAM address bus / VDACTEST_IN	DRAM
12	DWE_B	DRAM Write Enable; For External Bonding / PLL_SEL[1]	DRAM
13	VD33	3.3V power supply	P3.3V
14	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
15	DB[8]	DRAM data bus	DRAM
16	DB[9]	DRAM data bus	DRAM
17	DB[10]	DRAM data bus	DRAM
18	DB[11]	DRAM data bus	DRAM
19	DRAS2_B	SDRAM Bank Select 1 / GPIO83 / Debug_Mode (strap)	DRAM
20	DB[12]	DRAM data bus	DRAM
21	DB[13]	DRAM data bus	DRAM
22	VDD	1.2V power supply	P1.2V
23	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
24	DB[14]	DRAM data bus	DRAM
25	DB[15]	DRAM data bus	DRAM
26	DRAS1_B	SDRAM Bank Select 0 / GPIO84 /Boot_Int (strap)	DRAM
27	DB[0]	DRAM data bus	DRAM
28	DB[1]	DRAM data bus	DRAM
29	DB[2]	DRAM data bus	DRAM
30	DB[3]	DRAM data bus	DRAM
31	VD33	3.3V power supply	P3.3V
32	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
33	DQM	DRAM write control / PLL_SEL[0]	DRAM
34	DB[4]	DRAM data bus	DRAM
35	DB[5]	DRAM data bus	DRAM
36	DB[6]	DRAM data bus	DRAM
37	DB[7]	DRAM data bus	DRAM
38	DMA[10]	DRAM address bus / VDACTEST_IN	DRAM
39	DMA[11]	DRAM address bus / VDACTEST_IN	DRAM
40	RESET_B	Chip Reset (active low)	SYS
41	VD33	3.3V power supply	P3.3V

ES6460 PIN #	NAME	Pin Description	Type
42	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
43	DRAS0_B	DRAM address bus / PLL_SEL[2]	DRAM
44	DCAS_B	DRAM address bus / PLL_SEL[3]	DRAM
45	DCS_B	DRAM chip select / GPIO85	DRAM
46	VDD	1.2V power supply	P1.2V
47	KEY_IN	Digital key input	SYS
48	SPI_DI	SPI_DI	SRAM
49	SPI_DO	SPI_DO	SRAM
50	SPI_CS3	SPI_CS3 / Bank3_Sel (strap)	SRAM
51	SPI_CLK	SPI_CLK / Bank3_Serial (strap)	SRAM
52	AUX[7]	Original AUX[7] / XD_CS# / SM_CS# /GPIO105	AUX
53	AUX[6]	Original AUX[6] / SD_WP# / SM_WP_OUT# / XD_WP# / GPIO106 / HRST#	AUX
54	AUX[5]	Original AUX[5] / SPI_CS2/ MUTE / GPIO37 / NAND_CS#	AUX
55	AUX[4]	Original AUX[4] / IR	AUX
56	AUX[3]	Original AUX[3] / SM_CD# / SOUT / GPIO34 / DrvVbus1	AUX
57	VSS	1.2V Ground supply	G1.2V
	VSS3	3.3V Ground supply	G3.3V
58	PAD_RSET	VDAC Current Adjustment Resistor Input/ GPIO 94	VDAC
59	PAD_UDAC	UDAC / A-VB / GPIO90 / A-VR	VDAC
60	PAD_VDAC	VDAC / CVBS / GPIO96 / CVBS	VDAC
61	AVD33_VDAC	3.3V power supply (for VDAC)	PA3.3V
62	AVS33_VDAC	Ground (for VDAC)	GA3.3V
63	PAD_YDAC	YDAC / A-VG / GPIO95 / A-VG	VDAC
64	PAD_CDAC	CDAC / A-VR / GPIO92 / A-VB	VDAC
65	AUX[2]	Original AUX[2] / XD_CD# / SIN / GPIO33 / DrvVbus2	AUX
66	AUX[1]	Original AUX[1] / I2C-CLK	AUX
67	AUX[0]	Original AUX[0] / I2C-DATA	AUX
68	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
69	VDD	1.2V power supply	P1.2V
70	SR00	GPIO00 / HD[0] / MS_D[0] / SD_D[0] / XD_D[0] / SM_D[0] / NAND_D[0]	GPIO
71	SR01	GPIO01 / HD[1] / MS_D[1] / SD_D[1] / XD_D[1] / SM_D[1] / NAND_D[1]	GPIO
72	SR02	GPIO02 / HD[2] / MS_D[2] / SD_D[2] / XD_D[2] / SM_D[2] / NAND_D[2]	GPIO
73	SR03	GPIO03 / HD[3] / MS_D[3] / SD_D[3] / XD_D[3] / SM_D[3] / NAND_D[3]	GPIO
74	SR04	GPIO04 / HD[4] / XD_D[4] / SM_D[4] / NAND_D[4]	GPIO
75	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
76	VD33	3.3V power supply	P3.3V
77	SR05	GPIO05 / HD[5] / XD_D[5] / SM_D[5] / NAND_D[5]	GPIO
78	SR06	GPIO06 / HD[6] / XD_D[6] / SM_D[6] / NAND_D[6]	GPIO
79	SR07	GPIO07 / HD[7] / XD_D[7] / SM_D[7] / NAND_D[7]	GPIO
80	SR10	GPIO10 / MSBS / SDCMD	GPIO

ES6460 PIN #	NAME	Pin Description	Type
81	SR11	GPIO11 / MSCLK / SDCLK	GPIO
82	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
83	VDD	1.2V power supply	P1.2V
84	SR12	GPIO12 / SD_CD# / PWM_VGL (8ma)	GPIO
85	SR13	GPIO13 / MS_CD# / PWM_VGH (8ma)	GPIO
86	SR14	GPIO14 / A-CPH2 (8ma)	GPIO
87	SR15	GPIO15 / A-CPH3 (8ma)	GPIO
88	SR16	GPIO16 / A-VCOM (po-analog, 8ma)	GPIO
89	SR17	GPIO17 / A-CKV (8ma)	GPIO
90	SR20	GPIO20 / HIOCS16# / PWM_VLED (8ma)	GPIO
91	SR21	GPIO21 / HIORDY / NAND_RDY / XD_RDY / SM_RDY	GPIO
92	VD33	3.3V power supply	P3.3V
93	RTC_VCC	RTC 1.2V	RTC
94	RTC_XTAL_IN	RTC 32KHz crystal osc in	RTC
95	RTC_XTAL_OUT	RTC 32KHz crystal osc out	RTC
96	RTC_VD33	RTC battery in	RTC
97	USB_AGND	Analog ground for USB	USB
98	USB_DP	Analog USB signal 0 (plus)	USB
99	USB_DM	Analog USB signal 0 (minus)	USB
100	USB_VCCA	Analog power +3.3V for USB	USB
101	USB_RREF	Analog USB external reference	USB
102	USB_VDDA	Analog USB power for regulator	USB
103	USB_VBUS	Analog USB VBUS pin	USB
104	USB_ID	Analog USB ID pin	USB
105	VD33PLL	3.3V power supply (for PLL)	PA3.3V
106	VS33PLL	3.3V ground supply (for PLL)	GA3.3V
107	DAC_L/PWM_O1L/ TWS	Audio Transmit Frame Sync / Audio hyperstream out / GPIO35	AUDOUT
108	DAC_R/PWM_O1R / TBCLK	Audio Transmit Bit Clock/ Audio hyperstream out / GPIO36	AUDOUT
109	VID_XI	Crystal input	SYS
110	VID_XO	Crystal output	SYS
111	VD33	3.3V power supply	P3.3V
112	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
113	SR22	GPIO22 / HWR# / XD_WR# / SM_WR# / NAND_WR#	GPIO
114	SR23	GPIO23 / HRD# / XD_RD# / SM_RD# / NAND_RD#	GPIO
115	SR24	GPIO24 / HA[0] / XD_CLE / SM_CLE / NAND_CLE	GPIO
116	SR25	GPIO25 / HA[1] / XD_ALE / SM_ALE / NAND_ALE	GPIO
117	VDD	1.2V power supply	P1.2V
118	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V
119	SR26	GPIO26 / HA[2] / A-CPH1 (pol digital, 8ma)	GPIO
120	SR27	GPIO27 / A-STH (8ma)	GPIO
121	SR30	GPIO30 / HCS3# / A-STV (8ma)	GPIO
122	SR31	GPIO31 / A-OEH (8ma)	GPIO
123	SR32	GPIO32 / HRST# / A-OEV (8ma)	GPIO
124	SYSCLK	System PLL bypass clock	SYS
125	DSCK	DRAM Clock	DRAM

ES6460 PIN #	NAME	Pin Description	Type
126	VDD	1.2V power supply	P1.2V
127	VD33	3.3V power supply	P3.3V
128	VS33	3.3V Ground supply	G3.3V
	VSS	1.2V Ground supply	G1.2V

FUNCTIONAL DESCRIPTION

DMPX Device Architecture

The DMPX device architecture is comprised of an USB2.0 OTG controller, Analog/Digital TCON, PWM power controller, RTC, video encoder, 2-channel audio DAC, and a full-featured DMP processor.

DMP Backend Processor

The DMP processor of the DMPX consists of a RISC processor, two independent CRT controllers, transport stream parser, video encoder, dedicated SRAM and DRAM DMA controllers, On-Screen Display (OSD) controller, subpicture unit decoder, and video processor.

DMP RISC Processor

Embedded in the DMPX is the 32-bit data pipelined ESS RISC processor, with a combined 32 kb instruction and data cache subsystem. For applications involving an external host processor the communications between a host processor and the DMPX is handled by a host interface module. The host interface can also be used for high speed data input and output.

PMP Operation

The Programmable Multimedia Processor (PMP) core consists of the ESS RISC core and the video processor core. The ESS RISC core and the video processor operate in parallel and have separate data paths and data buses. The data paths and data buses are interconnected by the internal circuitry in the device architecture.

RISC Core

The ESS RISC core can either work alone or with an external DSP to supervise the operation of both the internal SRAM and DRAM DMA controllers. During encoding operations, the ESS RISC core can retrieve compressed video data and weave it with audio data to form an output compressed bit stream if the related DMA controller does not do so. During decoding operations, the ESS RISC core separates and processes the incoming audio and video data from the bit stream.

The ESS RISC core contains in its architecture a program count unit, instruction decode unit, execution unit, and register file.

The program count unit generates an instruction address signal that identifies the location of a 32-bit program instruction. Program instructions, typically load and store instructions, include source and destination information, which are passed on to the instruction decode unit.

The instruction decode unit typically generates specific signals which select their targeted registers in the register file. The decoded instruction has its data sent to the program count unit, where it is incremented to the next data instruction, or, in the case of a branch instruction, changes the data if a branch condition is met.

The execution unit contains a shifter, an arithmetic logic unit, and a multiplier/divider. The execution unit generates signal outputs from the respective data signals found in the register file. These outputs, in turn, are either re-stored in the register file, or asserted as address signals for load and store operations.

Video Processor Core

During decoding operations, the video processor core relies on its software to decompress the video data before storing it in memory. Once the decompressed data has been stored in the memory, the DRAM DMA controller transfers it to the video output interface for final playback to the external video monitor. The ESS RISC processor instruction and data cache subsystem is organized as a two-way set associative. On a cache load-miss and write- miss, the cache lines are allocated into the cache memory.

Cache Line Operation

Before cache line operation, the writeback operation may be performed if the cache content and main memory contents are different. The ESS RISC performs all power management and system configuration functions, as shown in the block diagram in Figure 1 .

The PMP core includes the proprietary Single Instruction, Multiple Data (SIMD) DSP, which can handle four 16-bit- wide data streams. Also included in the device architecture are a screen display controller, a digital video encoder with four DACs, a video input block, video system interfaces, FIFOs and DMA controllers.

The PMP core resource can be accessed only from the ESS RISC core. Together, the ESS RISC and the video processor cores form ESS Technology's field-proven PMP engine.

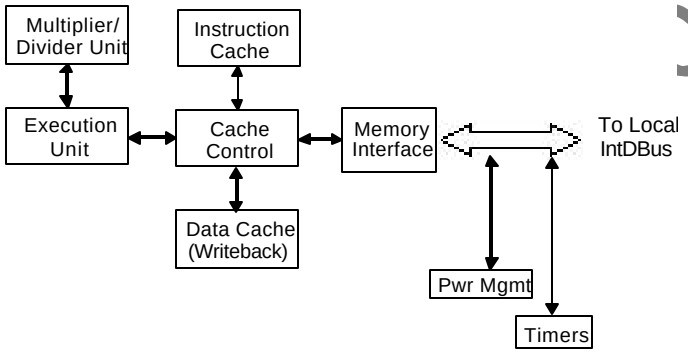


Figure 1 ESS RISC Block Diagram

RISC Interrupts

Twelve events can cause interrupts to the ESS RISC. Each event has a status bit to indicate the occurrence of the event and an enable bit to mask it from interrupting the ESS RISC. Figure 1 lists all of the ESS RISC interrupts and the conditions that cause them.

Table 1 ESS RISC Interrupts

Interrupt	Group	Caused By Condition	How To Clear
Video IRQ	0	Video line number equals value in'videoirq'register	RISC EPROM and SRAM wait states
Timer	0	Timer register wraps from 3FFFFh to 00000h	Writing1 to 'clrirq' register bit 3
BCDW	0	DMA Bus Controller Data is waiting to be read after DBUSREAD command	Reading the 'rlatch' register
Cmd Empty	0	DMA Bus Controller Command Queue goes empty	Writing a command to 'cmdque'
H En Idle	1	Huffman Encoder state machine goes idle	Writing 1 to 'clrirq' register bit 2
H De Idle	1	Huffman Decoder state machine goes idle	Writing 1 to 'clrirq' register bit 1
Data Transfer	1	Either Host-to-RISC Data TRE or RISC-to-Host DW (Host can select)	TRE cleared when RISC reads data; DW cleared when RISC writes data
Block Done	1	After DMA controller has read six blocks of RLAs from VP to DRAM	Write any data to 'clrhmade' register
Cmd Half- Empty	2	DMA Bus Controller Command Queue is less than or equal to half full	Write commands to 'cmdque' so queue becomes over half full
Debug	2	DEBUGIRQ pin goes high	DEBUGIRQ pin goes low
FIFO Level	2	Either Encoder Output FIFO or Decoder Input FIFO reach certain fullness	Writing 1 to bit 8 of 'mipctlreg' register
Host to RISC	2	Host sets Host-to-RISC interrupt bit 7 of 'HostControl0' register (Host address 2)	Writing 1 to bit 0 of 'mipctlreg' register

Command Queue and Video Processor

Command Queue

The command queue module controls the video processor module. The command queue allows the RISC to be decoupled from the video processor module by building a command list of instructions used to control its operation. The command list includes instructions for handling video processor DMA, data transfers, send and receive instructions, and waits to receive the current status of the video processor.

The depth of the command queue is approximately 64 entries. When the command queue is setting up DMAs for the video processor, the command queue automatically writes to DMA channel 0 of the bus controller. The BUSCON_CMDQUE_VPDMASETUP register accepts the video processor DMA access requests being routed to the command queue and prioritizes them in the respective order received.

The incoming commands are always executed in the order they are written to the queue by the RISC.

Both requests for 7-bit vales of delta-Y longwords (DELY[6:0]) and 9-bit values of delta-X scan lines (DELX[8:0]) are processed. The BUSCON_CMDQUE_VPDMAADDR register stores the DMA addresses of the incoming commands so that the command can be decoded when execution takes place.

The BUSCON_CMDQUE_STATUS register constantly monitors the status of the command queue. The command queue of the DMPX receives its DMA inputs from two of the three key bus controller registers.

Video Processor

The video processor consists of a programmable SIMD engine and 2 kb of internal cache memory. The video processor module performs instruction processing for four types of instructions:

- memory instructions
- conditional branch instructions
- compute instructions
- compute immediate instructions

The video processor executes macroblock level tasks, such as predictive coding, motion estimation, and motion compensation. The video processor can also be used for a wide range of time-critical signal processing tasks, including Dolby Digital (AC-3) audio decoding and both video pre-processing and post-processing.

The video processor enables the DMPX to perform arbitrary vertical filtering and scaling of outgoing video. The video processor is controlled by 32-bit and 16-bit wide dual issue micro-instructions. Commonly used microcode subroutines are stored in 8 kB of internal microcode ROM, while less frequently used microcode segments can be downloaded on demand to 2 kB of internal microcode RAM.

DMA Controller

The DMA bus controller is controlled by the video processor and controls multiple DMA channels for the transfer of 32-bit data between:

- video data bus and memory
- video decoder and memory
- ESS RISC and memory
- ESS RISC and video data bus.

Writes from the ESS RISC to the video processor command bus are also performed by the DMA bus controller, along with waits on status readback from the video processor status bus. A separate DMA channel is used for memory refresh. To improve memory bandwidth utilization, internal gateway FIFOs are used extensively. The DMA controller includes two registers in the device architecture that interface directly to the video processor.

The BUSCON_VP_CONTROL register performs all video processor microcode loading and reset. The BUSCON_VP_STAT register provides the status of the internal command queue of the video processor while monitoring the status of all sequencing, data transfers and I/O states.

Transport Stream Parser

The DMPX incorporates a micro-programmable system demultiplexer capable of handling MPEG-1 system stream, MPEG-2 program stream, MPEG-2 transport stream, and other proprietary system multiplexes. The transport mechanism contains a 32-entry packet ID table and satisfies the transport

requirements of the DVB standard.

The transport stream parser performs parsing of all packetized elementary streams (PESs) and selects the destinations for all of the audio and video elements in a given bit stream for processing by the ESS RISC engine. Each PES has a packet ID (PID) table, which includes a 4- bit destination field.

The transport stream parser determines the destination of the elements so that the ESS RISC engine knows where to send the final data output after processing. After processing, the transport stream parser also performs data flushing of all the buffer FIFOs in the device.

Input and Output CRT Controllers

The video output timing of the DMPX is controlled by a pixel clock and the horizontal and vertical sync signals. Pixels are clocked out of the DMPX by the pixel clock. The sync signals determine when the active video data is transferred.

The timing of the active video and sync signals is determined by the two independent CRT controllers inside the DMPX. The input CRT controller is slaved to the timing of CAMCLK from a camera or other video input source.

The input CRT controller uses HSYNCCAM and VSYNCCAM to determine when active video data is transferred. The clock timing of the output CRT controller is independent of the input CRT controller, and can either be internally generated or slaved to another video sync source.

Video MPEG Decoder

The DMP**X** MPEG decoder module performs both MPEG-1 and MPEG-2 decoding. A high-speed Huffman engine decodes MPEG Variable Length Codes (VLCs), using built-in MPEG-1 and MPEG-2 VLC tables. A programmable RAM-based table controls automatic switching from one VLC table to the next.

During decoding, the ESS RISC processor parses the MPEG data all the way to the macro-block level. A special start code search engine is used to locate the next MPEG start code, Macroblock address increments, macroblock modes, and motion vectors, which are encoded in VLC, are read from the Non-Run Length Amplitude (NRLA) FIFO, one of the two FIFOs of the Huffman engine. RLA data that constitutes the DCT coefficients are directly transferred to the SIMD DSP.

The RISC processor then orchestrates the transfer of prediction macro-block data to the SIMD DSP and the execution of various SIMD DSP microcode routines, including de-quantization, inverse DCT, and motion compensation. The resulting reconstructed blocks are transferred under RISC control back to the DRAM frame buffer for subsequent post-processing and display.

NTSC/PAL Video Encoder

The NTSC/PAL video encoder accepts digital linear CCIR656/601 YCbCr at the standard 13.5-MHz pixel data rate. Various color space conversion modes are provided to match the input data to the required output format. The data is then filtered to limit the bandwidth of the signals to within the supported ranges of the selected video standard.

The output of the encoder is fed directly into the output FIFO. The ESS RISC is also capable of writing variable length data into the FIFO in order to insert any non- TCOEFF parts into the bitstream. The RISC writes variable length data to the output FIFO up to 10 bits at a time. Smaller tokens can be written by right justifying fewer bits in the least significant bits of the data field. Since the output FIFO is shared between the ESS RISC and the encoder, the ESS RISC should only write to it when the encoder is idle.

The encoder generates all the necessary synchronization signals for NTSC and PAL standards, which are inserted into the composite and luma outputs. Digital syncs are also provided for the rest of the system.

The encoder also generates the corresponding sub-carrier frequency for color encoding. The encoder generates pixels at both square and nonsquare pixel data rates. This represents a pixel sampling rate of 13.5 MHz for both the NTSC and PAL video data streams.
These measurements assume internal 2x and 4x pixel data rate clock sources. Most of the processing is performed at a 2x pixel rate. The output rate is at a 4x pixel rate, which allows the output filtering to consist of a few passive components.

The encoder is a mixed digital/analog design that incorporates four 12-bit video DACs in the device architecture. This level of video DAC incorporation allows the DMPX to generate composite, luma, and chroma outputs both in Y/C and YUV modes. The S-video luma and chroma outputs are summed internally to generate the composite video output in Y/C mode.

All filtering of the luminance and chrominance signals is performed using DSP techniques. The filters are programmable so that the encoder can provide enhanced bandwidth video for S-video output, but can also provide correctly band-limited signals for composite NTSC/PAL. The sync:white ratio is 40:100 IRE for NTSC, and 43:100 IRE or 34:100 IRE for PAL.

On-Screen Display Controller

The 8-bit On-Screen Display (OSD) controller provides display support for 256 palletized colors in eight degrees of transparency and can occupy the entire viewable area of a display or a portion of the display, depending on the system design. The OSD bitmap, which is stored in the reference memory, is multiplexed into the output video stream before color space conversion is performed.

The DMPX performs its 3-bit blending of the on-screen display information when the LDMD bit (bit 2) of the VID_SCN_OSD_MISC register is set, enabling bits 2:0 of the VID_SCN_OSD_PALETTE registers to establish the desired blending value for the different types of pixel modes required.

The settings of the MODE field (bits 1:0) in the VID_SCN_OSD_MISC register determine the level of blending. Bits 3 of the VID_SCN_OSD_PALETTE registers enable the actual blending when set at 0. Modes 1 (2 bit/pixel), 2 (4 bits/pixel) and 3 (8-bit/pixel) are supported. For mode 3 (8-bit/pixel), the upper four bits of the pixel are the blend information, while the lower four bits of the pixel are the palette index and the blend information in the palette is ignored.

Subpicture Unit Decoder

The Subpicture Unit (SPU) decoder separates and decodes the run-length subpicture pixel data stream and the corresponding subpicture commands that change the color and contrast values of each pixel type for different regions.

The output YUV of the SPU decoder is blended with the main video screen YUV values, depending on the contrast values. The SPU decoder supports four pixel types, coded 00, 01, 10, and 11. Each type represents a color (YUV) and contrast value (blending value with main picture).

The subpicture display area can also be divided into several horizontal stripes, each potentially with a different set of color/contrast values. Each stripe can be divided vertically into a maximum of 9 vertical regions (default 0, and changes 1-8), each region containing its own color/contrast value for each pixel type. In addition, there is a highlight feature that overrides all other color/contrast information for the SPU.

Main subpicture commands, such as SPU on/off, setting the size of the subpicture display area, default color and contrast, and the pointers to the color/contrast and pixel data are done by the ESS RISC engine. The ESS RISC sets the appropriate registers in the SPU, as well as the DMA channel for the command and data FIFOs, based on these commands.

SPU Video Data Framing

The SPU decoder receives its incoming video data in the data framing scheme depicted in Figure 2. During decoding, the incoming SPU data packet is parsed for its pixel data and for its display control sequence information for decompression during video playback. If the last packet received by the SPU decoder is less than 2048 bytes, the packet will be stuffed with extra bytes.

Figure 2 Typical Subpicture Data Framing Format

NTSC Closed Captioning

The DMPX supports the NTSC-compatible Line 21 captioning character set as required by EIA-608 and by FCC Part 15.119. The DMPX displays the caption information during the blanked active line time of Line 21. The DMPX also detects the two-byte codes required by FCC Part 15.119 in the bitstream so that it can recognize the embedded captioning data that would otherwise go undetected during DMP playback.

Line 21 Standard Character Set

The ASCII-based Line 21 character set appearing in Table 2 is the same as the one found in EIA-608 and in FCC Part 15.119.

Table 2 Line 21 Standard Character Set

Code	Symbol	Description
20		space
21	!	exclamation mark
22	“	quotation mark
23	#	number sign or pound sign
24	$	dollar sign
25	%	percent sign
26	&	ampersand
27	‘	apostrophe
28	(	open parenthesis
29	)	close parenthesis
2A	á	lowercase a with acute accent
2B	+	plus sign

2C	,	comma
2D	-	hyphen or minus sign
2E	.	period
2F	/	slash
30	0	zero
31	1	one
32	2	two
33	3	three
34	4	four
35	5	five
36	6	six
37	7	seven
38	8	eight
39	9	nine
3A	:	colon
3B	;	semicolon
3C	<	less-than sign
3D	=	equal sign
3E	>	greater-than sign
3F	?	question mark
40	@	at sign
41	A	uppercase A
42	B	uppercase B
43	C	uppercase C
44	D	uppercase D
45	E	uppercase E
46	F	uppercase F
47	G	uppercase G
48	H	uppercase H
49	I	uppercase I
4A	J	uppercase J
4B	K	uppercase K
4C	L	uppercase L
4D	M	uppercase M
4E	N	uppercase N
4F	O	uppercase O
50	P	uppercase P
51	Q	uppercase Q
52	R	uppercase R
53	S	uppercase S
54	T	uppercase T
55	U	uppercase U
56	V	uppercase V

57	W	uppercase W
58	X	uppercase X
59	Y	uppercase Y
5A	Z	uppercase Z
5B	[	open square bracket
5C	è	lowercase e with acute accent
5D	]	close square bracket
5E	ì	lowercase i with acute accent
5F	ò	lowercase o with acute accent
60	ù	lowercase u with acute accent
61	a	lowercase a
62	b	lowercase b
63	c	lowercase c
64	d	lowercase d
65	e	lowercase e
66	f	lowercase f
67	g	lowercase g
68	h	lowercase h
69	i	lowercase i
6A	j	lowercase j
6B	k	lowercase k
6C	l	lowercase l
6D	m	lowercase m
6E	n	lowercase n
6F	o	lowercase o
70	p	lowercase p
71	q	lowercase q
72	r	lowercase r
73	s	lowercase s
74	t	lowercase t
75	u	lowercase u
76	v	lowercase v
77	w	lowercase w
78	x	lowercase x
79	y	lowercase y
7A	z	lowercase z
7B	ç	lowercase c with cedilla
7C	÷	division sign
7D	Ñ	uppercase N-tilde
7E	ñ	lowercase n-tilde
7F	♉	solid block

Line 21 Special Character Set

The Line 21 special character set appearing in Table 3 is the same as the one found in EIA-608 and in FCC Part 15.119.

Table 3 Line 21 Special Character Set

Hex	Example	Alternate	Description
30		See note[1]	Registered mark symbol
31	°		Degree sign
32	½		½ symbol
33	¿		Inverted (open) question mark (inverse query)
34	TM	See note[1]	Trademark symbol
35	¢		Cents symbol
36	£		Pounds sterling
37	♪		Musical note
38	à		Lowercase a, grave accent
39			Transparent space
3A	È		Lowercase e, grave accent
3B	Â		Lowercase a with circumflex
3C	Ê		Lowercase e with circumflex
3D	Î		Lowercase i with circumflex
3E	Ô		Lowercase o with circumflex
3F	Û		Lowercase u with circumflex

NOTE: **The registered and trademark symbols are used to satisfy certain legal requirements. There are various legal ways in which these symbols may be drawn or displayed. For example, the trademark symbol may be drawn with the "T" next to the "M" or over the "M." It is preferred that the trademark symbol be superscripted, i.e., XYZ**?. It is left to each individual manufacturer to interpret these symbols in any way that meets the legal needs of the user.

Progressive Scan

The DMPX supports the progressive scan reconstruction process as well as interlaced video for the NTSC and PAL formats during DMP playback. The DMPX supports both baseline and progressive JPEG decoding.

In order to show a progressive image, the CRT controllers of the DMPX are driven to generate and refresh the scan lines used to create the active display at a rate double that of the refresh speed used by the NTSC system in order to draw an entire frame in the same amount of time it takes to draw a single field.

The progressive scan features of the DMPX make the faster screen refresh possible, allowing for a flicker-free picture of superior quality to be displayed during DMP playback, while also reducing the number of scan lines visible to the unaided eye.

Unlike interlaced video, every scan line of a complex video frame is refreshed when using progressive

scan. Since the reconstruction process of de-interlaced video is a digital process, the reconstruction process is a lossless one during A/D and D/A conversion of the bitstream.

Video Error Concealment

The MPEG decoder handles bitstream errors while performing video error concealment during DMP playback.The DMPX processors all support the three modes of video error concealment presented in Table 4.

Table 4 Video Error Concealment Modes

Mode	Type	Description
0	Adaptive	Automatically switches the DMPX between the blocky and jerky modes.
1	Jerky	Show good pictures, but not smoothly.
2	Blocky	Shows pictures smoother, but in more of a blocky fashion.

HDMI Interface

The DMPX includes a High Definition Media Interface (HDMI) link for interfacing with external HDMI transmitters devices. Figure 3 depicts the HDMI link between an external HDMI transmitter and the DMPX.

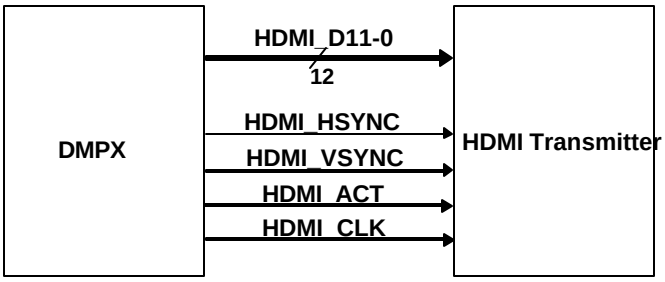


Figure 3 DMPX HDMI Link

The YCbCr data is output from the DMPX in 12 bit format along with the HDMI_HSYNC and HDMI_VSYNC scan control signals.

Device Interfaces

Audio Interface

The audio interface is a serial port that connects to an external audio DAC or ADC for the transfer of PCM (pulse coded modulation) audio data in I^2S format. It supports 16-, 24-, and 32-bit audio frames. No external master clock is required.

The DMPX offers three audio interface modes:

1. Stereo mode using the TSD0 pin.

2. Dolby Digital (AC-3) 5.1 channel mode using the TSD[3:0] pins.
3. Dolby Digital (AC-3) 5.1 channel mode using the S/PDIF pin.

The DMPX audio mode configuration is selectable, allowing it to interface directly with low-cost audio DACs and ADCs. The audio port provides a standard I^2S and S/PDIF (IEC958) interface input and output.

Stereo mode is in I^2S format while 5.1 channel Dolby Digital 5.1 channel audio output can be channeled through both the I^2S interface and the S/PDIF. The S/PDIF interface consists of a bi-phase mark encoder, which has low skew.

The transmit I^2S interface supports the 128, 192, 256, 384, and 512 sampling frequency formats, where sampling frequency Fs is usually 32 kHz, 44.1 kHz, 48 kHz, 96 kHz, or 192 kHz. The audio samples for the I^2S transmit interface can be 16, 18, 20, 24, and 32-bit samples.

For Linear PCM audio stream format, the DMPX supports 48 kHz and 96 kHz. Dolby Digital audio only supports 48 kHz. The DMPX incorporates a built-in programmable analog PLL in the device architecture in order to generate a master audio clock.

The MCLK pin is for the audio DAC clock and can either be an output from or an input to the DMPX. Audio data out (TSD) and audio frame sync (TWS) are clocked out of the DMPX based on the audio transmit bit clock (TBCK). Audio receive bit clock (RBCK) is used to clock in audio data in (RSD) and audio receive frame sync (RWS).

Storage Device Interfaces

The ES6460 supports Memory Stick (MS), SD, XD and Smart Media interfaces. In addition, ES6461 supports the AT Attachment Packet Interface (ATAPI), Compact Flash (CF) and Integrated Drive Electronics (IDE) interfaces.

ATA/IDE Interface

The host interface directly supports ATAPI devices with PIO modes. The ATA/IDE interface can directly control two devices through the use of the HCS1FX# and HCS3FX# signals. The ATA/IDE interface of the ES6461 uses a command execution protocol that allows for the operation of hard disk drives. Table 5 lists the packet commands and the respective command codes for ATAPI devices, as specified by SFF-8090i.

Table 5 Packet Commands for ATAPI Devices

Code	Command Name
00h	TEST UNIT READY
03h	REQUEST SENSE
04h	FORMAT UNIT
12h	INQUIRY
1Bh	START/STOP UNIT
1Eh	PREVENT/ALLOW MEDIUM REMOVAL
23h	READ FORMAT CAPACITIES
25h	READ CAPACITY
28h	READ (10)
2Ah	WRITE (10)
2Bh	SEEK

2Eh	WRITE AND VERIFY (10)
2Fh	VERIFY (10)
35h	SYNCHRONIZE CACHE
42h	READ SUBCHANNEL
43h	READ TOC/PMA/ATIP
44h	READ HEADER
45h	PLAY AUDIO (10)
46h	GET CONFIGURATION
47h	PLAY AUDIO MSF
4Ah	GET EVENT/STATUS NOTIFICATION
4Bh	PAUSE/RESUME
4Eh	STOP PLAY/SCAN
51h	READ DISC INFORMATION
52h	READ TRACK/RZONE INFORMATION
53h	RESERVE TRACK/RZONE
54h	SEND OPC INFORMATION
55h	MODE SELECT (10)
58h	REPAIR RZONE
5Ah	MODE SENSE (10)
5Bh	CLOSE TRACK/RZONE/SESSION/BORDER
5Dh	SEND CUE SHEET
A1h	BLANK
A2h	SEND EVENT
A3h	SEND KEY
A4h	REPORT KEY
A6h	LOAD/UNLOAD MEDIUM
A7h	SET READ AHEAD
A8h	READ (12)
AAh	WRITE (12)
ACh	GET PERFORMANCE
ADh	READ DMP STRUCTURE
B6h	SET STREAMING
B9h	READ CD MSF
BAh	SCAN
BBh	SET CD SPEED
BCh	PLAY CD
BDh	MECHANISM STATUS
BEh	READ CD
BFh	SEND DMP STRUCTURE

Compact Flash Interface

The ES6461 provides True IDE Mode I/O support for the Compact Flash storage card interface found on a variety of removable storage cards used by digital cameras and MP3 players. The ES6461 uses its host interface to communicate with Compact Flash devices.

By implementing Compact Flash support, the ES6461 can readily detect the insertion and removal of a Compact Flash card, which also constitutes a hot-swapping event. During a hot-swapping event, the CARD_DETECT signal is asserted by the Compact Flash, allowing it to determine the presence of the removable storage card fully inserted into its socket.

The ES6461 permits both 8- and 16-bit common memory I/O accesses with a removable storage card via the host interface. Table 6 lists the CF-ATA command set.

Table 6 CF-ATA Command Set

Class	Command	Code
1	CHECK POWER MODE	E5h or 98h
1	EXECUTE DRIVE DIAGNOSTIC	90h
1	ERASE SECTOR(S)	C0h
1	IDENTIFY DRIVE	ECh
1	IDLE	E3h or 97h
1	IDLE IMMEDIATE	E1h or 95h
1	INITIALIZE DRIVE PARAMETERS	91h
1	READ BUFFER	E4h
1	READ LONG SECTOR	22h or 23h
1	READ MULTIPLE	E4h
1	READ SECTOR(S)	20h or 21h
1	READ VERIFY SECTOR(S)	40h or 41h
1	RECALIBRATE	1Xh
1	REQUEST SENSE	03h
1	SECURITY DISABLE PASSWORD	F6h
1	SECURITY ERASE PREPARE	F3h
1	SECURITY ERASE UNIT	F4h
1	SECURITY FREEZE LOCK	F5h
1	SECURITY SET PASSWORD	F1h
1	SECURITY UNLOCK	F2h
1	SEEK	7Xh
1	SET FEATURES	EFh
1	SET MULTIPLE MODE	C6h
1	SET SLEEP MODE	E6h or 99h
1	STAND BY	E2h or 96h
1	STAND BY IMMEDIATE	E0h or 94h
1	TRANSLATE SECTOR	87h
1	WEAR LEVEL	F5h

2	FORMAT TRACK	50h
2	WRITE BUFFER	E8h
2	WRITE SECTOR(S)	30h or 31h
2	WRITE LONG SECTOR	32h or 33h
2	WRITE SECTOR(S) W/O ERASE	38h
3	WRITE VERIFY	3Ch
3	WRITE MULTIPLE	C5h
3	WRITE MULTIPLE W/O ERASE	CDh

Memory Stick Interface

The DMPX supports playback of digital media in the Memory Stick. This type of media can be applied to many types of devices, including but not limited to, MP3 players and digital still cameras.

More detailed Memory Stick specifications and information can be found at the Memory Stick Technical Support website at http://www.memorystick.org.

Memory Stick Addressing

The DMPX supports cluster-style addressing when data is being stored to a Memory Stick device, which makes the data as accessible from the device as it would be from a hard disk drive.

DRAM Memory Interface

The DMPX provides a glueless 16-bit interface to DRAM memory devices used as video memory for a DMP player. The maximum amount of memory supported is 16 MB of Synchronous DRAM (DRAM). The memory interface is configurable in depth to support 128-Mb addressing.

The memory bus interface generates all the control signals to interface with external memory. The DMPX supports different configurations using the memory configuration bits SDCFG[1:0] (bits 12:11), the SD8BIT bit (bit 14), and SD64M bit (bit 15) in the BUSCON_DRAM_CONTROL register. Configurations can be implemented in many ways. Table 7 lists the typical DRAM configurations used by the DMPX.

Table 7 Typical DRAM Configurations

Mem. Size (MB)	Bit Order				Memory Configuration (Mb per pc)
	SD64M	SD8BIT	SDCFG1	SDCFG0	
2	0	0	0	1	1 pc: 512Kx16x2 (16 Mb)
4	0	0	0	0	2 pcs: 512Kx16x2 (16 Mb)
4	0	1	0	1	2 pcs: 1Mx8x2 (16 Mb)
8	0	1	0	0	4 pcs: 1Mx8x2 (16 Mb)
8	1	0	X	X	1 pc: 1Mx16x4 (64 Mb)
16	1	0	X	X	2 pc: 1Mx16x4 (64 Mb)
16	1	1	X	X	2 pc: 2Mx8x4 (64 Mb)
16	1	1	X	X	1 pc: 2Mx16x4 (128 Mb)

The memory interface controls access to both external DRAM or EDO memories, which can be the sole

unified external read/write memory acting as program and data memory as well as various decoding and display buffers.

At high clock speeds, the memory bus interface has sufficient bandwidth to support the decoding and displaying of CCIR656/601 resolution images at full frame rate.

DRAM Considerations

The DMPX uses DRAM with a programmed CAS# latency of three clocks (CL = 3) and sequential burst of full page length. Performance based on DRAM is double that of EDO. DRAM must be software configured before any memory access. The programmable DRAM refresh period can be modified to meet any desired configuration.

DRAM Address Mapping

The memory address (LA) is mapped to the DMA address, which is formed by ADDR in the BUSCON_DMA_ADDR registers. The result is then converted into the DRAM control signals using the SDCFG[1:0] configuration bits (bits 12:11) and the SD8BIT bit (bit 14) in the BUSCON_DMA_CONTROL register.

DRAM Configuration Requirements

Table 8 lists the DRAM memory size configurations, each with its corresponding signal pins.

Table 8 DRAM Configurations and Signal Pins

Size (MB)	DRAM 0	DRAM 1	DRAM2	DRAM3	Memory Type
2	DCAS# DRAS0# DCS0# DB[0:15]	—	—	—	512Kx16x2 (16 Mb)
4	DCAS# DRAS0# DCS0# DB[0:15]	DCAS# DRAS0# DCS1# DB[0:15]	—	—	512Kx16x2 (16 Mb)
4	DCAS# DRAS0# DCS0# DB[0:7]	DCAS# DRAS0# DCS# DB[8:15]	—	—	1Mx8x2 (16 Mb)
8	DCAS# DRAS0# DCS0# DB[0:7]	DCAS# DRAS0# DCS0# DB[8:15]	DCAS# DRAS0# DCS1# DB[0:7]	DCAS# DRAS0# DCS1# DB[8:15]	1Mx8x2 (16 Mb)
8	DCAS# DRAS0# DCS0# DB[0:15]	—	—	—	1Mx16x4 (64 Mb)
16	DCAS# DRAS0# DCS0# DB[0:15]	DCAS# DRAS0# DCS1# DB[0:15]	—	—	1Mx16x4 (64 Mb)

16	DCAS# DRAS0# DCS0# DB[0:7]	DCAS# DRAS0# DCS0# DB[8:15]	—	—	2Mx8x4 (64 Mb)
16	DCAS# DRAS0# DCS0# DB[0:15]	—	—	—	2Mx16x4 (128 Mb)

TDM Interface

The DMPX implements a high-speed, bidirectional serial bus known as a TDM interface that supports a number of high-speed serial protocols. The TDM interface can also act as a general-purpose 16-Mbps serial link when not constrained by TDM protocols.

The TDM interface provides an easy connection between the DMPX and available communications chips. The TDM interface is a time-division-multiplexed bus that multiplexes byte data on up to 64 channels. Time slot 0 starts after N (which can be set in the XMT/RCVDELAY register) clocks after the frame starts.

Each slot is eight clock periods long, and either transmits or receives byte data during a write cycle or a read cycle. Immediately after slot 0 completes, slot 1 starts and so on. Each channel is allocated a different time slot on the bus, and the DMPX can be set to send and receive data in any combination of different time slots.

Data is assumed to be ordered by time slot; e.g., if time slots 6, 8, and 17 are used, the first DMA byte sent to memory would be in time slot 6, followed by time slots 8 and 17 in order. All DMA byte reordering is done in software. The interface consists of frame sync signal TDMFS, data receive signal TDMDR, and bit clock signal TDMCLK.
The timing of the data transfer is externally controlled. The TDM interface can support a number of different timings. The TDM interface can transfer data at a maximum rate of 16 Mbps, with a more typical configuration supporting a data rate of up to 4.096 Mbps with a frame sync frequency of 8 kHz. The TDM interface programmability includes independent receive, transmit, and frame sync clock edge selection and independent receive and transmit data offsets.

USB2.0 HS OTG Controller

The DMPX has two built-in high speed USB2.0 OTG ports capable of supporting host or device modes.

USB core description

The USB core can be viewed as an EHCI controller with a single port root hub to which an USB2.0 Hub is integrated on-chip. The external USB devices are connected to the Host controller through the USB2.0 hub. When the OTG port acts in host mode, the USB2.0 hub handles the control of this port. When the OTG port acts in peripheral mode, the control of this port is handled by the Device controller logic. Initially the EHCI enumerates the on-chip hub through a set of programmable register interface. Then it proceeds to enumerate the external devices through transaction scheduling. The host controller through the hub logic enumerates full speed devices by scheduling split transactions. The USB core can operate in the following modes:

Port1 or Port2 as

- OTG A-device.
- OTG B-device.
- OTG Dual Role Device.
- Standard Device controller.

The USB core provides the following features:

- Fully compliant with
  - On-The-Go Specification Rev 1.0
  - USB 2.0 Specification Rev 2.0
  - EHCI Specification Rev1.0.
- Interfaces with external UTMI+ Level 3 Transceiver.
- Supports 16-bit UTMI.
- Supports Bulk, Control, Interrupt and Isochronous transfers.
- Suspend Resume supported in Host & Device mode.
- Remote - wakeup supported in host mode.

USB Processor Interface

- High speed AHB support with 32/16/8-bit bus width.
- AHB master supports sequential bursts and non-sequential transfers.
- AHB slave provides only non-sequential accesses.

OTG Control Logic

- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) and USB Power Management requirements.
- Supports Dual Role mode of operation.

Host Controller

- The host controller is compliant with EHCI specification Rev1.0. The host controller contains an integrated root hub for downward compatibility to USB1.1.
- Supports Frame caching of isochronous transfer descriptors with a programmable memory depth. Can be increased in multiples with requirement.
- 1K DPRAM provided to support ISO transfer.
- Supports High/Full/Low speed USB data rates.
- Supports Bulk, Control, Interrupt and Isochronous Transfers.
- Supports external high speed or full speed compound / hub devices.
- Supports TestK, TestJ, TestSE0 and TestPacket modes for the downstream port

USB Device Controller

- Supports full or high speed USB rates.
- Automatic high speed Reset Handshake protocol detection.
- The device controller provides a control endpoint and up to 15 programmable endpoints that can programmed as Bulk / Interrupt / Isochronous with programmable maximum packet size and endpoint direction.
- Device controller provides a 32-bit configurable DPRAM for endpoint memory.
- Software programmable packet buffers for each endpoint.
- The Endpoint memory is accessible by either an external AHB slave or AHB master.
- Supports TestK, TestJ, and TestSE0 and TestPacket modes at the upstream port.

USB Transceiver

The built-in USB2.0 phy is UTMI+ Level 3 compatible USB2.0 OTG function transceiver. It is comprised of both USB1.1 and USB2.0 transceivers

- Compliant with UTMI+ Specification Version 1.0
- Compliant with USB2.0 OTG specification
- Supports HS(480Mbps)/FS(12Mbps) /LS(1.5Mbps) modes
- 16-bit, 30MHz or 8-bit, 60MHz parallel interface for HS/FS
- Support full speed and low speed serial mode
- All required terminations, including 1.5Kohm pull-up on DP and DM, and 15Kohm pull-down on DP and DM are internal to chip
- Serializing and De-serializing for transmitting and receiving data stream
- USB Data Recovery and Clock Recovery on receiving for HS/FS
- SYNC field and EOP detection on receive packets
- SYNC field and EOP generation on transmit packets
- Integrated Bit Stuffing and De-stuffing
- NZRI encoding and decoding
- 8 bit unidirectional Data Bus with handshake pins for 8-bit interface
- 16 bit bi-directional Data Bus with handshake pins for 16-bit interface
- Loop Back test mode in 8-bit interface
- Supports detection of USB reset, suspend and resume signaling
- Supports high speed identification and detection as defined by USB 2.0 Specification
- Supports OTG VBUS state detecting and SRP request
- Supports ID detect to distinguish A-Device and B-Device
- Support long EOP generation for host and hub application
- Support high speed host disconnection detection

Video Interface

Video Display Output

The video output section controls the transfer of video frames stored in memory to the internal TV encoder of the DMPX. The output section consists of a programmable CRT controller capable of operating either in Master or Slave mode. Figure 4 shows the display timing on the screen.

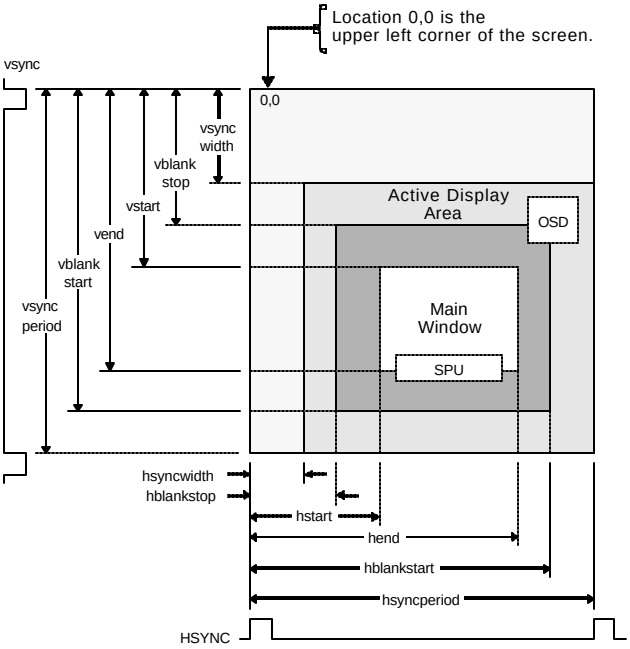


Figure 4 Video Output Timing

The video output section features internal line buffers that allow the outgoing luminance and chrominance data to match the internal clock rates with external pixel clock rates, easily facilitating YUV4:2:2 to YUV4:2:0 component and sample conversion. Arbitrary horizontal decimation and interpolation is achieved by a polyphase filter.

Together with programmable line dropping/duplication circuitry and micro-code based post-processing running on the video processor, the DMPX is capable of arbitrating image conversion. Examples include SIF to CCIR656/601, letter-box, NTSC to PAL, and PAL to NTSC conversions.

Video Bus

The DMPX video bus transfers digital video pixels out of the chip. In standalone applications the video bus will be connected to a monitor or an LCD panel. In workstation applications, the output bus will feed an overlay circuit so that the output video appears in a window of the Graphical User Interface (GUI).

The video bus has 8 YUV data pins that transfer luminance and chrominance (YUV) pixels in CCIR656/601 pixel format (4:2:2). In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance.

Safe Caption Area

The DMPX draws the safe caption area required by FCC Part 15.119, as shown in Figure 5.

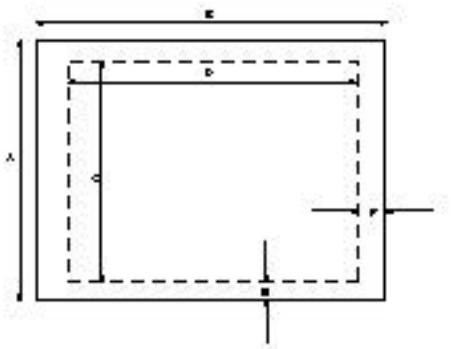


Figure 5 Safe Caption Area

The dimensions of the safe caption area are listed in Table 9.

Table 9 Safe Caption Area Dimensions

Label	Dimension	Percent of Picture Height
A	Television picture height	100.0
B	Television picture width	133.33
C	Height of safe caption area	80.0
D	Width of safe caption area	106.67
E	Vertical portion of safe caption area	10.0
F	Horizontal portion of safe caption area	13.33

Video Post-Processing

The DMPX video post-processing circuitry provides support for the color conversion, scaling, and filtering functions through a combination of special hardware and software. Horizontal up-sampling and filtering is done with a programmable, 7-tap polyphase filter bank for accurate non-integer interpolations. Vertical scaling is achieved by repeating and dropping lines in accordance with the applicable scaling ratio.

Figure 6 shows the video post-processing functional blocks. The first two processing steps are performed by the video processor core. Video post-processing can be applied on the decoded images to improve the picture quality.

The next stage in the processing, applicable only to low resolution MPEG-1 video, is an interlacing filter that generates even and odd fields from decoded frames for applications that use a TV screen. The filter improves both the spatial and temporal appearance of the decoded images on interlaced displays.

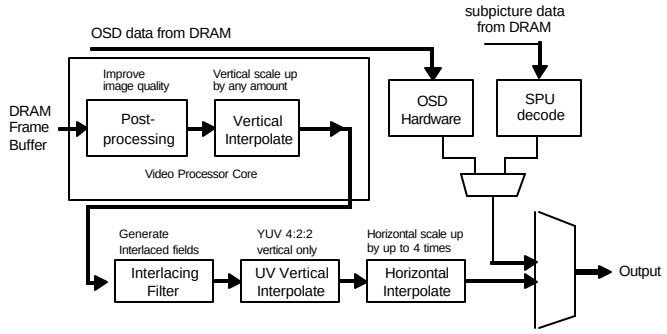


Figure 6 Video Post-Processing

Following the interlacing filter is an interpolation section that uses bilinear interpolation to increase the resolution of the chrominance components by a factor of two in the vertical dimension. This interpolation section converts from the MPEG chrominance subsampling to that used by CCIR656/601.

The resulting YUV pixels can then be passed through a 7- tap horizontal interpolation filter that increases the horizontal resolution of the image by up to four times. The horizontal filter automatically chooses between five sets of filter coefficients based on the fractional component of the new position of the pixel in the video data stream.

The filter coefficients are 8 bits wide. The filter length is selectable as 1, 3, 5, or 7 taps.

The relationship between the doubled pixel clock PCLK2CN and the internal ESS RISC clock is listed in Table 10.

Table 10 ESS RISC Clock Relationship to Pixel Clocks

Taps	Restrictions	Frequency
3	Pixel rate < (Internal RISC CLK)/2	27-MHz
5	Pixel rate < (Internal RISC CLK)/3	20-MHz
7	Pixel rate < (Internal RISC CLK)/4	Default 13.5-MHz

Video Timing

The video bus can be clocked either by double pixel clock and clock qualifier or by a single pixel clock. The double clock typically is used for TV displays, the single for computer displays. PCLKQSCN is ignored in 1x clock mode. The timing of the syncs and odd/even field indication is shown in Figure 7 and Figure 8.

The output video field indication is done by modifying the relative positions of VSYNC and HSYNC. At the start of an even field, the horizontal and vertical sync pulses will start on the same clock edge; in odd fields the horizontal sync pulse will be delayed by one clock cycle. The polarity of both horizontal and vertical syncs is programmable.

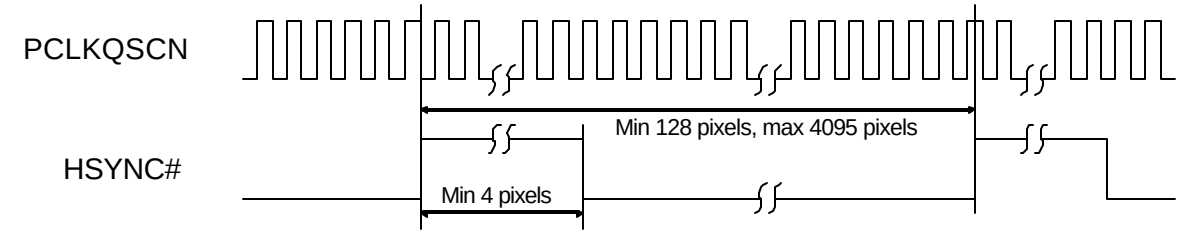


Figure 7 Horizontal Video Timing

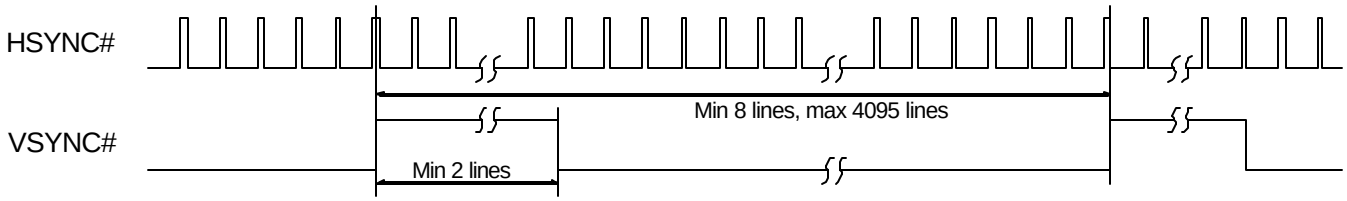


Figure 8 Vertical Video Timing

TIMING DIAGRAMS

Audio Interface Timing

The audio transmit and receive timing diagrams for the DMPX are shown in Figure 9 through Figure 13.

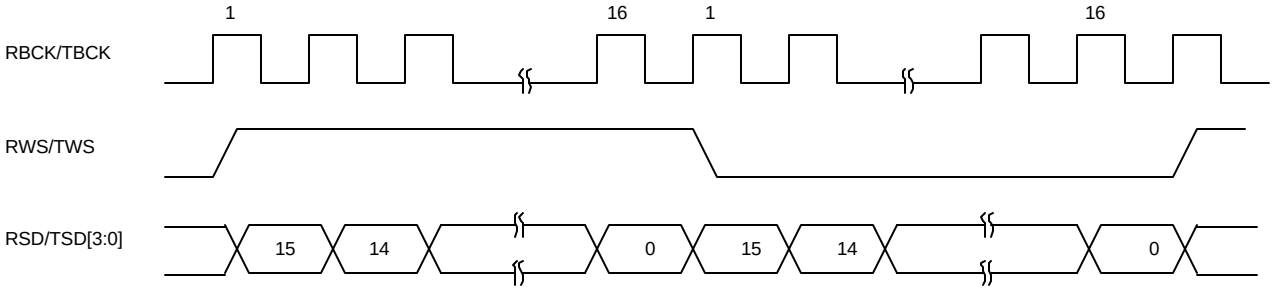


Figure 9 Right Justified Mode / 16-Bit Cycle Frame / 16-Bit Data Frame / MSB First

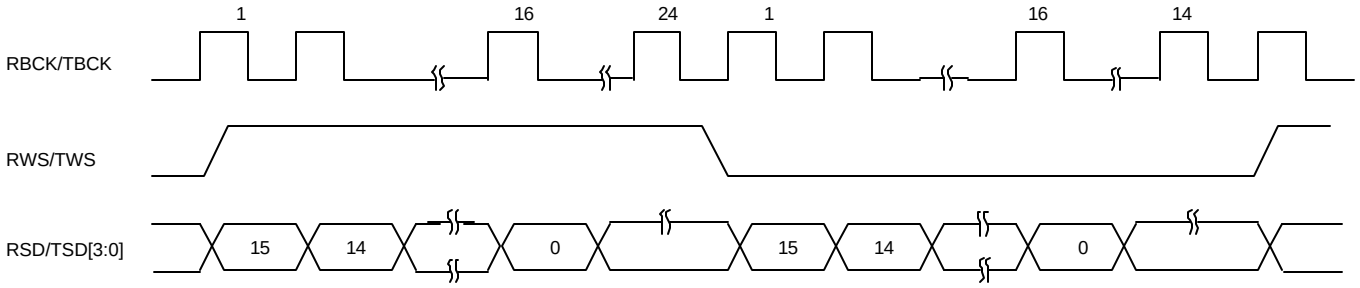


Figure 10 Right Justified Mode / 24-Bit Cycle Frame / 16-Bit Data Frame / MSB First

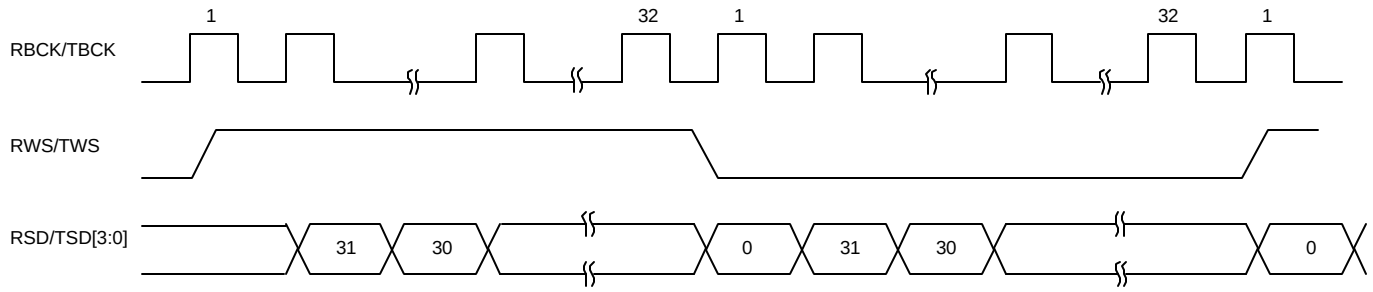


Figure 11 Right Justified Mode / 32-Bit Cycle Frame / 24-Bit Data Frame / LSB First

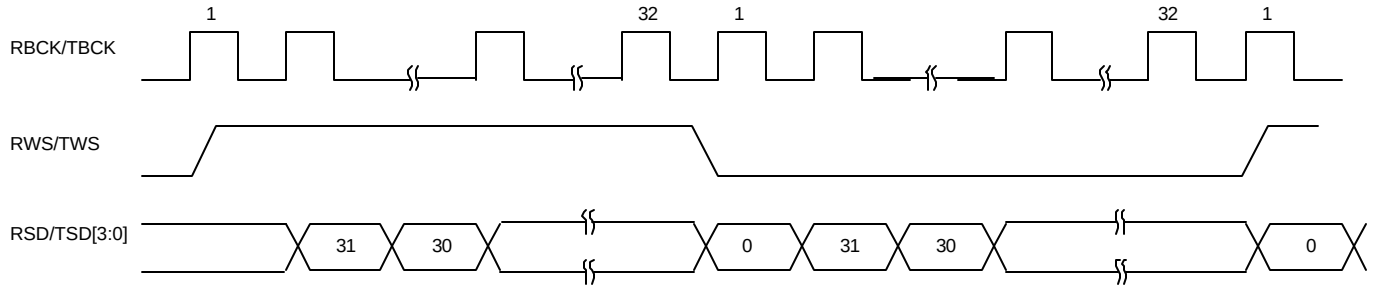


Figure 12 Left Justified Mode / 32-Bit Cycle Frame / 24-Bit Data Frame / MSB First

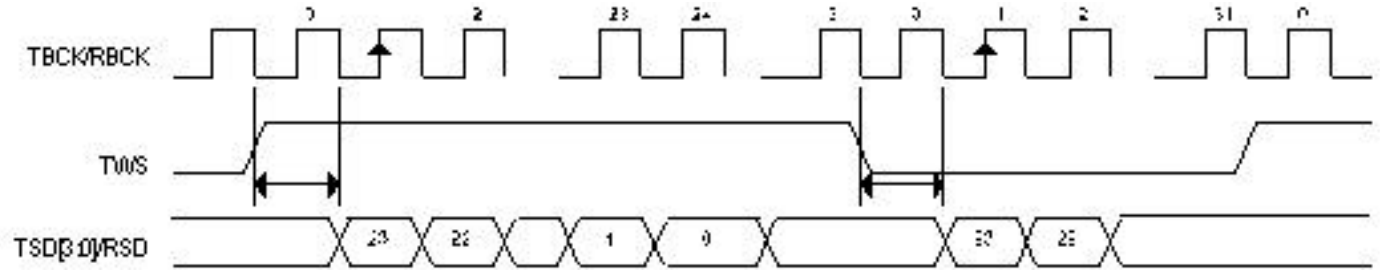
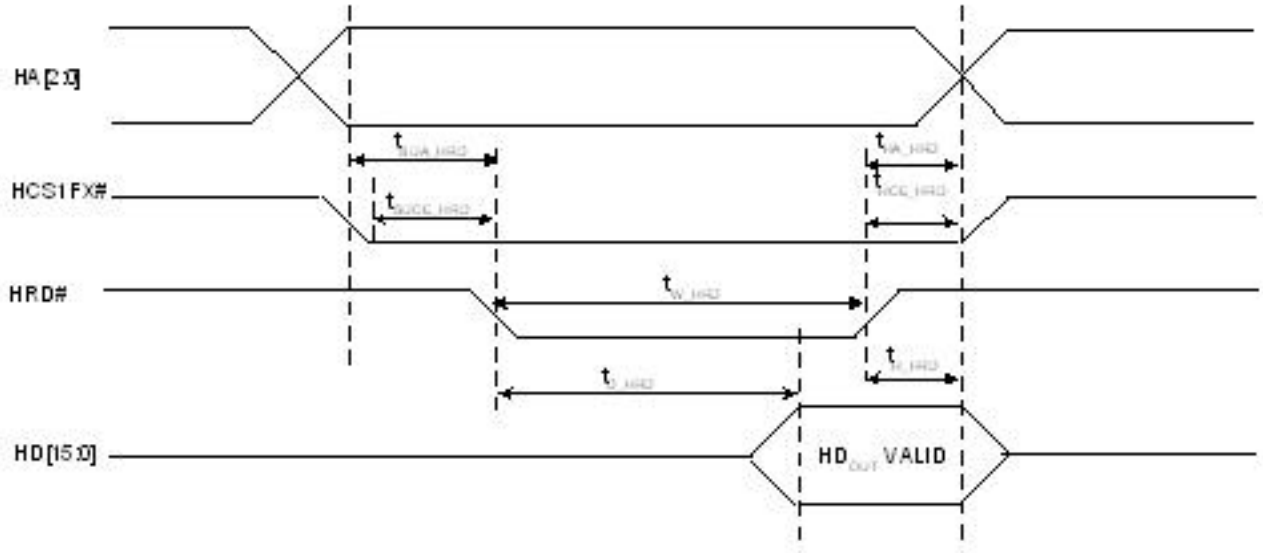


Figure 13 I^2S Mode

Compact Flash Interface Timing

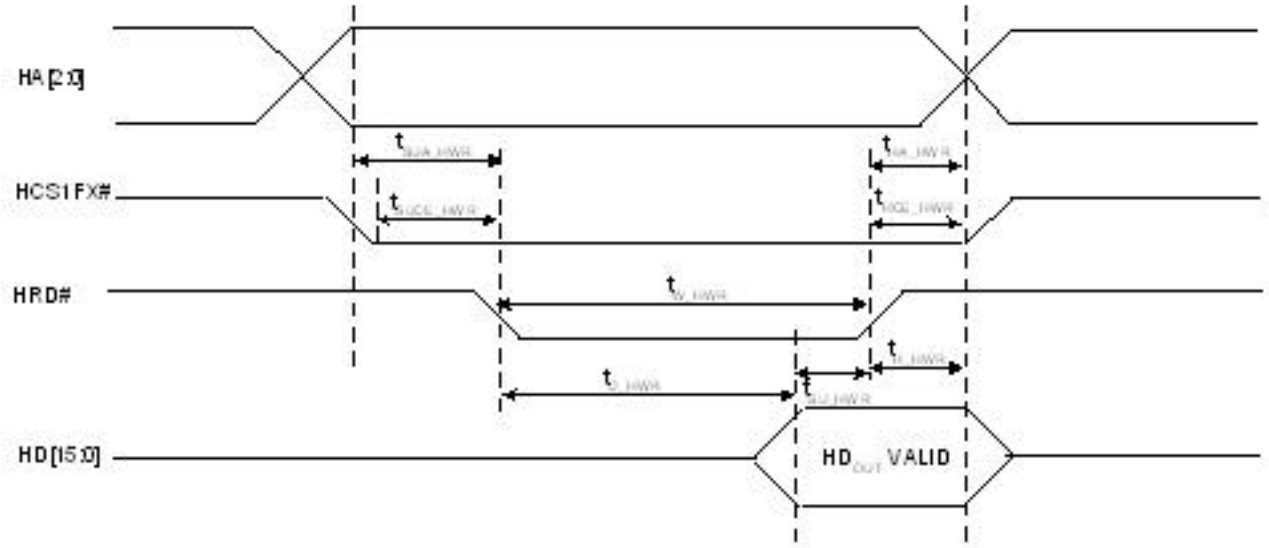
The Compact Flash interface timing diagrams for the ES6461 appear from Figure 14 to Figure 15.



Compact Flash True IDE Mode I/O Read Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
tD_HRD	Data delay after HRD#.			100	ns
tH_HRD	Data hold following HRD#.	0			
tW_HRD	HRD# width time.	165			
tSUA_HRD	Address setup before HRD#.	70			
tHA_HRD	Address hold following HRD#.	20			
tSUCE_HRD	CE# setup before HRD#.	5			
tHCE_HRD	CE# hold following HRD#.	20			

Figure 14 Compact Flash True IDE Mode I/O Read Timing



Compact Flash True IDE Mode I/O Write Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
tSU_HWR	Data setup before HWR#.	60			ns
tH_HWR	Data hold following HWR#.	30			
tW_HWR	HWR# width time.	165			
tSUA_HWR	Address setup before HWR#.	70			
tHA_HWR	Address hold following HWR#.	20			
tSUCE_HWR	CE# setup before HWR#.	5			
tHCE_HWR	CE# hold following HWR#.	20			

Figure 15 Compact Flash True IDE Mode I/O Write Timing

Host Interface Timing

The host interface timing diagrams for the DMPX are shown in Figure 16 and Figure 17.

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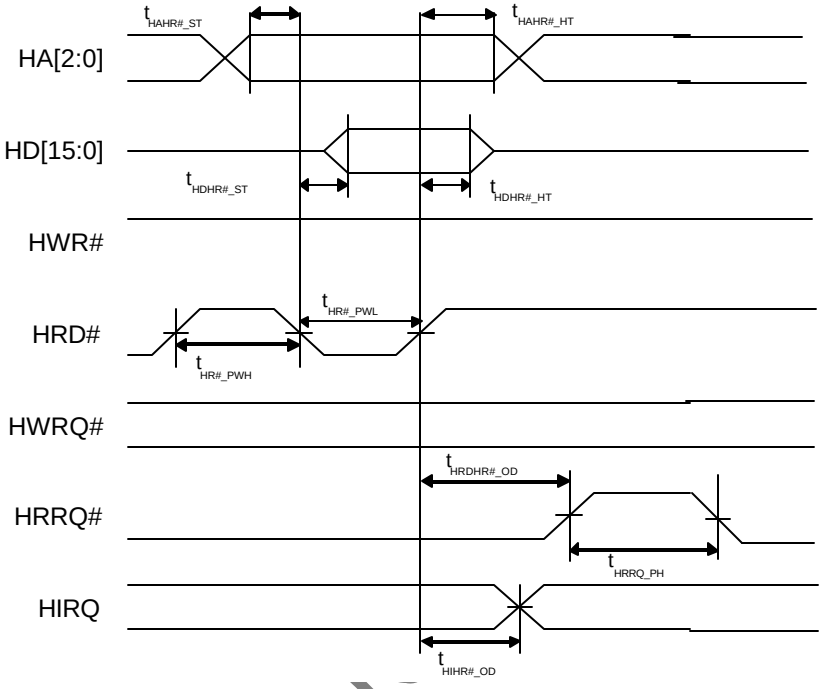


Figure 16 Host Bus Read Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
tHAHR#_ST	HA to HRD# setup time	4			ns
tHAHR#_HT	HA to HRD# hold time	2			
tHDHR#_ST	HD to HRD# setup time	0		4	
tHDHR#_HT	HD to HRD# hold time	2			
tHR#_PWH	HRD# pulse width high	30			
tHR#_PWL	HRD# pulse width low	30			
tHRDHR#_OD	HRRQ# to HRD# output delay	0		8	
tHIHR#_OD	HIRQ to HRD# output delay	0		8	
tHRRQ_PH	HRRQ# pulse width high (See note)	75			

NOTE: **HRRQ# is defined as a minimum value.**

NOTE: Host Bus Read Timing

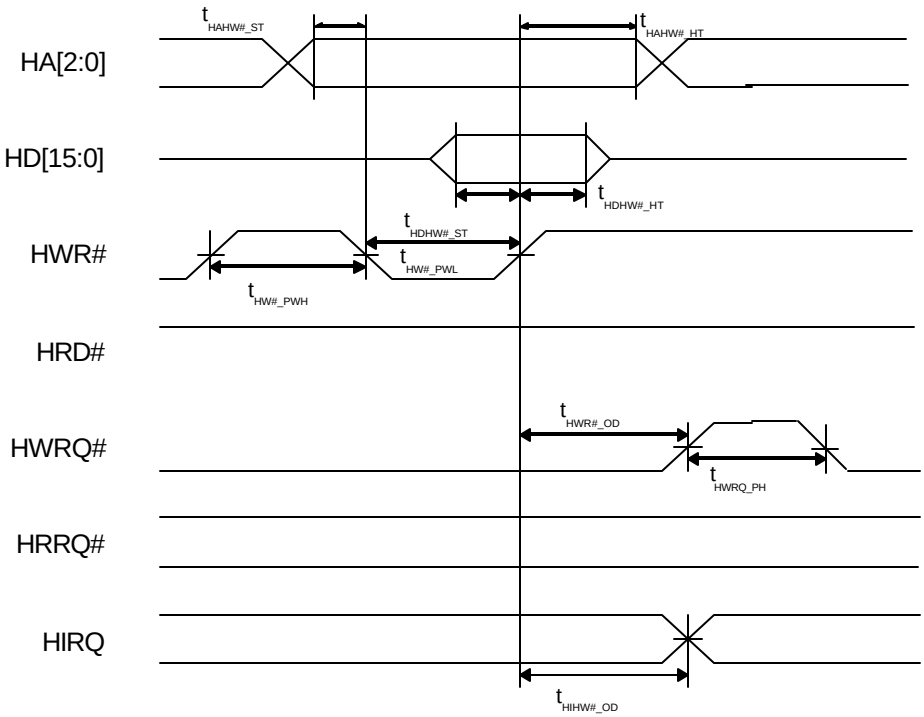


Figure 17 Host Bus Write Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
tHAHW#_ST	HA to HWR# setup time	4			ns
tHAHW#_HT	HA to HWR# hold time	2			
tHDHW#_ST	HD to HWR# setup time	4			
tHDHW#_HT	HD to HWR# hold time	2			
tHW#_PWL	HWR# pulse width low	30			
tHW#_PWH	HWR# pulse width high	30			
tHWR#_OD	HWRQ# to HWR# output delay	0		8	
tHIHW#_OD	HIRQ to HWR# output delay	0		8	
tHWRQ_PH	HWRQ# pulse width high (See note)	75			

NOTE: **HWRQ# is defined as a minimum value.**

NOTE: Host Bus Write Timing

Memory Stick Interface Timing

The Memory Stick interface timing diagrams for the DMPX appear from Figure 18 to Figure 19.

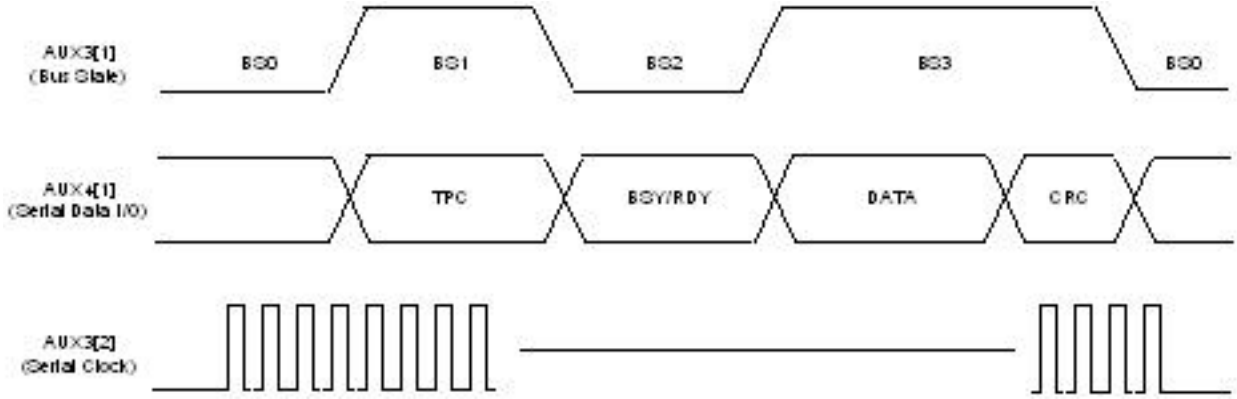


Figure 18 Memory Stick Read Timing

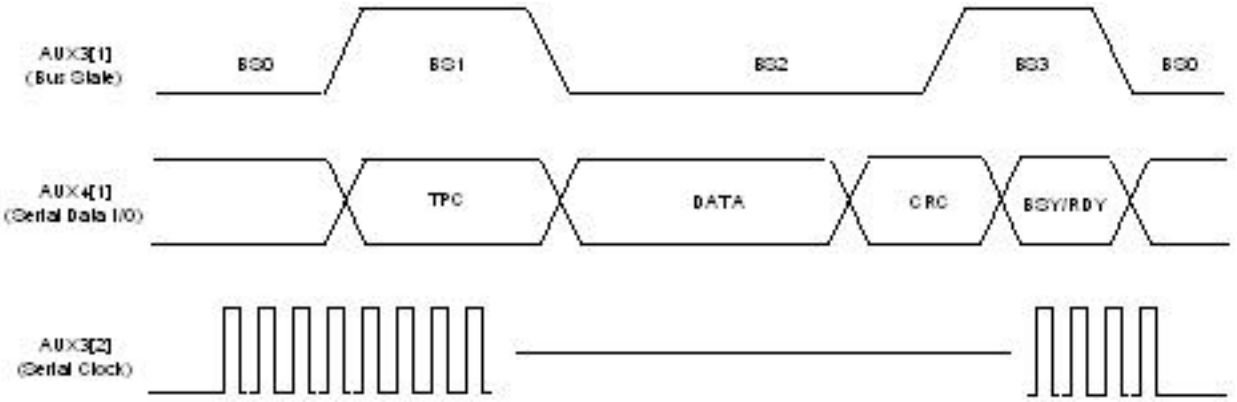


Figure 19 Memory Stick Write Timing

SDRAM Interface Timing

The SDRAM read and write timing diagrams for the DMPX are shown in Figure 20 through Figure 23.

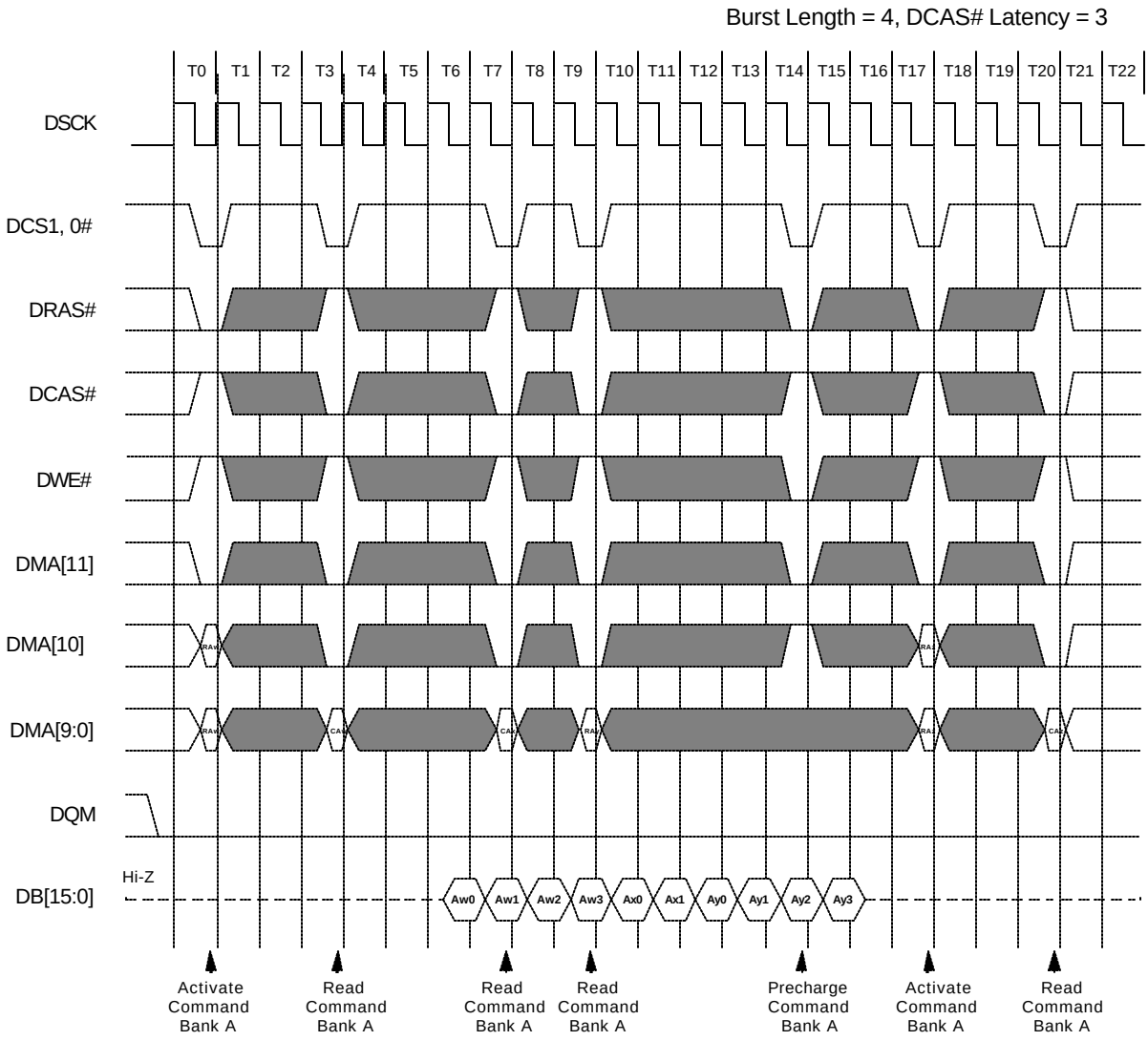


Figure 20 SDRAM Random Column Read Timing

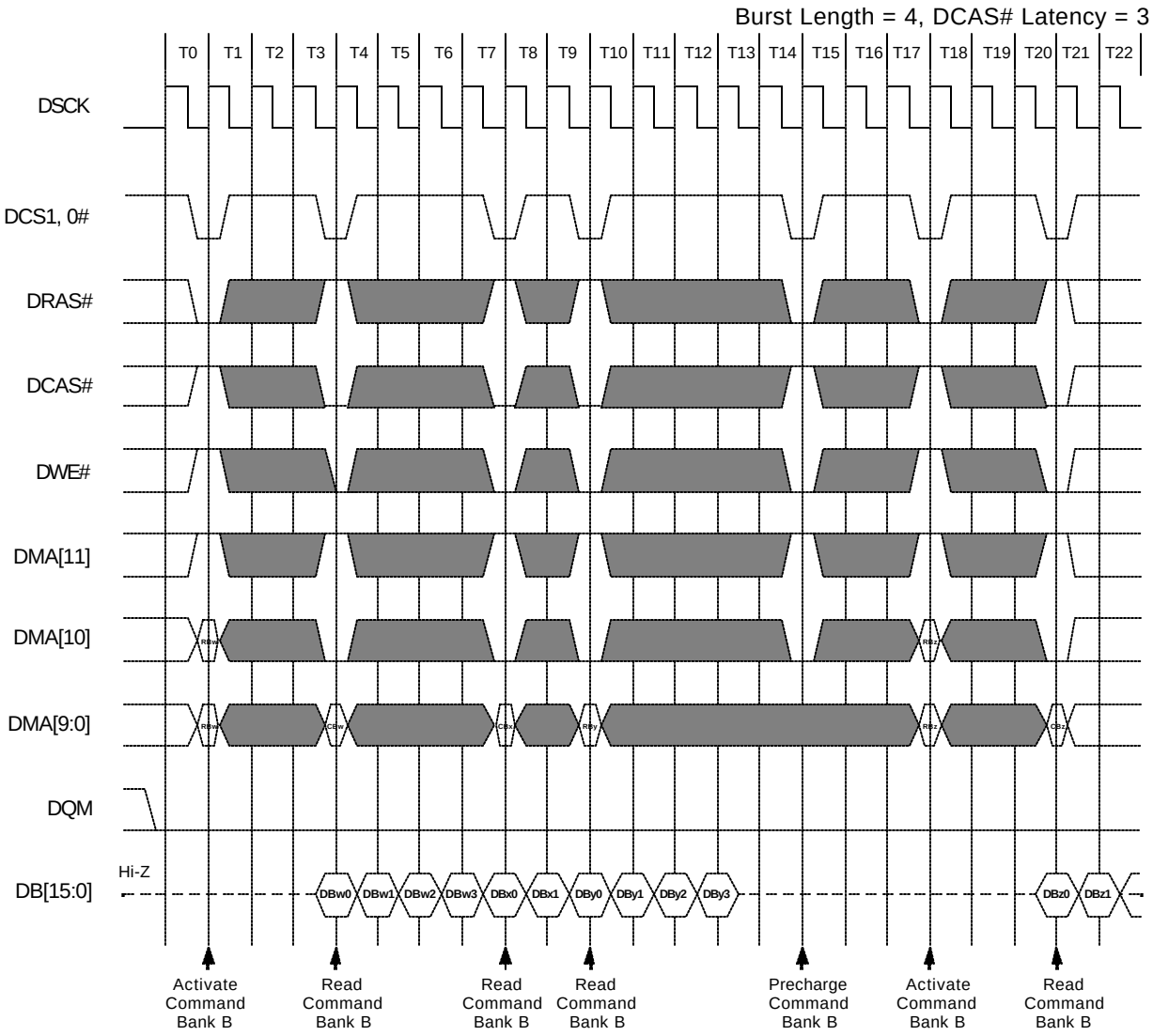


Figure 21 SDRAM Random Column Write Timing

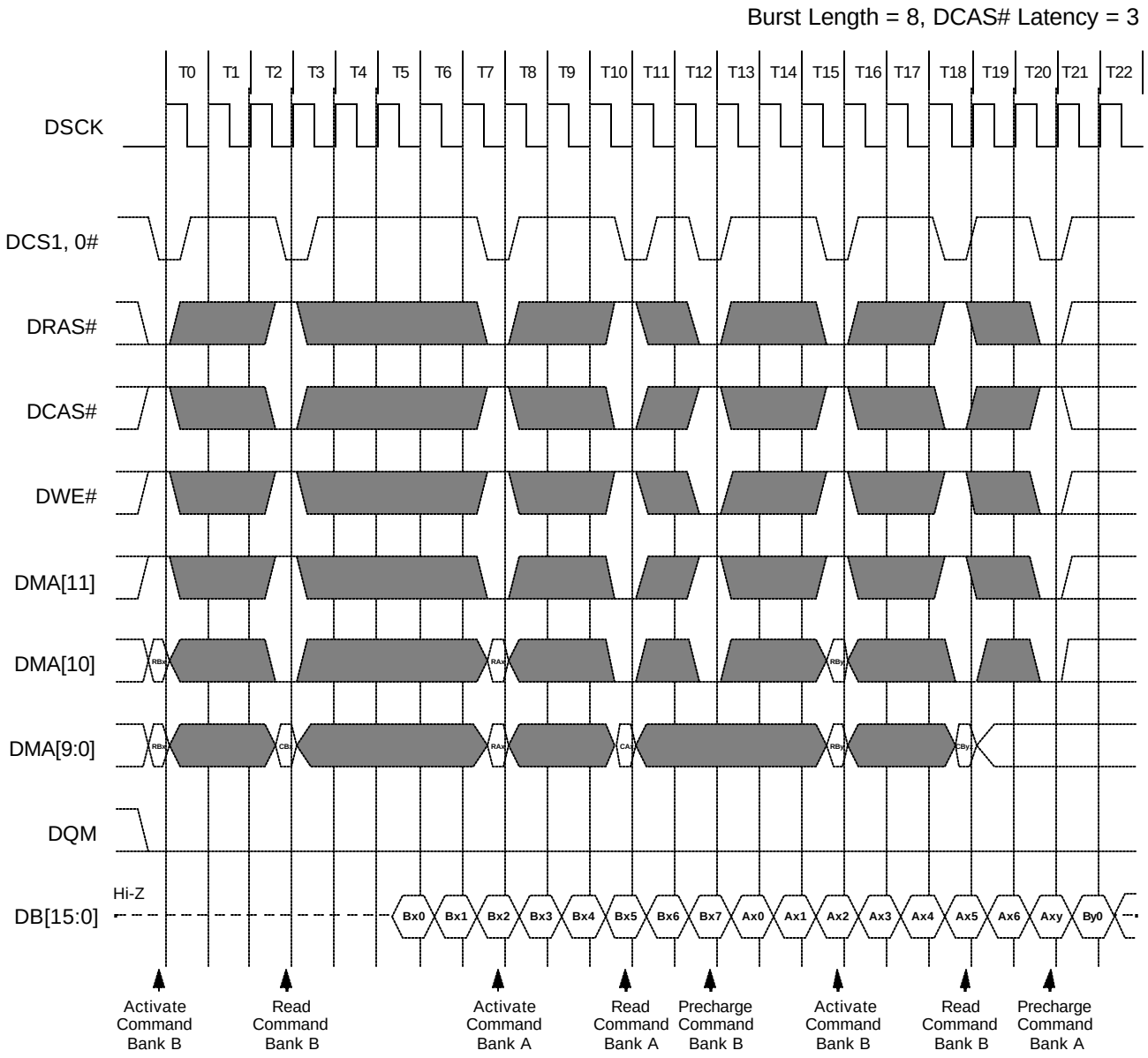


Figure 22 SDRAM Random Row Read Timing

Burst Length = 8, DCAS# Latency

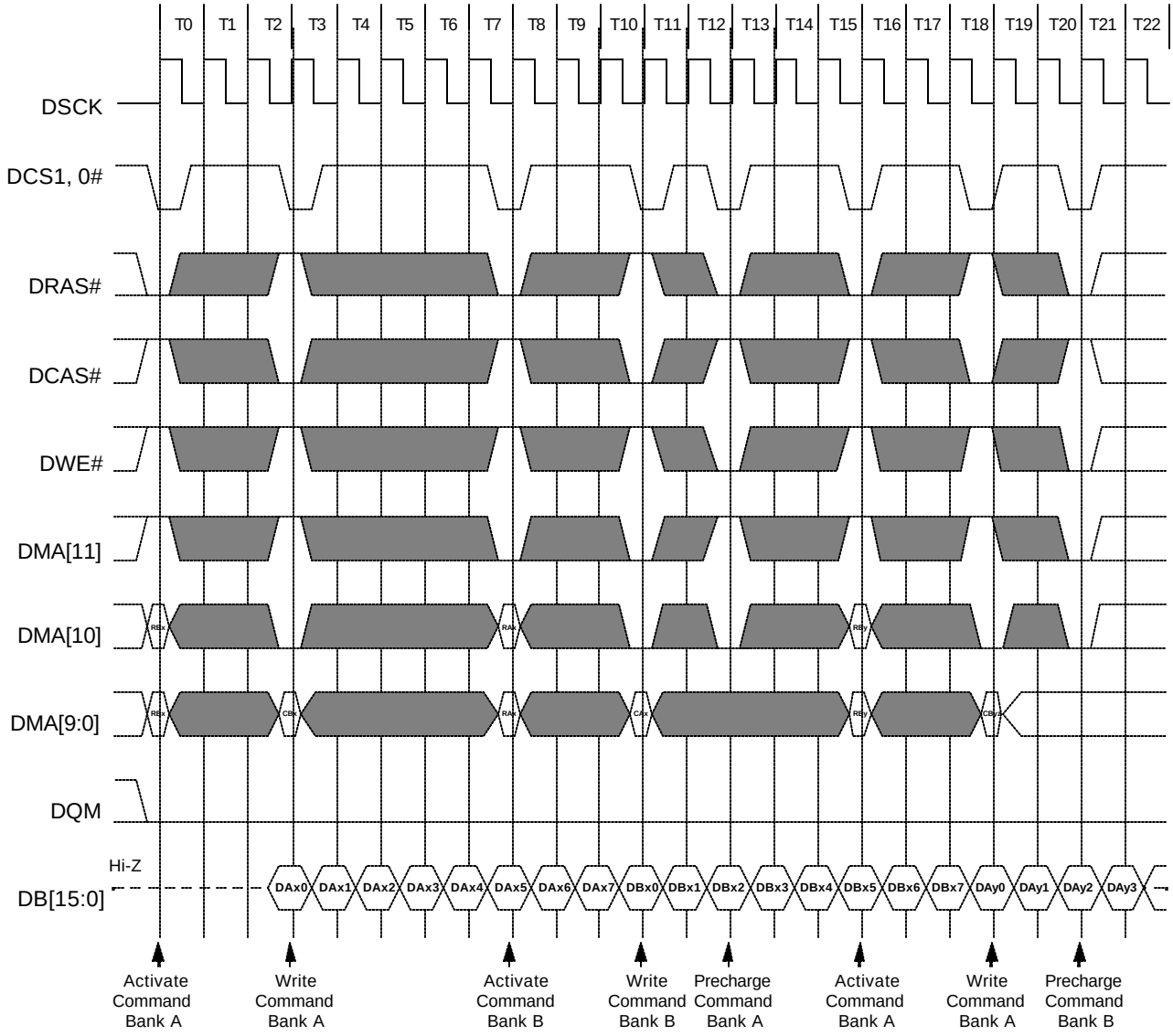


Figure 23 SDRAM Random Row Write Timing

Table 11 SDRAM Interface Timing

Symbol	Parameter (CAS Latency = 3)	Minimum	Maximum	Unit
tRRD	Row active to Row Active Delay	2		CLK
tRCD	DRAS# to DCAS# Delay	3		
tRP	Row precharge time	3		
tRAS	Row active time	6	200	
tRC	Row cycle time	10		
tCDL	Last data in to new column address delay	1		
tRDL	Last data in to row precharge	1		
tBDL	Last data in to burst stop	1		
tCCD	Column address to column address delay	1		

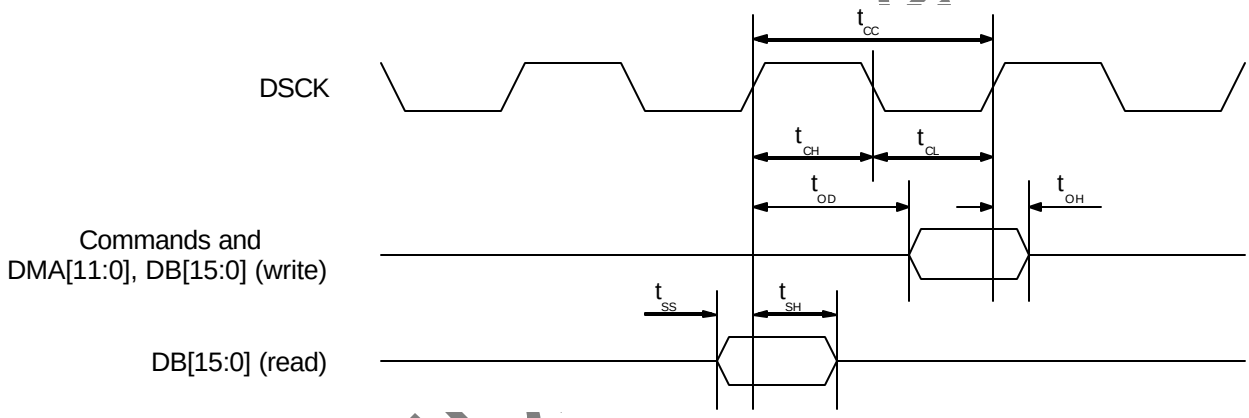


Figure 24 DMPX SDRAM Read and Write Timing

Table 12 SDRAM Read and Write Timing

Symbol	Parameter (CAS Latency = 3)	Minimum	Maximum	Unit
tCC	CLK cycle time	7.5		ns
tOD	CLK to valid output delay		6	ns
tOH	**Output data hold time**	**2**		**ns**
tCH	CLK high pulse width	3		ns
tCL	CLK low pulse width	3		ns
tSS	Input setup time	1.0		ns
tSH	Input hold time	0.5		ns
tSLZ	CLK to output in low-Z	1		ns
tSHZ	CLK to output in Hi-Z		6	ns

TDM Interface Timing

The TDM interface timing diagram for the DMPX is shown in Figure 24.

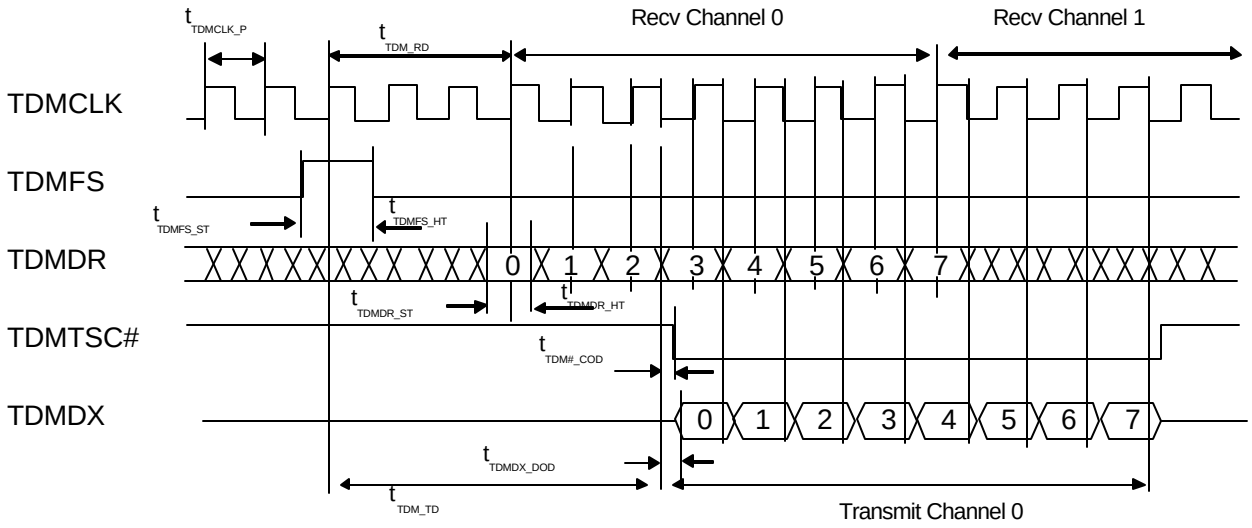


Figure 24 TDM Interface Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
tTDMCLK_P	TDM clock period	62.5			ns
tTDM#_COD	TDMTSC# control output delay to TDMCLK	0		2	
tTDMFS_ST	TDMFS setup time to TDMCLK	4			
tTDMFS_HT	TDMFS hold time to TDMCLK	2			
tTDMDR_ST	TDMDR data setup time to TDMCLK	4			
tTDMDR_HT	TDMDR data hold time to TDMCLK	2			
tTDMDX_DOD	TDMDX data output delay to TDMCLK	0		2	
tTDM_RD	TDM receive delay to TDMFS	0		8	Internal CPU clock cycle
tTDM_TD	TDM transmit delay to TDMFS	0		8	

USB Interface Timing

The USB interface timing diagram for the DMPX is shown in .

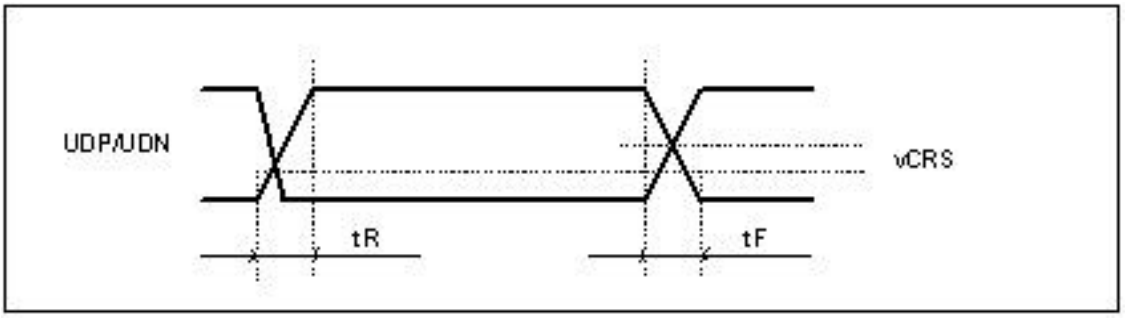


Table 13 USB Full-Speed Mode Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_R	Rise time	4		20	ns
t_F	Fall time	4		20	
t_{RFM}	Rise/Fall output	90		111	%
v_{CRS}	Cross level	1.3		2.0	V

Table 14 USB Low-Speed Mode Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_R	Rise time	75		300	ns
t_F	Fall time	75		300	
t_{RFM}	Rise/Fall output	80		125	%
v_{CRS}	Cross level	1.3		2.0	V

Table 2 USB Full Speed and Low Speed Timing

Video Timing

The video timing diagrams for the DMPX are shown in Figure 25 through Figure 26.

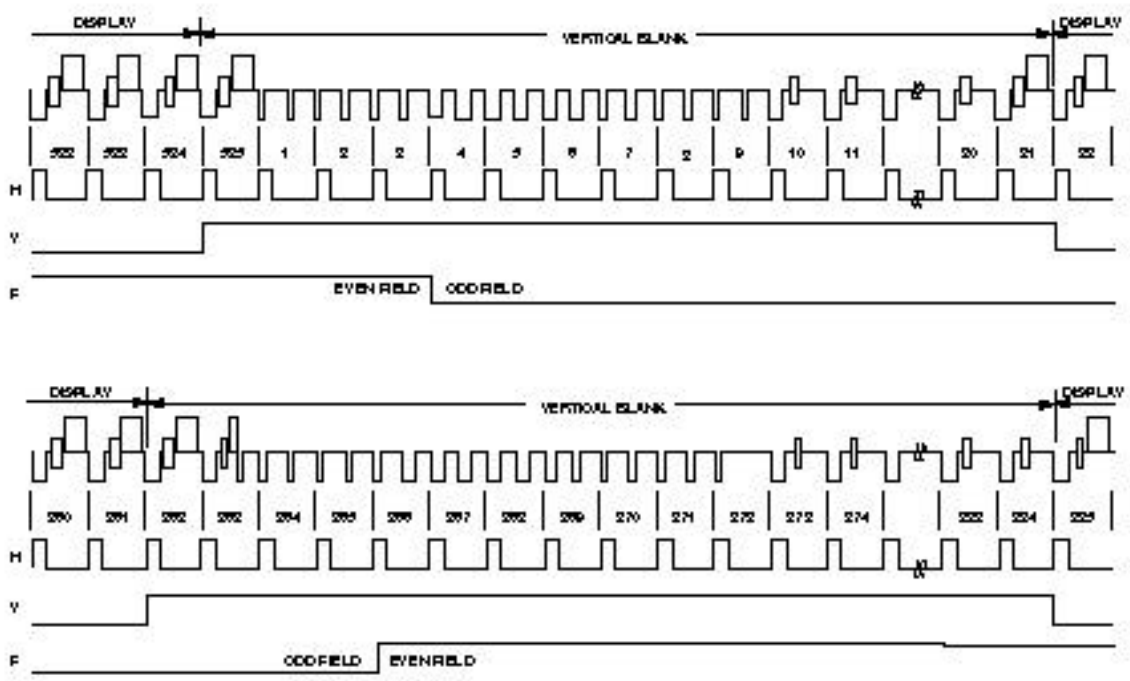


Figure 25 NTSC Timing

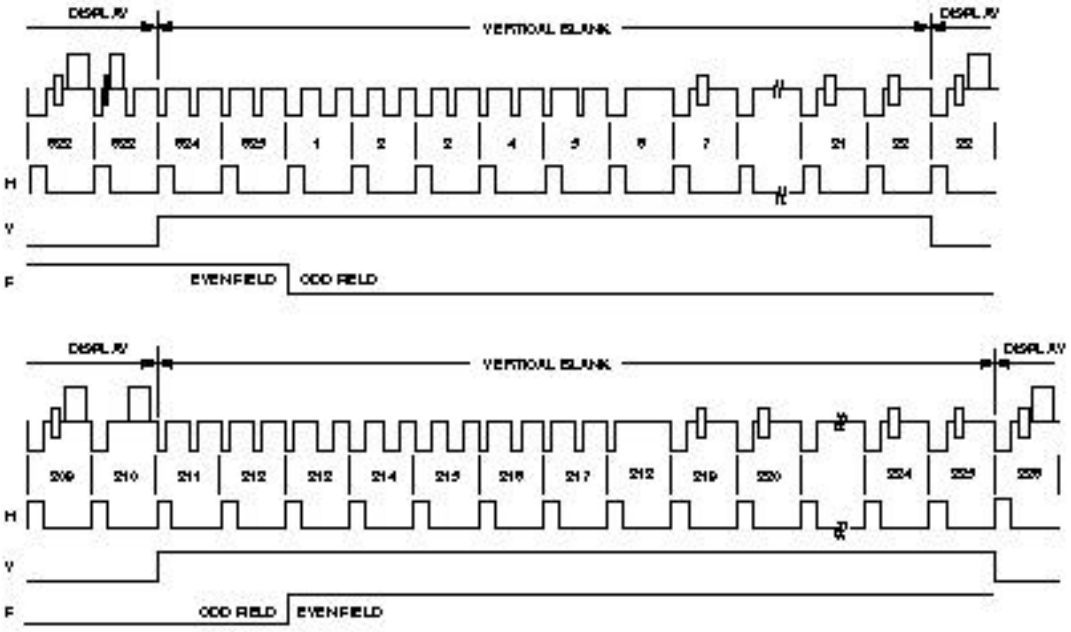


Figure 26 PAL Timing

PREAMBLE ADDRESS CODES

	Row 1	Row 2	Row 3	Row 4	Row 5	Row 6	Row 7	Row 8	Row 9	Row 10	Row 11	Row 12	Row 13	Row 14	Row 15
First byte of code pair:															
Data Channel 1	11	11	12	12	15	15	16	16	17	17	10	12	12	14	14
Data Channel 2	19	19	1A	1A	1D	1D	1E	1E	1F	1F	1C	1B	1B	1C	1C
Second byte of code pair:															
White	40	60	40	60	40	60	40	60	40	60	40	40	60	40	60
White Underline	41	61	41	61	41	61	41	61	41	61	41	41	61	41	61
Green	42	62	42	62	42	62	42	62	42	62	42	42	62	42	62
Green Underline	43	63	43	63	43	63	43	63	43	63	43	43	63	43	63
Blue	44	64	44	64	44	64	44	64	44	64	44	44	64	44	64
Blue Underline	45	65	45	65	45	65	45	65	45	65	45	45	65	45	65
Cyan	46	66	46	66	46	66	46	66	46	66	46	46	66	46	66
Cyan Underline	47	67	47	67	47	67	47	67	47	67	47	47	67	47	67
Red	48	68	48	68	48	68	48	68	48	68	48	48	68	48	68
Red Underline	49	69	49	69	49	69	49	69	49	69	49	49	69	49	69
Yellow	4A	6A	4A	6A	4A	6A	4A	6A	4A	6A	4A	4A	6A	4A	6A
Yellow Underline	4B	6B	4B	6B	4B	6B	4B	6B	4B	6B	4B	4B	6B	4B	6B
Magenta	4C	6C	4C	6C	4C	6C	4C	6C	4C	6C	4C	4C	6C	4C	6C
Magenta Underline	4D	6D	4D	6D	4D	6D	4D	6D	4D	6D	4D	4D	6D	4D	6D
White Italics	4E	6E	4E	6E	4E	6E	4E	6E	4E	6E	4E	4E	6E	4E	6E
White Italics Underline	4F	6F	4F	6F	4F	6F	4F	6F	4F	6F	4F	4F	6F	4F	6F
Indent 0	50	70	50	70	50	70	50	70	50	70	50	50	70	50	70
Indent 0 Underline	51	71	51	71	51	71	51	71	51	71	51	51	71	51	71
Indent 4	52	72	52	72	52	72	52	72	52	72	52	52	72	52	72
Indent 4 Underline	53	73	53	73	53	73	53	73	53	73	53	53	73	53	73
Indent 8	54	74	54	74	54	74	54	74	54	74	54	54	74	54	74
Indent 8 Underline	55	75	55	75	55	75	55	75	55	75	55	55	75	55	75
Indent 12	56	76	56	76	56	76	56	76	56	76	56	56	76	56	76
Indent 12 Underline	57	77	57	77	57	77	57	77	57	77	57	57	77	57	77
Indent 16	58	78	58	78	58	78	58	78	58	78	58	58	78	58	78
Indent 16 Underline	59	79	59	79	59	79	59	79	59	79	59	59	79	59	79
Indent 20	5A	7A	5A	7A	5A	7A	5A	7A	5A	7A	5A	5A	7A	5A	7A
Indent 20 Underline	5B	7B	5B	7B	5B	7B	5B	7B	5B	7B	5B	5B	7B	5B	7B
Indent 24	5C	7C	5C	7C	5C	7C	5C	7C	5C	7C	5C	5C	7C	5C	7C
Indent 24 Underline	5D	7D	5D	7D	5D	7D	5D	7D	5D	7D	5D	5D	7D	5D	7D
Indent 28	5E	7E	5E	7E	5E	7E	5E	7E	5E	7E	5E	5E	7E	5E	7E
Indent 28 Underline	5F	7F	5F	7F	5F	7F	5F	7F	5F	7F	5F	5F	7F	5F	7F

NOTE: All Indent codes (second byte equals 50h/5Dh, 70h/7Dh) assign white as the color attribute.

Table 15 Line 21 Preamble Address Codes (Same As FCC Part 15.119)

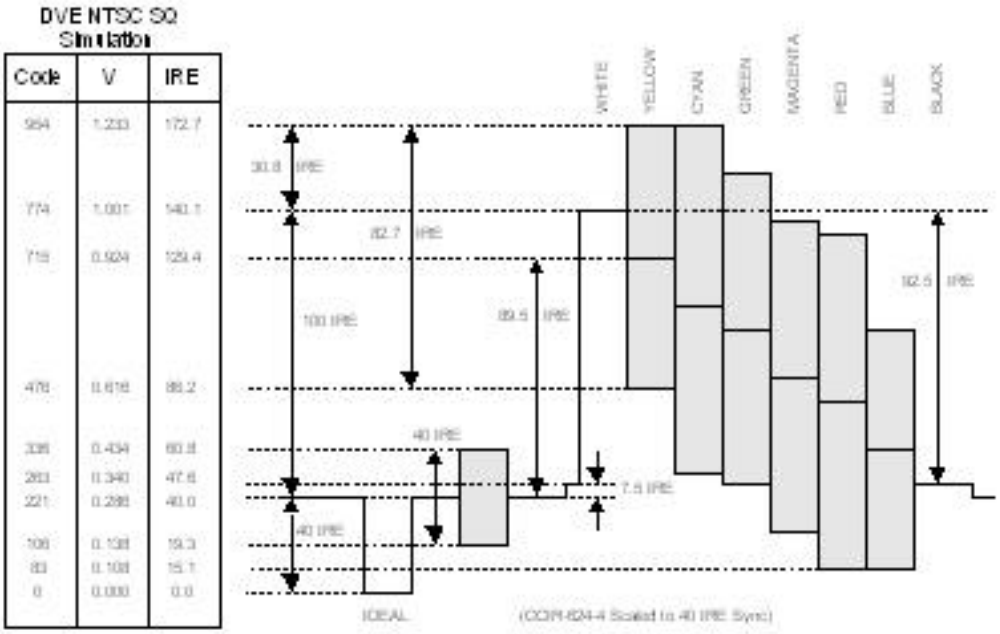


Figure 27 NTSC Composite (VDAC) Line Output Waveform

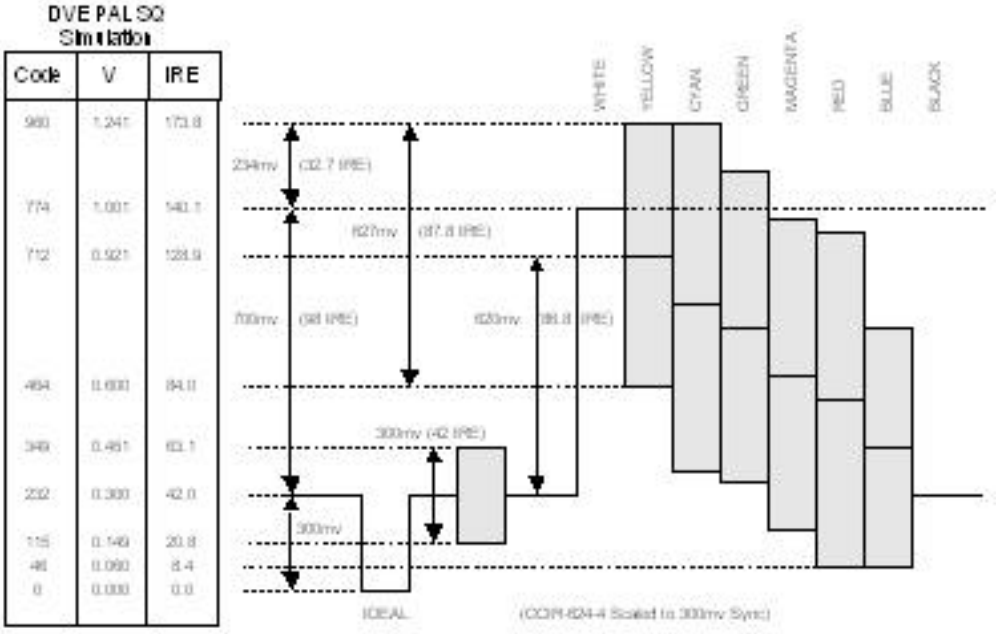


Figure 28 PAL Composite (VDAC) Line Output Waveform

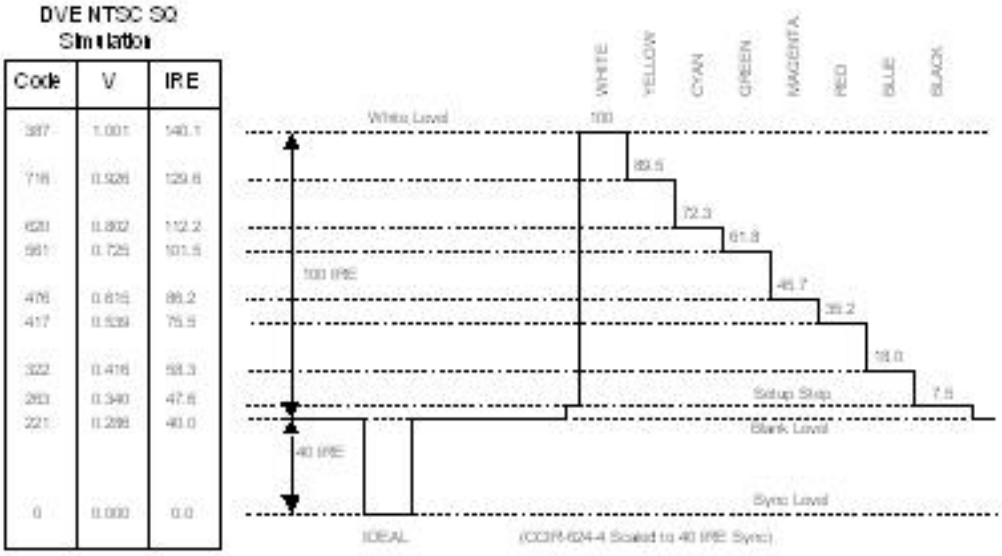


Figure 29 Luma (YDAC) Line Output Waveform

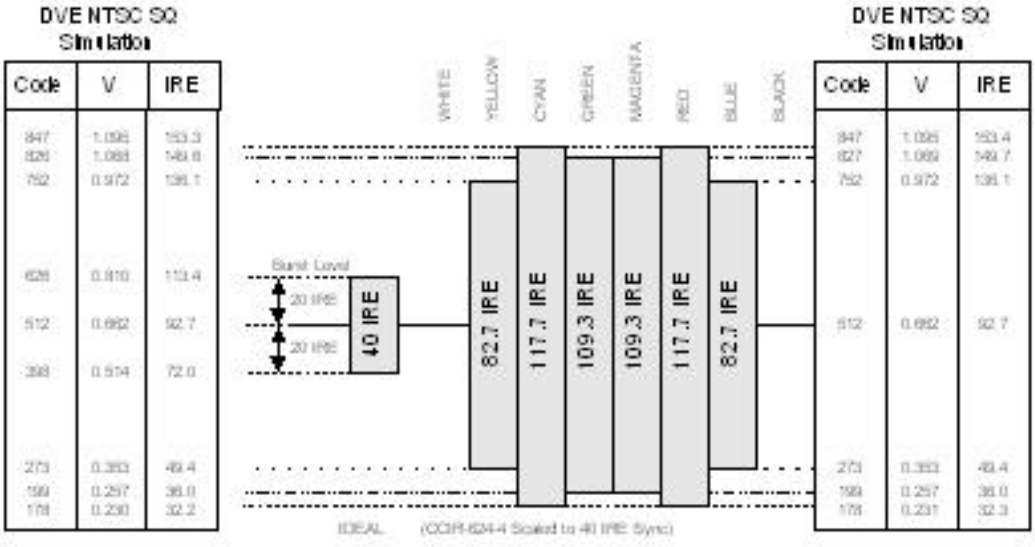


Figure 30 Chroma (CDAC) Line Output Waveform

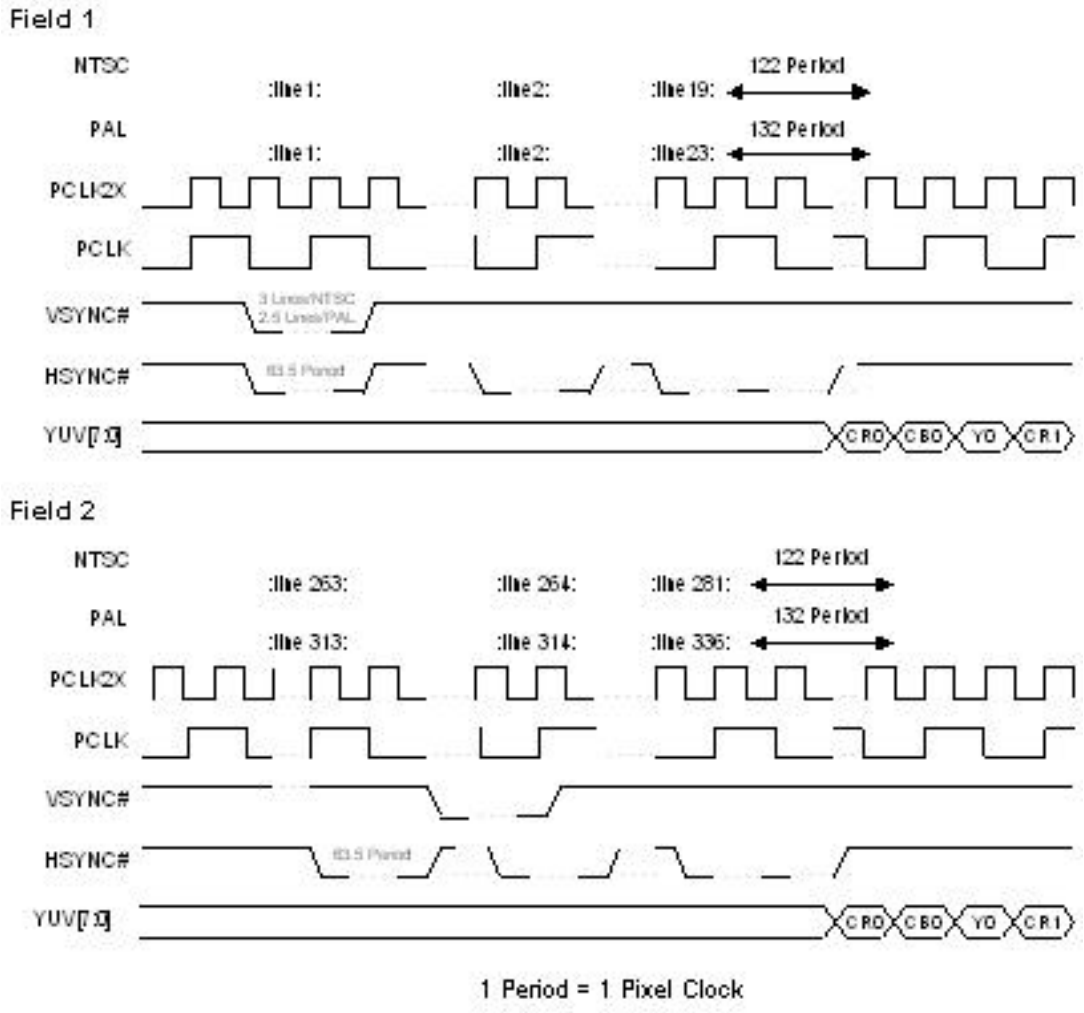


Figure 31 Sync and Pixel Clock Timings

Video AC Output to HDMI Transmitter Timing

The 12-/24-bit YCbCr output to the HDMI transmitter is shown in Figure 32 through Figure 34. Values shown are for normal operating conditions unless otherwise specified.

Table 16 Video AC Output to HDMI Transmitter

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
tCIP	IDCK Period, one pixel per clock		13.5		37	ns		
fCIP	IDCK Frequency, one pixel per clock		25		74.25	MHz		
tCIP12	IDCK Period, dual-edge clock		12.3		40	ns		
fCIP12	IDCK Frequency, dual-edge clock		27		81	MHz		
tDUTY	IDCK Duty Cycle		40%		60%	TCIP		
TIJIT	Worst Case IDCK Clock Jitter				2.0	ns		,
tSIDF	Setup Time to IDCK falling edge (EDGE = 0)	single-edge clocking mode	1.5			ns		
tHIDF	Hold Time to IDCK falling edge (EDGE = 0)		0.5			ns		
tSIDR	Setup Time to IDCK rising edge (EDGE = 0)		0.7			ns		
tHIDR	Hold Time to IDCK rising edge (EDGE = 0)		1.1			ns		
tSIDD	Setup Time to IDCK rising or falling edge	12-bit dual-edge clocking mode	1.3			ns		
tHIDD	Hold Time to IDCK rising or falling edge		0.8			ns		

Notes:

1. t_{CIP} and f_{CIP} apply in single-edge clocking modes. t_{CIP} is the inverse of f_{CIP} and is not a controlling specification.
2. t_{CIP12} and f_{CIP12} apply in dual-edge mode. t_{CIP12} is not a controlling specification.
3. Input clock jitter estimated by triggering a digital scope at the rising edge of input clock, and measuring the peak-to-peak time spread of the rising edge of input clock 1 microsecond after the triggering.
4. Actual jitter tolerance may be higher depending on the frequency of the jitter.
5. Setup and hold time specifications apply to Data, DE, VSYNC and HSYNC input pins, relative to IDCK input clock.
6. Setup and hold limits are not affected by EDGE bit setting for 12-bit, dual-edge clocking mode.

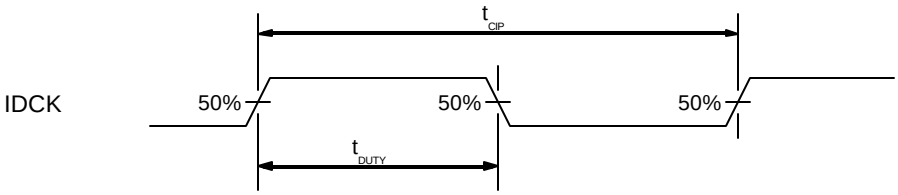


Figure 32 IDCK Clock for Output to HDMI Timing

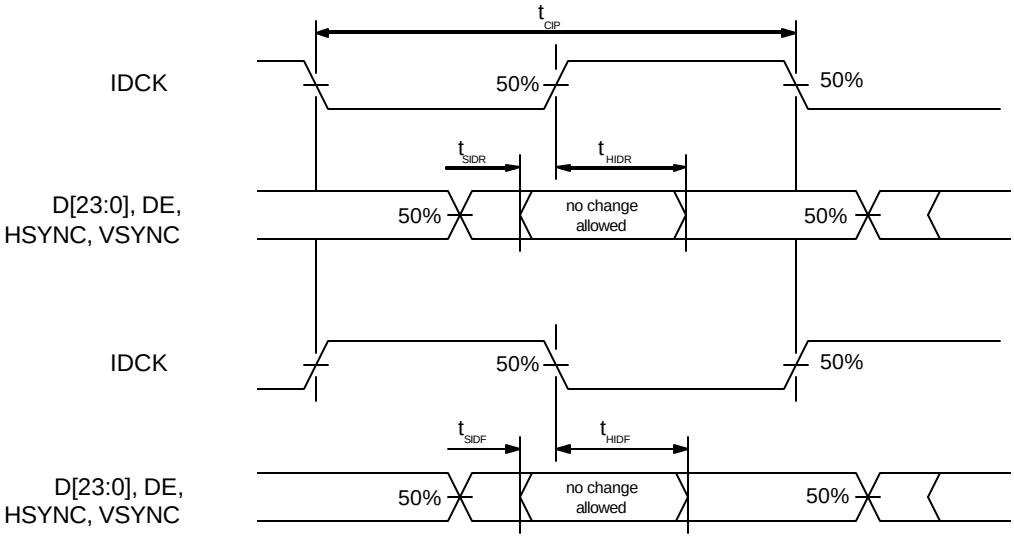


Figure 33 Single-Edge Output to HDMI Timing

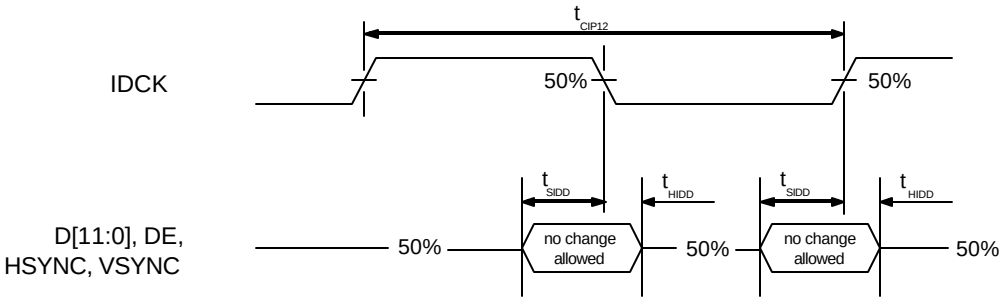


Figure 34 Dual-Edge Output to HDMI Timing

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Storage temperature range	–65° C to 150° C
Operating temperature range	0° C (ambient) to 85° C (case)
Voltage range for 5V tolerant input pins	–0.5 V to +5.5 V
Voltage range on all other pins	–0.5 V to (VD33 +0.5 V)

Recommended Operating Conditions

Operating temperature range	0° C (ambient) to 85° C (case)
Supply voltage VDD / DVCC	TBD
Supply voltage VD33 / AVDD33	3.30V ± 5%
Supply voltage VD33_DAC	3.30V ± 5%
Supply voltage VD33PLL	3.30V ± 5%

Power Dissipation

Power dissipation	TBD

WARNING: **Stress beyond those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section of this specification is not implied. Exposure to the Absolute Maximum Ratings conditions for extended periods may affect device reliability. For case temperatures exceeding 85° C, a heatsink may be required.**

WARNING: **Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.**

Electrical characteristics for the DMPX are listed in Table 17 through Table 19.

DC Electrical Characteristics

Table 17 DC Electrical Characteristics

Symbol	Parameter	Minimum	Maximum	Unit	Comments
VIH	High-level input voltage	2.0	VD33	V	All inputs TTL levels except CLK and 5V tolerant input pins
		2.0	5.5	V	All 5V tolerant inputs
VIL	Low-level input voltage	0.3	0.8	V	All inputs TTL levels except CLK
VCLKH	CLK high-level input	2.0	VD33 +0.25	V	TTL level input
VCLKL	CLK low-level input	0.3	0.8	V	
VOH	High-level output voltage	3.0		V	IOH = 1 mA
VOL	Low-level output voltage		0.45	V	IOL = 4 mA
ILI	Input leakage current		±15	µA	
ILO	Output leakage current		±15		
CIN	Input capacitance		10	pF	fc = 1 MHz
CO	Input/output capacitance		12		
CCLK	CLK capacitance		20	pF	fc = 1 MHz

Table 18 Video DAC DC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
DAC resolution		10		bits
Integral linearity (INL)		±2	±2	LSB
Differential linearity error (DNL)		±0.5	±1	LSB
Gain error			±5	%
DAC output impedance		20K		Ω
Output current-DAC	33.5	35.2	36.5	mA
Internal reference voltage (VREF)	1.17	1.235	1.29	V
Output load	34	37.5	42	Ω
Output capacitance			40	pF

AC Electrical Characteristics

Table 19 Video DAC AC Electrical Characteristics

Parameter	Minimum	Typical	Maximum	Unit
D/A Input Clock Rate			15	ns
Clock to Valid Output			15	
Analog Output Skew			30	

Output Rise and Fall Time		8	10	
Output Settling Time			12	
Glitch Energy		150	300	pYs
Power Dissipation		2.0		W
SLX On to Output Sleep			165	ns
SLX Off to Output Awake			1550	
SL On to Output Sleep			1665	
SL Off to Output Awake			62.2	ms

Audio Performance

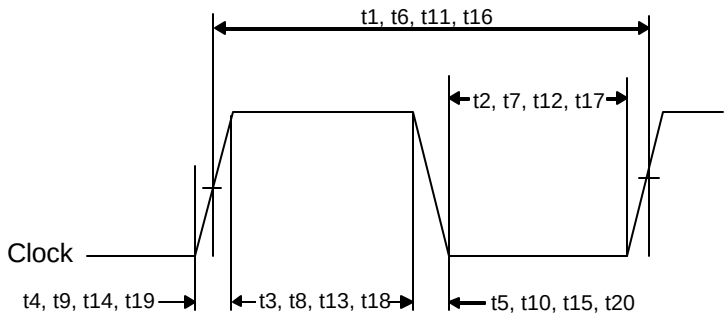
lists the audio performance characteristics of the digital audio processor of the DMPX under normal operating conditions.

Table 20 Audio Performance

Parameter	Minimum	Typical	Maximum	Unit
ADC Resolution	16		24	Bit
ADC Data Sample Rate	8		192	KHz
ADC Dynamic Range	78	80		dB
ADC THD		0.1	0.15	%
DAC Resolution	16		24	Bit
DAC Sample Rate	8		192	KHz
DAC THD+Noise	84	86	88	dB
DAC Dynamic Range	90	94	98	dB
DAC Bandwidth	3.63		20	KHz

Device Clock Characteristics

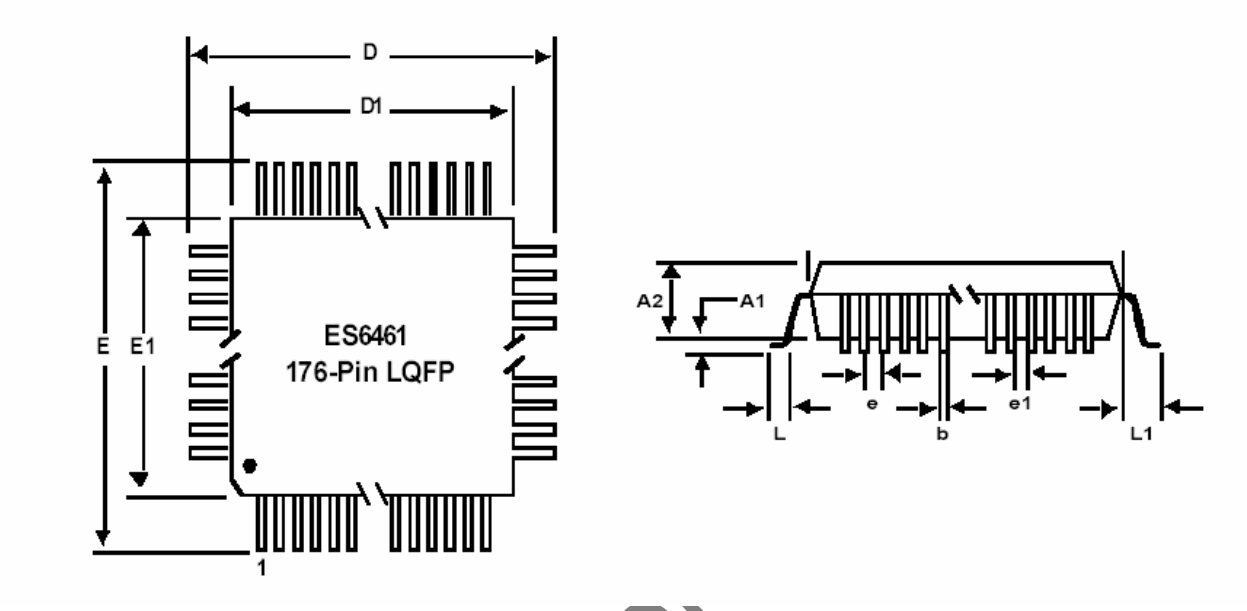
Device clock characteristics for the DMPX are shown in Figure 35 .



Symbol		Parameter	Minimum	Typical	Maximum	Unit	Comments
t1	tCLK_P	Clock period	30		100	ns	
t2	tCLK_LT	Clock low time	15			ns	
t3	tCLK_HT	Clock high time	15			ns	
t4	tCLK_RT	Clock rise time			6	ns	
t5	tCLK_FT	Clock fall time			6	ns	
t6	tPCLK_P	Pixel clock period	33			ns	
t7	tPCLK_LT	Pixel clock low time	15			ns	
t8	tPCLK_HT	Pixel clock high time	15			ns	
t9	tPCLK_RT	Pixel clock rise time			4	ns	
t10	tPCLK_FT	Pixel clock fall time			4	ns	
t11	tACLK_P	Audio clock period	40			ns	T = 1/192 kHz X 128
t12	tACLK_LT	Audio clock low time	9			ns	
t13	tACLK_HT	Audio clock high time	9			ns	
t14	tACLK_RT	Audio clock rise time			6	ns	
t15	tACLK_FT	Audio clock fall time			6	ns	
t16	tTDMCLK_P	TDM clock period	40			ns	T = 1/96 kHz X 256
t17	tTDMCLK_LT	TDM clock low time	14			ns	
t18	tTDMCLK_HT	TDM clock high time	14			ns	
t19	tTDMCLK_RT	TDM clock rise time			6	ns	
t20	tTDMCLK_FT	TDM clock fall time			6	ns	

Figure 35 Pixel, Doubled Pixel, TDM and Audio Master Clock Timing

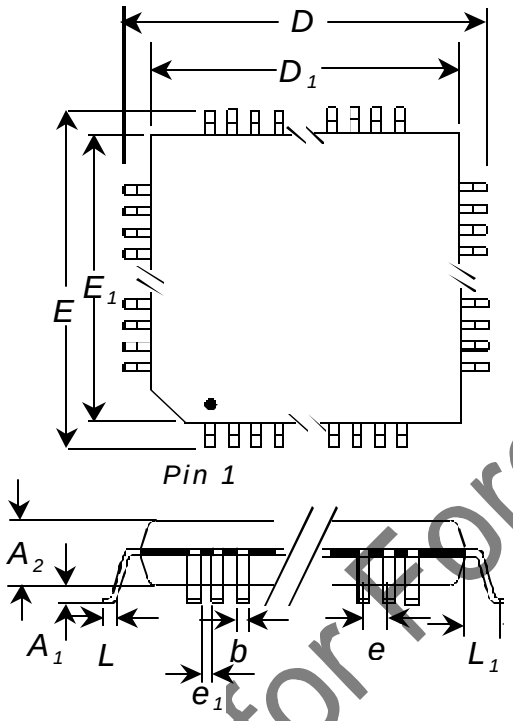
176 Pin LQFP Mechanical Dimensions



Symbol	Description	Millimeters		
		Minimum	Nominal	Maximum
D	Lead to lead, X-axis	--	22.00 BSC.	--
D1	Package's outside, X-axis	--	20.00 BSC.	--
E	Lead to lead, Y-axis	--	22.00 BSC.	--
E1	Package's outside, Y-axis	--	20.00 BSC.	--
A1	Board standoff	0.05	--	0.15
A2	Package thickness	1.35	1.40	1.45
b	Lead width	0.13	0.16	0.23
e	Lead pitch	--	0.40 BSC.	--
e1	Lead gap	0.27 REF	0.24 REF	0.17 REF
L	Foot length	0.45	0.60	0.75
L1	Lead length	--	1.00 REF	--
--	Foot angle	0°	--	7°
--	Co planarity	--	--	0.102
--	Number of leads in X-axis	--	44	--
--	Number of leads in Y-axis	--	44	--
--	Total number of leads	--	176	--
--	Package type	--	LQFP	--

For lead-free devices, the solder paste and PCB finish/plating must be 100% lead-free in order to ensure proper solderability.

128 Pin LQFP Mechanical Dimensions



		MILLIMETERS		
Symbol	**Description**	**Min.**	**Nom.**	**Max.**
D	Lead-to Lead, X-axis	15.75	16.00	16.25
D1	Package's Outside, X-axis	13.90	14.00	14.10
E	Lead-to Lead, Y-axis	15.75	16.00	16.25
E1	Package's Outside, Y-axis	13.90	14.00	14.10
A1	Board Standoff	0.05	0.10	0.15
A2	Package Thickness	1.35	1.40	1.45
b	Lead Width	0.13	0.16	0.23
e	Lead Pitch		0.40 BSC	
e_1	Lead Gap	0.17	0.24	0.27
L	Foot Length	0.45	0.60	0.75
L1	Lead Length		1.00	
	Co planarity			0.102
	Foot Angle	0º		7º
	No. of Leads in X-axis		32	
	No. of Leads in Y-axis		32	
	No. of Leads Total		128	
	Package Type		LQFP/TQFP	

ORDERING INFORMATION

Part Number	Description	Package
ES6460SAA	Digital Media Processor for Photo Frame	128-pin LQFP
ES6461SAA	Digital Media Processor for Photo Frame / HDD Player	176-pin LQFP
ES6461SAB	Digital Media Processor for Photo Frame / HDD Player with Dolby	176-pin LQFP

The letter S at the end of the part number identifies the package type LQFP.

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