Analog Reinvented

ES9039MSPRO & ES9039SPRO

32-bit High-Performance 8 Channel DAC

Product Datasheet

The ESS SABRE® ES9039MSPRO & ES9039SPRO are the fully redesigned flagship 32-bit 8 Channel digital-to-analog converters (DAC) that target high end consumer devices and professional audio applications. It was designed to create the new generation of the world's highest performing audio DAC.

The ES9039PRO has 8 integrated DACs which use ESS' patented Hyperstream® IV DAC Architecture. Using the QUAD modulator architecture, it delivers unprecedented SABRE PRO™ audio sound quality and specifications, including a world class +132dB DNR per channel, +140dB DNR and a THD+N of -122dB in mono mode.

The ES9039PRO SABRE® DAC improves on previous designs to include:

- TDM audio format & SPI serial communication support for more connectivity options.
- Lower power consumption than previous generations, including the Hyperstream IV DAC modulator.
- Hardware mode support for ease-of-use.
- MQA Hardware renderer (ES9039MPRO) to reveal the original master resolution.

TDM, DSD, DoP, and I²S, LJ, RJ master/slave interfaces are supported in synchronous or asynchronous modes. S/PDIF is supported in asynchronous mode.

The ES9039PRO has 7 built-in pre-programmed and programmable digital filters which allows the most discerning user to tune the SABRE sound to their own personal sound signature.

The ES9039MPRO includes a built-in stereo hardware MQA renderer that helps recreate the natural sound of the recording.

FEATURE	DESCRIPTION
Patented 32-bit HyperStream® IV Architecture DAC Technology	32-bit audio DAC with ultra-high dynamic range & ultra-low distortion
+140dB DNR mono mode +132db DNR per channel -122dB THD+N mono	Unprecedented dynamic range and ultra-low distortion
MQA Renderer (ES9039MPRO only)	Stereo MQA Renderer Built-In Easily paired with software MQA core decoder Eliminates the need for complicated DAC filter tuning
High Sample Rates	Up to PCM 768kHz & native DSD1024
Customizable filter characteristics	7 presets of digital optimal filters, with custom filter programmability for each channel to allow for a unique sound signature
Multiple Input formats are available	I²S, LJ, RJ, TDM, DSD, DoP and S/PDIF
I²C, SPI, and Hardware interface control	Configured by microcontroller or other I²C /SPI source, or pins through Hardware Mode
Lower Power Consumption than Previous Gen	Simplifies power supply design
Standardized Packaging	10mm x 10mm, 64 pin eTQFP for reduced PCB board space

Applications

- Professional Digital Audio Workstation (DAW) audio playback
- Personal Audio Devices, Media Streamers & A/V Receivers and High End Audiophile Equipment
- Car Audio including In Dash systems
- Any equipment that benefits from the very best SABRE PRO™ audio digital-to-analog conversion

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Functional Block Diagram

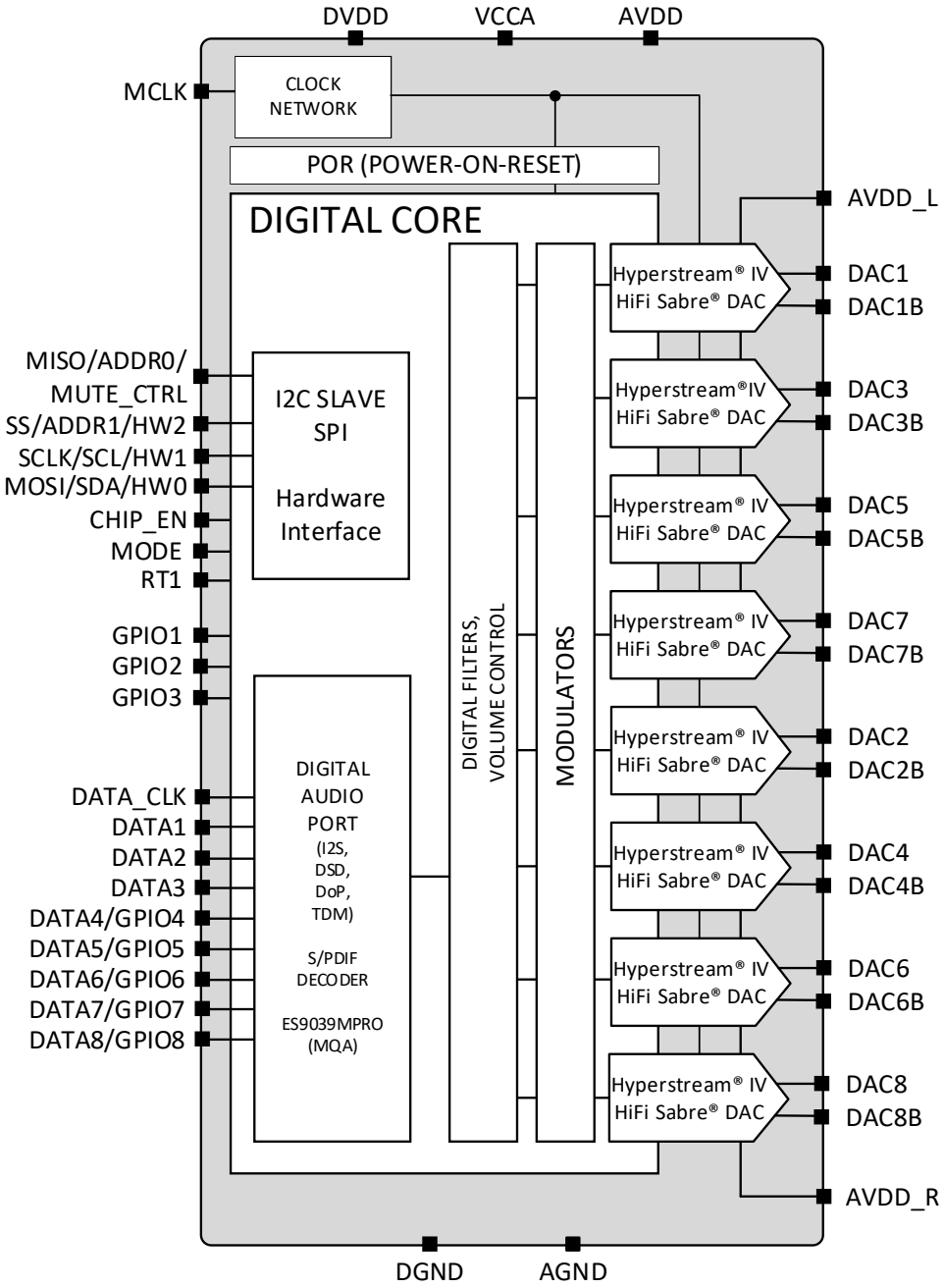


Figure 1 - ES9039MPRO & ES9039PRO

ES9039MPRO/ES9039PRO Pinout[1]

64 QFP Pinout

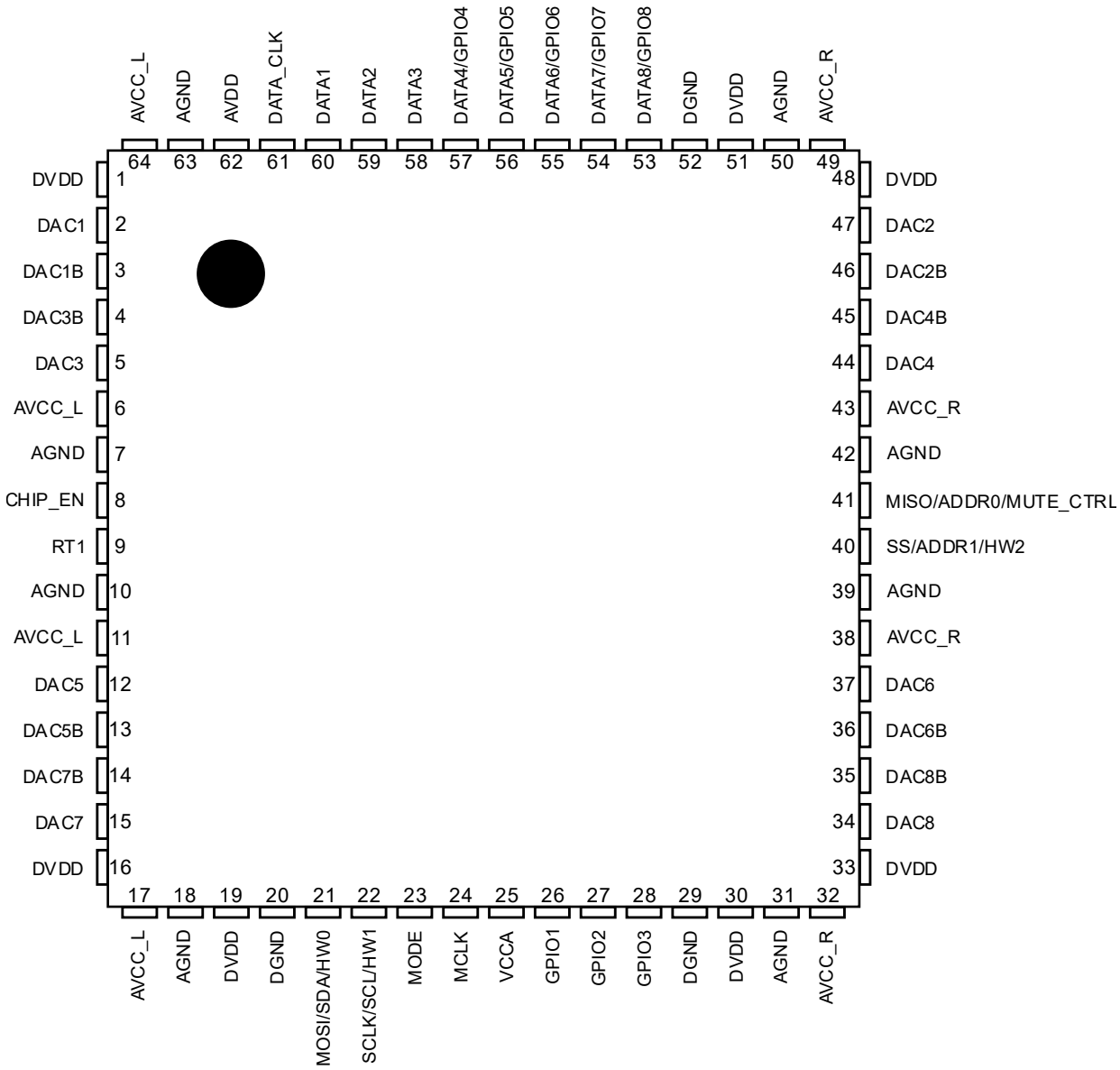


Figure 2 - 64QFN Pinout

[1] Pin 65 is a package pad, used for AGND, and should be connected to Analog Ground

64 QFP Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	DVDD	Power	Power	Digital Core Supply, 1.2V
2	DAC1	AO	Ground	Differential Positive Output for Channel 1
3	DAC1B	AO	Ground	Differential Negative Output for Channel 1
4	DAC3B	AO	Ground	Differential Negative Output for Channel 3
5	DAC3	AO	Ground	Differential Positive Output for Channel 3
6	AVCC_L	Power	Power	3.3V DAC analog output stage reference supply for the Left side
7	AGND	Ground	Ground	DAC analog output stage ground
8	CHIP_EN	I	HiZ	Active-high Chip Enable
9	RT1	I	HiZ	Reserved. Must be connected to DGND for normal operation.
10	AGND	Ground	Ground	DAC analog output stage ground
11	AVCC_L	Power	Power	3.3V DAC analog output stage reference supply for the Left side
12	DAC5	AO	Ground	Differential Positive Output for Channel 5
13	DAC5B	AO	Ground	Differential Negative Output for Channel 5
14	DAC7B	AO	Ground	Differential Negative Output for Channel 7
15	DAC7	AO	Ground	Differential Positive Output for Channel 7
16	DVDD	Power	Power	Digital Core Supply, 1.2V
17	AVCC_L	Power	Power	3.3V DAC analog output stage reference supply for the Left side
18	AGND	Ground	Ground	DAC analog output stage ground
19	DVDD	Power	Power	Digital Core Supply, 1.2V
20	DGND	Ground	Ground	Digital Ground
21	MOSI	I	HiZ	SPI Main Out Sub In pin, controlled by MODE
	SDA			I²C Serial Data pin, controlled by MODE
	HW0			Hardware 0 interface pin, controlled by MODE
22	SCLK	I	HiZ	SPI Serial Clock pin, controlled by MODE
	SCL			I²C Serial Clock pin, controlled by MODE
	HW1			Hardware 1 interface pin, controlled by MODE
23	MODE	I	HiZ	I²C /SPI Control selection or HW mode
24	MCLK	I	HiZ	Oscillator input
25	VCCA	Power	Power	Analog Supply, 3.3V
26	GPIO1	I/O	HiZ	General I/O w/extended functions
27	GPIO2	I/O	HiZ	General I/O w/extended functions
28	GPIO3	I/O	HiZ	General I/O w/extended functions
29	DGND	Ground	Ground	Digital Ground
30	DVDD	Power	Power	Digital Supply, 1.2V
31	AGND	Ground	Ground	DAC analog output stage ground
32	AVCC_R	Power	Power	3.3V DAC analog output stage reference supply for the Right side
33	DVDD	Power	Power	Digital Supply, 1.2V
34	DAC8	AO	Ground	Differential Positive Output for Channel 8
35	DAC8B	AO	Ground	Differential Negative Output for Channel 8
36	DAC6B	AO	Ground	Differential Negative Output for Channel 6
37	DAC6	AO	Ground	Differential Positive Output for Channel 6
38	AVCC_R	Power	Power	3.3V DAC analog output stage reference supply for the Right side
39	AGND	Ground	Ground	DAC analog output stage ground
40	SS	I	HiZ	SPI Slave Select pin, controlled by MODE

	ADDR1			I²C Address 1 pin, controlled by MODE
	HW2			Hardware 2 interface pin, controlled by MODE
41	MISO	I	HiZ	SPI Main In Sub Out pin, controlled by MODE
	ADDR0			I²C Address 0 pin, controlled by MODE
	MUTE_CTRL			Hardware Mute Control pin, controlled by MODE
42	AGND	Ground	Ground	DAC analog output stage ground for the Right Side
43	AVCC_R	Power	Power	3.3V DAC analog output stage reference supply for the Right side
44	DAC4	AO	Ground	Differential Positive Output for Channel 4
45	DAC4B	AO	Ground	Differential Negative Output for Channel 4
46	DAC2B	AO	Ground	Differential Negative Output for Channel 2
47	DAC2	AO	Ground	Differential Positive Output for Channel 2
48	DVDD	Power	Power	Digital Supply, 1.2V
49	AVCC_R	Power	Power	3.3V DAC analog output stage reference supply for the Right side
50	AGND	Ground	Ground	DAC analog output stage ground
51	DVDD	Power	Power	Digital Supply, 1.2V
52	DGND	Ground	Ground	Digital Core Ground
53	DATA8	I/O	HiZ	Serial DATA8
	GPIO8			General I/O 8
54	DATA7	I/O	HiZ	Serial DATA7
	GPIO7			General I/O 7
55	DATA6	I/O	HiZ	Serial DATA6
	GPIO6			General I/O 6
56	DATA5	I/O	HiZ	Serial DATA5
	GPIO5			General I/O 5
57	DATA4	I/O	HiZ	Serial DATA4
	GPIO4			General I/O 4
58	DATA3	I	HiZ	Serial DATA3 pin
59	DATA2	I	HiZ	Serial DATA2 pin
60	DATA1	I	HiZ	Serial DATA1 pin
61	DATA_CLK	I	HiZ	Serial Data Clock pin
62	AVDD	Power	Power	3.3V I/O Supply
63	AGND	Ground	Ground	DAC analog output stage ground
64	AVCC_L	Power	Power	3.3V DAC analog output stage reference supply for the Left side
65	Package Pad[1]	-	-	Connect to ground

Table 1 - Pin Descriptions

*Note: AO = Analog Output, I = Digital Input, I/O = Digital Input/Output

[1] Pin 65 is the package pad. See QFP dimensions for sizing. Connect to AGND.

Feature List

The ES9039MSPRO & ES9039SPRO are SABRE 8 channel Flagship performance digital to analog converters (DAC) with features and performance including the new Hyperstream IV modulator that produces a device that is well suited for all Consumer, Audiophile and PRO Audio applications.

These features include TDM & SPI support as well as a Hardware (HW) mode for simplifying configuration of the ES9039PRO. The ES9039MPRO includes a built in MQA renderer.

TDM / I²S / LJ / RJ / DSD / DoP interfaces are supported.

Sample rates up to 768kHz with PCM data and 7 selectable built-in digital filters as well as programmable filters. DSD rates up to DSD1024 are supported as well.

Configuration Modes

The ES9039MSPRO & ES9039SPRO supports 2 different software modes (SPI or I²C) and supports 2 different sets of hardware modes (PCM or TDM/DSD). These modes are controlled by the state of the MODE Pin (Pin 23).

MODE PIN	Configuration	Description
1	Software Mode	SPI interface
Pull 1	Hardware Mode	TDM, DSD, S/PDIF Modes
Pull 0	Hardware Mode	PCM Slave or Master Modes
0	Software Mode	I²C interface

Table 2 - Mode Pin Configuration Options

Design Information

Hardware pins can be configured four different ways. Each pin can be tied-high (1), pulled-high (Pull 1), pulled-low (Pull 0), or tied-low (0). HW0 and HW1 pins are always tied-high or tied-low. This also applies to MUTE_CTRL.

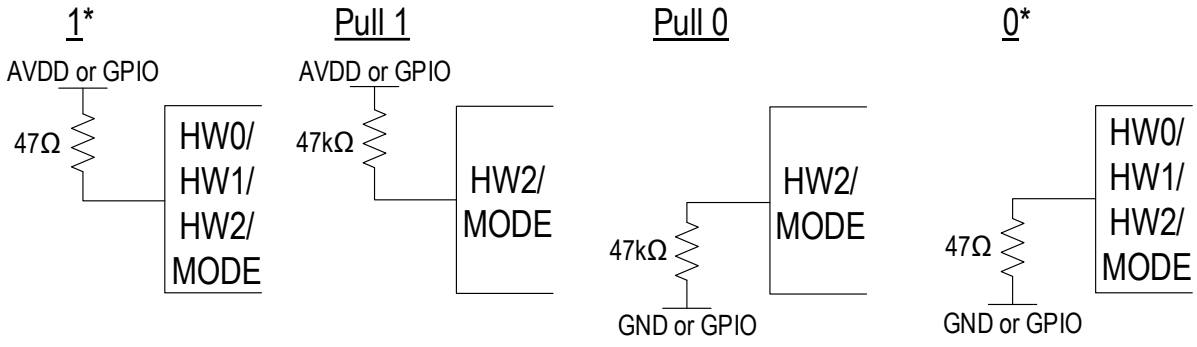


Figure 3 - Hardware Mode Pin Configurations

* Note: Hardware mode pin states 0 and 1 can be directly connected to GND or AVDD.

Software Mode

The ES9039MSPRO & ES9039SPRO support I²C or SPI serial communication. The ES9039MSPRO & ES9039SPRO have read/write register and read-only register.
Software modes are set with the MODE pin (Pin 23)

I²C Slave Interface Commands

The I²C slave interface is enabled when the MODE pin (Pin 23) is tied low (MODE=0). In I²C mode, ADDR1 (Pin 40) and ADDR0 (Pin 41) determine the I²C address and the R/W bit controls reading or writing.

For I²C Timing information, see Timing Characteristics.

The I²C Slave Interface can be accessed by:

- Pin 21 SDA
- Pin 22 SCL
- Pin 40 ADDR1
- Pin 41 ADDR0

I²C Slave Address = [5'b10010, ADDR1, ADDR0, R/W]

I²C Slave Address	ADDR1	ADDR0
0x90	0	0
0x92	0	1
0x94	1	0
0x96	1	1

Table 3 - I²C Slave Addresses

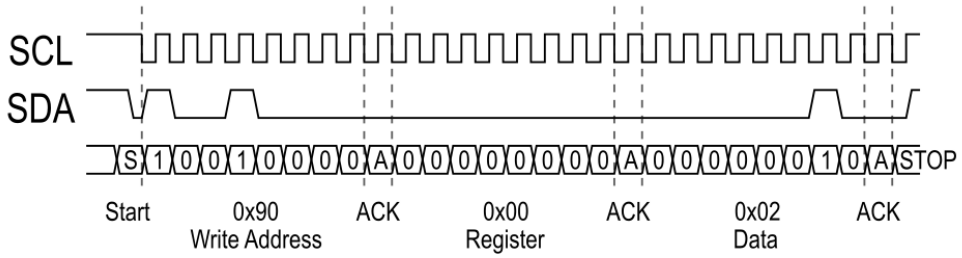


Figure 4 - I²C Write Example

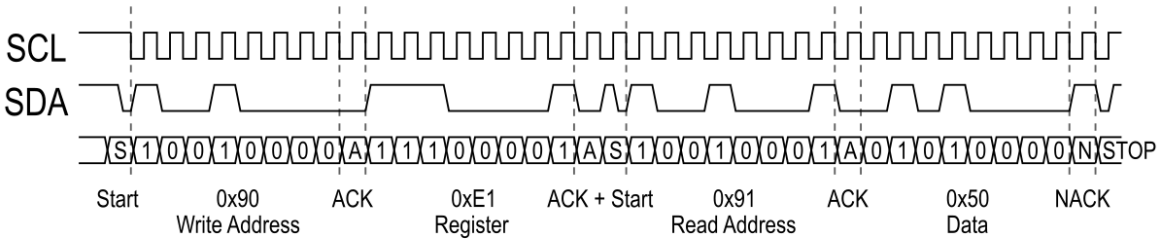


Figure 5 - I²C Read Example

Note: All bus transitions between start and stop must be part of the transaction when writing to the ESS device

SPI Slave Interface Commands

The SPI slave interface is used when the MODE pin (Pin 23) is tied high.

The SPI slave interface can be accessed using Pins 21, 22, 40, and 41.

- Pin 21 MOSI
- Pin 22 SCLK
- Pin 40 SS
- Pin 41 MISO

The 4-wire SPI data format is: Command (1 byte) + Address (1 byte) + Data.
SPI Commands:

- 0x01: Read
- 0x03: Write

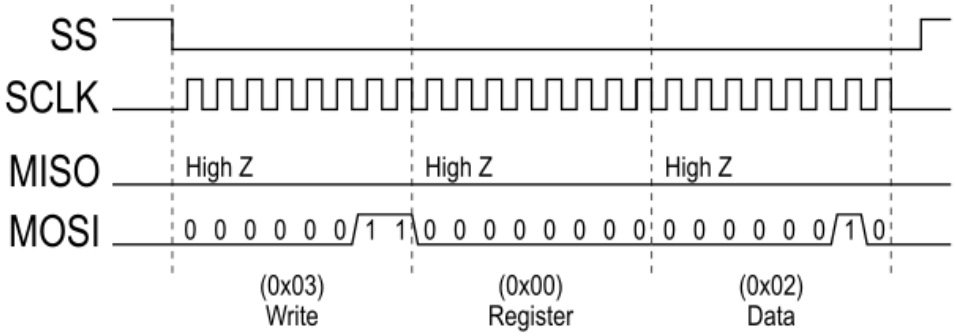


Figure 6 - SPI Single Byte Write

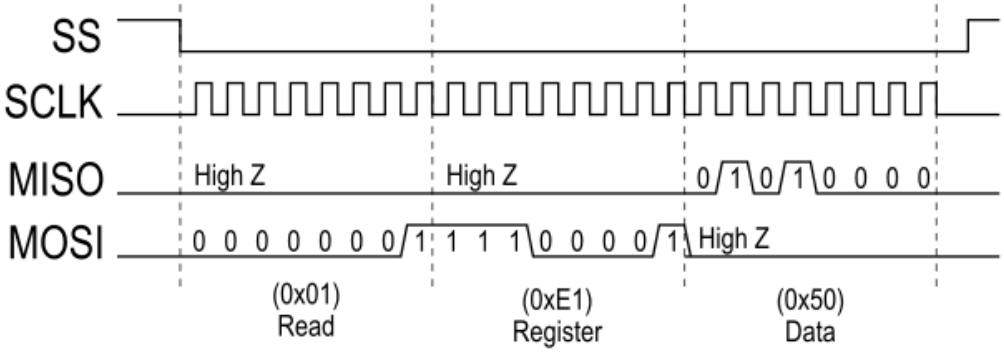


Figure 7 - SPI Single Byte Read

Hardware Mode

The ES9039MPRO & ES9039PRO have 32 pre-configured modes that can be set with external pin configuration. These modes configure the DAC for different input serial data rates and set the DAC muting.

These modes are set with pins:

- MODE (Pin 23)
- HW0 (Pin 21)
- HW1 (Pin 22)
- HW2 (Pin 40)
- MUTE_CTRL (Pin 41)

Recommended Hardware Mode Setup Sequence

The hardware mode setup sequence is shown below will all hardware pins being defined after CHIP_EN is asserted.

Note: It is recommended that MUTE_CTRL is set low until the HW mode is finalized, then asserted last.

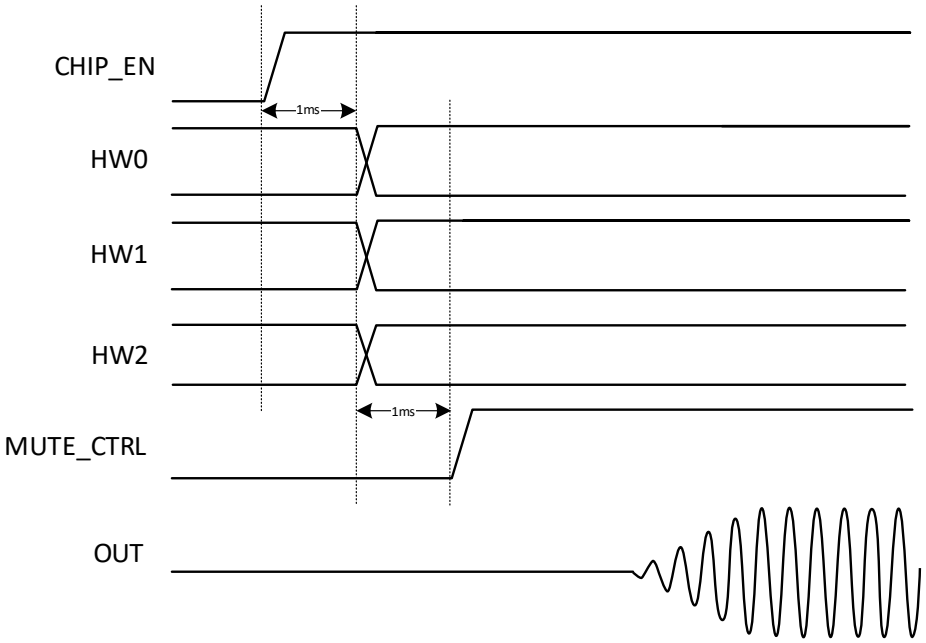


Figure 8 - Hardware Mode Startup Sequence

Hardware Mode Pin Configurations

The following table show the available hardware mode for the ES9039MPRO & ES9039PRO

HW#	Description	FS [kHz]	BCK [MHz]	MCLK [MHz]	MODE	HW2	HW1	HW0
32-bit PCM Master Modes								
0	I²S Master	MCLK/128	MCLK/2 (64*FS)	MCLK=128*FS ≤49.152	Pull 0	0	0	0
1	I²S Master	MCLK/256	MCLK/4 (64*FS)	MCLK=256*FS ≤49.152	Pull 0	0	0	1
2	I²S Master	MCLK/512	MCLK/8 (64*FS)	MCLK=512*FS ≤49.152	Pull 0	0	1	0
3	I²S Master	MCLK/1024	MCLK/16 (64*FS)	MCLK=1024*FS ≤49.152	Pull 0	0	1	1
4	LJ Master Mode	MCLK/128	64*FS	MCLK=128*FS ≤49.152	Pull 0	Pull 0	0	0
5	LJ Master Mode	MCLK/256	64*FS	MCLK=256*FS ≤49.152	Pull 0	Pull 0	0	1
6	LJ Master Mode	MCLK/512	64*FS	MCLK=512*FS ≤49.152	Pull 0	Pull 0	1	0
7	LJ Master Mode	MCLK/1024	64*FS	MCLK=1024*FS ≤49.152	Pull 0	Pull 0	1	1
32-bit PCM Slave Modes, SYNC								
8	I²S Slave SYNC, MCLK/1	8<FS<768	64*FS	64*FS≤MCLK ≤49.152	Pull 0	Pull 1	0	0
9	I²S Slave SYNC, MCLK/2	8<FS<384	64*FS	128*FS≤MCLK ≤49.152	Pull 0	Pull 1	0	1
10	I²S Slave SYNC, MCLK/4	8<FS<192	64*FS	256*FS≤MCLK ≤49.152	Pull 0	Pull 1	1	0
11	I²S Slave SYNC, Auto Clock Gear[1] (128FS)	8<FS<768	64*FS	64*FS≤MCLK ≤49.152	Pull 0	Pull 1	1	1
12	LJ Slave SYNC, MCLK/1	8<FS<768	64*FS	64*FS≤MCLK ≤49.152	Pull 0	1	0	0
13	LJ Slave SYNC, MCLK/2	8<FS<384	64*FS	128*FS≤MCLK ≤49.152	Pull 0	1	0	1
14	LJ Slave SYNC, MCLK/4	8<FS<192	64*FS	256*FS≤MCLK ≤49.152	Pull 0	1	1	0
15	LJ Slave SYNC, Auto Clock Gear[1] (128FS)	8<FS<768	64*FS	64*FS≤MCLK ≤49.152	Pull 0	1	1	1

See Table continuation on next page.

[1] ACG (Auto Clock Gearing) is enabled, it will normally gear the MCLK down to >=128*FS in SYNC, >130*FS in ASYNC, or 2*DSDCLK in DSD modes.

HW#	Description	FS [kHz]	BCK [MHz]	MCLK [MHz]	MODE	HW2	HW1	HW0
32-bit PCM Slave Modes & S/PDIF, ASYNC								
16*	S/PDIF[1], DoP[2] or I²S Slave ASYNC, MCLK/1	8<FS<384	64*FS	130*FS≤MCLK ≤50	Pull 1	0	0	0
17*	S/PDIF[1], DoP[2] or I²S Slave ASYNC, MCLK/2	8<FS<192	64*FS	260*FS<MCLK ≤50	Pull 1	0	0	1
18*	S/PDIF[1], DoP[2] or I²S Slave ASYNC, MCLK/4	8<FS<96	64*FS	520*FS≤MCLK ≤50	Pull 1	0	1	0
19	I²S Slave ASYNC, Auto Clock Gear[3] (>130FS)	8<FS<384	64*FS	130*FS≤MCLK ≤50	Pull 1	0	1	1
20	LJ Slave ASYNC, MCLK/1	8<FS<384	64*FS	130*FS≤MCLK ≤50	Pull 1	Pull 0	0	0
21	LJ Slave ASYNC, MCLK/2	8<FS<192	64*FS	260*FS<MCLK ≤50	Pull 1	Pull 0	0	1
22	LJ Slave ASYNC, MCLK/4	8<FS<96	64*FS	520*FS≤MCLK ≤50	Pull 1	Pull 0	1	0
23	LJ Slave ASYNC, Auto Clock Gear[3] (>130FS)	8<FS<384	64*FS	130*FS≤MCLK ≤50	Pull 1	Pull 0	1	1
DSD & TDM LJ Slave Modes								
24	DSD Slave SYNC, MCLK/1	BCK/64	DSD64-512	64*FS ≤ MCLK ≤ 45.1584	Pull 1	Pull 1	0	0
25	DSD Slave SYNC, Auto Clock Gear[3] (128*FS)	BCK/64	DSD64-512	64*FS ≤ MCLK ≤ 45.1584	Pull 1	Pull 1	0	1
26	DSD Slave ASYNC, MCLK/1	BCK/64	DSD64-512	130*FS ≤ MCLK ≤ 50	Pull 1	Pull 1	1	0
27	DSD Slave ASYNC, Auto Clock Gear[3] (>130*FS)	BCK/64	DSD64-512	130*FS ≤ MCLK ≤ 50	Pull 1	Pull 1	1	1
28	TDM[4] LJ Slave SYNC, Autodetect (Slots 1 to 8)	8<FS<384	Auto (256FS, 512FS, 1024FS)	256*FS≤MCLK ≤49.152	Pull 1	1	0	0
29	TDM[4] LJ Slave SYNC, Autodetect (Slots 9 to 16)	8<FS<384	Auto (512FS, 1024FS)	512*FS≤MCLK ≤49.152	Pull 1	1	0	1
30	TDM[4] LJ Slave SYNC, Autodetect (Slots 17 to 24)	8<FS<192	Auto (1024FS)	1024*FS≤MCLK ≤49.152	Pull 1	1	1	0
31	TDM[4] LJ Slave SYNC, Autodetect (Slots 25 to 32)	8<FS<192	Auto (1024FS)	1024*FS≤MCLK ≤49.152	Pull 1	1	1	1

Table 4 - Hardware Mode Pin Configuration

[1] For S/PDIF in HW Mode, DATA7/GPIO7 is the S/PDIF stream input. The ES9039MPRO/ES9039PRO must be reset (CHIP_EN) when changing to and from S/PDIF.

[2] To enable DoP in HW Mode, DATA8/GPIO8 pin bust be high.

[3] ACG (Auto Clock Gearing) is enabled, it will normally gear the MCLK down to >=128*FS in SYNC, >130*FS in ASYNC, or 2*DSDCLK in DSD modes.

[4] TDM uses auto channel detect to determine the amount of channels. 8 Channels of data on a single data line is required in hardware mode to map to all 8 DACs. In software mode, 4 channels on 2 data lines is also supported.

GPIO Functions in Hardware Mode

The following GPIO pins add functionality in Hardware Modes. Other unused GPIOs should be terminated to ground.

Pin	Functionality	Settings
GPIO1	Outputs Automute Status	Output 0: Automute not engaged Output 1: Automute engaged
GPIO2	SRC Locked Status	Output 0: SRC is unlocked or in SYNC mode Output 1: SRC is locked and in ASYNC mode
DATA6/GPIO6	Sets FILTER_SHAPE in Hardware Mode	1'b0: Minimum Phase 1'b1: Linear Phase Fast Roll-Off
DATA7/GPIO7	S/PDIF Input Stream[1]	-
DATA8/GPIO8	Enables the DoP decoder[2]	1'b0: DoP Disabled 1'b1: DoP Enabled

Table 5 - GPIO Functions in Hardware Mode

Muting

MUTE_CTRL (Pin 41) is used to control the muting of the output and enabling of the Automute feature while in Hardware Mode:

- 1 - Output Unmuted, No Automute
- Pull 1 - Output Unmuted, Automute Enabled
- Pull 0 - Output Muted, Automute Enabled
- 0 - Output Muted, No Automute

[1] S/PDIF is only supported in HW modes 16-18

[2] DoP is only supported in HW modes 16-18

Digital Features

Digital Signal Path

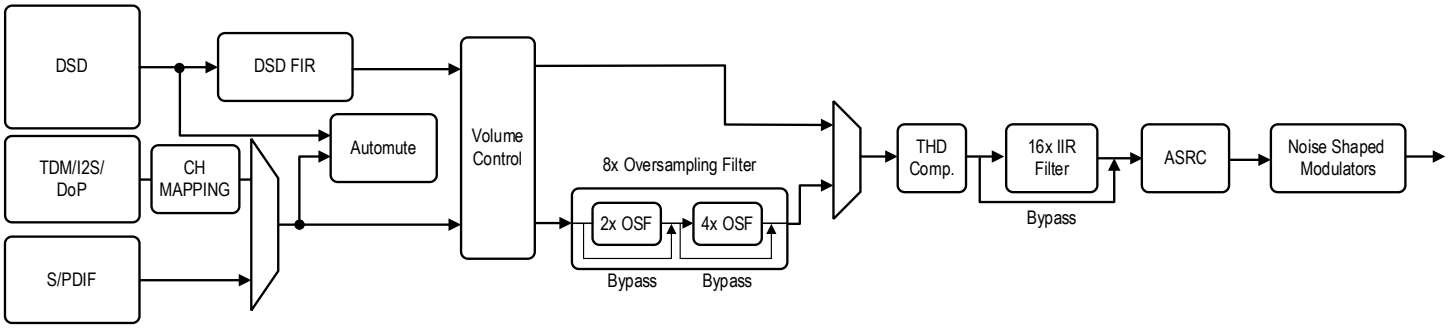


Figure 9 - Digital Signal Path

Note: Channel Mapping is only available with the TDM/I²S & DoP interface.

THD Compensation

THD Compensation minimizes the non-linearities of the DAC. The ES9039MSPRO & ES9039SPRO can help compensate for system second and third harmonic distortion. For best results, compensation coefficients should be tuned for each device in-situ.

THD Compensation Registers

- Register 91-98: THD C2 L
  - For C2 Channel 1-4
- Register 99-106: THD C2 H
  - For C2 Channel 5-8
- Register 107-114: THD C3 L
  - For C3 Channel 1-4
- Register 115-122: THD C3 H
  - For C3 Channel 5-8

GPIO Configuration

GPIO_CONFIG	Function	I/O Direction
0	Analog Shutdown	N/A
1	Output 1'b0	Output
2	Output 1'b1	Output
3	CLK_IDAC	Output
4	OR of All Interrupts	Output
5	Mute All DAC Channels	Input
6	System Mode Control	Input
7	SRC Locked Status	Output
8	CLKEN_1FS	Output
9	PWM1	Output
10	PWM2	Output
11	PWM3	Output
12	Volume min	Output
13	Automute status	Output
14	Soft Ramp finished	Output
15	MQA_Auth_True[1]	Output

Table 6 - Standard GPIO Functions

GPIOx Default states:

GPIO1: Automute Status
GPIO2: SRC Locked Status
GPIO3-8: Analog Shutdown

Analog Shutdown

Analog Shutdown is input disabled, output is tri-stated.

Output 1'b0

Outputs a constant 1'b0.

Output 1'b1

Outputs a constant 1'b1.

CLK_IDAC

Outputs the CLK_IDAC clock. Requires DAC to be on.

[1] MQA_Auth_True is for ES9039MPRO only

OR of All Interrupts

Bitwise OR of all masked interrupts.

Relevant Registers

- Register 10 INTERRUPT VOL MIN MASKP
- Register 11 INTERRUPT AUTOMUTE MASKP
- Register 12 INTERRUPT SS FULL RAMP MASKP
- Register 13-14 INTERRUPT MASKP
- Register 15 INTERRUPT VOL MIN MASKN
- Register 16 INTERRUPT AUTOMUTE MASKN
- Register 17 INTERRUPT SS FULL RAMP MASKN
- Register 18-19 INTERRUPT MASKN

Mute All DAC Channels

Mute all DAC Channels

System Mode Control

Change the system mode (enable/disable datapath) via GPIO. Register 46-47[15] GPIO_DAC_MODE changes whether a 1 on the GPIO will enable or disable the datapath.

When GPIOx input is 1'b0, the system mode will be determined by Register 0[1] DAC_MODE_REG.

Relevant Registers

- Register 46-47[15] GPIO_DAC_MODE
  - 1'b0: Disable datapath when GPIOx input is 1'b1
  - 1'b1: Enable datapath when GPIOx input is 1'b1
- Register 0[1] DAC_MODE_REG

SRC Locked Status

SRC (Sample Rate Converter) locked status output. Outputs LOW if the device is in a synchronous mode, outputs HIGH if the device is in asynchronous mode and the SRC is locked.

Relevant Registers

- Register 1[6] SYNC_MODE
  - Must be = 0 (default) for the ES9039PRO to be in ASYNC mode, enabling the SRC.

CLKEN_1FS

Outputs the CLKEN_1FS clock, which is a clock with an output every 1FS.

PWM1/PWM2/PWM3

Output a configurable PWM signal. The frequency and duty cycle of the PWM signal can be calculated with the following equations:

$$frequency\ [Hz] = \frac{MCLK}{PWM\_FREQ + 1}$$

$$Duty\ Cycle\ [\%] = \left(\frac{PWM\_COUNT}{PWM\_FREQ + 1}\right) \times 100$$

Relevant Registers

- Register 48 PWM1_COUNT
- Register 49-50 PWM1_FREQ
- Register 51 PWM2_COUNT
- Register 52-53 PWM2_FREQ
- Register 54 PWM3_COUNT
- Register 55-56 PWM3_FREQ

Volume min

Outputs HIGH when the DAC is muted. This can occur from manually muting, automuting, and setting the volume registers to 0xFF.
The output can be a channel specific flag, the logical AND of all flags (default), or the logical OR of all the flags.

Relevant Registers

- Register 46-47[4] GPIO_OR_VOL_MIN sets the output to be the logical AND of all channels' vol min flags.
- Register 46-47[1] GPIO_AND_VOL_MIN sets the output to be the logical OR of all channels' vol min flags.
- Register 46-47[8:6] FLAG_CH_SEL selects which of the individual DAC channel flags to output.

Automute status

Outputs HIGH when the DACs automute condition is met. The output can be a channel specific flag, the logical AND of all flags (default), or the logical OR of all the flags.

Relevant Registers

- Register 46-47[3] GPIO_OR_AUTOMUTE sets the output to be the logical OR of all channels' automute flags
- Register 46-47[0] GPIO_AND_AUTOMUTE sets the output to be the logical AND of all channels' automute flags
- Register 46-47[8:6] FLAG_CH_SEL sets the output to be one of the individual channels' flags

Soft Ramp finished

Outputs HIGH when the DAC is not in the process of ramping up or down. The output can be a channel specific flag, the logical AND of all flags (default), or the logical OR of all the flags.

Relevant Registers

- Register 46-47[5] GPIO_OR_SS_RAMP sets the output to be the logical OR of all channels soft ramp flags
- Register 46-47[2] GPIO_AND_SS_RAMP sets the output to be the logical AND of all channels soft ramp flags
- Register 46-47[8:6] FLAG_CH_SEL sets the output to be one of the individual channels flags

MQA_Auth_True (ES9039MPRO only)

Output is HIGH when the incoming stream is a valid MQA stream.

Audio Input Formats

The ES9039MSPRO & ES9039SPRO support multiple serial input data formats. Input format is selected either through Hardware Mode or Software Mode.

The ES9039MSPRO & ES9039SPRO can automatically determine the input data format by enabling Register 57[0] AUTO_INPUT_SEL, data must be provided on the DATA2 pin to properly decode the input format. The input data format can also be selected using Register 57[2:1] INPUT_SEL.

The formats include:

- PCM
  - Slave and master mode in 16, 24, 32-bit widths
  - I²S, Left Justified (LJ), and Right Justified (RJ)
  - Sample rates up to 768kHz (64fs mode)
  - Channel Remapping & Invert
- TDM
  - Up to 32 slots including daisy chain mode.
  - Slave mode in hardware mode. Slave and master modes in software mode.
  - LJ format in hardware modes. I²S or LJ in software modes.
  - Channel Remapping & Invert.
- DoP (DSD Over PCM)
  - Slave and master mode
  - Sample rates from DoP512 (24bit, 1.4112MHz PCM)
  - Channel Remapping & Invert
- Native DSD
  - Slave and master mode
  - Sample rates from DSD64 (2.8224Mbits.sec, 64 x 44.1kHz) to DSD1024
  - Channel Invert
- S/PDIF
  - Stereo data input

PCM (I²S/LJ)

Data is organized into 2 channels per data line. Any channel on any data line can be mapped to any DAC through the TDM_CHx_CONFIG channel mapping Registers 64-71. Data is latched on the positive edge of BCLK.

In hardware mode, PCM (I²S/LJ) data lines are fixed to the mapping shown in the table below.

In software mode, PCM (I²S/LJ) data lines can be re-mapped to any DAC.

PCM Pin Connections:

Pin Name	Function	Description
DATA_CLK	PCM BCLK	PCM Clock (Bit Clock), Master or Slave
DATA1	PCM WS	PCM WS (Word Select/Frame Select), Master or Slave
DATA2	PCM DATA	PCM Data Channel 1 & 2
DATA3	PCM DATA	PCM Data Channel 3 & 4
DATA4	PCM DATA	PCM Data Channel 5 & 6
DATA5	PCM DATA	PCM Data Channel 7 & 8

Table 7 - PCM Pin Connections

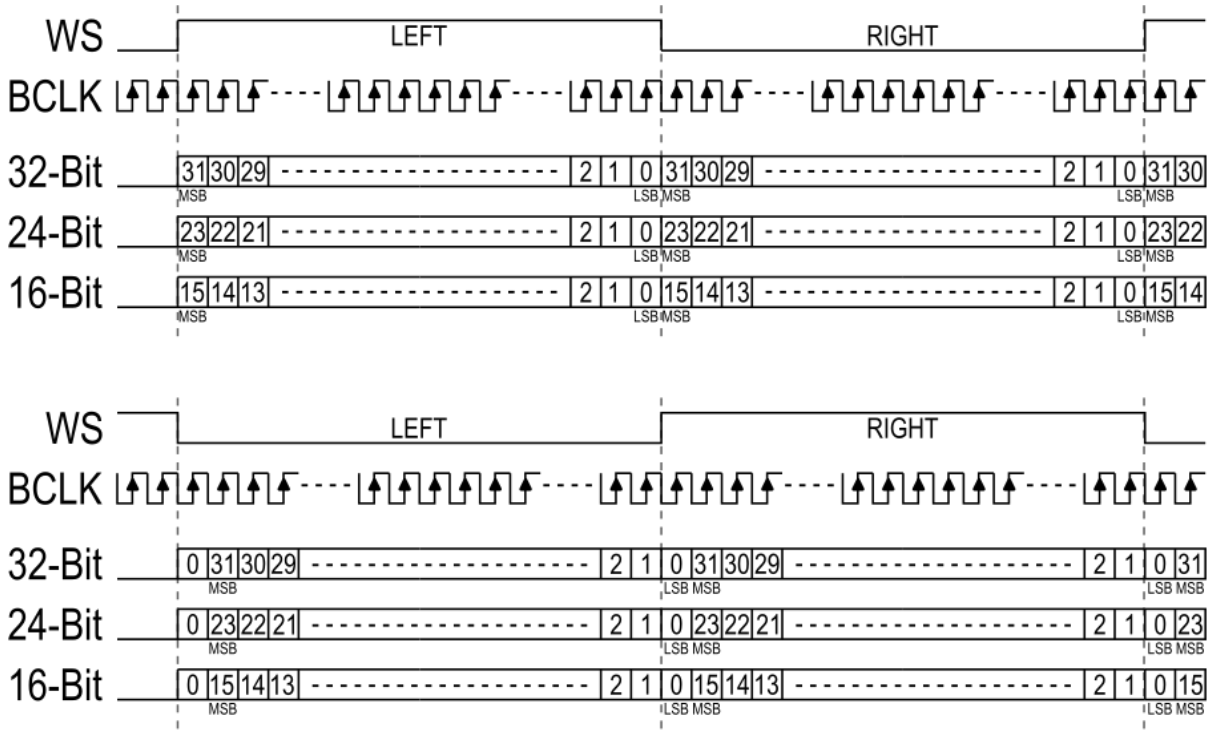


Figure 10 - LJ (top) & I²S (bottom) for 16,24, and 32-bit Word Widths

Note: RJ is only supported in software mode

TDM (Time-Division Multiplexing)

The ES9039MSPRO & ES9039SPRO support TDM format, allowing for 4, 8, 16, or 32 channels on a single data line. Supported formats are TDM4 (4ch), TDM8 (8ch), TDM16 (16ch) and TDM32 (32ch). TDM is supported in both software and hardware modes. Data is latched on the positive edge of BCLK.

In hardware mode, TDM8 and above are supported. Hardware modes require TDM data line to be input through DATA2. In hardware mode, TDM8 will map slots 1 to 8 to DACs 1 to 8, respectively. In the case of TDM16, the hardware mode will be configured so that slots 1 to 8 will map to one device (HW mode #16), and slots 9-16 to the next device (HW mode #17).

In software mode, Registers 64-71: TDM_CHx_CONFIG can be set to internally map any slot to each DAC. In this case TDM4, TDM8, TDM16 and TDM32 are all supported. Software mode allows the TDM Data to be input through any of the serial data lines (DATA2, DATA3, DATA4 or DATA5).

TDM Pin Connection

Pin Name	Function	Description
DATA_CLK	TDM BCLK	TDM Clock, Master, or Slave
DATA1	TDM WS	TDM WS (Word Select/Frame Select), Master or Slave
DATA2	TDM DATA	TDM DATA Channel 1 & 2 (default)
DATA3	TDM DATA	TDM DATA Channel 3 & 4 (default)
DATA4	TDM DATA	TDM DATA Channel 5 & 6 (default)
DATA5	TDM DATA	TDM DATA Channel 7 & 8 (default)

Table 8 - TDM Pin Connections

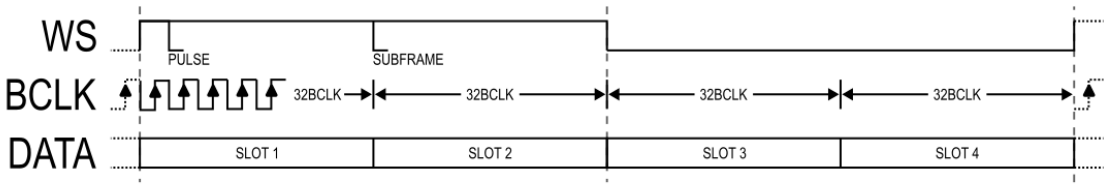


Figure 11 - TDM4 Mode

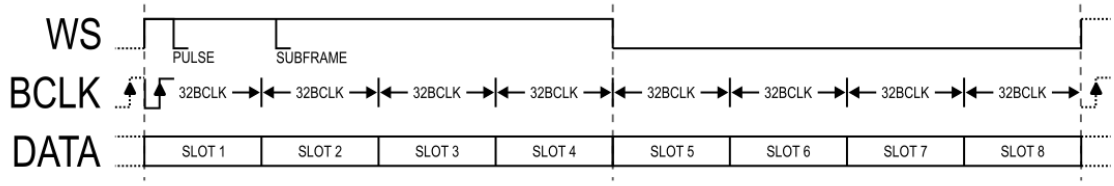


Figure 12 - TDM8 Mode

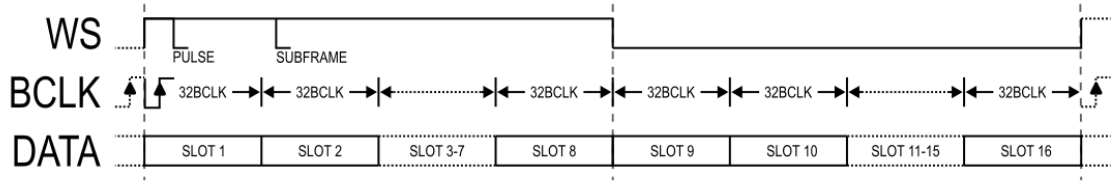


Figure 13 - TDM16 Mode

DSD[1]

In DSD mode, there is a single DSD clock line, and each channel of data is an additional DSD data line. There is no internal channel mapping for DSD input, DSD data input to DATA1 is sent to Ch1, DSD data input to DATA2 is sent to Ch2, etc.

For 4 channel and 2 channel applications, the interpolation path data can be copied from DAC1+DAC2 to the other DAC pairs, see Register 0[5:2] for details.

Data lines in hardware mode use the default configuration.

DSD Pin Connections (default configuration):

Pin Name	Function	Description
DATA_CLK	DSD CLK	DSD Clock
DATA1	DSD CH1	DSD DATA Channel 1
DATA2	DSD CH2	DSD DATA Channel 2
DATA3	DSD CH3	DSD DATA Channel 3
DATA4	DSD CH4	DSD DATA Channel 4
DATA5	DSD CH5	DSD DATA Channel 5
DATA6	DSD CH6	DSD DATA Channel 6
DATA7	DSD CH7	DSD DATA Channel 7
DATA8	DSD CH8	DSD DATA Channel 8

Table 9 - DSD Pin Connections

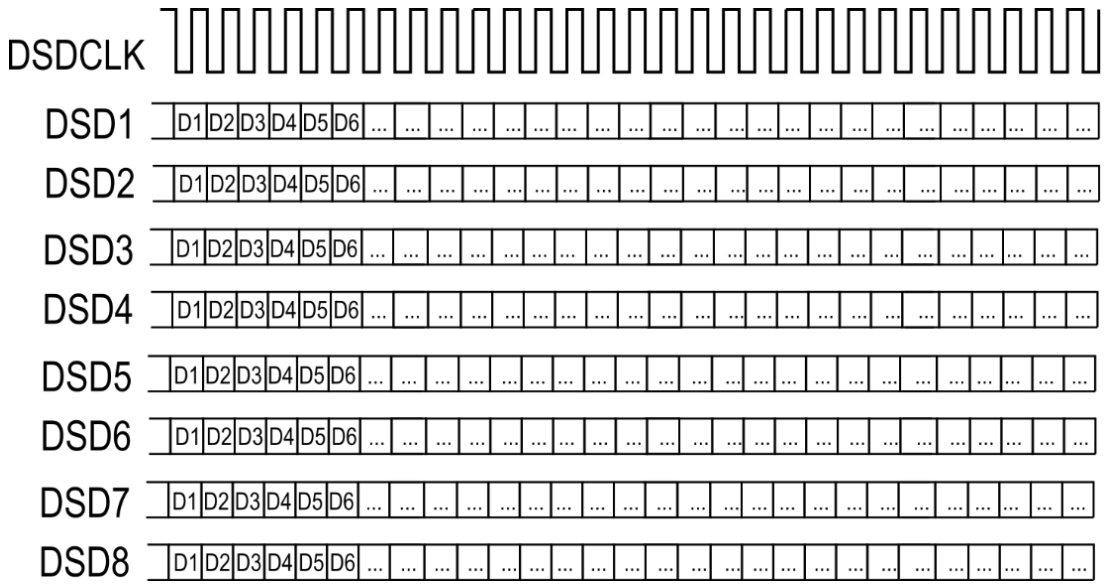


Figure 14 - DSD Format, 1-bit stream

[1] The Automute Feature is not available when using DSD mode.

S/PDIF

S/PDIF is transmitted over a single signal line using dual phase encoded data, which allows for clock extraction from the data signal line.

In S/PDIF mode, there is only stereo data input. Channel 1 data will be sent to all odd channel DACs; Channel 2 data will be sent to all even channel DACs.

Note: When using software mode (SW), either a reset (CHIP_EN) or toggle of register 58[6] BCK_INV is required after switching to a S/PDIF input. When using hardware mode (HW), a reset (CHIP_EN) is required after switching to S/PDIF input.

MQA Renderer (ES9039MPRO only)

The ES9039MPRO features a built in MQA renderer.

The MQA renderer is only available in software configuration mode and is accessible with Register 141 MQA CONFIG.

MQA uses Channel 1 and Channel 2 for output (DATA1 and DATA2 pins).

Channels can be remapped using Registers 64-71[4:0] TDM_CHx_SLOT_SEL.

Pre-Programmed Digital Filters

The ES9039MSPRO & ES9039SPRO have 7 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 88[2:0] FILTER_SHAPE for configuration)

#	Filter	Description
1	Minimum Phase (default)	Version 2 of minimum phase fast roll-off (#5) with less ripple and more image rejection
2	Linear Phase Apodizing Fast Roll-Off	Full image rejection by FS/2 to avoid any aliasing, with smooth roll-off starting before 20k.
3	Linear Phase Fast Roll-Off	Sabre legacy filter, optimized for image rejection @ 0.55 FS
4	Linear Phase Slow Roll-Off	Sabre legacy filter, optimized for lower latency, but symmetric impulse response
5	Minimum Phase Fast Roll-Off	Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55 FS
6	Minimum Phase Slow Roll-Off	Lowest latency at the cost of image rejection
7	Minimum Phase Fast Roll-Off Low Dispersion	Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band.

Table 10 - Pre-Programmed Digital Filter Descriptions

Note: Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

PCM Filter Latency

The following table shows the simulated latency of each filter at 44.1kHz sampling rate. The latency was measured at the peak amplitude of the impulse response prior to being down sampled to 1FS. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay
Minimum Phase (default)	7.23 / FS
Linear Phase Apodizing Fast Roll-Off	36.60 / FS
Linear Phase Fast Roll-Off	37.22 / FS
Linear Phase Slow Roll-Off	9.66 / FS
Minimum Phase Fast Roll-Off	7.23 / FS
Minimum Phase Slow Roll-Off	6.26 / FS
Minimum Phase Fast Roll-Off Low Dispersion	13.27 / FS

Table 11 - PCM Filter Latency

PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-97dB	0.55 FS			Hz
Group Delay		2.90/FS		8.99/FS	s
Flatness (ripple)	0.0012				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41 FS	Hz
Stop band	-107dB	0.50 FS			Hz
Group Delay			32.81/FS		s
Flatness (ripple)	0.0024				dB

Linear Phase Fast Roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.45 FS	Hz
Stop band	-117dB	0.55 FS			Hz
Group Delay			33.43/FS		s
Flatness (ripple)	0.0030				dB

Linear Phase Slow Roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.44 FS	Hz
Stop band	-91dB	0.75 FS			Hz
Group Delay			5.87/FS		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-98dB	0.55 FS			Hz
Group Delay		2.91/FS		9.14/FS	s
Flatness (ripple)	0.0023				dB

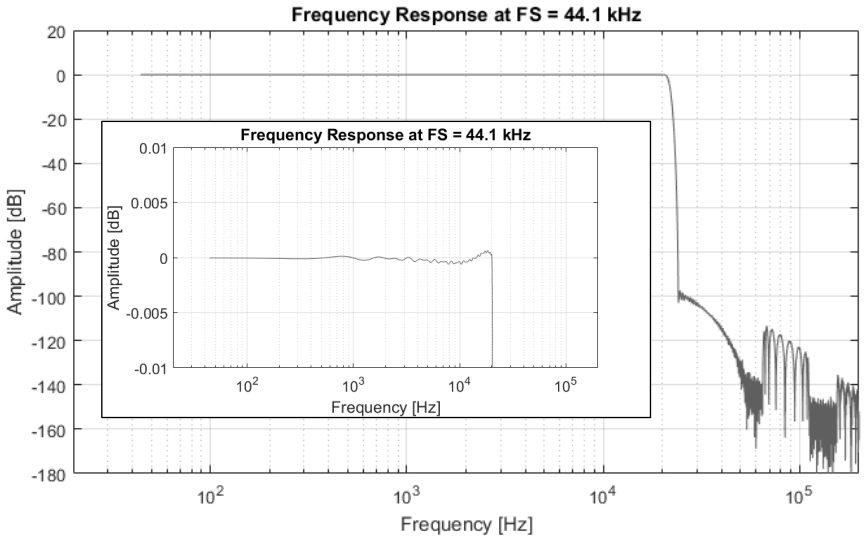
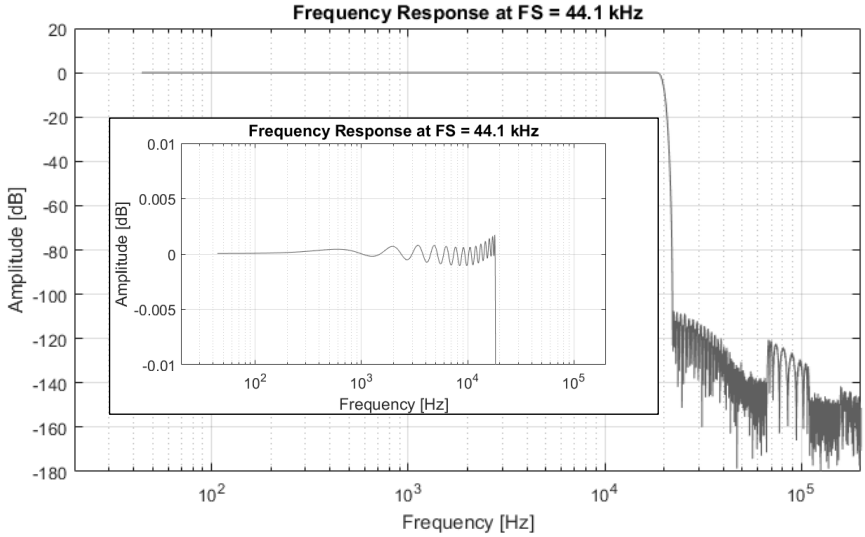
Minimum Phase Slow Roll-off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.43 FS	Hz
Stop band	-91dB	0.80 FS			Hz
Group Delay		2.08/FS		3.56/FS	s
Flatness (ripple)					dB

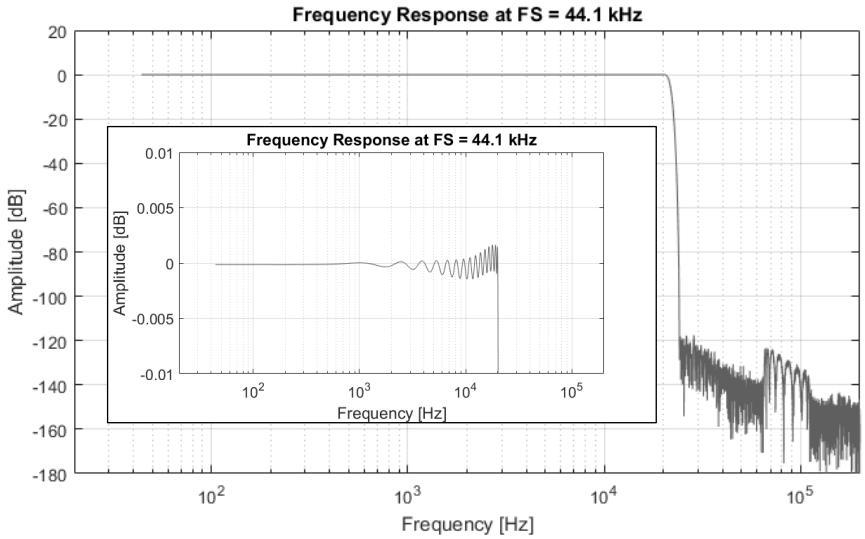
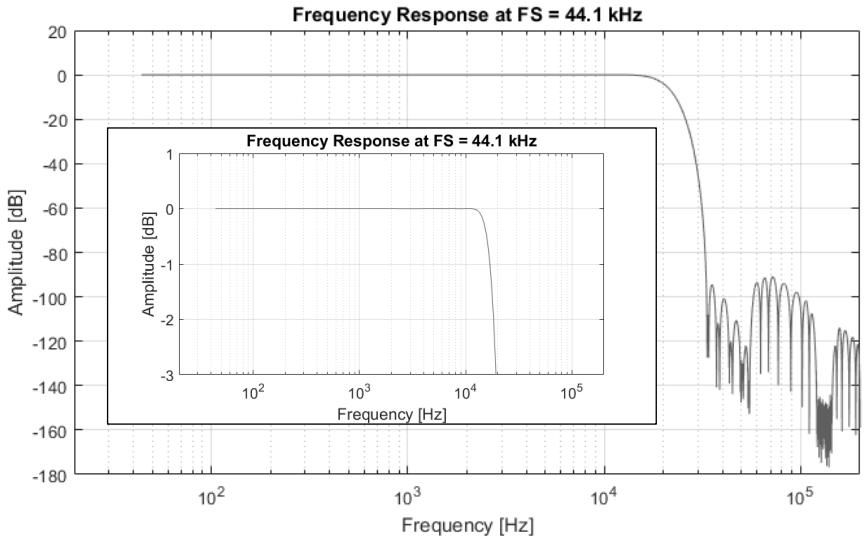
Minimum Phase Slow Roll-off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.43 FS	Hz
Stop band	-91dB	0.80 FS			Hz
Group Delay		9.32/FS		9.93/FS	s
Flatness (ripple)					dB

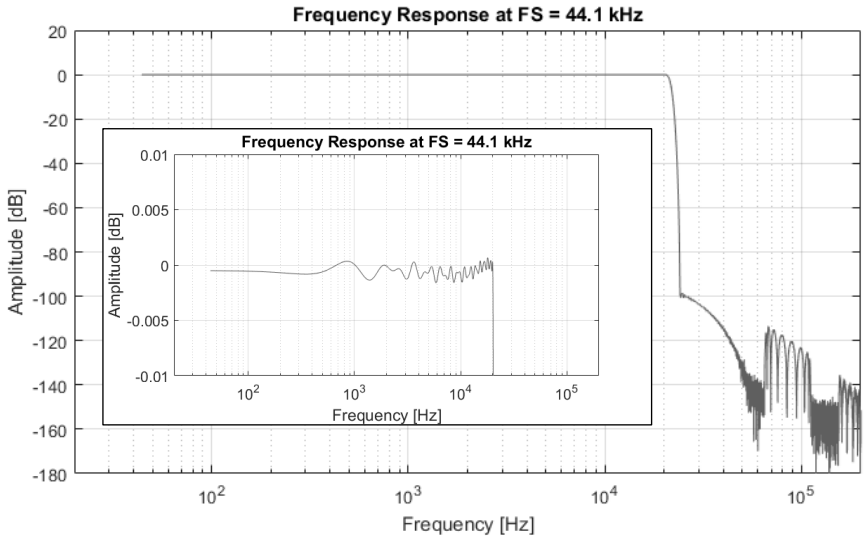
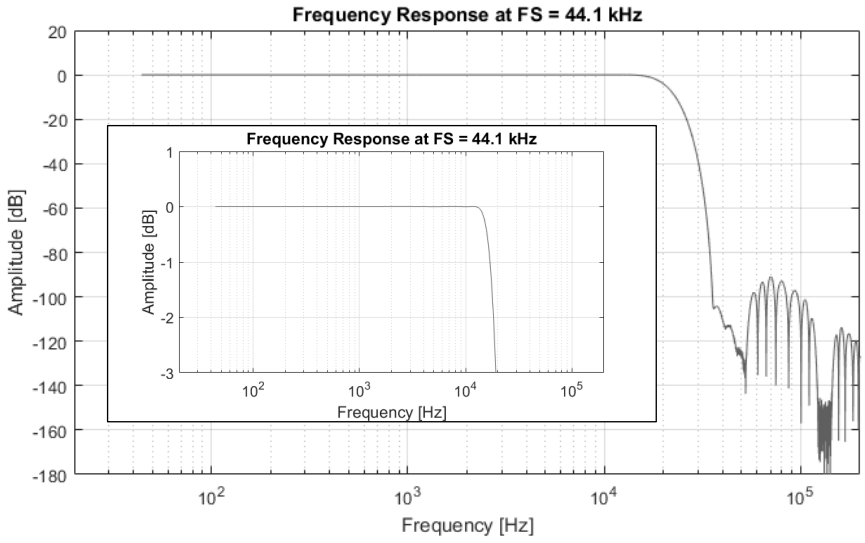
Table 12 - PCM Filter Properties

PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-off	
Linear Phase Slow Roll-off	

Minimum Phase Fast Roll-off	
Minimum Phase Slow Roll-off	

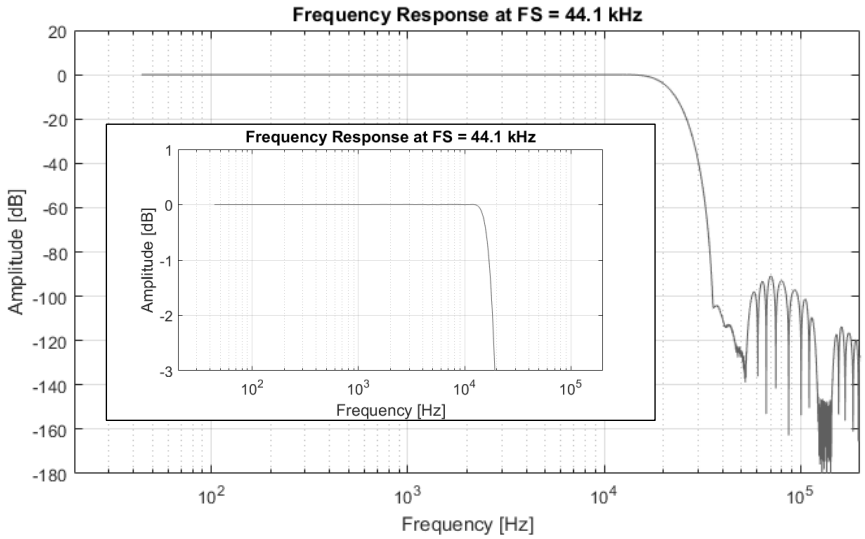
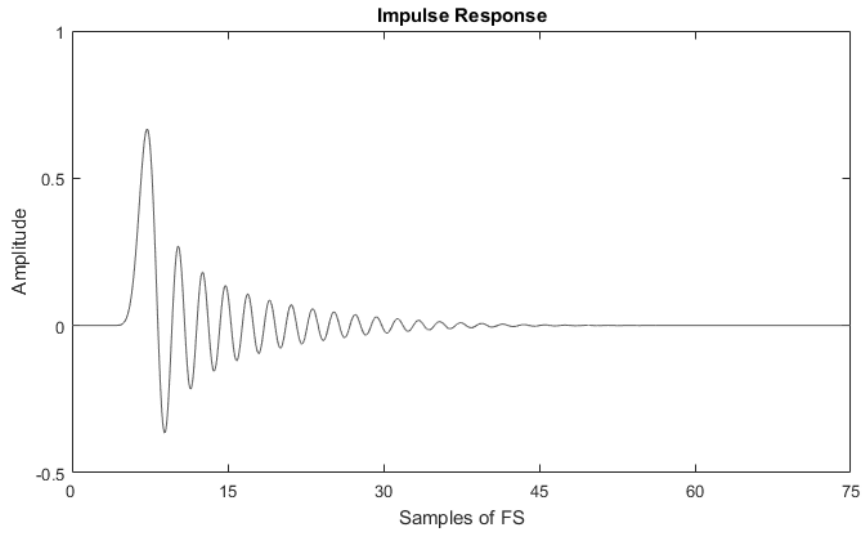
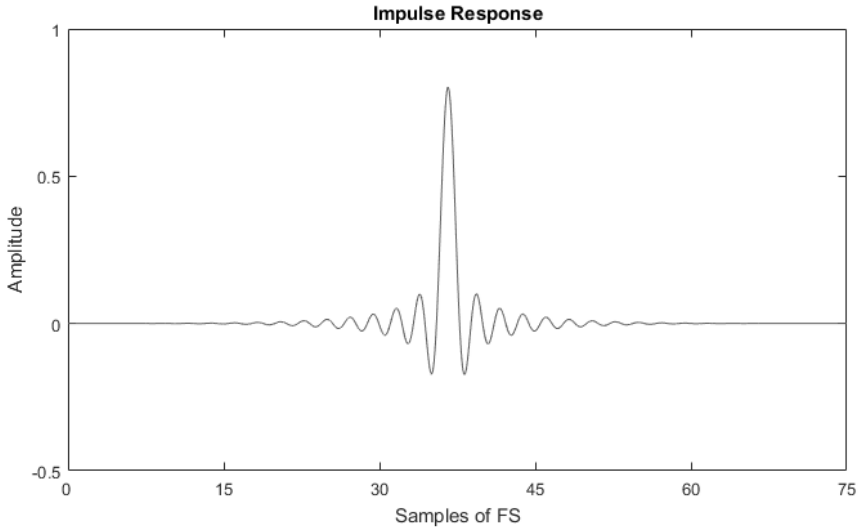
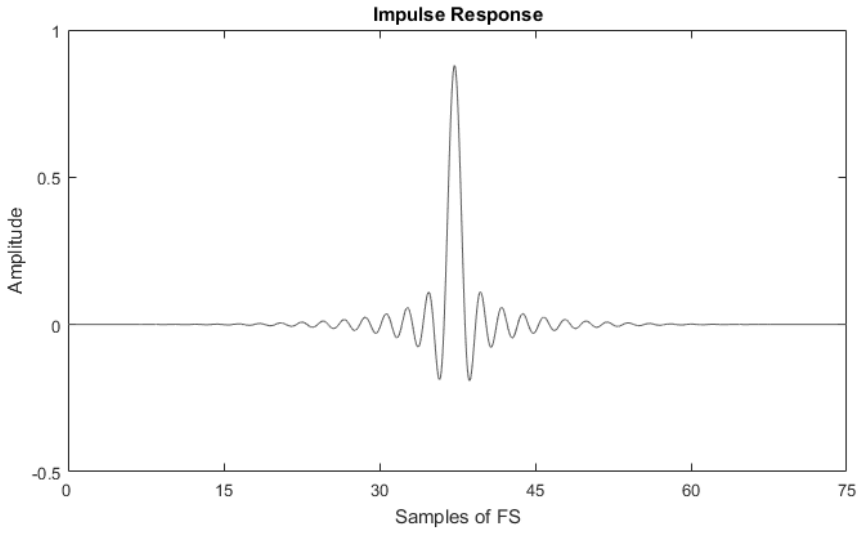
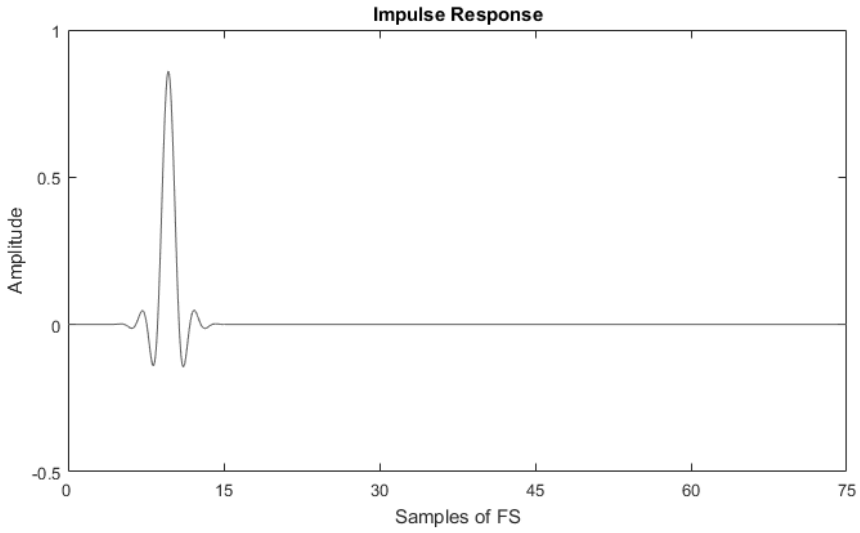
Minimum Phase Slow Roll-off Low Dispersion	

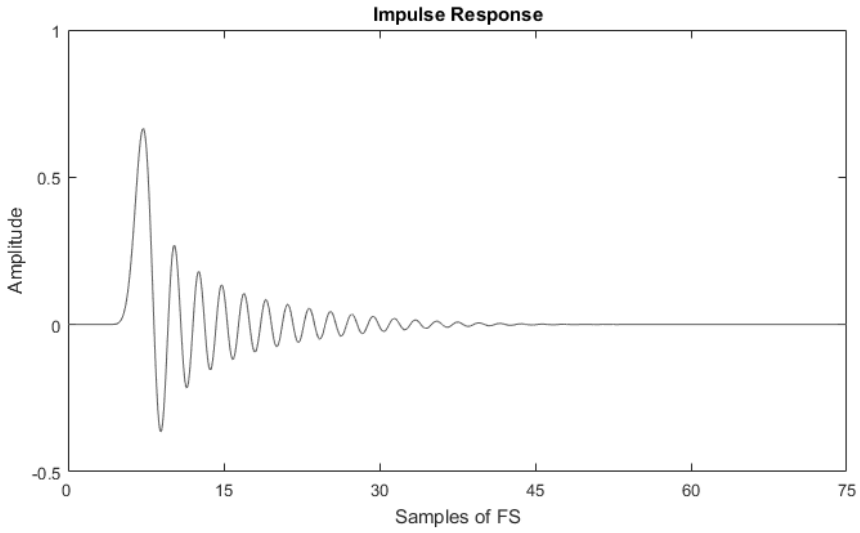
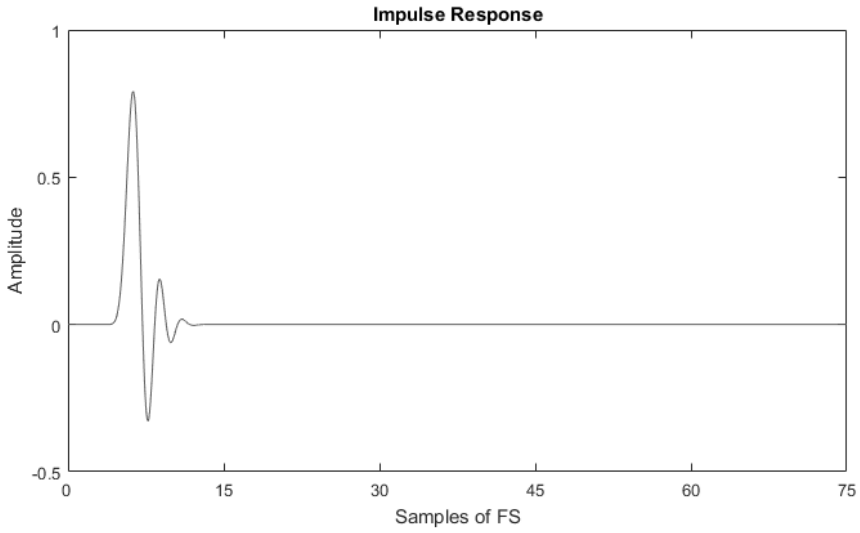
Table 13 - PCM Filter Frequency Response

PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They were measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Slow Roll-Off	

Minimum Phase Fast Roll-Off	
Minimum Phase Slow Roll-Off	

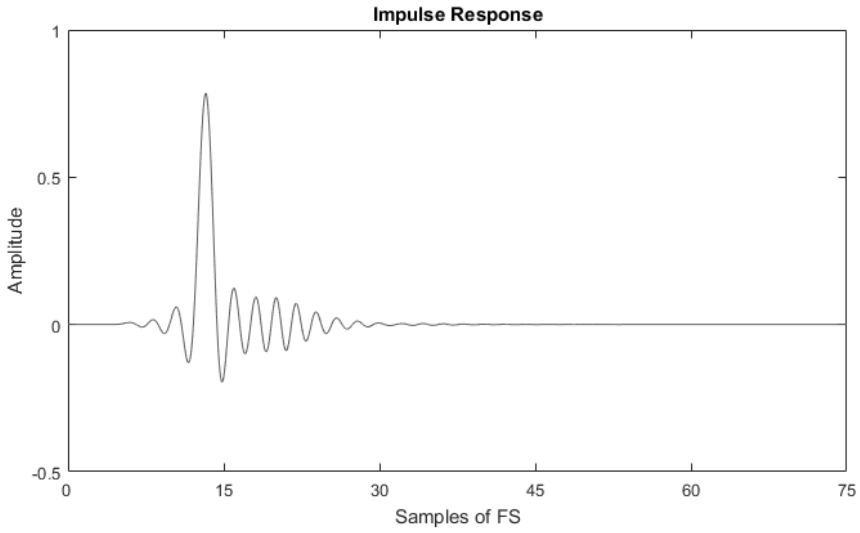
Minimum Phase Slow Roll-Off Low Dispersion	

Table 14 - PCM Filter Impulse Response

64FS Mode

When 64FS (MCLK/FS) ratio is required, it is necessary for the ES9039MSPRO & ES9039SPRO to be in 64FS mode. 64FS Mode can be enabled by setting:

Software Register

- SYNC Mode: Register 0[6] ENABLE_64FS_MODE = 1'b1
  - Manually enables 64FS mode
  - Should be used with high sample rates like 705.6kHz & 768kHz
- SYNC Mode: Register 3[7] AUTO_FS_DETECT = 1'b1
  - Auto tunes the SYS_CLK/CLK_IDAC ratio according to detected sampling frequency
  - Automatically enables 64FS mode when SYS_CLK/CLK_IDAC ratio is 64

Minimum Phase 64FS Mode Latency

The following table shows the simulated latency at 705.6kHz sampling rate and is very similar at 768kHz. The measurement was taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay
Minimum Phase Double Rate	5.65 / FS

Table 15 - Minimum Phase 64FS Latency

Minimum Phase 64FS Properties

Minimum Phase 64FS Mode					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	–3dB			0.45 FS	Hz
Stop band	-62dB	0.68 FS			Hz
Group Delay		1.55/FS		2.35/FS	s
Flatness (ripple)					dB

Table 16 - Minimum Phase 64FS Properties

Minimum Phase 64FS Frequency Response

This filter gets selected automatically when MCLK/FS = 64. The following frequency response was obtained from software simulations with a sample rate of 705.6kHz

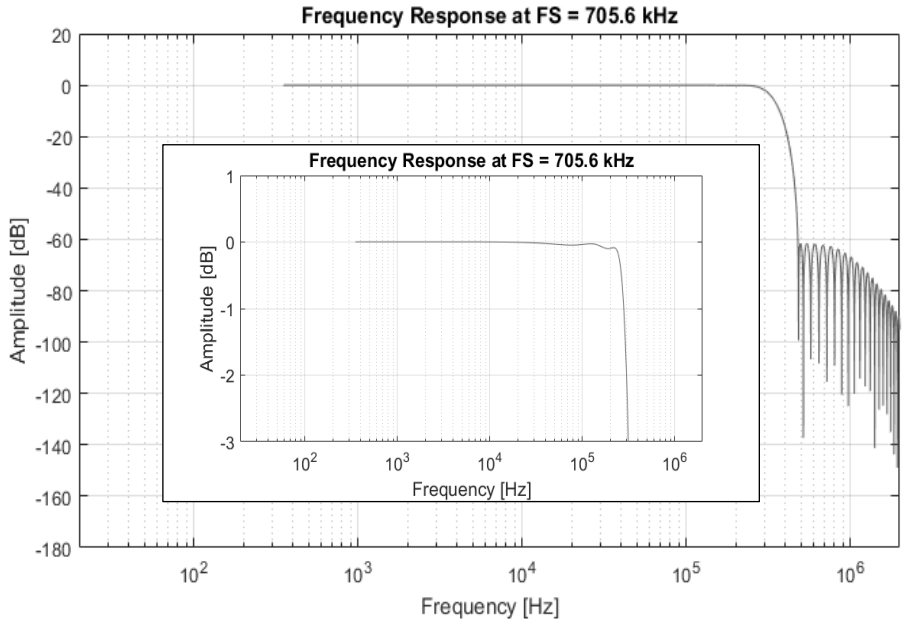


Figure 15 - Minimum Phase 64FS Frequency Response

Minimum Phase 64FS Impulse Response

The following impulse response was obtained from software simulations. It was measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream.

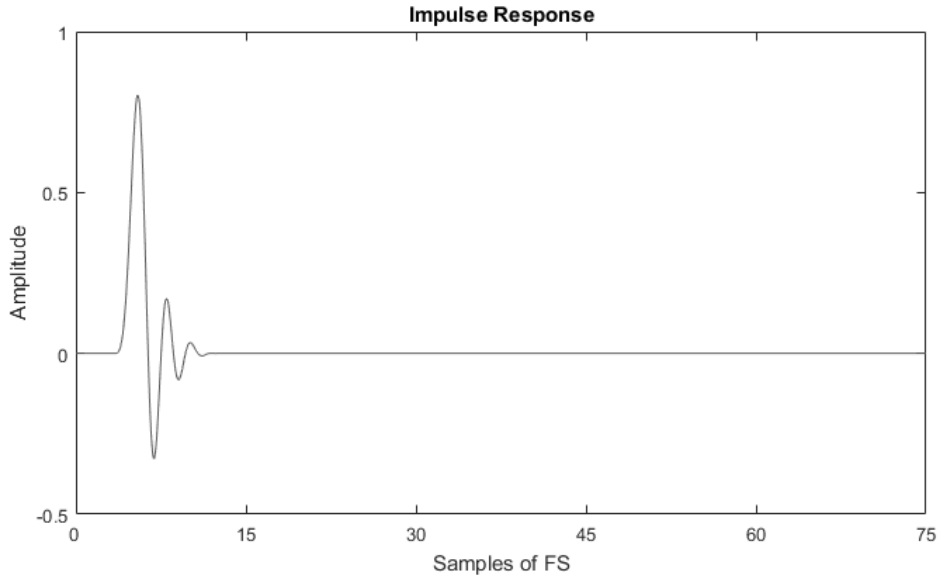


Figure 16 - Minimum Phase 64FS Impulse Response

Clock Distribution

The ES9039MSPRO & ES9039SPRO include features for selecting and manipulating the input clock source.

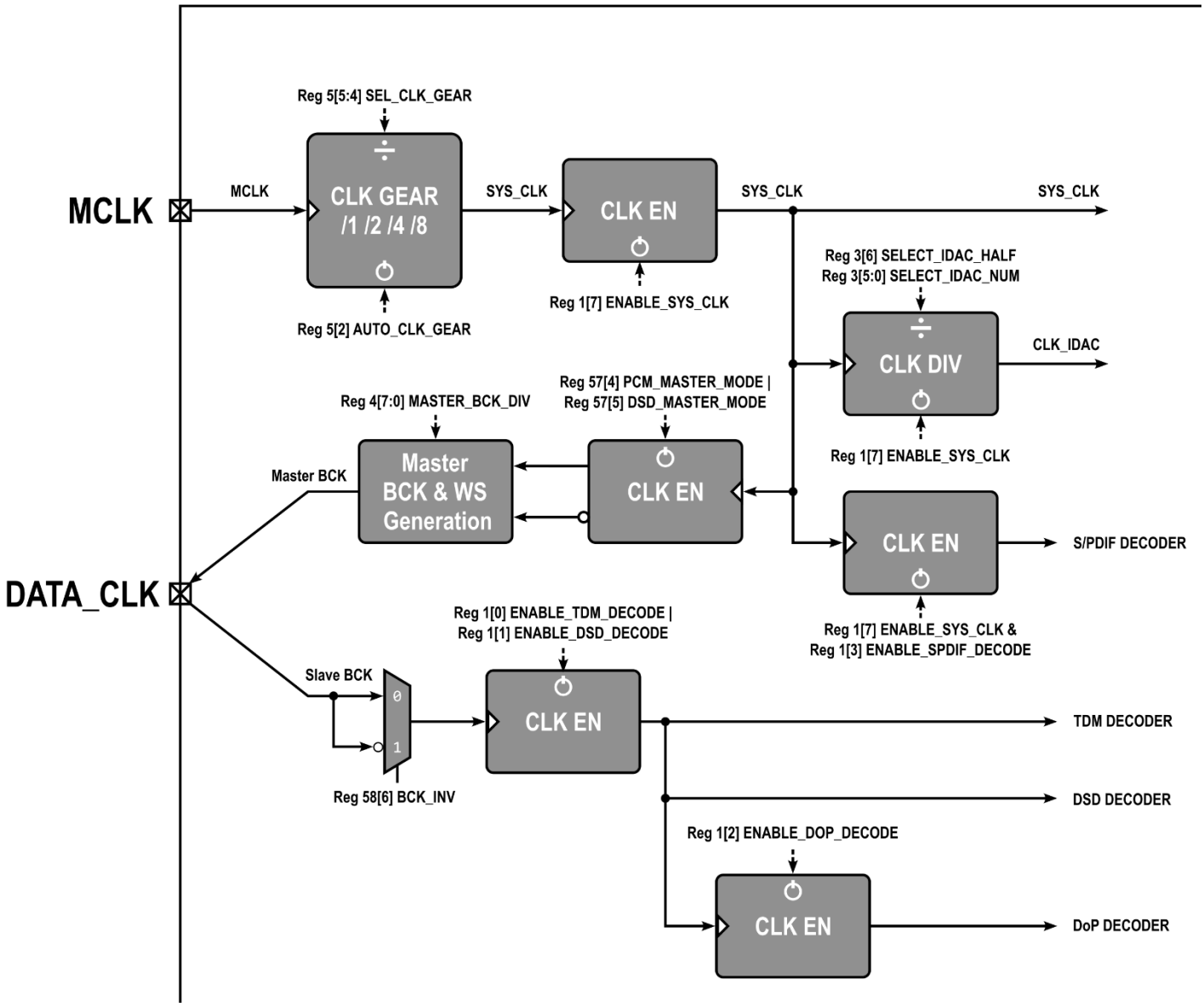


Figure 17 - Clock Distribution

The following list shows the various clocks of the ES9039MSPRO & ES9039SPRO and the associated registers for configuration.

SYS_CLK

SYS_CLK can be enabled and geared down from MCLK manually or automatically with the use of registers.

- Register 1[7] ENABLE_SYS_CLK
- Register 5[5:4] SEL_CLK_GEAR
- Register 5[2] AUTO_CLK_GEAR

CLK_IDAC

Synchronous Mode

CLK_IDAC must be tuned such that the $\text{SYS\_CLK} * \frac{\text{SELECT\_IDAC\_HALF}}{\text{SELECT\_IDAC\_NUM}+1} = \text{CLK\_IDAC} = 128 * \text{WS}$. The ratio can be automatically tuned to the incoming sample rate by using AUTO_FS_DETECT.

- Register 3[6] SELECT_IDAC_HALF
- Register 3[5:0] SELECT_IDAC_NUM
- Register 3[7] AUTO_FS_DETECT

Asynchronous Mode

CLK_IDAC must be tuned such that the $\text{SYS\_CLK} * \frac{2^{\text{SELECT\_IDAC\_HALF}}}{\text{SELECT\_IDAC\_NUM}+1} = \text{CLK\_IDAC} \geq 130 * \text{WS}$.

AUTO_FS_DETECT cannot be used in ASYNC mode.

Master BCK

The Master BCK & WS Generation block is enabled when either PCM or DSD Master Mode is enabled. The generated BCK is output on the DATA_CLK pin, and the frequency will need to be set with the divider register.

- Register 4[7:0] MASTER_BCK_DIV
- Register 57[4] PCM_MASTER_MODE
- Register 57[5] DSD_MASTER_MODE
- Register 58[0] MASTER_BCK_INVERT
- Register 58[1] MASTER_WS_INVERT
- Register 58[2] MASTER_WS_PULSE_MODE
- Register 58[4:3] MASTER_FRAME_LENGTH

Slave BCK

The Input Slave BCK is sourced from the DATA_CLK pin, which means a BCK can be provided externally or generated internally.

- Register 58[6] BCK_INV

Decoders

Each of the TDM, DSD, DoP, and S/PDIF decoders have their own enable registers.

- Register 1[0] ENABLE_TDM_DECODE
- Register 1[1] ENABLE_DSD_DECODE
- Register 1[2] ENABLE_DOP_DECODE
- Register 1[3] ENABLE_SPDIF_DECODE

Analog Features

Calibration Resistor

The ES9039MSPRO & ES9039SPRO feature a ~50kΩ calibration resistor accessible through GPIO3 (Pin 28) and terminated to ground as shown in the below figure. The calibration resistor is enabled by default but can be disabled with Register 34[6] CAL_RES_ENB = 1.

ESS' ES9312 features a calibration mode that can be paired with the ES9039MSPRO & ES9039SPRO to compensate AVCCL and AVCCR supplies. The ES9312 connects to the ES9039MSPRO & ES9039SPRO integrated calibration resistor and adjusts the output supplies to maintain a tighter distribution on the output level in an application. See Recommended Power Supply for connections.

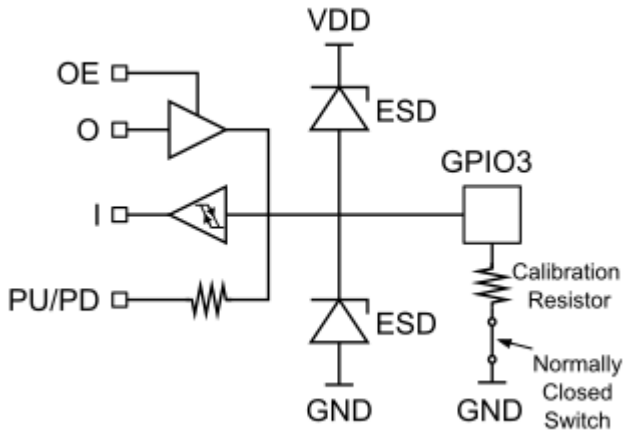


Figure 18 – GPIO3 Digital I/O with Calibration Resistor

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_L • AVCC_R • AVDD • VCCA • DVDD	 • +3.7V with respect to Ground • +3.7V with respect to Ground • +3.7V with respect to Ground • +3.7V with respect to Ground • +1.4V with respect to Ground
Storage temperature	–65°C to +150°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	–0.3V to AVDD (nom)+0.3V

Table 17 - Absolute Maximum Ratings

Warning: Stresses beyond those listed under here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions in not implied.

Warning: Electrostatic Discharge (ESD) can damage this device. Proper procedure must be followed to avoid ESD when handling this device.

ESD Ratings

ESD Standard	Rating
Human Body Model (HBM), ANSI/ESDA/JEDEC JS-001	2kV
Charge Device Model (CDM), ANSI/ESDA/JEDEC JS-002	500V

Table 18 - ESD Ratings

IO Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
High-level input voltage	VIH	(AVDD / 2) + 0.4		V
Low-level input voltage	VIL		0.4	V
High-level output voltage	VOH	AVDD – 0.2		V
Low-level output voltage	VOL		0.2	V

Table 19 - IO Electrical Characteristics

Switching Characteristics

Synchronous Mode

Parameter	Notes	Min.	Typ.	Max.	Unit
MCLK[1]					
Frequency		44.1kHz*128	-	49.152	MHz
Duty Cycle		45	-	55	%
PCM Mode[2]					
WS Frequency (Word Select Clock)	64FS Mode is not supported in Async. Mode	8	-	384	kHz
BCLK Frequency (Bit Clock)		0.256	TDM_BIT_WIDTH)* (TDM_CH_NUM+1)*WS	24.576	MHz
WS Frequency (Word Select Clock)	64FS Mode[3]	352.8	MCLK/64	768	kHz
BCLK Frequency (Bit Clock)		22.5792	MCLK	49.152	MHz
TDM Mode					
WS Frequency (Word Select Clock)	TDM4	8	-	MCLK/128	kHz
	TDM8		-	MCLK/256	kHz
	TDM16		-	MCLK/512	kHz
	TDM32		-	MCLK/1024	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	(TDM_BIT_WIDTH)* (TDM_CH_NUM+1)*WS	MCLK	MHz
DSD Mode					
DSD Clock Frequency		2.8224	-	MCLK/2	MHz

Table 20 - Synchronous Switching Characteristics

[1] MCLK is Synchronous to the digital serial audio clock

[2] In Hardware Mode, only 32-bit word widths are supported for both PCM and TDM.

[3] 64FS mode is for 705.6/768kHz with 45.1584/49.152MHz or 352.8/384kHz with 22.5792/24.576MHz.

Asynchronous Mode

Parameter	Notes	Min.	Typ.	Max.	Unit
MCLK[1]					
Frequency		44.1kHz*130	-	50	MHz
Duty Cycle		45		55	%
PCM Mode[2]					
WS Frequency (Word Select Clock)	64FS Mode is not supported in Async. Mode	8	-	MCLK/130[3]	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	TDM_BIT_WIDTH)* (TDM_CH_NUM+1)*WS	49.152	MHz
TDM Mode					
WS Frequency (Word Select Clock)	TDM4	8	-	MCLK/130	kHz
	TDM8		-	MCLK/260	kHz
	TDM16		-	MCLK/520	kHz
	TDM32		-	MCLK/1040	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	(TDM_BIT_WIDTH)* (TDM_CH_NUM+1)*WS	49.152	MHz
DSD Mode					
DSD Clock Frequency		2.8224	-	MCLK/3	MHz

Table 21 - Asynchronous Switching Characteristics

[1] MCLK is Asynchronous to the digital serial audio clock.

[2] In Hardware Mode, only 32bit word widths are supported for both PCM and TDM.

[3] MCLK must be greater than or equal to 130*FS.

Timing Characteristics

Bit-Clock (BCLK) and Word-Select (WS) Timing

Test Conditions 1 (unless otherwise noted)
TA = 25ºC, AVCC_R = AVCC_L = VCCA = AVDD = +3.3V, DVDD= +1.2V, fs = 48kHz, DAC enabled, 1kHz sine full scale.

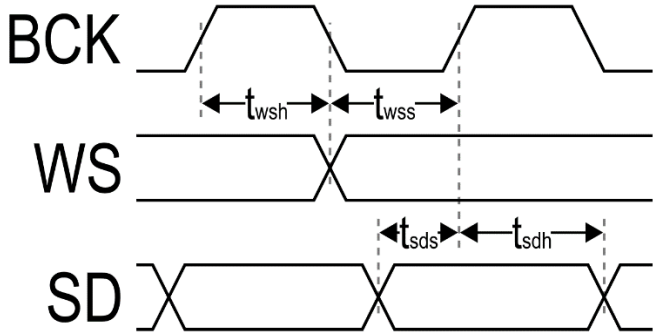


Figure 19 - Bit-Clock and Word-Select Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
WS hold time	t_{wsh}	1	-	-	ns
WS setup time	t_{wss}	3.0	-	-	ns
SD hold time	t_{sds}	4.2	-	-	ns
SD setup time	t_{sdh}	3.0	-	-	ns

Table 22 - Bit-Clock and Word-Select Timing Definitions

I²C Slave Interface Timing

The I²C slave interface is used when the MODE pin (Pin 23) is pulled low.

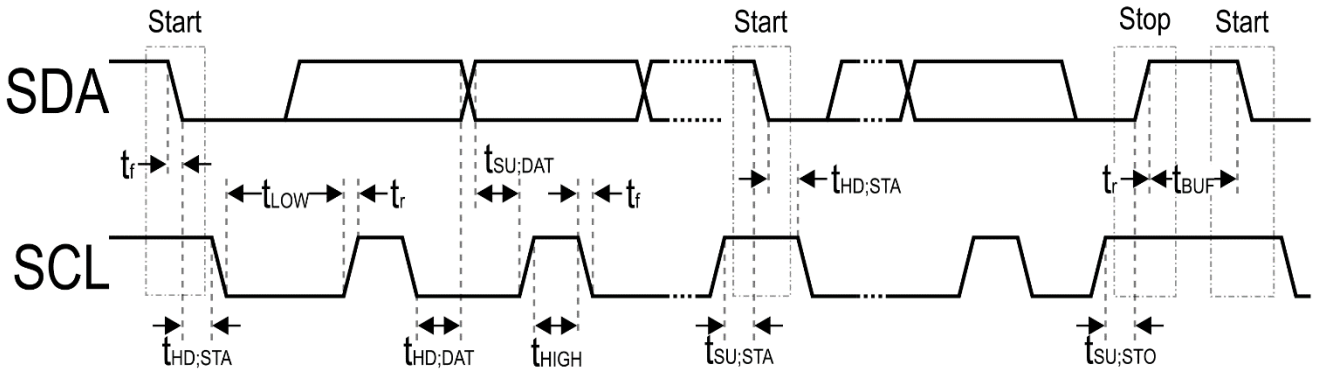


Figure 20 - I²C Slave Control Interface Timing

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD;STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU;STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All Except NACK Read - NACK Read Only	$t_{HD;DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU;DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000		300	ns
Fall time of SDA and SCL	t_f		-	300		300	ns
STOP condition setup time	$t_{SU;STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

Table 23 - I²C Slave/Synchronous Slave Interface Timing Definitions

Note: All bus transitions between start and stop must be part of the transaction when writing to the ESS device

SPI Slave Interface Timing

The SPI slave interface is used when MODE pin (Pin 23) is pulled high.

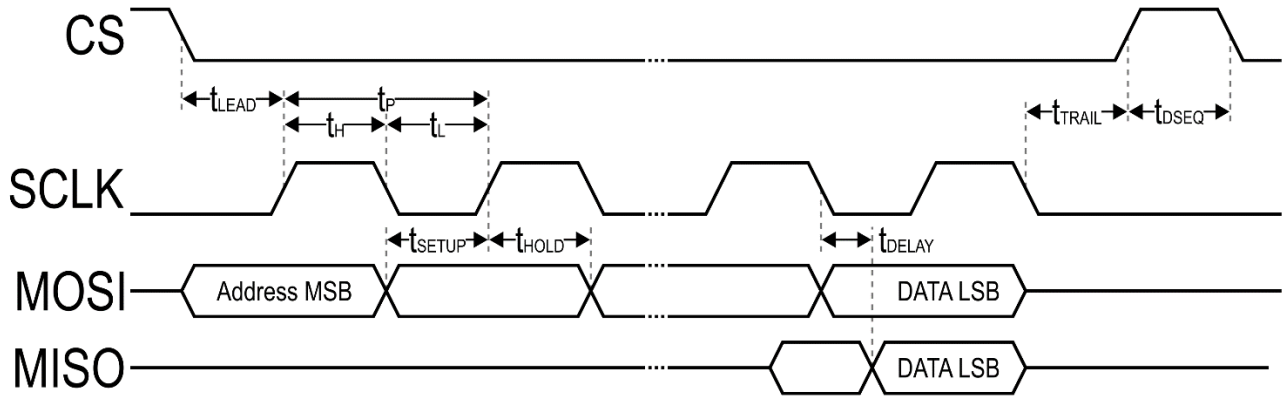


Figure 21 - SPI Slave Interface Timing

Parameter	Symbol	Min	Max	Unit
CS Lead Time (SCLK rising edge)	t_{LEAD}	5	-	ns
CS Trail Time (SCLK falling edge)	t_{TRAIL}	5	-	ns
MOSI Data Setup Time	t_{SETUP_MOSI}	-35	-	ns
MOSI Data Hold Time	t_{HOLD_MOSI}	61	-	ns
SCLK-MISO Delay Time	t_{DELAY_MISO}	-	80	ns
SCLK Period	t_{P_SCLK}	123	-	ns
SCLK High Pulse Duration	t_{H_SCLK}	95	-	ns
SCLK Low Pulse Duration	t_{L_SCLK}	61	-	ns
Sequential Transfer Delay	t_{DSEQ}	39	-	ns

Table 24 - SPI Slave Interface Timing Definitions

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Operating Temperature	T_A	–20°C to +85°C
AVCC_L		3.3V
AVCC_R		3.3V
AVDD		3.3V
VCCA		3.3V
DVDD		1.2V

Table 25 - Recommended Operating Conditions

Power Consumption

Power numbers are given when the device is in slave mode.

Test Conditions 1 (unless otherwise noted)
T_A=25ºC, AVCC_R=AVCC_L=VCCA=AVDD=+3.3V, DVDD=+1.2V, fs=48kHz, DAC enabled, 1kHz sine full scale

Parameter	Min	Typ.	Max	Unit
Standby (CHIP_EN=0)				
AVCC		<60		µA
AVDD		3		µA
VCCA		1		µA
DVDD		1.4		mA
Hardware Mode: 3 (MCLK = 49.152MHz) Master Mode 1024*fs				
AVCC_R		57.0		mA
AVCC_L		57.0		mA
VCCA		1.1		mA
AVDD		2.4		mA
DVDD		69.4		mA
Hardware Mode: 2 (MCLK = 24.576MHz)				
AVCC_R		50.5		mA
AVCC_L		50.5		mA
VCCA		0.6		mA
AVDD		2.4		mA
DVDD		36.0		mA
Hardware Mode: 18 (MCLK = 50MHz)				
AVCC_R		45.3		mA
AVCC_L		45.3		mA
VCCA		0.42		mA
AVDD		0.4		mA
DVDD		41.6		mA

Table 26 - Power Consumption with Test Condition 1

Test Conditions 2 (unless otherwise noted)
T_A=25ºC, AVCC_R=AVCC_L=VCCA=AVDD=+3.3V, DVDD=+1.2V, fs=48kHz, DAC enabled, streaming zeros

Parameter	Min	Typ.	Max	Unit
Hardware Mode: 3 (MCLK = 49.152MHz)				
AVCC_R		13.7		mA
AVCC_L		13.7		mA
VCCA		1.0		mA
AVDD		2.3		mA
DVDD		42.3		mA
Hardware Mode: 2 (MCLK = 24.576MHz)				
AVCC_R		7.6		mA
AVCC_L		7.6		mA
VCCA		0.6		mA
AVDD		2.4		mA
DVDD		17.1		mA
Hardware Mode: 18 (MCLK = 50MHz)				
AVCC_R		4.0		mA
AVCC_L		4.0		mA
VCCA		0.5		mA
AVDD		0.4		mA
DVDD		29.3		mA

Table 27 - Power Consumption with Test Condition 2

Performance

Test Conditions 1 (unless otherwise notes)
T_A=25ºC, AVCC_R=AVCC_L=VCCA=AVDD=+3.3V, DVDD=+1.2V, fs=48kHz, HW mode 3

Parameter		Min	Typ.	Max	Unit
Resolution			32		Bit
Max MCLK frequency				50	MHz
THD+N Ratio @ fs=48kHz, BW=20Hz-20kHz (differential) 8 Channel			-120		dB
THD+N Ratio @ fs=48kHz, BW=20Hz-20kHz (differential) Mono			-122		dB
DNR (A-weighted) 8 Channel mode – Single channel diff	-60dBFS		132		dB
DNR (A-weighted) (Stereo mode – 4 channel sum diff)			137		dB
DNR (A-weighted) (Mono mode – 8 channel sum diff)			140		dB
Voltage output amplitude	Full-scale out		$0.889 * \mathrm{AVCC}$		Vpp
Voltage output offset	Bipolar zero out		$\frac{\mathrm{AVCC}}{2}$		V
Current output amplitude	Full-scale out		$\frac{1000 * 0.889 * \mathrm{AVCC}}{\mathrm{Rdac}}$		mApp
Current output offsets	Bipolar zero out		$\frac{1000 * \left(\frac{\mathrm{AVCC}}{2} - \mathrm{Vg}\right)}{\mathrm{Rdac}}$		mA
Output impedance (Per + or – pin of each differential DAC output pair)	Rdac		195±15%		Ω

Table 28 - Performance Metrics

Register Overview

I²C Slave Interface

This interface uses device addresses 0x90-0x97 and contains Read/Write and Read-only registers. A system clock must be present.

Read/Write Register Addresses

Registers 0-130 (0x00 - 0x82) are read/write registers.

Read-only Register Addresses

Register 224-249 (0xE0 - 0xF9) are read only registers.

Multi-Byte Registers

Multi-Byte registers must be written from LSB to MSB. Data is latched when MSB is written.
Multi-Byte registers must be read from LSB to MSB. Data is latched when LSB is read.
MSB is always stored in the highest address.

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYSTEM CONFIG	SOFT_RESET	ENABLE_64FS_ MODE	CH78_SEL		CH56_SEL	CH34_SEL	DAC_MODE_ REG	RESERVED
0x01	1	SYS MODE CONFIG	ENABLE_SYS_ CLK	SYNC_MODE	RESERVED		ENABLE_SPDIF _DECODE	ENABLE_DOP_ DECODE	ENABLE_DSD_ DECODE	ENABLE_TDM_ DECODE
0x02	2	CLOCK ENABLE	RESERVED							
0x03	3	DAC CLOCK CONFIG	AUTO_FS_ DETECT	SELECT_IDAC_ HALF	SELECT_IDAC_NUM					
0x04	4	CLOCK CONFIG	MASTER_BCK_DIV							
0x05	5	CLK GEAR SELECT	RESERVED		SEL_CLK_GEAR		RESERVED	AUTO_CLK_GE AR	RESERVED	
0x06-0x09	6-9	RESERVED	RESERVED							
0x0A	10	INTERRUPT VOL MIN MASKP	VOL_MIN_CH8_ MASKP	VOL_MIN_CH7_ MASKP	VOL_MIN_CH6_ MASKP	VOL_MIN_CH5_ MASKP	VOL_MIN_CH4_ MASKP	VOL_MIN_CH3_ MASKP	VOL_MIN_CH2_ MASKP	VOL_MIN_CH1_ MASKP
0x0B	11	INTERRUPT AUTOMUTE MASKP	AUTOMUTE_ FLAG_CH8_ MASKP	AUTOMUTE_ FLAG_CH7_ MASKP	AUTOMUTE_ FLAG_CH6_ MASKP	AUTOMUTE_ FLAG_CH5_ MASKP	AUTOMUTE_ FLAG_CH4_ MASKP	AUTOMUTE_ FLAG_CH3_ MASKP	AUTOMUTE_ FLAG_CH2_ MASKP	AUTOMUTE_ FLAG_CH1_ MASKP
0x0C	12	INTERRUPT SS FULL RAMP MASKP	SS_FULL_ RAMP_CH8_ MASKP	SS_FULL_ RAMP_CH7_ MASKP	SS_FULL_ RAMP_CH6_ MASKP	SS_FULL_ RAMP_CH5_ MASKP	SS_FULL_ RAMP_CH4_ MASKP	SS_FULL_ RAMP_CH3_ MASKP	SS_FULL_ RAMP_CH2_ MASKP	SS_FULL_ RAMP_CH1_ MASKP
0x0D	13	INTERRUPT MASKP	INPUT_SELECT_OVERRIDE_MASKP		TDM_VALID_ EDGE_MASKP	RESERVED			BCK_WS_FAIL_ MASKP	DOP_VALID_ MASKP
0x0E	14	RESERVED	RESERVED							
0x0F	15	INTERUPT VOL MIN MASKN	VOL_MIN_CH8_ MASKN	VOL_MIN_CH7_ MASKN	VOL_MIN_CH6_ MASKN	VOL_MIN_CH5_ MASKN	VOL_MIN_CH4_ MASKN	VOL_MIN_CH3_ MASKN	VOL_MIN_CH2_ MASKN	VOL_MIN_CH1_ MASKN
0x10	16	INTERRUPT AUTOMUTE MASKN	AUTOMUTE_ FLAG_CH8_ MASKN	AUTOMUTE_ FLAG_CH7_ MASKN	AUTOMUTE_ FLAG_CH6_ MASKN	AUTOMUTE_ FLAG_CH5_ MASKN	AUTOMUTE_ FLAG_CH4_ MASKN	AUTOMUTE_ FLAG_CH3_ MASKN	AUTOMUTE_ FLAG_CH2_ MASKN	AUTOMUTE_ FLAG_CH1_ MASKN
0x11	17	INTERRUPT SS FULL RAMP MASKN	SS_FULL_ RAMP_CH8_ MASKN	SS_FULL_ RAMP_CH7_ MASKN	SS_FULL_ RAMP_CH6_ MASKN	SS_FULL_ RAMP_CH5_ MASKN	SS_FULL_ RAMP_CH4_ MASKN	SS_FULL_ RAMP_CH3_ MASKN	SS_FULL_ RAMP_CH2_ MASKN	SS_FULL_ RAMP_CH1_ MASKN
0x12	18	INTERRUPT MASKN	INPUT_SELECT_OVERRIDE_MASKN		TDM_VALID_ EDGE_MASKN	RESERVED			BCK_WS_FAIL_ MASKN	DOP_VALID_ MASKN
0x13	19	RESERVED	RESERVED							
0x14	20	INTERRUPT VOL MIN CLEAR	VOL_MIN_CH8_ CLEAR	VOL_MIN_CH7_ CLEAR	VOL_MIN_CH6_ CLEAR	VOL_MIN_CH5_ CLEAR	VOL_MIN_CH4_ CLEAR	VOL_MIN_CH3_ CLEAR	VOL_MIN_CH2_ CLEAR	VOL_MIN_CH1_ CLEAR
0x15	21	INTERRUPT AUTOMUTE CLEAR	AUTOMUTE_ FLAG_CH8_ CLEAR	AUTOMUTE_ FLAG_CH7_ CLEAR	AUTOMUTE_ FLAG_CH6_ CLEAR	AUTOMUTE_ FLAG_CH5_ CLEAR	AUTOMUTE_ FLAG_CH4_ CLEAR	AUTOMUTE_ FLAG_CH3_ CLEAR	AUTOMUTE_ FLAG_CH2_ CLEAR	AUTOMUTE_ FLAG_CH1_ CLEAR
0x16	22	INTERRUPT SS FULL RAMP CLEAR	SS_FULL_ RAMP_CH8_ CLEAR	SS_FULL_ RAMP_CH7_ CLEAR	SS_FULL_ RAMP_CH6_ CLEAR	SS_FULL_ RAMP_CH5_ CLEAR	SS_FULL_ RAMP_CH4_ CLEAR	SS_FULL_ RAMP_CH3_ CLEAR	SS_FULL_ RAMP_CH2_ CLEAR	SS_FULL_ RAMP_CH1_ CLEAR
0x17	23	INTERRUPT CLEAR	INPUT_SELECT_OVERRIDE_CLEAR		TDM_VALID_ EDGE_CLEAR	RESERVED			BCK_WS_FAIL_ CLEAR	DOP_VALID_ CLEAR
0x18-0x1C	24-28	RESERVED	RESERVED							
0x1D	29	DPLL BW	DPLL_BW				RESERVED			ASYNC_64FS_ EN
0x1E-0x21	30-33	RESERVED	RESERVED							
0x22	34	DIGITAL AUTO CONTROL CONFIG	RESERVED	CAL_RES_ENB	RESERVED					
0x23-0x24	35-36	RESERVED	RESERVED							
0x25	37	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG			
0x26	38	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x27	39	GPIO5/6 CONFIG	GPIO6_CFG				GPIO5_CFG			
0x28	40	GPIO7/8 CONFIG	GPIO8_CFG				GPIO7_CFG			
0x29	41	GPIO OUTPUT ENABLE	GPIO8_OE	GPIO7_OE	GPIO6_OE	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x2A	42	GPIO INPUT	GPIO8_SDB	GPIO7_SDB	GPIO6_SDB	GPIO5_SDB	GPIO4_SDB	GPIO3_SDB	GPIO2_SDB	GPIO1_SDB
0x2B	43	GPIO WK EN	GPIO8_WK_EN	GPIO7_WK_EN	GPIO6_WK_EN	GPIO5_WK_EN	GPIO4_WK_EN	GPIO3_WK_EN	GPIO2_WK_EN	GPIO1_WK_EN
0x2C	44	INVERT GPIO	INVERT_GPIO8	INVERT_GPIO7	INVERT_GPIO6	INVERT_GPIO5	INVERT_GPIO4	INVERT_GPIO3	INVERT_GPIO2	INVERT_GPIO1
0x2D	45	GPIO READ CONTROL	GPIO8_READ	GPIO7_READ	GPIO6_READ	GPIO5_READ	GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ
0x2E	46	GPIO OUTPUT LOGIC	FLAG_CH_SEL		GPIO_OR_SS_ RAMP	GPIO_OR_VOL_ MIN	GPIO_OR_ AUTOMUTE	GPIO_AND_SS_ RAMP	GPIO_AND_VOL _MIN	GPIO_AND_ AUTOMUTE
0x2F	47		GPIO_DAC_ MODE	RESERVED						FLAG_CH_SEL
0x30	48	PWM1 COUNT	PWM1_COUNT							
0x31	49	PWM1 FREQUENCY	PWM1_FREQ							
0x32	50		PWM1_FREQ							
0x33	51	PWM2 COUNT	PWM2_COUNT							
0x34	52	PWM2 FREQUENCY	PWM2_FREQ							
0x35	53		PWM2_FREQ							
0x36	54	PWM3 COUNT	PWM3_COUNT							
0x37	55	PWM3 FREQUENCY	PWM3_FREQ							
0x38	56		PWM3_FREQ							
0x39	57	INPUT SELECTION	AUTO_CH_ DETECT	ENABLE_DSD_ FAULT_ DETECTION	DSD_MASTER_ MODE	PCM_MASTER_ MODE	RESERVED	INPUT_SEL		AUTO_INPUT_ SEL
0x3A	58	SERIAL MASTER ENCODER CONFIG	TDM_RESYNC	BCK_INV	RESERVED	MASTER_FRAME_LENGTH		MASTER_WS_ PULSE_MODE	MASTER_WS_ INVERT	MASTER_BCK_ INVERT
0x3B	59	TDM CONFIG	RESERVED		TDM_CH_NUM					
0x3C	60	TDM CONFIG1	TDM_LJ_MODE	TDM_VALID_ EDGE	RESERVED					
0x3D	61	TDM CONFIG2	ENABLE_ ASYNC_LOCK_ MONITOR	TDM_BIT_WIDTH	RESERVED					
0x3E	62	BCK/WS MONITOR CONFIG	DISABLE_DSD_ DC	DISABLE_DSD_ MUTE	ENABLE_WS_ MONITOR	ENABLE_BCK_ MONITOR	DISABLE_PCM_ DC	RESERVED		

0x3F	63	RESERVED	RESERVED							
0x40	64	TDM CH1 CONFIG	RESERVED	TDM_CH1_LINE_SEL	TDM_CH1_SLOT_SEL					
0x41	65	TDM CH2 CONFIG	RESERVED	TDM_CH2_LINE_SEL	TDM_CH2_SLOT_SEL					
0x42	66	TDM CH3 CONFIG	RESERVED	TDM_CH3_LINE_SEL	TDM_CH3_SLOT_SEL					
0x43	67	TDM CH4 CONFIG	RESERVED	TDM_CH4_LINE_SEL	TDM_CH4_SLOT_SEL					
0x44	68	TDM CH5 CONFIG	RESERVED	TDM_CH5_LINE_SEL	TDM_CH5_SLOT_SEL					
0x45	69	TDM CH6 CONFIG	RESERVED	TDM_CH6_LINE_SEL	TDM_CH6_SLOT_SEL					
0x46	70	TDM CH7 CONFIG	RESERVED	TDM_CH7_LINE_SEL	TDM_CH7_SLOT_SEL					
0x47	71	TDM CH8 CONFIG	RESERVED	TDM_CH8_LINE_SEL	TDM_CH8_SLOT_SEL					
0x48-0x49	72-73	RESERVED	RESERVED							
0x4A	74	VOLUME CH1	VOLUME_CH1							
0x4B	75	VOLUME CH2	VOLUME_CH2							
0x4C	76	VOLUME CH3	VOLUME_CH3							
0x4D	77	VOLUME CH4	VOLUME_CH4							
0x4E	78	VOLUME CH5	VOLUME_CH5							
0x4F	79	VOLUME CH6	VOLUME_CH6							
0x50	80	VOLUME CH7	VOLUME_CH7							
0x51	81	VOLUME CH8	VOLUME_CH8							
0x52	82	DAC VOL UP RATE	DAC_VOL_RATE_UP							
0x53	83	DAC VOL DOWN RATE	DAC_VOL_RATE_DOWN							
0x54	84	DAC VOL DOWN RATE FAST	DAC_VOL_RATE_FAST							
0x55	85	RESERVED	RESERVED							
0x56	86	DAC MUTE	DAC_MUTE_CH8	DAC_MUTE_CH7	DAC_MUTE_CH6	DAC_MUTE_CH5	DAC_MUTE_CH4	DAC_MUTE_CH3	DAC_MUTE_CH2	DAC_MUTE_CH1
0x57	87	DAC INVERT	DAC_INVERT_CH8	DAC_INVERT_CH7	DAC_INVERT_CH6	DAC_INVERT_CH5	DAC_INVERT_CH4	DAC_INVERT_CH3	DAC_INVERT_CH2	DAC_INVERT_CH1
0x58	88	FILTER SHAPE	RESERVED					FILTER_SHAPE		
0x59	89	IIR BANDWIDTH & S/PDIF SELECT	SPDIF_SEL				VOLUME_HOLD	IIR_BW		
0x5A	90	DAC PATH CONFIG	RESERVED					BYPASS_IIR	BYPASS_FIR4X	BYPASS_FIR2X
0x5B	91	THD C2 L	THD_C2_CH1							
0x5C	92		THD_C2_CH1							
0x5D	93		THD_C2_CH2							
0x5E	94		THD_C2_CH2							
0x5F	95		THD_C2_CH3							
0x60	96		THD_C2_CH3							
0x61	97		THD_C2_CH4							
0x62	98		THD_C2_CH4							
0x63	99	THD C2 H	THD_C2_CH5							
0x64	100		THD_C2_CH5							
0x65	101		THD_C2_CH6							
0x66	102		THD_C2_CH6							
0x67	103		THD_C2_CH7							
0x68	104		THD_C2_CH7							
0x69	105		THD_C2_CH8							
0x6A	106		THD_C2_CH8							
0x6B	107	THD C3 L	THD_C3_CH1							
0x6C	108		THD_C3_CH1							
0x6D	109		THD_C3_CH2							
0x6E	110		THD_C3_CH2							
0x6F	111		THD_C3_CH3							
0x70	112		THD_C3_CH3							
0x71	113		THD_C3_CH4							
0x72	114		THD_C3_CH4							
0x73	115	THD C3 H	THD_C3_CH5							
0x74	116		THD_C3_CH5							
0x75	117		THD_C3_CH6							
0x76	118		THD_C3_CH6							
0x77	119		THD_C3_CH7							
0x78	120		THD_C3_CH7							
0x79	121		THD_C3_CH8							
0x7A	122		THD_C3_CH8							
0x7B	123	AUTOMUTE ENABLE	AUTOMUTE_EN_CH8	AUTOMUTE_EN_CH7	AUTOMUTE_EN_CH6	AUTOMUTE_EN_CH5	AUTOMUTE_EN_CH4	AUTOMUTE_EN_CH3	AUTOMUTE_EN_CH2	AUTOMUTE_EN_CH1
0x7C	124	AUTOMUTE TIME	AUTOMUTE_TIME							
0x7D	125		RESERVED				AUTOMUTE_RAMP_TO_GROUND	AUTOMUTE_TIME		
0x7E	126	AUTOMUTE LEVEL	AUTOMUTE_LEVEL							
0x7F	127		AUTOMUTE_LEVEL							
0x80	128	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL							
0x81	129		AUTOMUTE_OFF_LEVEL							
0x82	130	SOFT RAMP CONFIG	RESERVED		SOFT_RAMP_TIME					
0x83-0x86	131-134	RESERVED	RESERVED							
0x87	135	PROGRAM ROM CONTROL	RESERVED						PROG_COEFF_WE	PROG_COEFF_EN
0x88	136	S/PDIF READ CONTROL	RESERVED		SPDIF_DATA_SEL					
0x89	137	PROGRAM RAM ADDRESS	PROG_COEFF_STAGE	PROG_COEFF_ADDR						
0x8A	138	PROGRAM RAM DATA	PROG_COEFF_IN							
0x8B	139		PROG_COEFF_IN							
0x8C	140		PROG_COEFF_IN							
0x8D	141	MQA CONFIG	RESERVED					MQB_READER_ENABLE		MQA_RENDERING_ENABLE
0x8E-0x91	142-145	RESERVED	RESERVED							
0xE0	224	SYS READ	RESERVED				MODES		ADDR1	ADDR0
0xE1	225	CHIP ID READ	CHIP_ID							

0xE2-0xE4	226-228	RESERVED							
0xE5	229	INTERRUPT STATE	VOL_MIN_STATE						
0xE6	230		AUTOMUTE_STATE						
0xE7	231		SS_FULL_RAMP_STATE						
0xE8	232		INPUT_SELECT_OVERRIDE_STATE		TDM_DATA_VALID_STATE	RESERVED		BCK_WS_FAIL_STATE	DOP_VALID_STATE
0xE9	233	RESERVED	RESERVED						
0xEA	234	INTERRUPT SOURCE	VOL_MIN_SOURCE						
0xEB	235		AUTOMUTE_SOURCE						
0xEC	236		SS_FULL_RAMP_SOURCE						
0xED	237		INPUT_SELECT_OVERRIDE_SOURCE		TDM_DATA_VALID_SOURCE	RESERVED		BCK_WS_FAIL_SOURCE	DOP_VALID_SOURCE
0xEE	238	RESERVED	RESERVED						
0xEF	239	RATIO VALID READ	RATIO_VALID	IDAC_DIV_HALF_AUTO	IDAC_DIV_NUM_AUTO				
0xF0	240	GPIO READBACK	GPIO8_I_READ	GPIO7_I_READ	GPIO6_I_READ	GPIO5_I_READ	GPIO4_I_READ	GPIO3_I_READ	GPIO2_I_READ	GPIO1_I_READ
0xF1	241	VOL MIN READ	VOL_MIN_CH8	VOL_MIN_CH7	VOL_MIN_CH6	VOL_MIN_CH5	VOL_MIN_CH4	VOL_MIN_CH3	VOL_MIN_CH2	VOL_MIN_CH1
0xF2	242	AUTOMUTE READ	AUTOMUTE_CH8	AUTOMUTE_CH7	AUTOMUTE_CH6	AUTOMUTE_CH5	AUTOMUTE_CH4	AUTOMUTE_CH3	AUTOMUTE_CH2	AUTOMUTE_CH1
0xF3	243	SOFT RAMP UP READ	SS_RAMP_UP_CH8	SS_RAMP_UP_CH7	SS_RAMP_UP_CH6	SS_RAMP_UP_CH5	SS_RAMP_UP_CH4	SS_RAMP_UP_CH3	SS_RAMP_UP_CH2	SS_RAMP_UP_CH1
0xF4	244	SOFT RAMP DOWN READ	SS_RAMP_DOWN_CH8	SS_RAMP_DOWN_CH7	SS_RAMP_DOWN_CH6	SS_RAMP_DOWN_CH5	SS_RAMP_DOWN_CH4	SS_RAMP_DOWN_CH3	SS_RAMP_DOWN_CH2	SS_RAMP_DOWN_CH1
0xF5	245	S/PDIF, TDM, DOP, AND INPUT READBACK	SPDIF_VALID	TDM_DATA_VALID	DOP_VALID				INPUT_SELECT_OVERRIDE	
0xF6	246	PROG COEFF OUT READ	PROG_COEFF_OUT							
0xF7	247		PROG_COEFF_OUT							
0xF8	248		PROG_COEFF_OUT							
0xF9-0xFA	249-250	RESERVED	AUTO_CH_NUM					RESERVED		
0xFB	251	S/PDIF DATA READ	SPDIF_DATA_READ							

Table 29 - Register Map

Register Listing

System Registers

Register 0: SYSTEM CONFIG

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	2'b00	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core. • 1'b0: Normal operation • 1'b1: Reset digital core (all settings are set to default)
[6]	ENABLE_64FS_MODE	Enables 64FS mode to run the DAC interpolation path at 64FS. • 1'b0: 64FS mode disabled (default) • 1'b1: 64FS mode enabled Note: This mode should be used for high sample rate (i.e., 705.6/768kHz)
[5:4]	CH78_SEL	Selects ch7/8 nsmod input. • 2'b00: Input from ch7/8 interpolation path (default) • 2'b01: Input from ch5/6 interpolation path • 2'b10: Input from ch1/2 interpolation path • 2'b11: Reserved
[3]	CH56_SEL	Selects ch5/6 nsmod input. • 1'b0: Input from ch5/6 interpolation path (default) • 1'b1: Input from ch1/2 interpolation path
[2]	CH34_SEL	Selects ch3/4 nsmod input. • 1'b0: Input from ch3/4 interpolation path (default) • 1'b1: Input from ch1/2 interpolation path
[1]	DAC_MODE_REG	Enables DAC datapath. • 1'b0: DAC disabled • 1'b1: DAC enabled
[0]	RESERVED	N/A

Register 1: SYS MODE CONFIG

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b0	2'b11	1'b0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	ENABLE_SYS_CLK	Enables System Clock input into the DAC Datapath. • 1'b0: SYS_CLK disabled • 1'b1: SYS_CLK enabled (default)
[6]	SYNC_MODE	Enables SYNC mode. • 1'b0: ASYNC mode enabled (default) • 1'b1: SYNC mode enabled
[5:4]	RESERVED	N/A
[3]	ENABLE_SPDIF_DECODE	Enables S/PDIF decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	ENABLE_DOP_DECODE	Enables DoP decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ENABLE_DSD_DECODE	Enables DSD decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ENABLE_TDM_DECODE	Enables TDM decoding. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 2: RESERVED

Register 3: DAC CLOCK CONFIG

Bits	[7]	[6]	[5:0]
Default	1'b1	1'b0	6'd0

Bits	Mnemonic	Description
[7]	AUTO_FS_DETECT	• 1'b0: Disabled • 1'b1: Auto tune SYS_CLK/CLK_IDAC ratio according to detected FS (default) Note: Cannot be used in ASYNC mode
[6]	SELECT_IDAC_HALF	• 1'b0: Divide by SELECT_IDAC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_IDAC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	SELECT_IDAC_NUM	CLK_IDAC divider. Whole number divide value + 1 for CLK_IDAC (SYS_CLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 • 6'd1: Whole number divide value + 1 = 2 • 6'd63: Whole number divide value + 1 = 64

Register 4: CLOCK CONFIG

Bits	[7:0]
Default	8'd7

Bits	Mnemonic	Description
[7:0]	MASTER_BCK_DIV	Master mode clock divider. Whole number divide value + 1 for generated Master BCK (SYS_CLK/divide_value).

Register 5: CLK GEAR SELECT

Bits	[7:6]	[5:4]	[3]	[2]	[1:0]
Default	2'b00	2'd0	1'b0	1'b0	2'b00

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5:4]	SEL_CLK_GEAR	Clock Gearing • 2'd0: MCLK/1 • 2'd1: MCLK/2 • 2'd2: MCLK/4 • 2'd3: MCLK/8
[3]	RESERVED	N/A
[2]	AUTO_CLK_GEAR	• 1'b0: Disable automatic clock gearing. SYS_CLK = SEL_CLK_GEAR • 1'b1: Enable automatic clock gearing. SYS_CLK will decrease up to SEL_CLK_GEAR
[1:0]	RESERVED	N/A

Register 9-6: RESERVED

Register 10: INTERRUPT VOL MIN MASKP

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[6]	VOL_MIN_CH7_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	VOL_MIN_CH6_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	VOL_MIN_CH5_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	VOL_MIN_CH4_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	VOL_MIN_CH3_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	VOL_MIN_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	VOL_MIN_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 11: INTERRUPT AUTOMUTE MASKP

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_FLAG_CH8_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[6]	AUTOMUTE_FLAG_CH7_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	AUTOMUTE_FLAG_CH6_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	AUTOMUTE_FLAG_CH5_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	AUTOMUTE_FLAG_CH4_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	AUTOMUTE_FLAG_CH3_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	AUTOMUTE_FLAG_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	AUTOMUTE_FLAG_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 12: INTERRUPT SS FULL RAMP MASKP

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SS_FULL_RAMP_CH8_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[6]	SS_FULL_RAMP_CH7_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	SS_FULL_RAMP_CH6_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4]	SS_FULL_RAMP_CH5_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[3]	SS_FULL_RAMP_CH4_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[2]	SS_FULL_RAMP_CH3_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[1]	SS_FULL_RAMP_CH2_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	SS_FULL_RAMP_CH1_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 14-13: INTERRUPT MASKP

Bits	[15:8]	[7:6]	[5]	[4:2]	[1]	[0]
Default	8'b00000000	2'b00	1'b0	3'b000	1'b0	1'b0

Bits	Mnemonic	Description
[15:8]	RESERVED	N/A
[7:6]	INPUT_SELECT_OVERRIDE_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[5]	TDM_VALID_EDGE_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[4:2]	RESERVED	N/A
[1]	BCK_WS_FAIL_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive
[0]	DOP_VALID_MASKP	Masks negative to positive interrupt toggling. • 1'b0: Ignore interrupt if toggled from negative to positive • 1'b1: Service interrupt if toggled from negative to positive

Register 15: INTERUPT VOL MIN MASKN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[6]	VOL_MIN_CH7_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	VOL_MIN_CH6_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	VOL_MIN_CH5_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	VOL_MIN_CH4_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	VOL_MIN_CH3_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	VOL_MIN_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	VOL_MIN_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 16: INTERRUPT AUTOMUTE MASKN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_FLAG_CH8_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[6]	AUTOMUTE_FLAG_CH7_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	AUTOMUTE_FLAG_CH6_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	AUTOMUTE_FLAG_CH5_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	AUTOMUTE_FLAG_CH4_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	AUTOMUTE_FLAG_CH3_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	AUTOMUTE_FLAG_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	AUTOMUTE_FLAG_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 17: INTERRUPT SS FULL RAMP MASKN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SS_FULL_RAMP_CH8_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[6]	SS_FULL_RAMP_CH7_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	SS_FULL_RAMP_CH6_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4]	SS_FULL_RAMP_CH5_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[3]	SS_FULL_RAMP_CH4_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[2]	SS_FULL_RAMP_CH3_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[1]	SS_FULL_RAMP_CH2_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	SS_FULL_RAMP_CH1_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 19-18: INTERRUPT MASKN

Bits	[15:8]	[7:6]	[5]	[4:2]	[1]	[0]
Default	8'b00000000	2'b00	1'b0	3'b000	1'b0	1'b0

Bits	Mnemonic	Description
[15:8]	RESERVED	N/A
[7:6]	INPUT_SELECT_OVERRIDE_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[5]	TDM_VALID_EDGE_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[4:2]	RESERVED	N/A
[1]	BCK_WS_FAIL_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative
[0]	DOP_VALID_MASKN	Masks positive to negative interrupt toggling. • 1'b0: Ignore interrupt if toggled from positive to negative • 1'b1: Service interrupt if toggled from positive to negative

Register 20: INTERRUPT VOL MIN CLEAR

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8_CLEAR	Write a 1'b1 to clear the interrupt
[6]	VOL_MIN_CH7_CLEAR	
[5]	VOL_MIN_CH6_CLEAR	
[4]	VOL_MIN_CH5_CLEAR	
[3]	VOL_MIN_CH4_CLEAR	
[2]	VOL_MIN_CH3_CLEAR	
[1]	VOL_MIN_CH2_CLEAR	
[0]	VOL_MIN_CH1_CLEAR	

Register 21: INTERRUPT AUTOMUTE CLEAR

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	AUTOMUTE_FLAG_CH8_CLEAR	
[6]	AUTOMUTE_FLAG_CH7_CLEAR	
[5]	AUTOMUTE_FLAG_CH6_CLEAR	
[4]	AUTOMUTE_FLAG_CH5_CLEAR	
[3]	AUTOMUTE_FLAG_CH4_CLEAR	
[2]	AUTOMUTE_FLAG_CH3_CLEAR	
[1]	AUTOMUTE_FLAG_CH2_CLEAR	
[0]	AUTOMUTE_FLAG_CH1_CLEAR	

Register 22: INTERRUPT SS FULL RAMP CLEAR

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SS_FULL_RAMP_CH8_CLEAR	
[6]	SS_FULL_RAMP_CH7_CLEAR	
[5]	SS_FULL_RAMP_CH6_CLEAR	
[4]	SS_FULL_RAMP_CH5_CLEAR	
[3]	SS_FULL_RAMP_CH4_CLEAR	
[2]	SS_FULL_RAMP_CH3_CLEAR	
[1]	SS_FULL_RAMP_CH2_CLEAR	
[0]	SS_FULL_RAMP_CH1_CLEAR	

Register 24-23: INTERRUPT CLEAR

Bits	[15:8]	[7:6]	[5]	[4:2]	[1]	[0]
Default	8'b00000000	2'b00	1'b0	3'b000	1'b0	1'b0

Bits	Mnemonic	Description
[15:8]	RESERVED	N/A
[7:6]	INPUT_SELECT_OVERRIDE_CLEAR	
[5]	TDM_VALID_EDGE_CLEAR	
[4:2]	RESERVED	N/A
[1]	BCK_WS_FAIL_CLEAR	
[0]	DOP_VALID_CLEAR	

Register 25: RESERVED

Register 29-26: DPLL BW

Bits	[31:28]	[27:0]
Default	4'd4	28'd0

Bits	Mnemonic	Description
[31:28]	DPLL_BW	Sets the bandwidth of the DPLL. • 4'd0: Reserved • 4'd1: Lowest Bandwidth • 4'd4: Default Bandwidth • 4'd15: Highest Bandwidth
[27:0]	RESERVED	N/A

Register 33-30: RESERVED

Register 34: DIGITAL AUTO CONTROL CONFIG

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'b000000

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	CAL_RES_ENB	Selects the calibration resistor on GPIO3. • 1'b0: DAC calibration resistor enabled (default) • 1'b1: DAC calibration resistor disabled
[5:0]	RESERVED	N/A

Register 36-35: RESERVED

GPIO Registers

Register 37: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd7	4'd13

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configures GPIO2 • 4'd0: Analog shutdown – shutdown • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: OR of All Interrupts – output • 4'd5: Mute All DAC Channels – input • 4'd6: System Mode Control – input • 4'd7: SRC Locked Status – output (default) • 4'd8: CLKEN_1FS – output • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Volume Minimum – output • 4'd13: Automute Status – output • 4'd14: Soft Ramp Done – output • 4'd15: MQA_AUTH_TRUE – output
[3:0]	GPIO1_CFG	Configures GPIO1 • 4'd0: Analog shutdown – shutdown • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: OR of All Interrupts – output • 4'd5: Mute All DAC Channels – input • 4'd6: System Mode Control – input • 4'd7: SRC Locked Status – output • 4'd8: CLKEN_1FS – output • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Volume Minimum – output • 4'd13: Automute Status – output (default) • 4'd14: Soft Ramp Done – output • 4'd15: MQA_AUTH_TRUE – output

Register 38: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configures GPIO4 • 4'd0: Analog shutdown – shutdown • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: OR of All Interrupts – output • 4'd5: Mute All DAC Channels – input • 4'd6: System Mode Control – input • 4'd7: SRC Locked Status – output • 4'd8: CLKEN_1FS – output • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Volume Minimum – output • 4'd13: Automute Status – output • 4'd14: Soft Ramp Done – output • 4'd15: MQA_AUTH_TRUE – output
[3:0]	GPIO3_CFG	Configures GPIO3 • 4'd0: Analog shutdown – shutdown • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: OR of All Interrupts – output • 4'd5: Mute All DAC Channels – input • 4'd6: System Mode Control – input • 4'd7: SRC Locked Status – output • 4'd8: CLKEN_1FS – output • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Volume Minimum – output • 4'd13: Automute Status – output • 4'd14: Soft Ramp Done – output • 4'd15: MQA_AUTH_TRUE – output

Register 39: GPIO5/6 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO6_CFG	Configures GPIO6 • 4'd0: Analog shutdown – shutdown • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: OR of All Interrupts – output • 4'd5: Mute All DAC Channels – input • 4'd6: System Mode Control – input • 4'd7: SRC Locked Status – output • 4'd8: CLKEN_1FS – output • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Volume Minimum – output • 4'd13: Automute Status – output • 4'd14: Soft Ramp Done – output • 4'd15: MQA_AUTH_TRUE – output
[3:0]	GPIO5_CFG	Configures GPIO5 • 4'd0: Analog shutdown – shutdown • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: OR of All Interrupts – output • 4'd5: Mute All DAC Channels – input • 4'd6: System Mode Control – input • 4'd7: SRC Locked Status – output • 4'd8: CLKEN_1FS – output • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Volume Minimum – output • 4'd13: Automute Status – output • 4'd14: Soft Ramp Done – output • 4'd15: MQA_AUTH_TRUE – output

Register 40: GPIO7/8 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO8_CFG	Configures GPIO8 • 4'd0: Analog shutdown – shutdown • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: OR of All Interrupts – output • 4'd5: Mute All DAC Channels – input • 4'd6: System Mode Control – input • 4'd7: SRC Locked Status – output • 4'd8: CLKEN_1FS – output • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Volume Minimum – output • 4'd13: Automute Status – output • 4'd14: Soft Ramp Done – output • 4'd15: MQA_AUTH_TRUE – output
[3:0]	GPIO7_CFG	Configures GPIO7 • 4'd0: Analog shutdown – shutdown • 4'd1: Output 0 – output • 4'd2: Output 1 – output • 4'd3: CLK_IDAC – output • 4'd4: OR of All Interrupts – output • 4'd5: Mute All DAC Channels – input • 4'd6: System Mode Control – input • 4'd7: SRC Locked Status – output • 4'd8: CLKEN_1FS – output • 4'd9: PWM1 signal – output • 4'd10: PWM2 signal – output • 4'd11: PWM3 signal – output • 4'd12: Volume Minimum – output • 4'd13: Automute Status – output • 4'd14: Soft Ramp Done – output • 4'd15: MQA_AUTH_TRUE – output

Register 41: GPIO OUTPUT ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b1

Bits	Mnemonic	Description
[7]	GPIO8_OE	• 1'b0: Tristate GPIO8 (default) • 1'b1: GPIO8 Output Enable
[6]	GPIO7_OE	• 1'b0: Tristate GPIO7 (default) • 1'b1: GPIO7 Output Enable
[5]	GPIO6_OE	• 1'b0: Tristate GPIO6 (default) • 1'b1: GPIO6 Output Enable
[4]	GPIO5_OE	• 1'b0: Tristate GPIO5 (default) • 1'b1: GPIO5 Output Enable
[3]	GPIO4_OE	• 1'b0: Tristate GPIO4 (default) • 1'b1: GPIO4 Output Enable
[2]	GPIO3_OE	• 1'b0: Tristate GPIO3 (default) • 1'b1: GPIO3 Output Enable
[1]	GPIO2_OE	• 1'b0: Tristate GPIO2 • 1'b1: GPIO2 Output Enable (default)
[0]	GPIO1_OE	• 1'b0: Tristate GPIO1 • 1'b1: GPIO1 Output Enable (default)

Register 42: GPIO INPUT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b1	1'b1	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO8_SDB	• 1'b0: Disables GPIO8 input (default) • 1'b1: Enables GPIO8 input
[6]	GPIO7_SDB	• 1'b0: Disables GPIO7 input (default) • 1'b1: Enables GPIO7 input
[5]	GPIO6_SDB	• 1'b0: Disables GPIO6 input (default) • 1'b1: Enables GPIO6 input
[4]	GPIO5_SDB	• 1'b0: Disables GPIO5 input • 1'b1: Enables GPIO5 input (default)
[3]	GPIO4_SDB	• 1'b0: Disables GPIO4 input • 1'b1: Enables GPIO4 input (default)
[2]	GPIO3_SDB	• 1'b0: Disables GPIO3 input (default) • 1'b1: Enables GPIO3 input
[1]	GPIO2_SDB	• 1'b0: Disables GPIO2 input (default) • 1'b1: Enables GPIO2 input
[0]	GPIO1_SDB	• 1'b0: Disables GPIO1 input (default) • 1'b1: Enables GPIO1 input

Register 43: GPIO WK EN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO8_WK_EN	• 1'b0: GPIO8 weak keeper disabled (default) • 1'b1: GPIO8 weak keeper enabled
[6]	GPIO7_WK_EN	• 1'b0: GPIO7 weak keeper disabled (default) • 1'b1: GPIO7 weak keeper enabled
[5]	GPIO6_WK_EN	• 1'b0: GPIO6 weak keeper disabled (default) • 1'b1: GPIO6 weak keeper enabled
[4]	GPIO5_WK_EN	• 1'b0: GPIO5 weak keeper disabled (default) • 1'b1: GPIO5 weak keeper enabled
[3]	GPIO4_WK_EN	• 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[2]	GPIO3_WK_EN	• 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[1]	GPIO2_WK_EN	• 1'b0: GPIO2 weak keeper disabled (default) • 1'b1: GPIO2 weak keeper enabled
[0]	GPIO1_WK_EN	• 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled

Register 44: INVERT GPIO

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	INVERT_GPIO8	• 1'b1: Inverts GPIO8 output.
[6]	INVERT_GPIO7	• 1'b1: Inverts GPIO7 output.
[5]	INVERT_GPIO6	• 1'b1: Inverts GPIO6 output.
[4]	INVERT_GPIO5	• 1'b1: Inverts GPIO5 output.
[3]	INVERT_GPIO4	• 1'b1: Inverts GPIO4 output.
[2]	INVERT_GPIO3	• 1'b1: Inverts GPIO3 output.
[1]	INVERT_GPIO2	• 1'b1: Inverts GPIO2 output.
[0]	INVERT_GPIO1	• 1'b1: Inverts GPIO1 output.

Register 45: GPIO READ CONTROL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	GPIO8_READ	• 1'b0: GPIO8 Readback disabled (default) • 1'b1: Allow readback of GPIO8_I
[6]	GPIO7_READ	• 1'b0: GPIO7 Readback disabled (default) • 1'b1: Allow readback of GPIO7_I
[5]	GPIO6_READ	• 1'b0: GPIO6 Readback disabled (default) • 1'b1: Allow readback of GPIO6_I
[4]	GPIO5_READ	• 1'b0: GPIO5 Readback disabled (default) • 1'b1: Allow readback of GPIO5_I
[3]	GPIO4_READ	• 1'b0: GPIO4 Readback disabled (default) • 1'b1: Allow readback of GPIO4_I
[2]	GPIO3_READ	• 1'b0: GPIO3 Readback disabled (default) • 1'b1: Allow readback of GPIO3_I
[1]	GPIO2_READ	• 1'b0: GPIO2 Readback disabled (default) • 1'b1: Allow readback of GPIO2_I
[0]	GPIO1_READ	• 1'b0: GPIO1 Readback disabled (default) • 1'b1: Allow readback of GPIO1_I

Register 47-46: GPIO OUTPUT LOGIC

Bits	[15]	[14:9]	[8:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	6'd0	3'd0	1'b0	1'b0	1'b0	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[15]	GPIO_DAC_MODE	When any GPIOx_CFG = 6 (input system mode control): • 1'b0: Power down when GPIO input is 1 • 1'b1: HIFI when GPIO input is 1 When GPIO input is 0, system mode is determined by register DAC_MODE_REG (register 0, bit[1])
[14:9]	RESERVED	N/A
[8:6]	FLAG_CH_SEL	When GPIOx_CFG = 12, 13 or 14, and the corresponding GPIO_AND and GPIO_OR are not set: • 3'd0: Outputs status/flag from ch1 • 3'd1: Outputs status/flag from ch2 • 3'd2: Outputs status/flag from ch3 • 3'd3: Outputs status/flag from ch4 • 3'd4: Outputs status/flag from ch5 • 3'd5: Outputs status/flag from ch6 • 3'd6: Outputs status/flag from ch7 • 3'd7: Outputs status/flag from ch8
[5]	GPIO_OR_SS_RAMP	When GPIOx_CFG = 14 (output soft ramp done flag): • 1'b0: The soft ramp done flag is determined by GPIO_AND_SS_RAMP and GPIO_SEL (default) • 1'b1: The soft ramp done flag is the "OR" of all 8ch soft ramp done flags
[4]	GPIO_OR_VOL_MIN	When GPIOx_CFG = 12 (output vol_min flag): • 1'b0: The vol_min flag is determined by GPIO_AND_VOL_MIN and GPIO_SEL (default) • 1'b1: The vol_min flag is the "OR" of all 8ch vol_min flags
[3]	GPIO_OR_AUTOMUTE	When GPIOx_CFG = 13 (output automute status): • 1'b0: The automute status is determined by GPIO_AND_AUTOMUTE and GPIO_SEL (default) • 1'b1: The automute status is the "OR" of all 8ch automute status
[2]	GPIO_AND_SS_RAMP	When GPIOx_CFG = 14 (output soft ramp done flag) and GPIO_OR_SS_RAMP is not set: • 1'b0: The soft ramp done flag is from a single channel selected by GPIO_SEL • 1'b1: The soft ramp done flag is the "AND" of all 8ch soft ramp done flags (default)
[1]	GPIO_AND_VOL_MIN	When GPIOx_CFG = 12 (output vol_min flag) and GPIO_OR_VOL_MIN is not set: • 1'b0: The vol_min flag is from a single channel selected by GPIO_SEL • 1'b1: The vol_min flag is the "AND" of all 8ch vol_min flags (default)

[0]	GPIO_AND_AUTOMUTE	When GPIOx_CFG = 13 (output automute status) and GPIO_OR_AUTOMUTE is not set: • 1'b0: The automute status is from a single channel selected by GPIO_SEL • 1'b1: The automute status is the "AND" of all 8ch automute status (default)

Register 48: PWM1 COUNT

Bits	**[7:0]**
Default	8'h00

Bits	**Mnemonic**	**Description**
[7:0]	PWM1_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 50-49: PWM1 FREQUENCY

Bits	**[15:0]**
Default	16'h0000

Bits	**Mnemonic**	**Description**
[15:0]	PWM1_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{Frequency [Hz]} = \frac{\text{SYS\_CLK}}{\text{PWM1\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \frac{\text{PWM1\_COUNT}}{\text{PWM1\_FREQ} + 1} x100$

Register 51: PWM2 COUNT

Bits	**[7:0]**
Default	8'h00

Bits	**Mnemonic**	**Description**
[7:0]	PWM2_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 53-52: PWM2 FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM2_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{Frequency [Hz]} = \frac{\text{SYS\_CLK}}{\text{PWM2\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \frac{\text{PWM2\_COUNT}}{\text{PWM2\_FREQ} + 1} x100$

Register 54: PWM3 COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM3_COUNT	8-bit value to set the number of SYS_CLK periods the PWM signal is high for. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 56-55: PWM3 FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM3_FREQ	16-bit value to set the frequency of the PWM signal in terms of SYS_CLK divisions. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{Frequency [Hz]} = \frac{\text{SYS\_CLK}}{\text{PWM3\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \frac{\text{PWM3\_COUNT}}{\text{PWM3\_FREQ} + 1} x100$

DAC Registers

Register 57: INPUT SELECTION

Bits	[7]	[6]	[5]	[4]	[3]	[2:1]	[0]
Default	1'b0	1'b1	1'b0	1'b0	1'b0	2'd0	1'b0

Bits	Mnemonic	Description
[7]	AUTO_CH_DETECT	Auto detect BCK/FRAME ratio to determine the number of TDM channels. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ENABLE_DSD_FAULT_DETECTION	Sets a channel to a DSD mute pattern (0x96) if the DSD data has no changes in 64 DATA_CLKs. • 1'b0: Disabled • 1'b1: Enabled (default)
[5]	DSD_MASTER_MODE	DSD master mode config. • 1'b0: DSD slave mode (default) • 1'b1: DSD master mode. DSD_CLK outputs from DATA_CLK
[4]	PCM_MASTER_MODE	PCM master mode config. • 1'b0: PCM slave mode (default) • 1'b1: PCM master mode enabled. Master BCK and WS output from DATA_CLK and DATA1
[3]	RESERVED	N/A
[2:1]	INPUT_SEL	Selects input data format when AUTO_INPUT_SEL is disabled. • 2'd0: TDM (default) • 2'd1: DSD • 2'd2: DoP • 2'd3: S/PDIF
[0]	AUTO_INPUT_SEL	Automatic input data selection config. • 1'b0: Disables auto input select. Input data format is set by INPUT_SEL (default) • 1'b1: Automatically determine the input data format. Note: When enabled, data must be provided on the DATA2 pin, to properly decode the input format.

Register 58: SERIAL MASTER ENCODER CONFIG

Bits	[7]	[6]	[5]	[4:3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	2'b00	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7]	TDM_RESYNC	Force TDM decoder to resync. • 1'b0: Let decoder sync (default) • 1'b1: Force decoder not sync
[6]	BCK_INV	Invert the slave BCK • 1'b0: Normal operation • 1'b1: Invert slave BCK
[5]	RESERVED	N/A
[4:3]	MASTER_FRAME_LENGTH	Selects the bit length in each TDM channel in master mode. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit • 2'b11: Reserved
[2]	MASTER_WS_PULSE_MODE	When enabled, master WS is a pulse signal instead of a 50% duty cycle signal. The pulse width is 1 BCK cycle. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[1]	MASTER_WS_INVERT	Inverts master WS. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	MASTER_BCK_INVERT	Inverts master BCK or DSD_CLK. • 1'b0: Non-inverted • 1'b1: Inverted (default)

Register 59: TDM CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_CH_NUM	Total number of TDM slots per frame = TDM_CH_NUM + 1.

Register 60: TDM CONFIG1

Bits	[7]	[6]	[5:0]
Default	1'b0	1'b0	6'b000001

Bits	Mnemonic	Description
[7]	TDM_LJ_MODE	TDM LJ mode. • 1'b0: Standard I2S (default) • 1'b1: LJ mode
[6]	TDM_VALID_EDGE	TDM WS valid edge. • 1'b0: negative edge (default) • 1'b1: positive edge
[5:0]	RESERVED	N/A

Register 61: TDM CONFIG2

Bits	[7]	[6:5]	[4:0]
Default	1'b1	2'b00	5'd0

Bits	Mnemonic	Description
[7]	ENABLE_ASYNC_LOCK_MONITOR	Monitors the lock status of the SRC, when in ASYNC mode. Sets BCK_WS_FAIL on unlock. • 1'b0: Disabled • 1'b1: Enabled (default)
[6:5]	TDM_BIT_WIDTH	Bit width of each TDM slot. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit • 2'b11: Reserved
[4:0]	RESERVED	N/A

Register 62: BCK/WS MONITOR CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2:0]
Default	1'b0	1'b0	1'b1	1'b1	1'b0	3'd0

Bits	Mnemonic	Description
[7]	DISABLE_DSD_DC	• 1'b0: DSD DC can trigger an automute if automute is enabled (default) • 1'b1: DSD DC is ignored.
[6]	DISABLE_DSD_MUTE	• 1'b0: DSD mute pattern can trigger an automute is automute is enabled (default) • 1'b1: DSD mute pattern is ignored.
[5]	ENABLE_WS_MONITOR	Enable WS monitor. • 1'b0: Disable • 1'b1: Enable (default)
[4]	ENABLE_BCK_MONITOR	Enable BCK monitor. • 1'b0: Disable • 1'b1: Enable (default)
[3]	DISABLE_PCM_DC	• 1'b0: PCM DC signal can trigger an automute if automute is enabled. • 1'b1: PCM DC is ignored.
[2:0]	RESERVED	N/A

Register 63: RESERVED

Register 64: TDM CH1 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_CH1_LINE_SEL	CH1 data line selection, only valid for TDM, PCM and DoP. CH1 receives data from: • 2'd0: DATA2 (default) • 2'd1: DATA3 • 2'd2: DATA4/GPIO4 • 2'd3: DATA5/GPIO5 Note: Must have GPIO4_SDB and GPIO5_SDB set to access DATA4 & DATA5
[4:0]	TDM_CH1_SLOT_SEL	CH1 data slot selection. CH1 receives data from the selected slot. Selected Slot = TDM_CH1_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 65: TDM CH2 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_CH2_LINE_SEL	CH2 data line selection, only valid for TDM, PCM and DoP. CH2 receives data from: • 2'd0: DATA2 (default) • 2'd1: DATA3 • 2'd2: DATA4/GPIO4 • 2'd3: DATA5/GPIO5 Note: Must have GPIO4_SDB and GPIO5_SDB set to access DATA4 & DATA5
[4:0]	TDM_CH2_SLOT_SEL	CH2 data slot selection. CH2 receives data from the selected slot. Selected Slot = TDM_CH2_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 66: TDM CH3 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd1	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_CH3_LINE_SEL	CH3 data line selection, only valid for TDM, PCM and DoP. CH3 receives data from: • 2'd0: DATA2 • 2'd1: DATA3 (default) • 2'd2: DATA4/GPIO4 • 2'd3: DATA5/GPIO5 Note: Must have GPIO4_SDB and GPIO5_SDB set to access DATA4 & DATA5
[4:0]	TDM_CH3_SLOT_SEL	CH3 data slot selection. CH3 receives data from the selected slot. Selected Slot = TDM_CH3_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 67: TDM CH4 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd1	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_CH4_LINE_SEL	CH4 data line selection, only valid for TDM, PCM and DoP. CH4 receives data from: • 2'd0: DATA2 • 2'd1: DATA3 (default) • 2'd2: DATA4/GPIO4 • 2'd3: DATA5/GPIO5 Note: Must have GPIO4_SDB and GPIO5_SDB set to access DATA4 & DATA5
[4:0]	TDM_CH4_SLOT_SEL	CH4 data slot selection. CH4 receives data from the selected slot. Selected Slot = TDM_CH4_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 68: TDM CH5 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd2	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_CH5_LINE_SEL	CH5 data line selection, only valid for TDM, PCM and DoP. CH5 receives data from: • 2'd0: DATA2 • 2'd1: DATA3 • 2'd2: DATA4/GPIO4 (default) • 2'd3: DATA5/GPIO5 Note: Must have GPIO4_SDB and GPIO5_SDB set to access DATA4 & DATA5
[4:0]	TDM_CH5_SLOT_SEL	CH5 data slot selection. CH5 receives data from the selected slot. Selected Slot = TDM_CH5_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 69: TDM CH6 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd2	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_CH6_LINE_SEL	CH6 data line selection, only valid for TDM, PCM and DoP. CH6 receives data from: • 2'd0: DATA2 • 2'd1: DATA3 • 2'd2: DATA4/GPIO4 (default) • 2'd3: DATA5/GPIO5 Note: Must have GPIO4_SDB and GPIO5_SDB set to access DATA4 & DATA5
[4:0]	TDM_CH6_SLOT_SEL	CH6 data slot selection. CH6 receives data from the selected slot. Selected Slot = TDM_CH6_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 70: TDM CH7 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd3	5'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_CH7_LINE_SEL	CH7 data line selection, only valid for TDM, PCM and DoP. CH7 receives data from: • 2'd0: DATA2 • 2'd1: DATA3 • 2'd2: DATA4/GPIO4 • 2'd3: DATA5/GPIO5 (default) Note: Must have GPIO4_SDB and GPIO5_SDB set to access DATA4 & DATA5
[4:0]	TDM_CH7_SLOT_SEL	CH7 data slot selection. CH7 receives data from the selected slot. Selected Slot = TDM_CH7_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 71: TDM CH8 CONFIG

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd3	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:5]	TDM_CH8_LINE_SEL	CH8 data line selection, only valid for TDM, PCM and DoP. CH8 receives data from: • 2'd0: DATA2 • 2'd1: DATA3 • 2'd2: DATA4/GPIO4 • 2'd3: DATA5/GPIO5 (default) Note: Must have GPIO4_SDB and GPIO5_SDB set to access DATA4 & DATA5
[4:0]	TDM_CH8_SLOT_SEL	CH8 data slot selection. CH8 receives data from the selected slot. Selected Slot = TDM_CH8_SLOT_SEL + 1. Note: Valid for TDM, PCM and DoP.

Register 73-72: RESERVED

Register 74: VOLUME CH1

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_CH1	DAC ch1 volume. -0dB to -127.5dB, 0.5dB steps • 8'h00: -0dB • 8'hFF: -127.5dB

Register 75: VOLUME CH2

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_CH2	DAC ch2 volume. -0dB to -127.5dB, 0.5dB steps • 8'h00: -0dB • 8'hFF: -127.5dB

Register 76: VOLUME CH3

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_CH3	DAC ch3 volume. -0dB to -127.5dB, 0.5dB steps • 8'h00: -0dB • 8'hFF: -127.5dB

Register 77: VOLUME CH4

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_CH4	DAC ch4 volume. -0dB to -127.5dB, 0.5dB steps • 8'h00: -0dB • 8'hFF: -127.5dB

Register 78: VOLUME CH5

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_CH5	DAC ch5 volume. -0dB to -127.5dB, 0.5dB steps • 8'h00: -0dB • 8'hFF: -127.5dB

Register 79: VOLUME CH6

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_CH6	DAC ch6 volume. -0dB to -127.5dB, 0.5dB steps • 8'h00: -0dB • 8'hFF: -127.5dB

Register 80: VOLUME CH7

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_CH7	DAC ch7 volume. -0dB to -127.5dB, 0.5dB steps • 8'h00: -0dB • 8'hFF: -127.5dB

Register 81: VOLUME CH8

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	VOLUME_CH8	DAC ch8 volume. -0dB to -127.5dB, 0.5dB steps • 8'h00: -0dB • 8'hFF: -127.5dB

Register 82: DAC VOL UP RATE

Bits	[7:0]
Default	8'h04

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_UP	Value by which the old VOLUME value is incremented to reach the new VOLUME value. $ramp\_rate[s] = 2^{15}/(DAC\_VOL\_RATE\_UP \cdot FS)$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h04: Default value • 8'hFF: Fastest change

Register 83: DAC VOL DOWN RATE

Bits	[7:0]
Default	8'h04

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_DOWN	Value by which the old VOLUME value is incremented to reach the new VOLUME value. $ramp\_rate[s] = 2^{15}/(DAC\_VOL\_RATE\_DOWN \cdot FS)$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h04: Default value • 8'hFF: Fastest change

Register 84: DAC VOL DOWN RATE FAST

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	DAC_VOL_RATE_FAST	Value by which the old VOLUME value is incremented to reach the new VOLUME value. Only used during abnormal mute (PLL unlock or BCK_WS ratio failed) $ramp\_rate[s] = 2^{15}/(DAC\_VOL\_RATE\_FAST \cdot FS)$ • 8'h00: Instant change • 8'h01: Slowest change • 8'hFF: Fastest change (default)

Register 85: RESERVED

Register 86: DAC MUTE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DAC_MUTE_CH8	• 1'b0: Normal operation (default) • 1'b1: Mute ch8
[6]	DAC_MUTE_CH7	• 1'b0: Normal operation (default) • 1'b1: Mute ch7
[5]	DAC_MUTE_CH6	• 1'b0: Normal operation (default) • 1'b1: Mute ch6
[4]	DAC_MUTE_CH5	• 1'b0: Normal operation (default) • 1'b1: Mute ch5
[3]	DAC_MUTE_CH4	• 1'b0: Normal operation (default) • 1'b1: Mute ch4
[2]	DAC_MUTE_CH3	• 1'b0: Normal operation (default) • 1'b1: Mute ch3
[1]	DAC_MUTE_CH2	• 1'b0: Normal operation (default) • 1'b1: Mute ch2
[0]	DAC_MUTE_CH1	• 1'b0: Normal operation (default) • 1'b1: Mute ch1

Register 87: DAC INVERT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DAC_INVERT_CH8	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch8, OUT/OUTB are phase inverted
[6]	DAC_INVERT_CH7	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch7, OUT/OUTB are phase inverted
[5]	DAC_INVERT_CH6	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch6, OUT/OUTB are phase inverted
[4]	DAC_INVERT_CH5	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch5, OUT/OUTB are phase inverted
[3]	DAC_INVERT_CH4	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch4, OUT/OUTB are phase inverted
[2]	DAC_INVERT_CH3	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch3, OUT/OUTB are phase inverted
[1]	DAC_INVERT_CH2	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch2, OUT/OUTB are phase inverted
[0]	DAC_INVERT_CH1	• 1'b0: Normal operation (default) • 1'b1: Invert the output on Ch1, OUT/OUTB are phase inverted

Register 88: FILTER SHAPE

Bits	[7:3]	[2:0]
Default	5'b10111	3'd0

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2:0]	FILTER_SHAPE	Selects the 8x interpolation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase fast roll-off apodizing • 3'd2: Linear phase fast roll-off • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion

Register 89: IIR BANDWIDTH & S/PDIF SELECT

Bits	[7:4]	[3]	[2:0]
Default	4'd0	1'b0	3'd4

Bits	Mnemonic	Description
[7:4]	SPDIF_SEL	Selects the S/PDIF data input pin. • 4'd0: Disconnected (default) • 4'd1: GPIO1 • 4'd2: GPIO2 • 4'd3: GPIO3 • 4'd4: DATA1 • 4'd5: DATA2 • 4'd6: DATA3 • 4'd7: DATA4/GPIO4 • 4'd8: DATA5/GPIO5 • 4'd9: DATA6/GPIO6 • 4'd10: DATA7/GPIO7 • 4'd11: DATA8/GPIO8 • Others: Reserved Note: GPIOx pins also require the GPIO input to be enabled
[3]	VOLUME_HOLD	Hold volume coefficients to allow for all channels to update at same time.
[2:0]	IIR_BW	Controls the IIR bandwidth in the digital datapath. • 3'd0: Reserved • 3'd1: BW * 8 • 3'd2: BW * 4 • 3'd3: BW * 2 • 3'd4: BW (default) • 3'd5: BW / 2 • 3'd6: BW / 4 • 3'd7: BW / 8

Register 90: DAC PATH CONFIG

Bits	[7:3]	[2]	[1]	[0]
Default	5'b00000	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2]	BYPASS_IIR	• 1'b0: Non-bypass IIR (default) • 1'b1: Bypass IIR
[1]	BYPASS_FIR4X	• 1'b0: Non-bypass IFir_4x (default) • 1'b1: Bypass IFir_4x
[0]	BYPASS_FIR2X	• 1'b0: Non-bypass IFir_2x (default) • 1'b1: Bypass IFir_2x

Register 98-91: THD C2 L

Bits	[63:48]	[47:32]	[31:16]	[15:0]
Default	16'd0	16'd0	16'd0	16'd0

Bits	Mnemonic	Description
[63:48]	THD_C2_CH4	A 16-bit signed coefficient for correcting for the CH4 second harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[47:32]	THD_C2_CH3	A 16-bit signed coefficient for correcting for the CH3 second harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[31:16]	THD_C2_CH2	A 16-bit signed coefficient for correcting for the CH2 second harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[15:0]	THD_C2_CH1	A 16-bit signed coefficient for correcting for the CH1 second harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 106-99: THD C2 H

Bits	[63:48]	[47:32]	[31:16]	[15:0]
Default	16'd0	16'd0	16'd0	16'd0

Bits	Mnemonic	Description
[63:48]	THD_C2_CH8	A 16-bit signed coefficient for correcting for the CH8 second harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[47:32]	THD_C2_CH7	A 16-bit signed coefficient for correcting for the CH7 second harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[31:16]	THD_C2_CH6	A 16-bit signed coefficient for correcting for the CH6 second harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[15:0]	THD_C2_CH5	A 16-bit signed coefficient for correcting for the CH5 second harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 114-107: THD C3 L

Bits	[63:48]	[47:32]	[31:16]	[15:0]
Default	16'd0	16'd0	16'd0	16'd0

Bits	Mnemonic	Description
[63:48]	THD_C3_CH4	A 16-bit signed coefficient for correcting for the CH4 third harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[47:32]	THD_C3_CH3	A 16-bit signed coefficient for correcting for the CH3 third harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[31:16]	THD_C3_CH2	A 16-bit signed coefficient for correcting for the CH2 third harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[15:0]	THD_C3_CH1	A 16-bit signed coefficient for correcting for the CH1 third harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 122-115: THD C3 H

Bits	[63:48]	[47:32]	[31:16]	[15:0]
Default	16'd0	16'd0	16'd0	16'd0

Bits	Mnemonic	Description
[63:48]	THD_C3_CH8	A 16-bit signed coefficient for correcting for the CH8 third harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[47:32]	THD_C3_CH7	A 16-bit signed coefficient for correcting for the CH7 third harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[31:16]	THD_C3_CH6	A 16-bit signed coefficient for correcting for the CH6 third harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$
[15:0]	THD_C3_CH5	A 16-bit signed coefficient for correcting for the CH5 third harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$

Register 123: AUTOMUTE ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	AUTOMUTE_EN_CH8	• 1'b0: Disables ch8 automute • 1'b1: Enables ch8 automute (default) Note: Automute is available for PCM only
[6]	AUTOMUTE_EN_CH7	• 1'b0: Disables ch7 automute • 1'b1: Enables ch7 automute (default) Note: Automute is available for PCM only
[5]	AUTOMUTE_EN_CH6	• 1'b0: Disables ch6 automute • 1'b1: Enables ch6 automute (default) Note: Automute is available for PCM only
[4]	AUTOMUTE_EN_CH5	• 1'b0: Disables ch5 automute • 1'b1: Enables ch5 automute (default) Note: Automute is available for PCM only
[3]	AUTOMUTE_EN_CH4	• 1'b0: Disables ch4 automute • 1'b1: Enables ch4 automute (default) Note: Automute is available for PCM only
[2]	AUTOMUTE_EN_CH3	• 1'b0: Disables ch3 automute • 1'b1: Enables ch3 automute (default) Note: Automute is available for PCM only
[1]	AUTOMUTE_EN_CH2	• 1'b0: Disables ch2 automute • 1'b1: Enables ch2 automute (default) Note: Automute is available for PCM only
[0]	AUTOMUTE_EN_CH1	• 1'b0: Disables ch1 automute • 1'b1: Enables ch1 automute (default) Note: Automute is available for PCM only

Register 125-124: AUTOMUTE TIME

Bits	[15:12]	[11]	[10:0]
Default	4'd0	1'b1	11'd15

Bits	Mnemonic	Description
[15:12]	RESERVED	N/A
[11]	AUTOMUTE_RAMP_TO_GROUND	• 1'b0: When ramped to min volume during normal mute, do not soft ramp to ground • 1'b1: When ramped to min volume during normal mute, soft ramp to ground for power saving (default) Note: Normal mute includes: automute, mute by register, mute by GPIO
[10:0]	AUTOMUTE_TIME	Configures the time the audio must remain below AUTOMUTE_LEVEL to trigger an automute condition. • 11'h000: Disabled • 11'h001: Slowest • 11'h00F: Default • 11'h7FF: Fastest $Time[s] = 2^{18}/(AUTOMUTE\_TIME \cdot FS)$

Register 127-126: AUTOMUTE LEVEL

Bits	[15:0]
Default	16'h0008

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_LEVEL	Configures the threshold which the audio must be below before an automute condition is flagged. • 16'h0001: -138dB • 16'h0008: -120dB (default) • 16'hFFFF: -42dB $\text{level [dB]} = 20\log10\left(\frac{\text{AUTOMUTE\_LEVEL}}{(2^{16}-1)\cdot 2^{7}}\right)$ Note: Works in tandem with AUTOMUTE_TIME to create the automute condition

Register 129-128: AUTOMUTE OFF LEVEL

Bits	[15:0]
Default	16'h000A

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_OFF_LEVEL	The threshold which the audio must be above before the automute condition is immediately cleared. • 16'h0001: -138dB • 16'h000A: -118dB (default) • 16'hFFFF: -42dB $\text{level [dB]} = 20\log10\left(\frac{\text{AUTOMUTE\_OFF\_LEVEL}}{(2^{16}-1)\cdot 2^{7}}\right)$

Register 130: SOFT RAMP CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd3

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	SOFT_RAMP_TIME	Sets the amount of time that it takes to perform a soft start ramp. This time affects both ramp to ground and ramp to AVCC/2. Valid from 0 to 20 (inclusive). $\text{Time [s]} = 4096 \cdot \frac{2^{\text{SOFT\_RAMP\_TIME}+1}}{\text{CLK\_IDAC [Hz]}}$

Register 134-131: RESERVED

Register 135: PROGRAM RAM CONTROL

Bits	[7:2]	[1]	[0]
Default	6'b000000	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	PROG_COEFF_WE	Enables writing to the programmable coefficient RAM. • 1'b0: Disables write signal to the coefficient RAM (default). • 1'b1: Enables write signal to the coefficient RAM.
[0]	PROG_COEFF_EN	Enables the custom oversampling filter coefficients. • 1'b0: Uses a built-in filter selected by filter_shape (default). • 1'b1: Uses the coefficients programmed via prog_coeff_data.

Register 136: S/PDIF READ CONTROL

Bits	[7:5]	[4:0]
Default	3'b000	5'd0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	SPDIF_DATA_SEL	Selects the byte of the S/PDIF payload in Register 251 SPDIF_PAYLOAD_READ

Register 137: PROGRAM RAM ADDRESS

Bits	[7]	[6:0]
Default	1'b0	7'd0

Bits	Mnemonic	Description
[7]	PROG_COEFF_STAGE	Selects which stage of the filter to write. • 1'b0: Selects the 2x stage of the oversampling filter (default). • 1'b1: Selects the 4x stage of the oversampling filter.
[6:0]	PROG_COEFF_ADDR	Selects the coefficient address when writing custom coefficients for the oversampling filter.

Register 140-138: PROGRAM RAM DATA

Bits	[23:0]
Default	24'd0

Bits	Mnemonic	Description
[23:0]	PROG_COEFF_IN	A 24bit signed filter coefficient that will be written to the address defined in prog_coeff_addr.

Register 141: MQA CONFIG

Bits	[7:3]	[2:1]	[0]
Default	5'b10000	2'b00	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2:1]	MQB_READER_ENABLE	Enable the MQB stream reader • 2'b00: The MQB stream reader is disabled. (default) • 2'b01: The MQB stream reader is enabled (Normal Operation, 24-bit) • 2'b10: The MQB stream reader is enabled (16-bit) • 2'b11: Reserved Note: ES9039MPRO has a MQA renderer built in, MQA stream must be decoded by MQA core decoder first.
[0]	MQA_RENDERING_ENABLE	This allows the Sabre ES9039MPRO to render decoded MQA streams. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 145-142: RESERVED

Readback Registers

Register 224: SYS READ

Bits	[7:4]	[3:2]	[1]	[0]
Default		-	-	-

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3:2]	MODES	Chip mode readback. Based off MODE Pin • 2'b00: I2C • 2'b11: SPI Note: All other values are invalid
[1]	ADDR1	I2C address select bit 1 readback.
[0]	ADDR0	I2C address select bit 0 readback.

Register 225: CHIP ID READ

Bits	[7:0]
Default	8'h52

Bits	Mnemonic	Description
[7:0]	CHIP_ID	• ES9039SPRO: 0x50 • ES9039SMPRO: 0x52

Register 228-226: RESERVED

Register 233-229: INTERRUPT STATE

Bits	[39:32]	[31:30]	[29]	[28:26]	[25]	[24]	[23:16]	[15:8]	[7:0]
Default		-	-		-	-	-	-	-

Bits	Mnemonic	Description
[39:32]	RESERVED	N/A
[31:30]	INPUT_SELECT_OVERRIDE_STATE	State of the INPUT_SELECT_OVERRIDE interrupt. Note: Interrupt clear bits are required to reset value.
[29]	TDM_DATA_VALID_STATE	State of the TDM_DATA_VALID interrupt. Note: Interrupt clear bit is required to reset value.
[28:26]	RESERVED	N/A
[25]	BCK_WS_FAIL_STATE	State of the BCK_WS_FAIL interrupt. Note: Interrupt clear bit is required to reset value.
[24]	DOP_VALID_STATE	State of the DOP_VALID interrupt. Note: Interrupt clear bit is required to reset value.
[23:16]	SS_FULL_RAMP_STATE	State of each channel's SS_FULL_RAMP interrupt. Note: Interrupt clear bit is required to reset value.
[15:8]	AUTOMUTE_STATE	State of each channel's AUTOMUTE_STATE interrupt. Note: Interrupt clear bit is required to reset value.
[7:0]	VOL_MIN_STATE	State of each channel's VOL_MIN_STATE interrupt. Note: Interrupt clear bit is required to reset value.

Register 238-234: INTERRUPT SOURCE

Bits	[39:32]	[31:30]	[29]	[28:26]	[25]	[24]	[23:16]	[15:8]	[7:0]
Default		-	-		-	-	-	-	-

Bits	Mnemonic	Description
[39:32]	RESERVED	N/A
[31:30]	INPUT_SELECT_OVERRIDE_SOURCE	Output of the AUTO_INPUT_SELECT logic.
[29]	TDM_DATA_VALID_SOURCE	TDM data valid flag.
[28:26]	RESERVED	N/A
[25]	BCK_WS_FAIL_SOURCE	Validity of BCK, WS, and ASYNC_LOCK flag. Requires respective monitor bits to be set.
[24]	DOP_VALID_SOURCE	Valid DoP flag for Channels 1 and 2.
[23:16]	SS_FULL_RAMP_SOURCE	Channel flag for whether it is fully ramped up or down.
[15:8]	AUTOMUTE_SOURCE	Channel flag for whether it is automute is active.
[7:0]	VOL_MIN_SOURCE	Channel flag for whether the corresponding volume register = 0x00

Register 239: RATIO VALID READ

Bits	[7]	[6:0]
Default	-	

Bits	Mnemonic	Description
[7]	RATIO_VALID	Indicates validity of the CLK_DAC/CLK_IDAC ratio • 1'b0: Invalid • 1'b1: Valid
[6:0]	RESERVED	N/A

Register 240: GPIO READBACK

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	GPIO8_I_READ	GPIO8 Readback
[6]	GPIO7_I_READ	GPIO7 Readback
[5]	GPIO6_I_READ	GPIO6 Readback
[4]	GPIO5_I_READ	GPIO5 Readback
[3]	GPIO4_I_READ	GPIO4 Readback
[2]	GPIO3_I_READ	GPIO3 Readback
[1]	GPIO2_I_READ	GPIO2 Readback
[0]	GPIO1_I_READ	GPIO1 Readback

Register 241: VOL MIN READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	VOL_MIN_CH8	Volume min flag ch8
[6]	VOL_MIN_CH7	Volume min flag ch7
[5]	VOL_MIN_CH6	Volume min flag ch6
[4]	VOL_MIN_CH5	Volume min flag ch5
[3]	VOL_MIN_CH4	Volume min flag ch4
[2]	VOL_MIN_CH3	Volume min flag ch3
[1]	VOL_MIN_CH2	Volume min flag ch2
[0]	VOL_MIN_CH1	Volume min flag ch1

Register 242: AUTOMUTE READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	AUTOMUTE_CH8	Automute status ch8
[6]	AUTOMUTE_CH7	Automute status ch7
[5]	AUTOMUTE_CH6	Automute status ch6
[4]	AUTOMUTE_CH5	Automute status ch5
[3]	AUTOMUTE_CH4	Automute status ch4
[2]	AUTOMUTE_CH3	Automute status ch3
[1]	AUTOMUTE_CH2	Automute status ch2
[0]	AUTOMUTE_CH1	Automute status ch1

Register 243: SOFT RAMP UP READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	SS_RAMP_UP_CH8	Soft ramped up flag ch8
[6]	SS_RAMP_UP_CH7	Soft ramped up flag ch7
[5]	SS_RAMP_UP_CH6	Soft ramped up flag ch6
[4]	SS_RAMP_UP_CH5	Soft ramped up flag ch5
[3]	SS_RAMP_UP_CH4	Soft ramped up flag ch4
[2]	SS_RAMP_UP_CH3	Soft ramped up flag ch3
[1]	SS_RAMP_UP_CH2	Soft ramped up flag ch2
[0]	SS_RAMP_UP_CH1	Soft ramped up flag ch1

Register 244: SOFT RAMP DOWN READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	SS_RAMP_DOWN_CH8	Soft ramped down flag ch8
[6]	SS_RAMP_DOWN_CH7	Soft ramped down flag ch7
[5]	SS_RAMP_DOWN_CH6	Soft ramped down flag ch6
[4]	SS_RAMP_DOWN_CH5	Soft ramped down flag ch5
[3]	SS_RAMP_DOWN_CH4	Soft ramped down flag ch4
[2]	SS_RAMP_DOWN_CH3	Soft ramped down flag ch3
[1]	SS_RAMP_DOWN_CH2	Soft ramped down flag ch2
[0]	SS_RAMP_DOWN_CH1	Soft ramped down flag ch1

Register 245: SPDIF, TDM, DOP, AND INPUT READBACK

Bits	[7]	[6]	[5:2]	[1:0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7]	SPDIF_VALID	SPDIF valid flag
[6]	TDM_DATA_VALID	TDM valid data flag
[5:2]	DOP_VALID	DoP valid flag
[1:0]	INPUT_SELECT_OVERRIDE	AUTO_INPUT_SEL value

Register 248-246: PROG COEFF OUT READ

Bits	[23:0]
Default	-

Bits	Mnemonic	Description
[23:0]	PROG_COEFF_OUT	Programmable FIR coefficient readback

Register 250-249: RESERVED

Register 251: S/PDIF DATA READ

Bits	[7:0]
Default	-

Bits	Mnemonic	Description
[7:0]	SPDIF_DATA_READ	Contains 1 byte of the SPDIF payload. Byte is controlled by Register 136[4:0] SPDIF_DATA_SEL

ES9039MPRO/ES9039PRO Reference Schematic

Hardware Mode

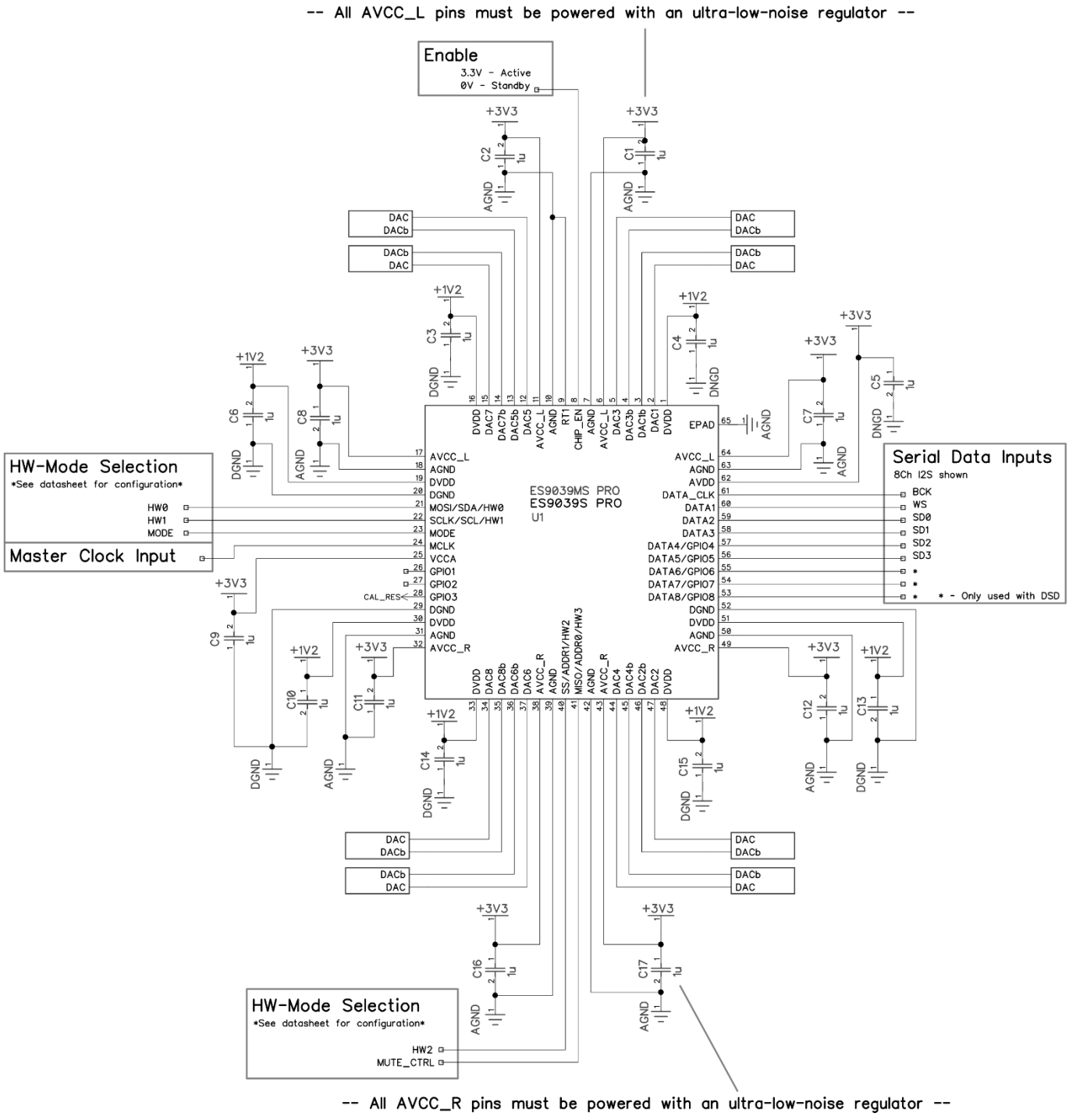


Figure 22 - ES9039MPRO Hardware Mode Reference Schematic

Note: The ES9039MSPRO & ES9039SPRO QFN package have an exposed pad (Pin 65) that should be connected to analog ground.

Software Mode

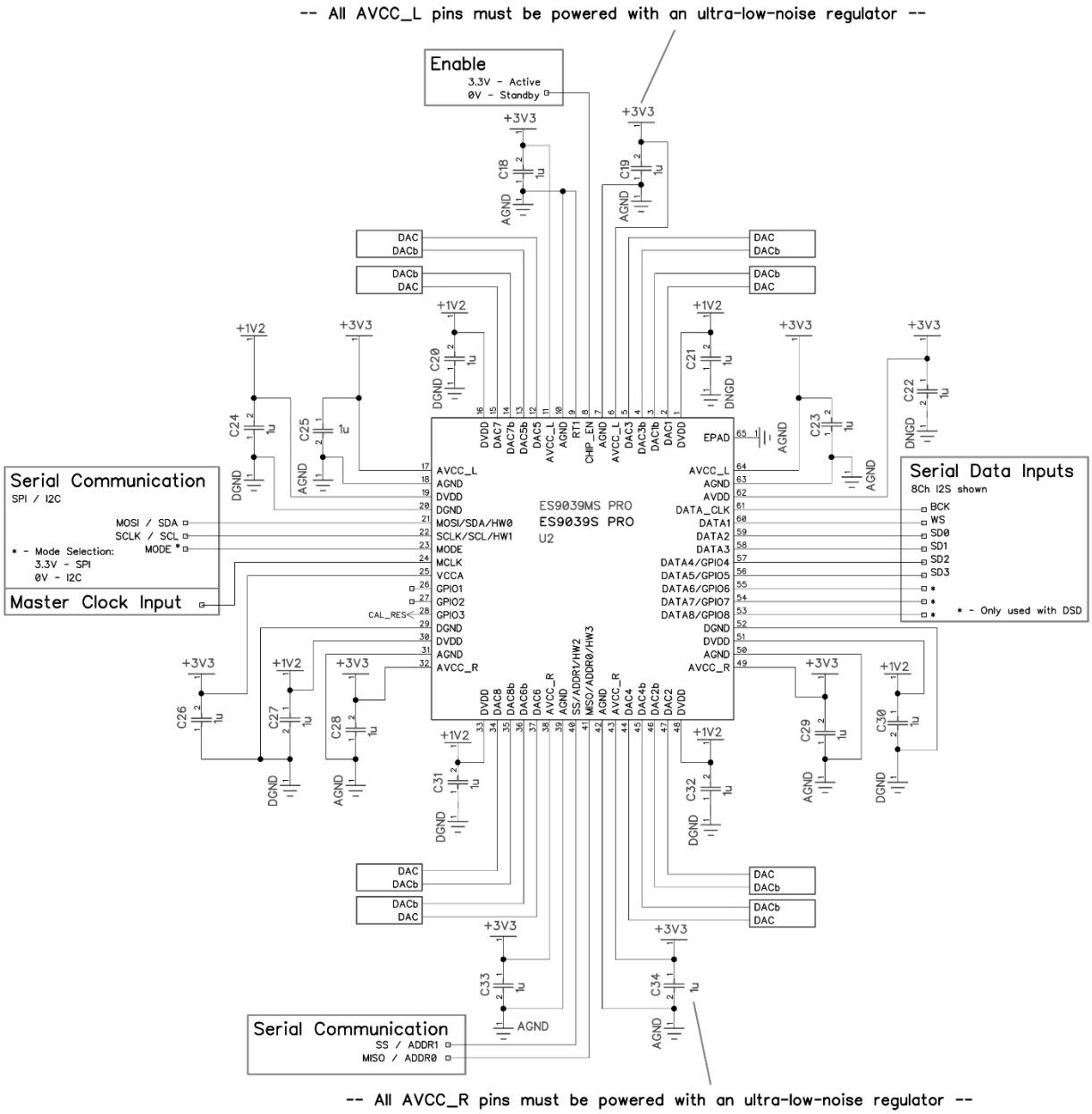


Figure 23 - ES9039MPRO Software Mode Reference Schematic

Note: The ES9039MSPRO & ES9039SPRO QFN package have an exposed pad (Pin 65) that should be connected to analog ground.

Recommended Output Stages

Dual Op-Amp Output Stage

This output stage uses two Op-Amps and is used on the ES9039PRO 1v3 Evaluation Board (EVB).

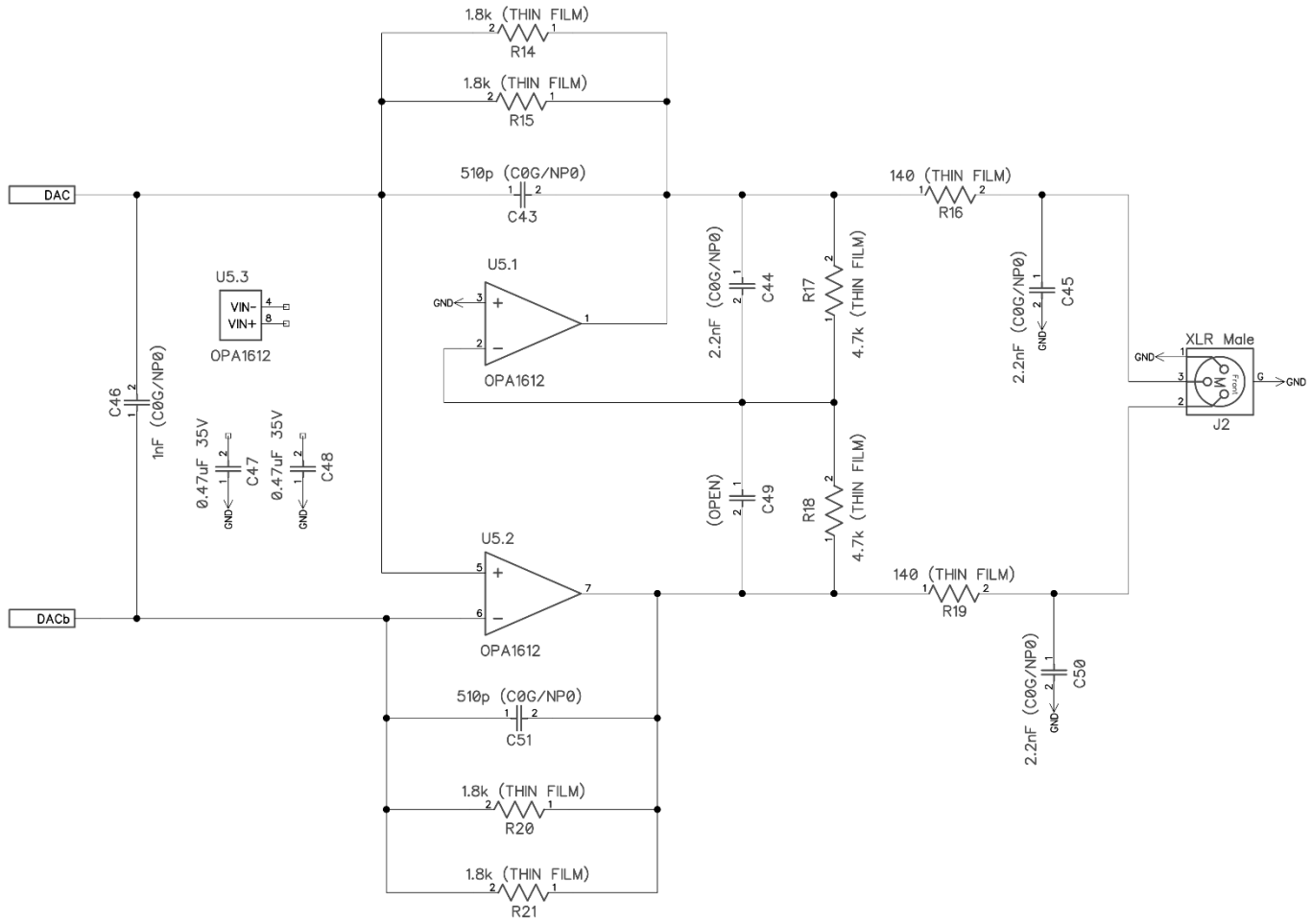


Figure 24 - ES9039MSPRO & ES9039SPRO Dual Op-Amp Output Stage Reference Schematic

Note: C46 (1nF) value can change depending on Op-Amps used.

Triple Op-Amp Output Stage

This output stage uses three Op-Amps and is used on the ES9039PRO 1v1 Evaluation Board (EVB).

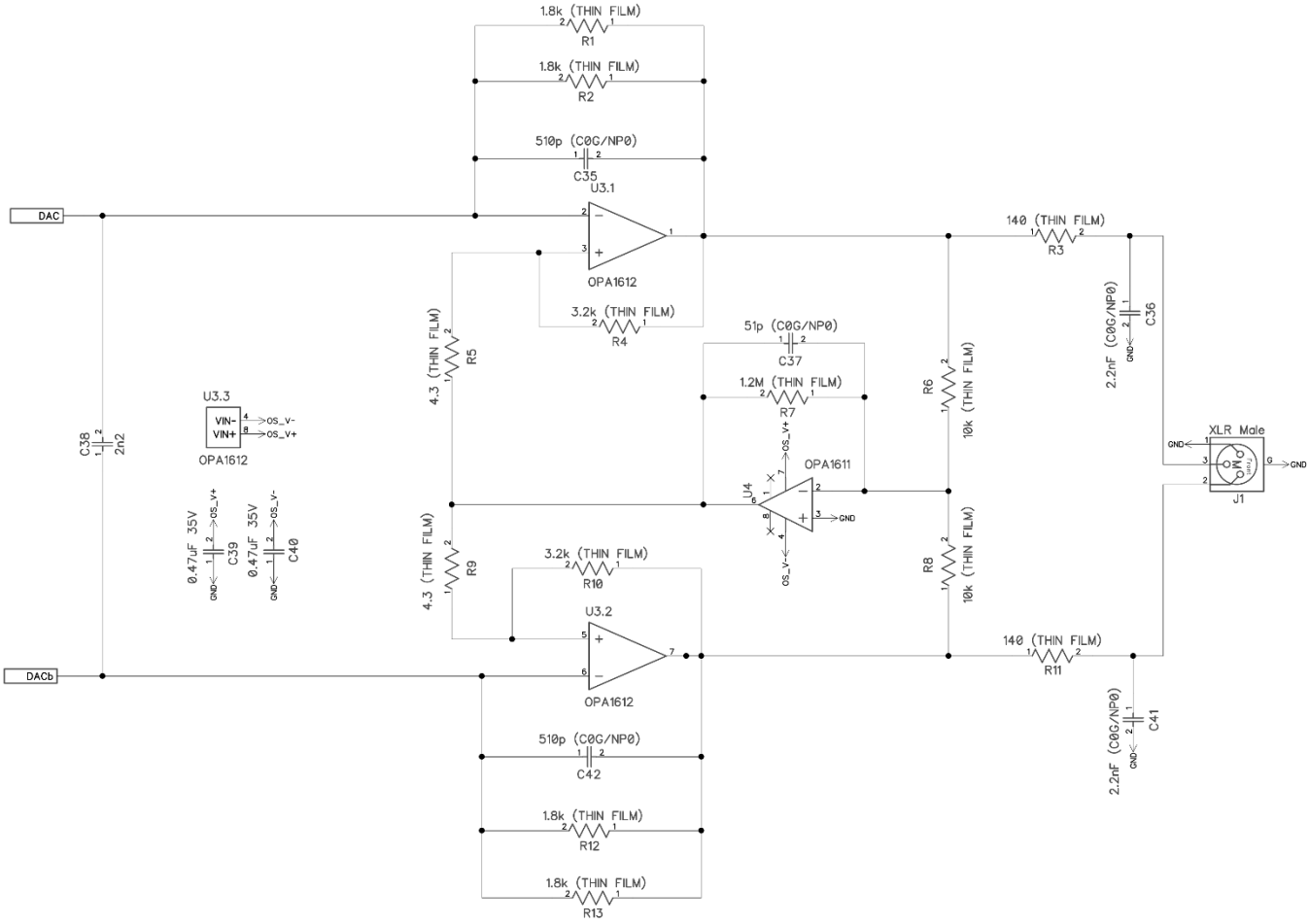


Figure 25 - ES9039MSPRO & ES9039SPRO Triple Op-Amp Output Stage Reference Schematic

Recommended Power Supply

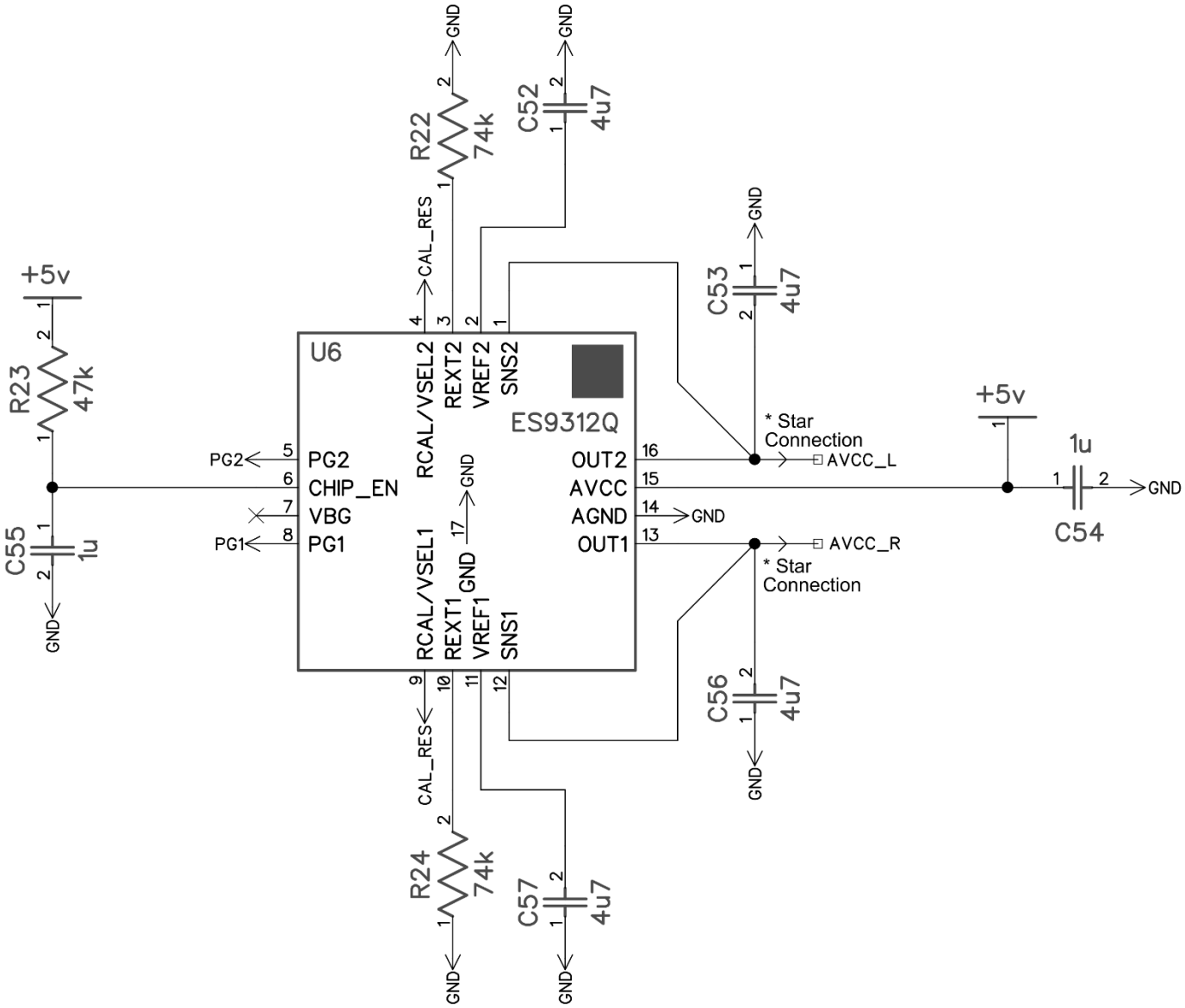


Figure 26 - ES9039MSPRO & ES9039SPRO Power Supply Schematic

Note: In all configurations V_{BG} must remain floating. SNSx and OUTx pins need to be star connected to 4.7uF capacitors which are located close to ES9312.

ES9039MSPRO & ES9039SPRO PCB Layout Guidelines

To maximize the performance of the ES9039MSPRO & ES9039SPRO, ESS Technology makes the following PCB Layout recommendations:

- Use of a 4+ layer PCB with an uninterrupted ground plane immediately beneath the chip. Both analog and digital ground signal can be connected here.
- All bypass capacitors to be placed as close to the chip as possible while keeping clear ground paths between them and the chip's ground pins.
- The use of multiple vias for each supply near its bypass capacitor and chip ground pin.
- Minimize the use of vias for high-speed data and clock lines and avoid routing them near or directly underneath the analog output signals.
- Ensure the package pad is connected to the ground plane on the back side of the PCB with multiple vias for heat dissipation.

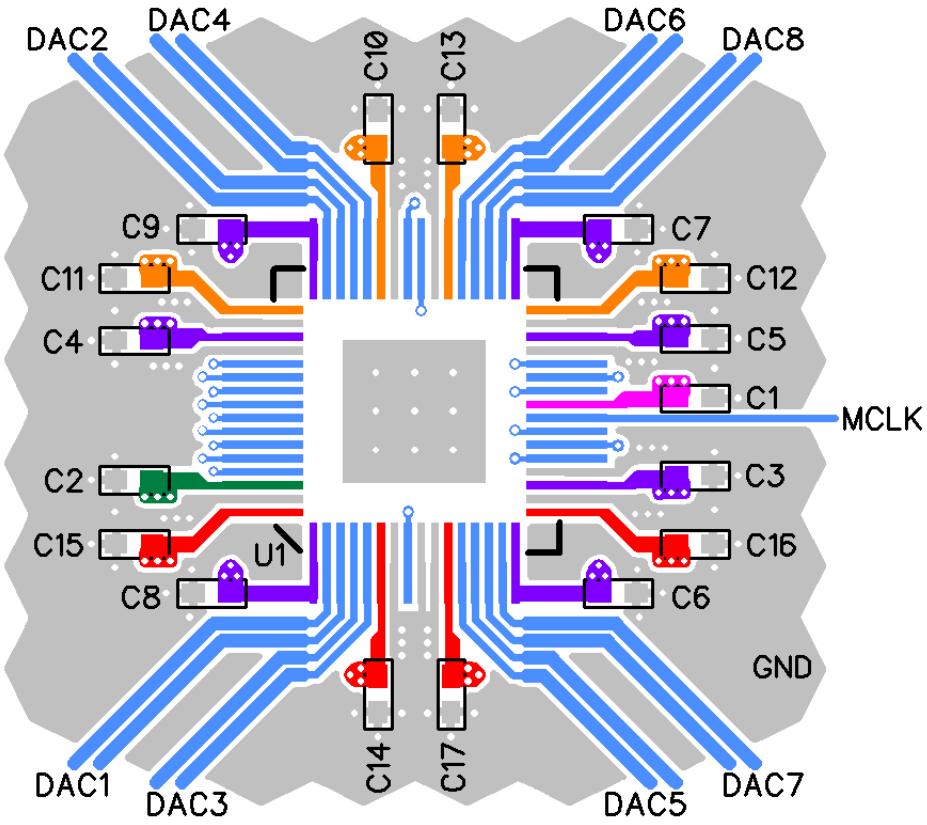
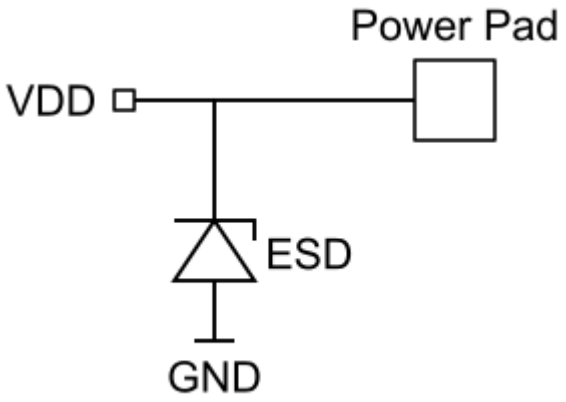
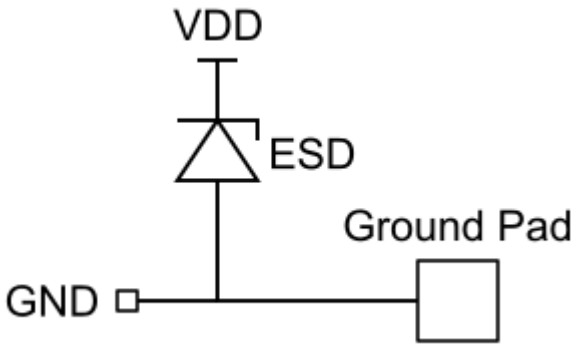
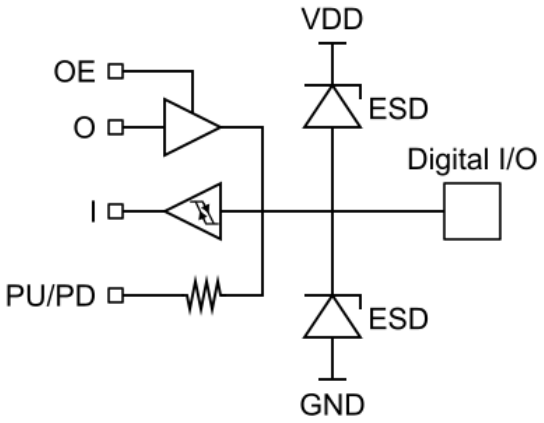
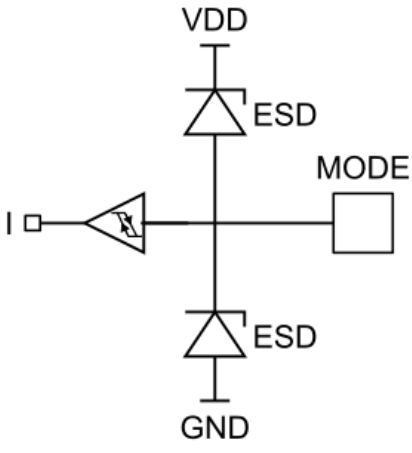
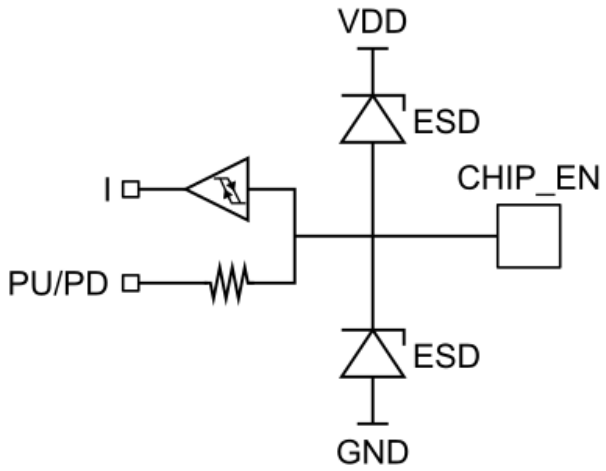
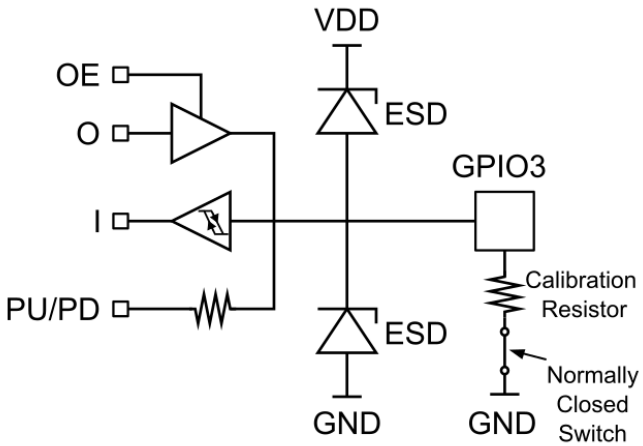
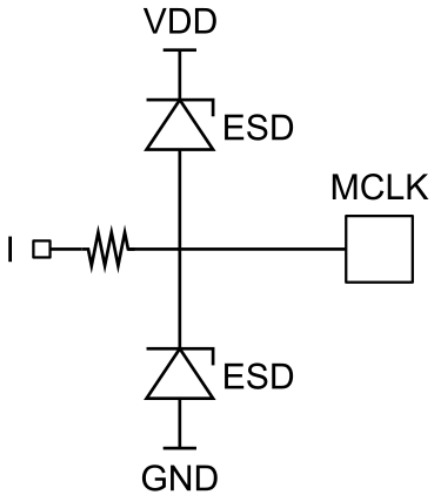


Figure 27 - ES9039MSPRO & ES9039SPRO Recommended PCB Layout Guidelines

Internal Pad Circuitry

Pin Name	Pin	Type	Equivalent Circuit
AVCC_L AVCC_L AVCC_L VCCA AVCC_R AVCC_R AVCC_R AVCC_R AVDD AVCC_L	6 11 17 25 32 38 43 49 62 64	Power	
AGND AGND AGND DGND DGND AGND AGND AGND AGND DGND AGND	7 10 18 20 29 31 39 42 50 52 63	Ground	

RT1 MOSI/SDA/HW0 SCLK/SCL/HW1 GPIO1 GPIO2 SS/ADDR1/HW2 MISO/ADDR0/MUTE_CTRL DATA8/GPIO8 DATA7/GPIO7 DATA6/GPIO6 DATA5/GPIO5 DATA4/GPIO4 DATA3 DATA2 DATA1 DATA_CLK	9 21 22 26 27 40 41 53 54 55 56 57 58 59 60 61	Digital I/O	
MODE	23	Digital I	

CHIP_EN	8	Digital I	
GPIO3	28	Digital I/O	
MCLK	24	Analog I	

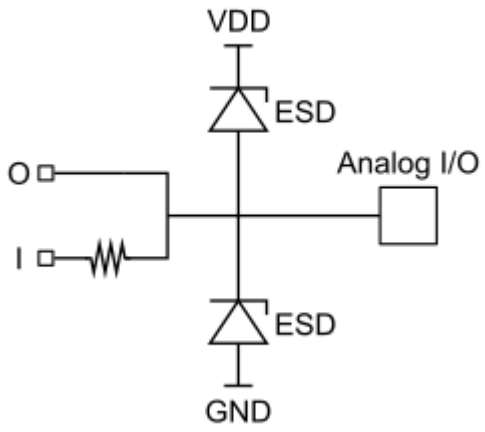
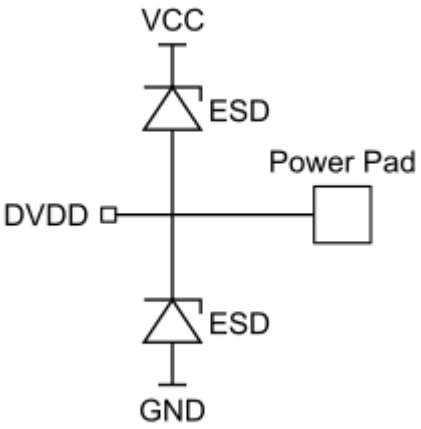
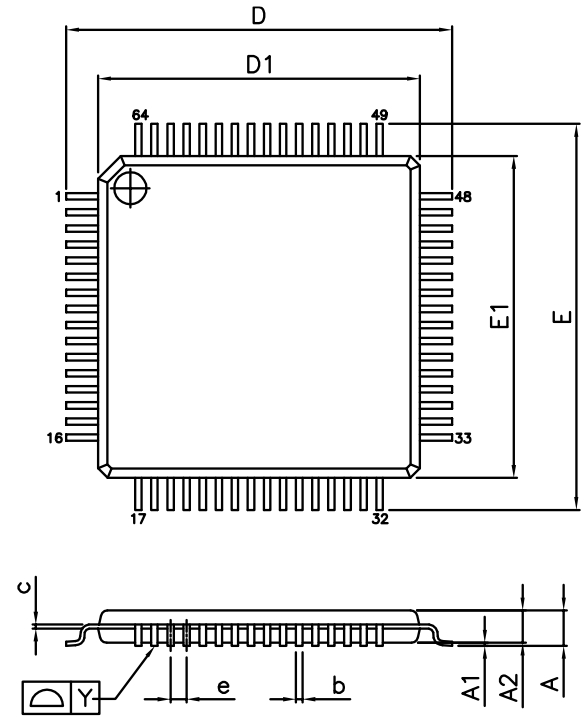
DAC1 DAC1B DAC3B DAC3 DAC5 DAC5B DAC7B DAC7 DAC8 DAC8B DAC6B DAC6 DAC4 DAC4B DAC2B DAC2	2 3 4 5 12 13 14 15 34 35 36 37 44 45 46 47	Analog IO DAC	
DVDD DVDD DVDD DVDD DVDD DVDD DVDD	1 16 19 30 33 48 51	IO Power	

Table 30 - Internal Pad Circuitry

64 eTQFP Package Dimensions

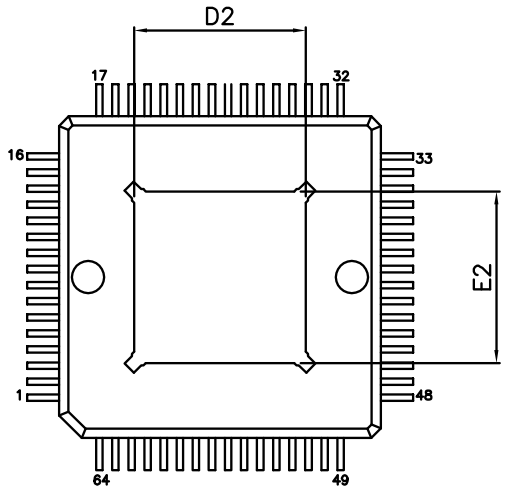


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
b	0.17	0.22	0.27
c	0.09	—	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
e	0.50 BSC		
θ	0°	3.5°	7°
Y	0.08		

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	D2		E2	
	MIN.	MAX.	MIN.	MAX.
210X 210 MIL	5.13	5.48	5.13	5.48



PAD SIZE : 210X210 MIL

(THERMALLY ENHANCED VARIATIONS ONLY)

NOTES:

1.JEDEC OUTLINE :
MS-026 ACD.
MS-026 ACD-HD (THERMALLY ENHANCED VARIATIONS ONLY).

2.DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H] .

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

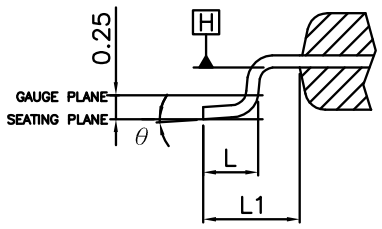


Figure 28 - ES9039MSPRO/ES9039SPRO 64 eTQFP Package Dimensions

64 eTQFP Top view Marking

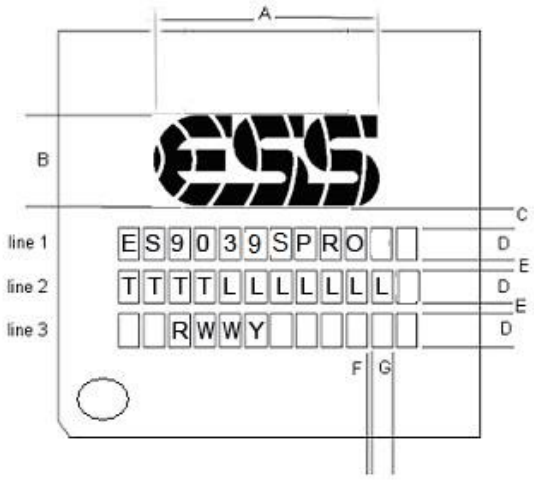


Figure 29 - ES9039SPRO Marking

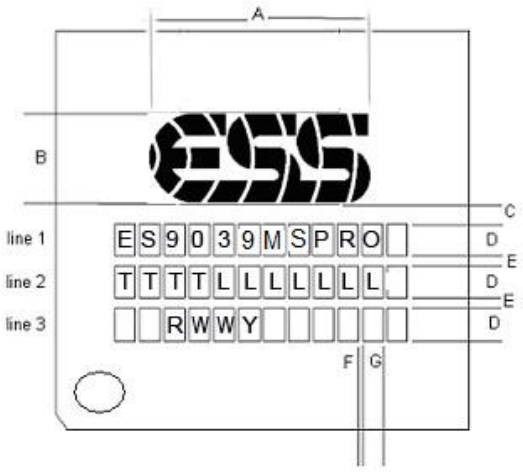


Figure 30 - ES9039MSPRO Marking

	Dimension in mm						
Package Type	A	B	C	D	E	F	G
64L eTQFP 10mm x 10mm	7.4	3.5	0.45	0.8	0.3	0.15	0.4

T	Tracking number
W	Work week
Y	Last digit of year
L	Lot number
R	Silicon Revision

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2-Pb-Free Process - Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

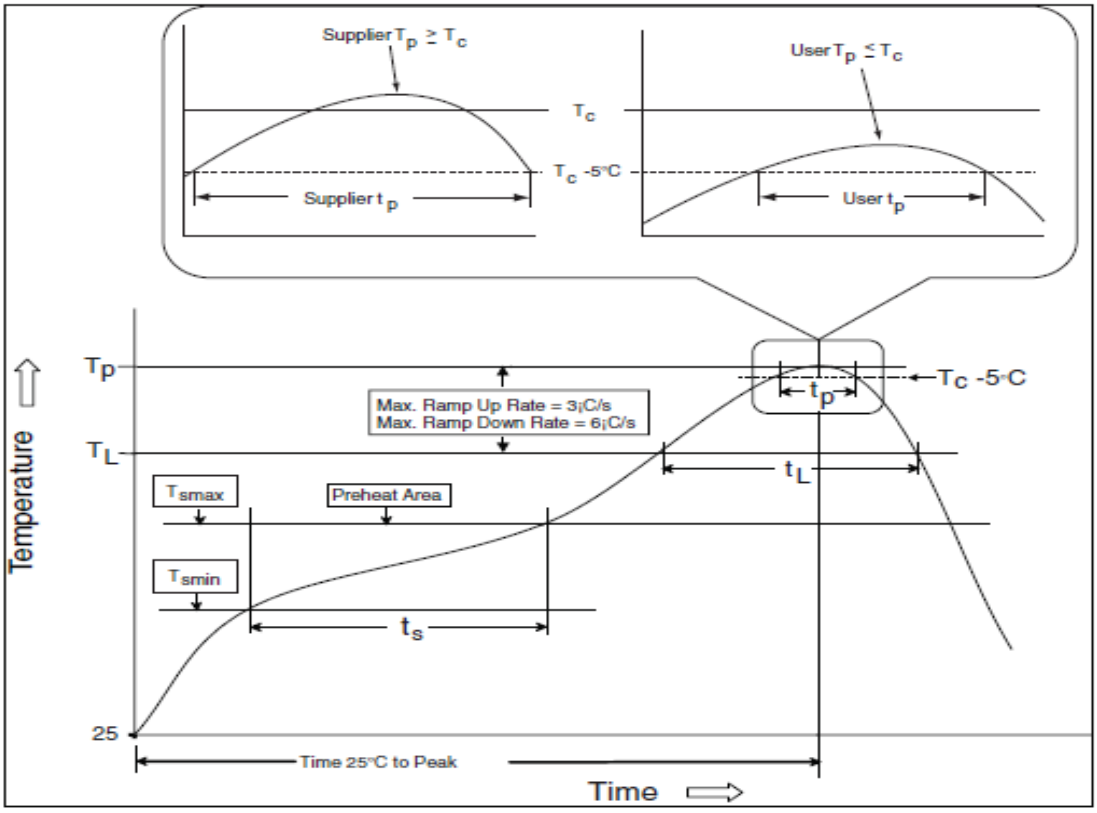


Figure 31 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time, bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350ºC no longer than 3 seconds.

RPC-1 Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc)	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 31 - RPC-1 Classification Reflow Profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 32 - RPC-2 Pb Free Classification Temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9039MSPRO	SABRE PRO™ 32-bit 8 Channel Flagship DAC and MQA renderer	10mm x 10mm 64 eTQFP
ES9039SPRO	SABRE PRO™ 32-bit 8 Channel Flagship DAC	

Table 33 - Ordering Information

Revision History

Current Version 0.4.0

Rev.	Date	Notes
0.1.3	June, 2022	Initial release
0.3.2	April, 2024	• See revision notes of version 0.3.2 for all changes • Unreserved Registers 34[6], 61[7], 136[4:0], 251 • Reserved Reg 61[4:0] • Added Bit-Clock (BCLK) and Word-Select (WS) Timing
0.4.0	August, 2025	• Fixed number reference in Digital Filter 1 • Renamed Register 1[7] to ENABLE_SYS_CLK • Updated Hardware Mode Pin Configurations #8, 11, 12, 15-27 • Updated Calibration Resistor • Updated Reference Schematic component numbering • Added Clock Distribution • Added Dual Op-amp Output Stage • Added PCB Layout Guidelines