ES9218P
32-bit Stereo Low Power DAC with Headphone Amplifier, Analog Volume Control, and Output Switch

The ***ES9218P*** is a high-performance 32-bit, 2-channel audio **SABRE HiFi®** D/A converter with QUAD DAC™ technology, headphone amplifier, analog volume control, and output switch designed for audiophile-grade portable power sensitive applications such as digital music players, consumer applications such as USB DACs and A/V receivers, as well as professional applications such as mixer consoles and digital audio workstations.

Using critically acclaimed QUAD DAC™ technology, patented 32-bit HyperStream® DAC architecture and Time Domain Jitter Eliminator, the ***ES9218P*** delivers up to 121dB DNR and –114dB THD+N in HiFi mode, a performance level that will satisfy the most demanding audio enthusiasts.

The ***ES9218P's*** integrated SABRE DAC supports up to 32-bit 384kHz PCM and DSD256 audio data via master/slave I²S/DSD interface in synchronous and asynchronous sampling modes. A user-programmable FIR filter with 8 presets is included for customizable sound signature. Additionally, the ***ES9218P's*** integrated SABRE Headphone Amp supports up to 2.0Vrms output with analog gain control to reduce output noise at real-life listening levels. An integrated output switch allows an auxiliary source such as voice to bypass the ***ES9218P*** for lowest power consumption in non-HiFi mode. Residual distortion from suboptimal PCB components and layout can be minimized using ***ES9218P's*** unique THD compensation circuit, while PCB footprint and bill-of-material are minimized via the ***ES9218P's*** integrated feedback resistors and low-noise DAC reference LDO.

The ***ES9218P*** sets the standard for HD audio performance enabling **SABRE HiFi®** experience all the way from the DAC to headphones for today's most demanding digital-audio applications in an easy-to-use 41-CSP package or 40 pin QFN package.

FEATURE	DESCRIPTION
Patented 32-bit HyperStream® II DAC/HPA QUAD DAC™ technology +130dB SNR, +121dB DNR -114 dB THD+N, 1.0Vrms into 100kΩ -112 dB THD+N, 2.0Vrms into 300Ω -106 dB THD+N, 300mVrms into 32Ω	Industry's highest performance 32-bit mobile audio DAC/HPA with unprecedented dynamic range & ultra-low distortion Support synchronous and asynchronous sampling modes Enable SABRE HiFi® experience all the way to headphones
Patented Time Domain Jitter Eliminator	Unmatched audio clarity free from input clock jitter
64-bit accumulator & 32-bit processing	Distortion free signal processing
Versatile digital input	Support master/slave PCM (I2S, LJ 16-32-bit), DSD or DoP
Customizable filter characteristics	8 preset filters User-programmable filter for custom sound signature
Output Switch for Auxiliary Source	Voice mode bypass with ultra-low power consumption
Integrated Low Noise AVCC LDO	Eliminate external LDO and reduce PCB size
Adjustable Analog Gain with Integrated HPA Feedback Resistors	Reduce noise at real-life listening levels Eliminate external thin film resistors and reduce PCB size
THD Compensation	Minimize DAC non-linearity
41-CSP Package and 40 pin QFN Package	Minimize PCB footprint
< 80mW quiescent power < 1mW standby power	Maximize battery life

APPLICATIONS

- Mobile phones / Tablets / Digital music players / Portable multimedia players
- Consumer and Audiophile USB DAC headphone amplifiers and A/V receivers
- Professional digital audio workstations and mixer consoles

Table of Contents

Functional Block Diagram

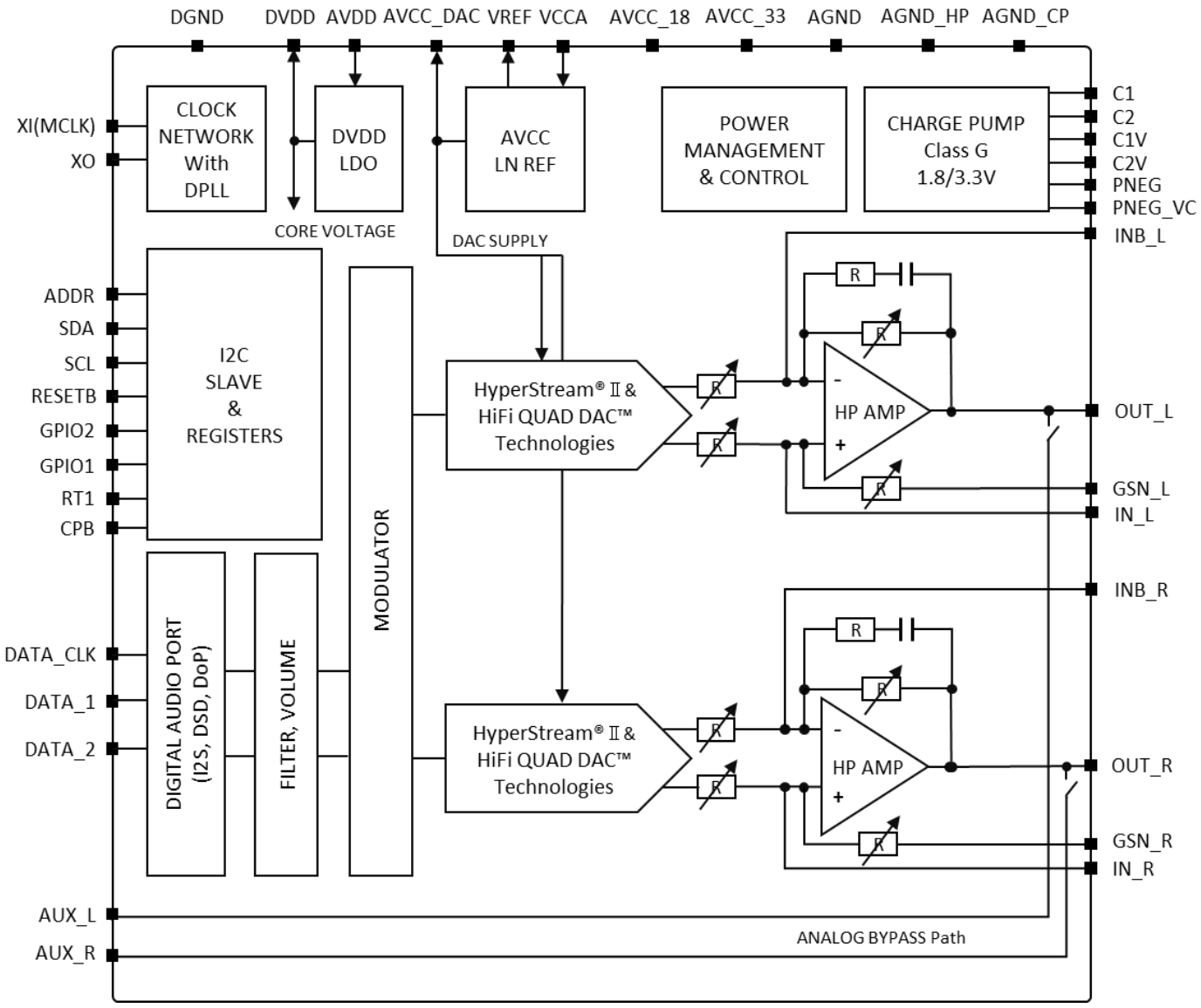


Figure 1. Block Diagram

Typical Application

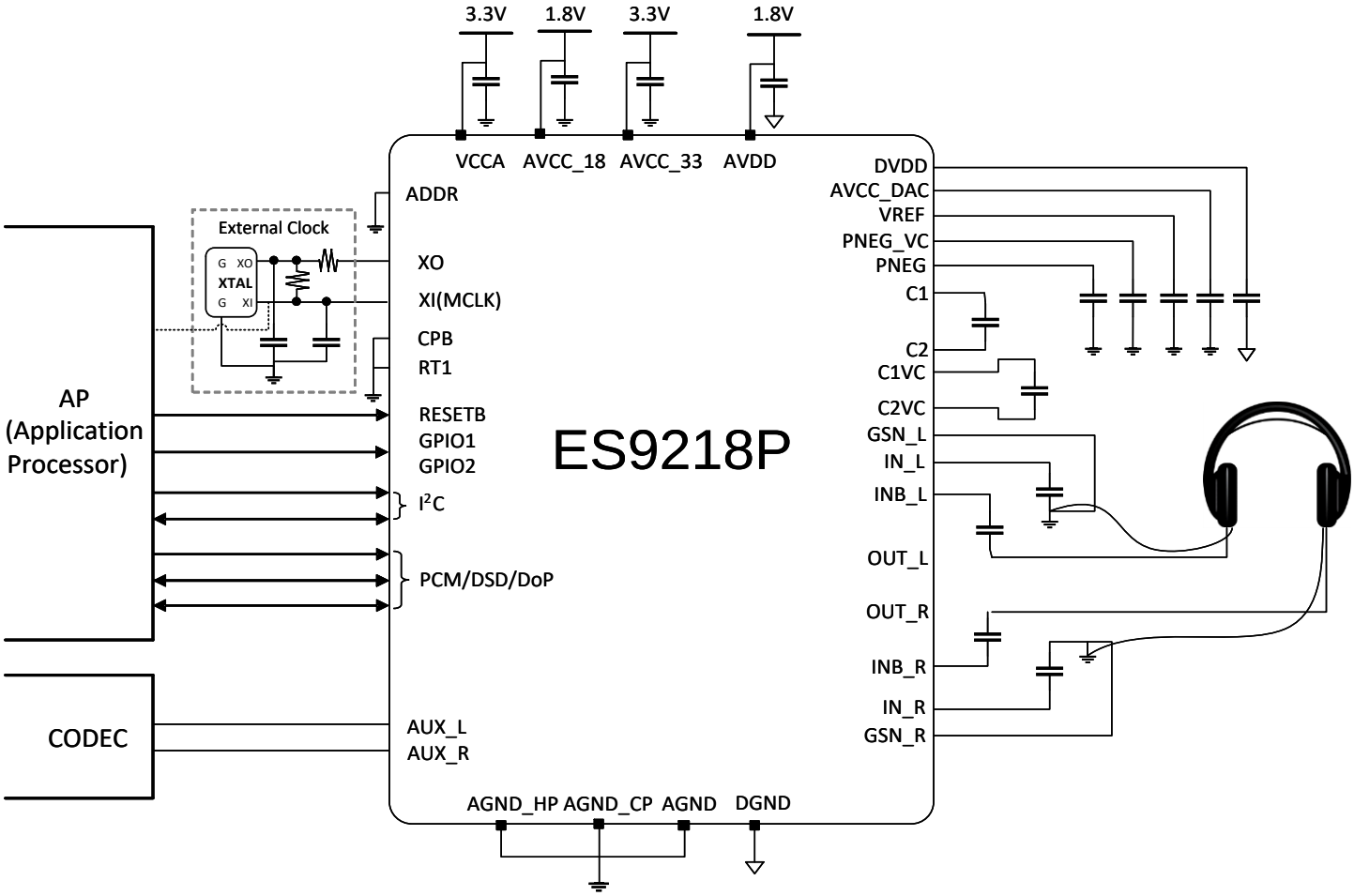
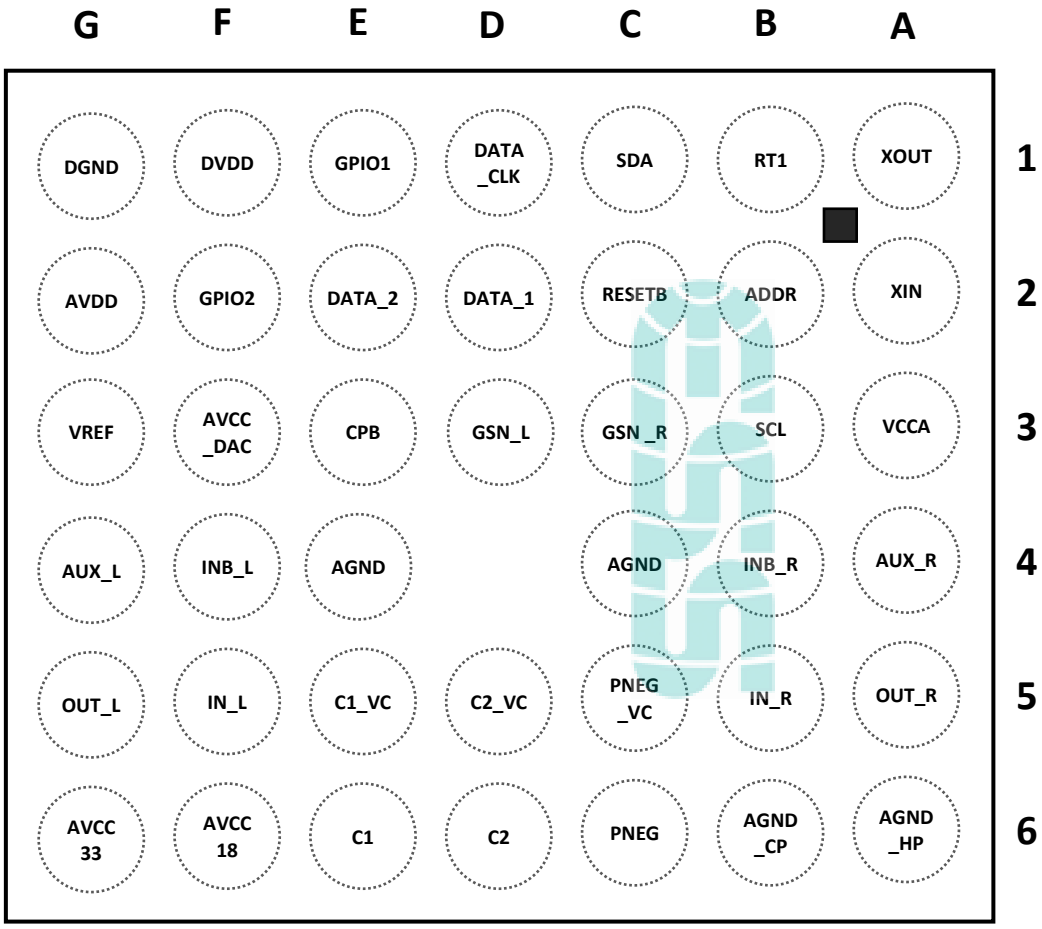


Figure 2. Typical Application Diagram

41 CSP Pinout

*Note D4 has no bump.

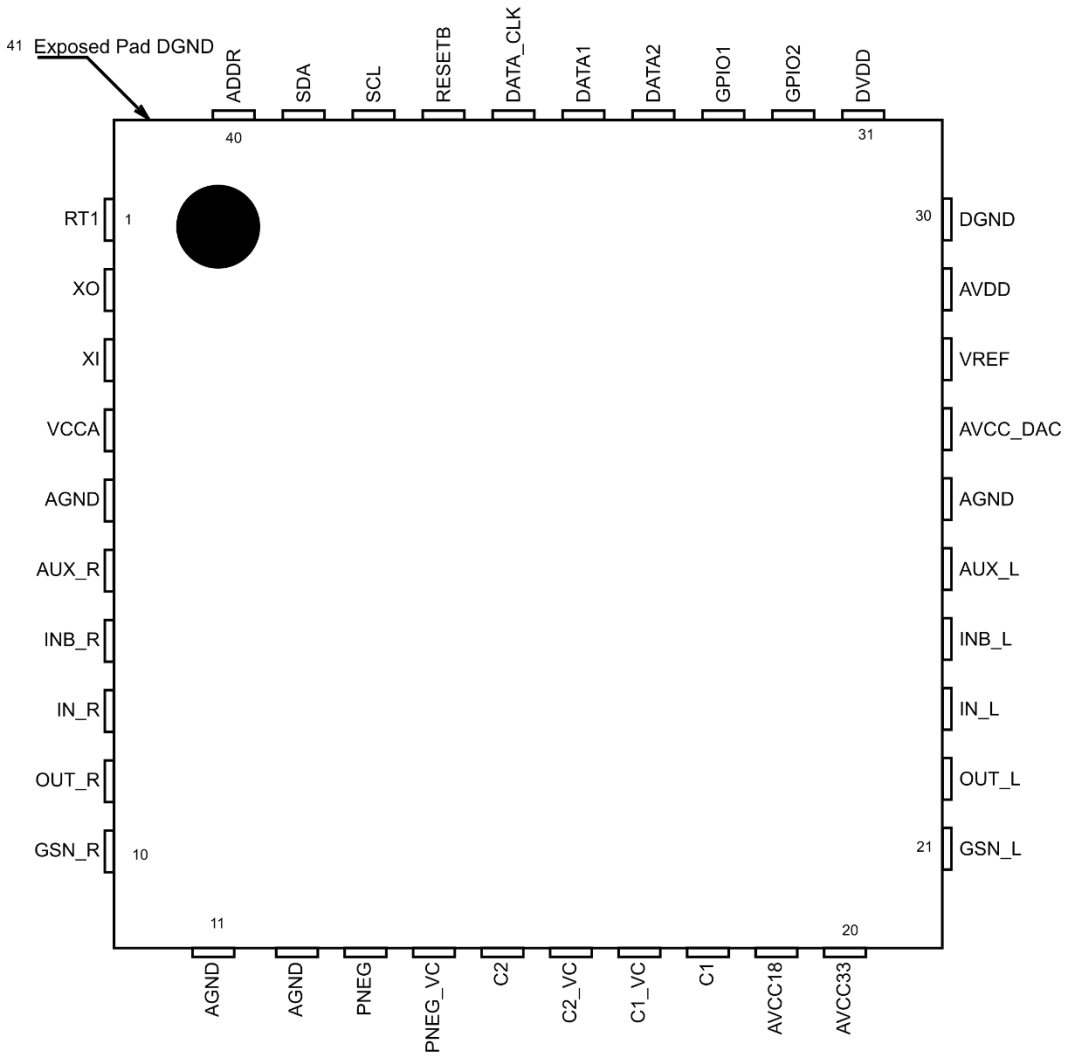


Pin Layout of ES9218PC
(Top View – Bump Side Down)

41 CSP Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
A1	XO	AO	Floating	XTAL output
A2	XI	AI	Floating	XTAL / MCLK input
A3	VCCA	Power	Power	Analog 1.8V/3.3V for OSC and on-chip AVCC_DAC regulator.
A4	AUX_R	AI	-	Auxiliary analog input (Right Channel)
A5	OUT_R	AO	-	Amplifier output (Right Channel)
A6	AGND_HP	Ground	Ground	Amplifier analog ground
B1	RT1	I	Tri-stated	Reserved. Must be connected to DGND for normal operation.
B2	ADDR	I	Tri-stated	I²C address select.
B3	SCL	I	Tri-stated	I²C serial clock input.
B4	INB_R	AI	-	Amplifier differential inverting input (Right Channel)
B5	IN_R	AI	-	Amplifier differential non-inverting input (Right Channel)
B6	AGND_CP	Ground	Ground	Charge pump analog ground.
C1	SDA	I/O	Tri-stated	I²C serial data input/output.
C2	RESETB	I	1'b0	Power down. Active low.
C3	GSN_R	-	-	Amplifier load ground sense. Right Channel
C4	AGND	Ground	Ground	DAC analog ground
C5	PNEG_VC	Power	Power	AVC negative supply. Internally supplied.
C6	PNEG	Power	Power	Amplifier negative supply. Internally supplied.
D1	DATA_CLK	I/O	Tri-stated	Slave Mode: Input for PCM Bit Clock or DSD Bit Clock, Master Mode: Output for PCM Bit Clock
D2	DATA1	I/O	Tri-stated	Slave Mode: Input for PCM Frame Clock or Input for DSD Data1 (Left Channel) Master Mode: Output for PCM Frame Clock
D3	GSN_L	-	-	Amplifier load ground sense. Left channel.
D5	C2_VC	-	-	AVC charge pump negative flying capacitor pin.
D6	C2	-	-	Amplifier charge pump negative flying capacitor pin.
E1	GPIO1	I/O	Tri-stated	GPIO 1
E2	DATA_2	I	Tri-stated	PCM Data Ch1+Ch2 or DSD Data2 (Right Channel)
E3	CPB	I	Tri-stated	Charge pump enable. Active low.
E4	AGND	Ground	Ground	DAC analog ground
E5	C1_VC	-	-	AVC charge pump positive flying capacitor pin.
E6	C1	-	-	Amplifier charge pump positive flying capacitor pin.
F1	DVDD	Power	Power	Digital core supply. Internally supplied.
F2	GPIO2	I/O	Tri-stated	GPIO 2 *special function in standby* (Aux. Path)
F3	AVCC_DAC	Power	Power	DAC analog supply. Internally supplied.
F4	INB_L	AI	-	Amplifier differential inverting input (Left Channel)
F5	IN_L	AI	-	Amplifier differential non-inverting input (Left Channel)
F6	AVCC18	Power	Power	Analog 1.8V supply for Amplifier, switch, AVC and charge pumps.
G1	DGND	Ground	Ground	Digital ground.
G2	AVDD	Power	Power	Digital 1.8V/3.3V supply for I/O and on-chip DVDD regulator.
G3	VREF	Power	Power	Low Noise reference for on-chip AVCC_DAC regulator.
G4	AUX_L	AI	-	Auxiliary analog input (Left Channel)
G5	OUT_L	AO	-	Amplifier output (Left Channel).
G6	AVCC33	Power	Power	Analog 3.3V supply for Amplifier, switch, AVC and charge pumps.

40 Pin QFN Pinout



ES9218PQ
(Top View)

40 Pin QFN Pin Descriptions

Pin	Name	Pin Type	Reset State	Pin Description
1	RT1	I	Tri-stated	Reserved. Must be connected to DGND for normal operation.
2	XO	AO	Floating	XTAL output
3	XI	AI	Floating	XTAL / MCLK input
4	VCCA	Power	Power	Analog 1.8V/3.3V for OSC and on-chip AVCC_DAC regulator.
5	AGND	Ground	Ground	DAC analog ground (Right Channel)
6	AUX_R	AI	-	Auxiliary analog input (Right Channel)
7	INB_R	AI	-	Amplifier differential inverting input (Right Channel)
8	IN_R	AI	-	Amplifier differential non-inverting input (Right Channel)
9	OUT_R	AO	-	Amplifier output (Right Channel)
10	GSN_R	-	-	Amplifier load ground sense (Right Channel)
11	AGND	Ground	Ground	Analog ground
12	AGND	Ground	Ground	Analog ground
13	PNEG	Power	Power	Amplifier negative supply. Internally supplied.
14	PNEG_VC	Power	Power	AVC negative supply. Internally supplied.
15	C2	-	-	Amplifier charge pump negative flying capacitor pin.
16	C2_VC	-	-	AVC charge pump negative flying capacitor pin.
17	C1_VC	-	-	AVC charge pump positive flying capacitor pin.
18	C1	-	-	Amplifier charge pump positive flying capacitor pin.
19	AVCC18	Power	Power	Analog 1.8V supply for Amplifier, switch, AVC and charge pumps.
20	AVCC33	Power	Power	Analog 3.3V supply for Amplifier, switch, AVC and charge pumps.
21	GSN_L	-	-	Amplifier load ground sense. Left channel.
22	OUT_L	AO	-	Amplifier output (Left Channel).
23	IN_L	AI	-	Amplifier differential non-inverting input (Left Channel)
24	INB_L	AI	-	Amplifier differential inverting input (Left Channel)
25	AUX_L	AI	-	Auxiliary analog input (Left Channel)
26	AGND	Ground	Ground	DAC analog ground (Left Channel)
27	AVCC_DAC	Power	Power	DAC analog supply. Internally supplied.
28	VREF	Power	Power	Low Noise reference for on-chip AVCC_DAC regulator.
29	AVDD	Power	Power	Digital 1.8V/3.3V supply for I/O and on-chip DVDD regulator.
30	DGND	Ground	Ground	Digital ground.
31	DVDD	Power	Power	Digital core supply. Internally supplied.
32	GPIO2	I/O	Tri-stated	GPIO 2 *special function in standby* (Aux. Path)
33	GPIO1	I/O	Tri-stated	GPIO 1
34	DATA_2	I	Tri-stated	PCM Data Ch1+Ch2 or DSD Data2 (Right Channel)
35	DATA1	I/O	Tri-stated	Slave Mode: Input for PCM Frame Clock or Input for DSD Data1 (Left Channel) Master Mode: Output for PCM Frame Clock
36	DATA_CLK	I/O	Tri-stated	Slave Mode: Input for PCM Bit Clock or DSD Bit Clock, Master Mode: Output for PCM Bit Clock
37	RESETB	I	1'b0	Power down. Active low.
38	SCL	I	Tri-stated	I^2C serial clock input.
39	SDA	I/O	Tri-stated	I^2C serial data input/output.
40	ADDR	I	Tri-stated	I^2C address select.
41	DGND	Ground	Ground	Exposed pad. Digital ground.

Functional Description

Sample Rate Notation

Mode	fs (target sample rate)	FSR (raw sample rate)
PCM Normal Mode	Frame Clock Rate	Frame Clock Rate
PCM OSF Bypass Mode	Frame Clock Rate / 8	Frame Clock Rate
DSD Mode	DSD Clock (DATA_CLK)	DSD data rate

PCM Pin Connections

The clock requirements in System Clock XI(MCLK) must be met for proper operation in PCM mode.

Pin Name	Description
DATA_2	2-channel PCM serial data
DATA_1	Frame clock
DATA_CLK	Bit clock

DSD Pin Connections

The clock requirements in System Clock XI(MCLK) must be met for proper operation in DSD mode.

Pin Name	Description
DATA_2	DSD Data mapped to Left Channel by default.
DATA_1	DSD Data mapped to Right Channel by default.
DATA_CLK	Bit clock

DoP Pin Connections

The clock requirements in System Clock XI(MCLK) must be met for proper operation in DoP mode.

Pin Name	Description
DATA_2	2-channel DSD data encoded into PCM frames according to the DoP standard.
DATA_1	Frame clock
DATA_CLK	Bit clock

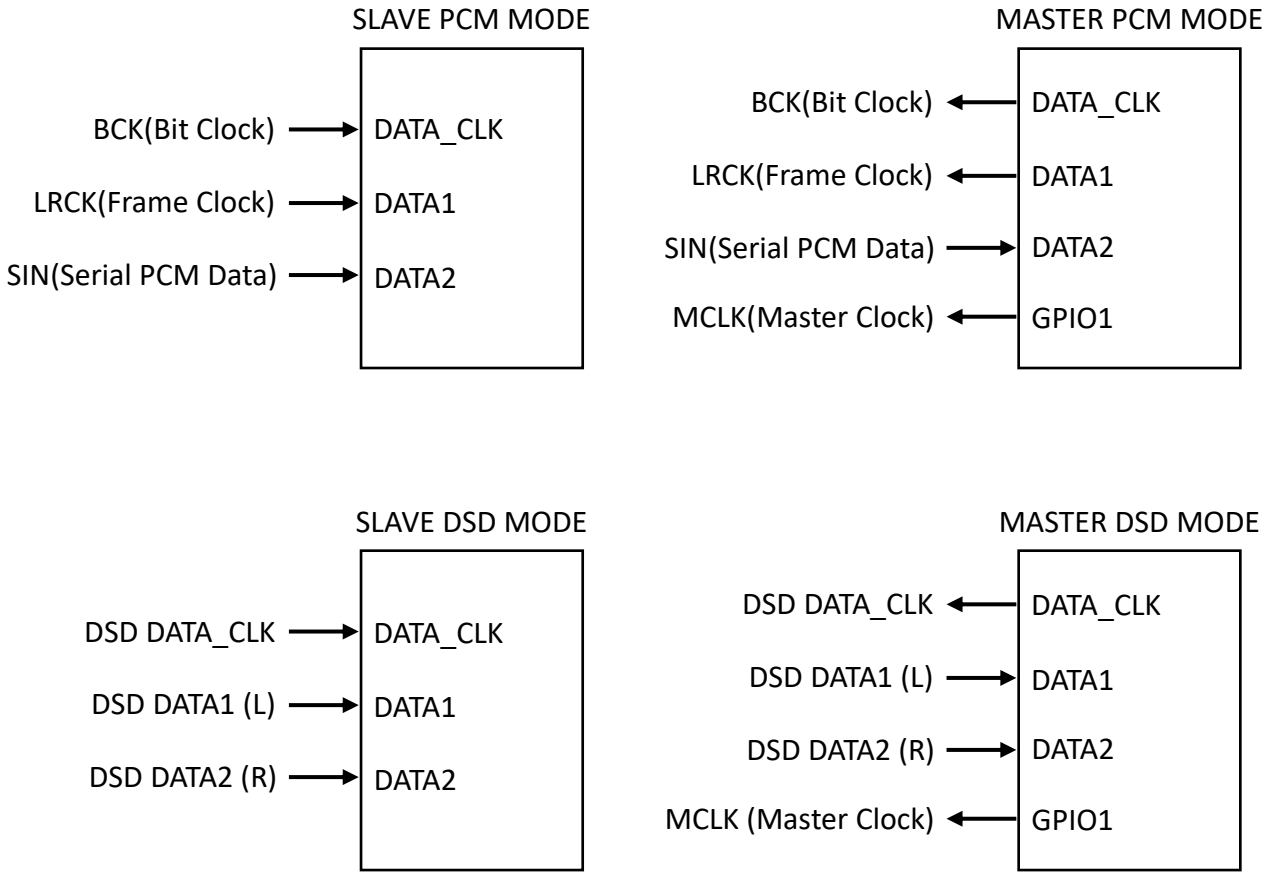
Master Mode

The DAC can be configured for master mode operation using Register 10: Master Mode and Sync Configuration (0x0A).
Register 1: Input selection (0x01) *input_select* must also be set to either DSD or Serial mode. Auto Select will not work correctly in master mode.

DATA_CLK frequency can be configured using one of the following methods:

1. Set the desired *master_div* in Register 10: Master Mode and Sync Configuration (0x0A)
   OR
2. Use NCO mode to set CLK/FSR ratio with Register 34-37: Programmable NCO (0x22 - 0x25). When NCO mode is enabled it has precedence and the *master_div* setting will be ignored.

An available GPIO pin can be configured to output CLK using Register 8: GPIO1-2 Configuration (0x08). GPIO1 is recommended for this purpose since GPIO2 is used to control Low Power Bypass mode.



Contact your local FAE for DoP master mode support.

Functional Description – Digital Features

Digital Audio Path

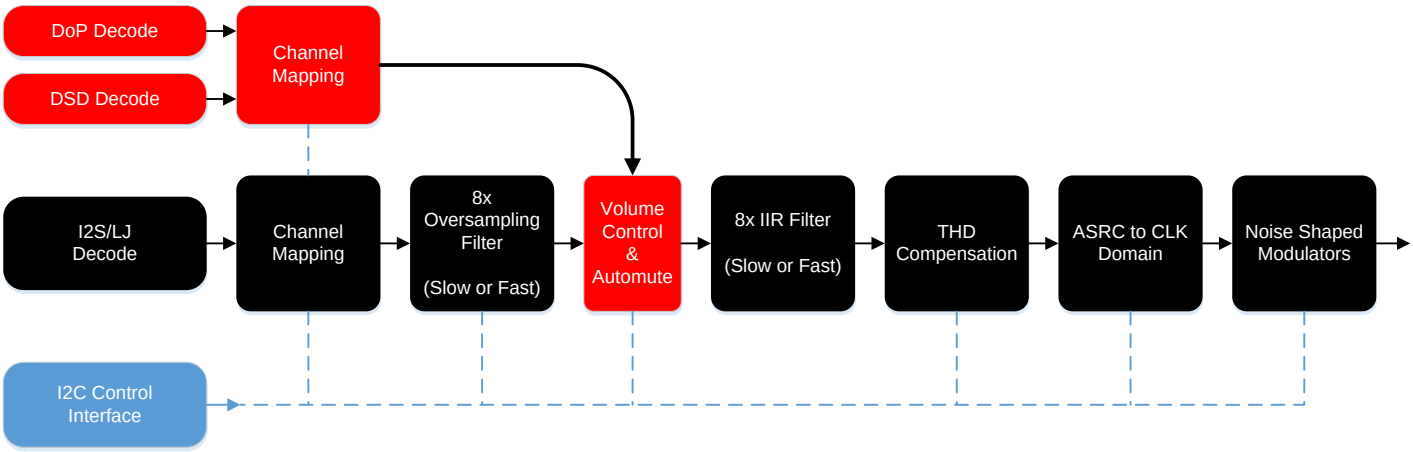


Figure 3 - Digital audio path

Soft Mute

When Mute is asserted the output signal will be ramped to the –∞ level. When Mute is reset the attenuation level will ramp back up to the previous level set by the volume control register. Asserting Mute will not change the value of the volume control register. The ramp rate is set by Register 6: DoP and Volume Ramp Rate (0x06) according to the following relationship:

$$\frac{2^{\text{vol\_rate}} * \text{FS}}{512} \text{ dB/s}$$

Mute can be triggered by any of the following settings:

- GPIO. See Register 8: GPIO1-2 Configuration (0x08).
- Explicit register setting. See Register 7: Filter Bandwidth and System Mute (0x07).
- Automute. See Automute.

Automute

Automute must be enabled and configured using Register 2: Mixing, Serial Data and Automute Configuration (0x02). It is disabled by default. Automute is triggered when any one of the following conditions are met:

Mode	Detection Condition	Time
PCM	Data is lower than *automute_level* for the specified time	2096896 / (*automute_time* x 64 x fs)
DSD	Equal number of 1s and 0s in every 8 bits of data	2096896 / (*automute_time*) x DATA_CLK)

Automute_time can be set using Register 4: Automute Time (0x04).
Automute_level can be set using Register 5: Automute Level (0x05).

Volume Control

Each output channel has its own attenuation circuit. The attenuation for each channel is controlled independently. Each channel can be attenuated from 0dB to –127dB in 0.5dB steps. Each 0.5dB step transition takes up to 64 intermediate levels, depending on the *vol_rate* setting in Register 6: DoP and Volume Ramp Rate (0x06). The result being that the level changes are done using small enough steps so that no switching noise occurs during the transition of the volume control. When a new volume level is set, the attenuation circuit will ramp softly to the new level.

The volume control can be either channel independent or synchronized using Register 27: General Configuration (0x1B) *ch1_volume*.

Master Trim

The master trim sets the 0dB reference level for the digital volume control of each DAC. The master trim is programmable via Register 17-20: Master Trim (0x11 - 0x14). The master trim registers store a 32bit signed number.

This register value should never exceed the full scale signed value 32'h7FFFFFFF

Example: Setting the reference value to -1dB (from full-scale) = 32'h721482BF

System Clock XI(MCLK)

A system clock is required for proper operation of the digital filters and modulation circuitry.

Automatic clock gearing is supported to save power with the full XI(MCLK) clock rate is not required.

$$\mathrm{CLK} = \frac{\mathrm{XI}}{clock\_div}$$

The minimum XI(MCLK) frequency must satisfy the following conditions:

Data Type	Minimum MCLK Frequency
DSD Data	CLK > 3 x FSR , FSR = 2.8224MHz (x 1, 2, or 4)
Serial Normal Mode	CLK > 128 x FSR, FSR ≤ 384kHz CLK = 128 x FSR (synchronous MCLK) with FSR ≤ 384kHz
Serial OSF Bypass Mode	CLK > 24 x FSR, FSR ≤ 768kHz

Data Clock

DATA_CLOCK must be (2 x *i2s_length*) x FSR for PCM mode, and FSR for DSD modes. This pin should be pulled low if not used.

Built-in Digital Filters

Eight digital filters are included for PCM mode.
See PCM Filter Frequency Response for filter characteristics and Register 7: Filter Bandwidth and System Mute (0x07) for available filter settings.

Standby Mode

For lowest power consumption, the following should be performed to enter stand-by mode:
Shut down the amplifier portion of the chip with Register 32: Amplifier Configuration (0x20)

1. Pull RESETB low. This will:
    a. Shut off the DACs, oscillator and internal regulators.
    b. Force all digital I/O pins into tri-state mode
2. If XI is supplied externally, it should be stopped at a logic low level
3. Disable any power supplies connected to the chip

To resume from standby mode:

1. Enable all power supplies
2. Pull RESETB up
3. Reinitialize all registers

To resume from standby mode, bring RESETB to a logic-high and reinitialize all registers.

OPERATION Mode	RESETB	GPIO2
HiFi Mode (DAC & HPA: ON, AUX SW: OFF)	H	X
AUX Mode (DAC & HPA: OFF, AUX SW: ON)	L	H
Standby(Shutdown) Mode (DAC, HPA, AUX SW: OFF)	L	L

DVDD Supply

The ES9218P is equipped with a regulated DVDD supply powered from AVDD. The internal DVDD regulator should be decoupled to DGND with a capacitor that maintains a minimum value of 1μF at 1.2V over the target operating temperature range.

Programmable FIR filter

A two stage interpolating FIR design is used. The interpolating FIR filter is generated using MATLAB, and can then be downloaded using a custom C code.

Example Source Code for Loading a Filter

```
// only accept 128 or 16 coefficients
// Note:  The coefficients must be quantized to 24 bits for this method!
// Note:  Stage 1 consists of 128 values (0-127 being the coefficients)
// Note:  Stage 2 consists of 16 values (0-13 being the coefficients, 14-15 are zeros)
// Note:  Stage 2 is symmetric about coefficient 13.  See the example filters for more information.
byte reg40 = (byte)(coeffs.Count == 128 ? 0 : 128);
for (int i = 0; i < coeffs.Count; i++)
{
    // stage 1 contains 128 coefficients, while stage 2 contains 16 coefficients
    registers.WriteRegister(40, (byte)(reg26 + i));

    // write the coefficient data
    registers.WriteRegister(41, (byte)(coeffs[i] & 0xff));
    registers.WriteRegister(42, (byte)((coeffs[i] >> 8) & 0xff));
    registers.WriteRegister(43, (byte)((coeffs[i] >> 16) & 0xff));

    registers.WriteRegister(44, 0x02);   // set the write enable bit
}
// disable the write enable bit when we're done
registers.WriteRegister(44, (byte)(setEvenBit ? 0x04 : 0x00));
```

For more information on programming a custom filter, contact your local FAE.

OSF Bypass

The oversampling FIR filter can be bypassed using *bypass_osf* in Register 7: Filter Bandwidth and System Mute (0x07), sourcing data directly into the IIR filter. The audio input should be oversampled at 8 x fs rate when OSF is bypassed to have the same IIR filter bandwidth as PCM audio sampled at fs rate. For example, an external signal at 44.1kHz can be oversampled externally to 8 x 44.1kHz = 352.8kHz and then applied to the serial decoder in either I^2S or LJ format. The maximum sample rate that can be applied is 768kHz (8 x 96kHz).

DSD Filter

A DSD filter with cutoff at 47kHz scaled by fs/44100 is available. See DSD FILTER Characteristics for more information.

THD Compensation

THD Compensation minimizes the non-linearity of the DAC output resistors and to a lesser degree the non-linearity of passive components in the output stage.

Non-linearity of the DAC output resistors can lead to output distortion in two ways:

1. Amplitude modulation of the output current from the DAC
2. Gain modulation of the output stage as the output impedance of the DAC swings with the audio signal

The ES9218P includes models for its output resistors and can compensate for their characteristic curve by finely adjusting the DAC codes for large and small signal amplitudes.

THD compensation can be enabled via *bypass_thd* in Register 13: THD Compensation Bypass & Mono Mode (0x0D)
The coefficient for manipulating second harmonic distortion is stored in Register 22-23: THD Compensation C2 (0x16 - 0x17)
The coefficient for manipulating third harmonic distortion is stored in Register 24-25: THD Compensation C3 (0x18 - 0x19)
Left and right channels use the same compensation coefficients unless enable_seperate_thd_comp in Register 48: Analog Control (0x30) is used.

Functional Description – Amplifier and Switch

Charge Pump

The ES9218P includes two charge pumps.

The main low noise charge pump uses a 500kHz switching frequency, which is outside the audio band and therefore does not interfere with audio signals. The chargepump switches are sequence controlled to minimize pops and clicks. This supply requires a 2.2μF (minimum) ceramic flying capacitor between pins C1 and C2 and a 22μF (recommended) ceramic hold capacitor from PNEG to AGND_CP. See ES9218PC Reference Schematic.

The auxiliary charge pump uses the same switching frequency as the main chargepump, so no intermodulation frequencies are generated. It requires a 1μF (recommended) ceramic flying capacitor across pins C1_VC and C2_VC and a 1μF (recommended) ceramic hold capacitor from PNEG_VC to AGND_CP. See ES9218PC Reference Schematic.

Use capacitors with an Equivalent Series Resistance (ESR) of less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the main charge pump. For best performance over the extended temperature range select capacitors with a minimum X5R dielectric, the X7R dielectric is preferred.

Analog Volume Control

ES9218P

Analog volume control (AVC) provides improved noise performance as the gain is reduced. The hardware default programmable analog gain is -24dB with 1dB steps up to 0dB. See Register 3: Analog Volume Control (0x03).

The AVC is forced to minimum gain until the transition to HiFi mode is complete. The ES9218P follows a programmed timing sequence to enter HiFi mode. Enabling the AVC is one of the last steps in that sequence. This procedure will not change the value of the analog volume control register.

See Register 32: Amplifier Configuration (0x20).

Compensation Components

For optimum performance, matched feedback capacitors should be installed between OUT_L and INB_L, IN_L and GSN_L, OUT_R and INB_R, IN_R and GSN_R. These components set the bandwidth of the headphone amplifier. These capacitors should have a low temperature coefficient, NP0/C0G type are recommended. See ES9218PC Reference Schematic

The ES9218P includes internal feedback resistors for reduced part-count. 2.2nF NP0/C0G feedback capacitors are recommended to filter out-of-band noise. (2.2nF equals 70KHz bandwidth @ 0dB analog gain, 2.0nF equals 80KHz bandwidth, and 1.5nF equals 100KHz bandwidth).

Output Switch

The output signal is selected by an ultra-low THD analog switch that connects either to the HiFi audio headphone amplifier or to an alternate audio source. A typical alternate source may be voice or another DAC. There are two different ways to use the output switch:

LowFi Mode

The ultra-low THD analog switch may be controlled using Register 32: Amplifier Configuration (0x20). This allows audio to pass from an alternate source to the output. The digital core remains powered on and ready for a quick transition back to HiFi mode. All supplies must be enabled.

Low Power Bypass Mode

The ultra-low THD analog switch may be controlled using GPIO2 after RESETb is asserted and the chip is in standby. This allows audio to pass from an alternate source to the output without the use of the digital core. AVCC_HP and AVCC_CP supplies must be enabled.

This mode is activated when RESETB = pulled down and GPIO2=pulled up.

Overcurrent Protection

Overcurrent Protection (OCP) protects the amplifier output stage by independently sensing the positive and negative output current on the OUT_R and OUT_L pins. Once the current exceeds a built-in threshold for a cumulative user programmable timeout period, an OCP event will be triggered and both DAC channels will be muted.

OCP must be enabled and configured using *oc_sd_en* and *oc_sd_gain* in Register 11: Overcurrent Protection (0x0B); it is disabled by default.

When an overcurrent event is triggered, *oc_sd_mute* Register 72 (Read-Only): Input Selection and Automute Status (0x48) will be set and latched to indicate which channel triggered the event.

OCP does not automatically reset when the overcurrent condition is removed. After an OCP event occurs, the state of the OCP circuit needs to be manually cleared. This is accomplished by toggling OCP disabled-enabled with *oc_sd_en*.

Once enabled, the OCP status can be monitored in one of two ways:

1. Poll the *oc_sd_mute* flags in Register 72 (Read-Only): Input Selection and Automute Status (0x48).
2. Configure Register 8: GPIO1-2 Configuration (0x08) to set the desired GPIO pin to Interrupt mode and set Register 33: Interrupt Mask (0x21) appropriately.

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVDD, VCCA • AVCC_33 • AVCC_18 • DVDD	 +4.0V with respect to GND +4.0V with respect to GND +4.0V with respect to GND +1.8V with respect to GND
Negative Supply Voltage (PNEG & PNEG_VC)	–4.0V with respect to GND
Output Short-Circuit to GND (OUT_L, OUT_R)	Default Disable (Register setting)
Storage temperature	–65°C to +150°C
Operating Junction Temperature	+125°C
Voltage range for digital input pins	–0.3V to AVDD+ 0.3V
ESD Protection Human Body Model (HBM) Charge Device Model (CDM)	 2000V 500V

WARNING: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Operating temperature	T_A	–20°C to +70°C

Power Supply	Symbol	Voltage	Nominal Current / Power Consumption (Note 1)			
			HiFi 2V mode	HiFi 1V mode	AUX mode	Standby mode
Digital I/O	AVDD	+1.8V ±5%	7.2 mA	10.3 mA	3 uA	3 uA
Analog core	VCCA	+3.3V ±5%	9.0 mA	2.8 mA	185 uA	TBD
Analog power	AVCC_18 AVCC_33	+1.8V ±5% +3.3V ±5%	0 mA 11.0 mA	3.4 mA 5.5 mA	172 uA 742 uA	1 uA 1 uA
Internally Generated	DVDD AVCC_DAC PNEG PNEG_VC	+1.2V ±5% +1.25, 1.4, 2.5 or 2.8V ±5% -1.8V or -3.3V ±5% -3.3V ±5%				
Total			79 mW	52 mW	3.4 mW	< 1mW

Notes:

1) fs = 44.1kHz, external XI = 27MHz, auto clock gearing, I^2S input, output unloaded, internal DVDD, all external supply voltages at nominal values.

DC Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT	COMMENTS
High-level input voltage	VIH	AVDD / 2 + 0.4		V	
Low-level input voltage	VIL		0.4	V	
High-level output voltage	VOH	AVDD – 0.2		V	IOH = 1.5mA
Low-level output voltage	VOL		0.2	V	IOL = 7.5mA

Analog Performance

Test Conditions (unless otherwise stated)

1. T_A = 25ºC, VCCA =+3.3V, AVDD = +1.8V, internal DVDD with 4.7µF ±20% decoupling, fs = 44.1kHz, XI(MCLK) = 38MHz & 32-bit data
2. SNR/DNR: A-weighted over 20Hz-20kHz in averaging mode, Reference 2.0Vrms, HiFi2V mode.
   THD+N: un-weighted over 20Hz-20kHz bandwidth

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			32		Bits
CLK (PCM normal mode)	Note *1	128FSR		50M	Hz
CLK (PCM OSF bypass mode)		24FSR			
CLK (DSD mode)		3FSR			
DYNAMIC PERFORMANCE (digital input to headphone amplifier output @ HiFi Mode)					
Full Scale Output	0dBFS 600Ω		2.0	2.06	Vrms
SNR	Zero input 600Ω (Note *3)		136		dB-A
DNR	–60dBFS 600Ω		121		dB-A
THD+N	2Vrms into 300Ω		-112		dB
OUTPUT AMPLIFIER					
Output offset voltage	Note *2		TBD		mV
AUXILIARY ANALOG INPUTS					
Input voltage				1.0	Vrms
Digital Filter Performance					
Mute Attenuation			127		dB
PCM Filter Characteristics (Linear Phase Fast Roll Off)					
Pass band	±0.002dB			0.453 x fs	Hz
	–3dB			0.484 x fs	Hz
Stop band	< –120dB	0.55 x fs			Hz
Group Delay			35 / fs		s
PCM Filter Characteristics (Linear Phase Slow Roll Off)					
Pass band	±0.01dB			0.357 x fs	Hz
	–3dB			0.450 x fs	Hz
Stop band	< –82dB	0.639 x fs			Hz
Group Delay			8.75 / fs		s
PCM Filter Characteristics (Minimum Phase Fast Roll Off)					
Pass band	±0.005dB			0.453 x fs	Hz
	–3dB			0.491 x fs	Hz
Stop band	< –100dB	0.547 x fs			Hz
Group Delay			5.4 / fs		s
PCM Filter Characteristics (Minimum Phase Slow Roll Off)					
Pass band	±0.015dB			0.363 x fs	Hz
	–3dB			0.435 x fs	Hz
Stop band	< -97dB	0.634 x fs			Hz
Group Delay			3.5 / fs		s
PCM Filter Characteristics (Apodizing Fast Roll Off Type 1)					
Pass band	±0.075dB			0.409 x fs	Hz

	–3dB			0.461 x fs	Hz
Stop band	< -80dB < -100dB	0.5 x fs 0.66 x fs			Hz
Group Delay			35 / fs		s
PCM Filter Characteristics (Apodizing Fast Roll Off Type 2)					
Pass band	±0.1dB			0.409 x fs	Hz
	–3dB			0.461 x fs	Hz
Stop band	< -81dB < -97dB	0.5 x fs 0.506 x fs			Hz
Group Delay			5.5 / fs		s
PCM Filter Characteristics (Hybrid Fast Roll Off)					
Pass band	±0.01dB			0.404 x fs	Hz
	–3dB			0.430 x fs	Hz
Stop band	< -94.5dB < -106dB	0.504 x fs 0.513 x fs			Hz
Group Delay			18.5 / fs		s
PCM Filter Characteristics (Brick Wall)					
Pass band	±0.015dB			0.435 x fs	Hz
	–3dB			0.451 x fs	Hz
Stop band	< -100dB	0.5 x s			Hz
Group Delay			35 / fs		s

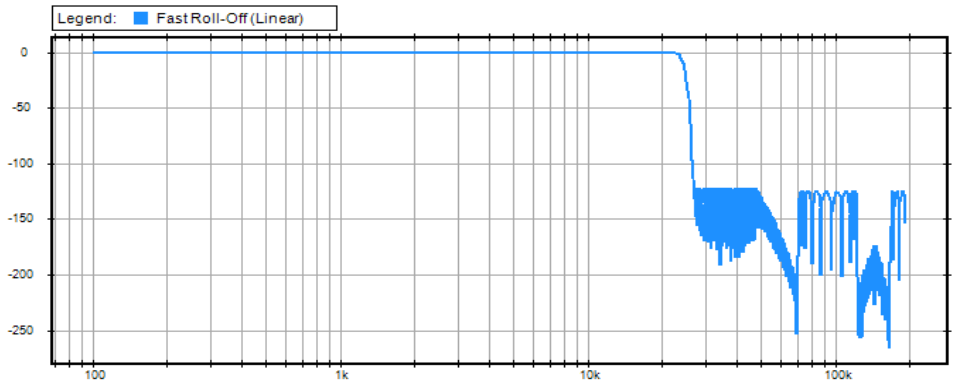
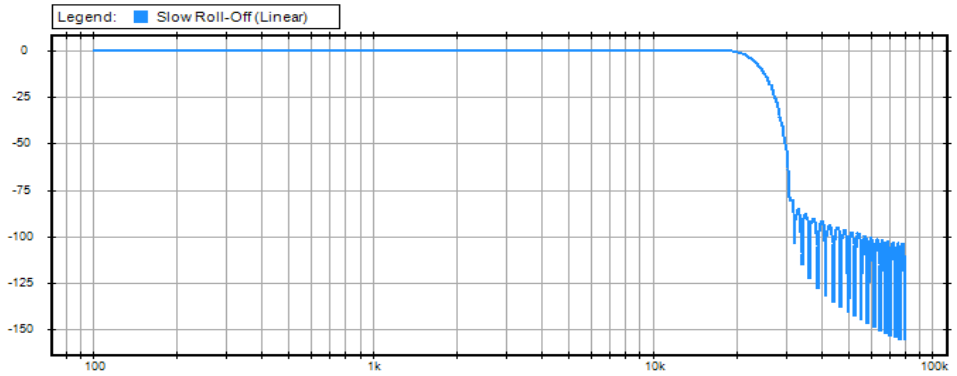
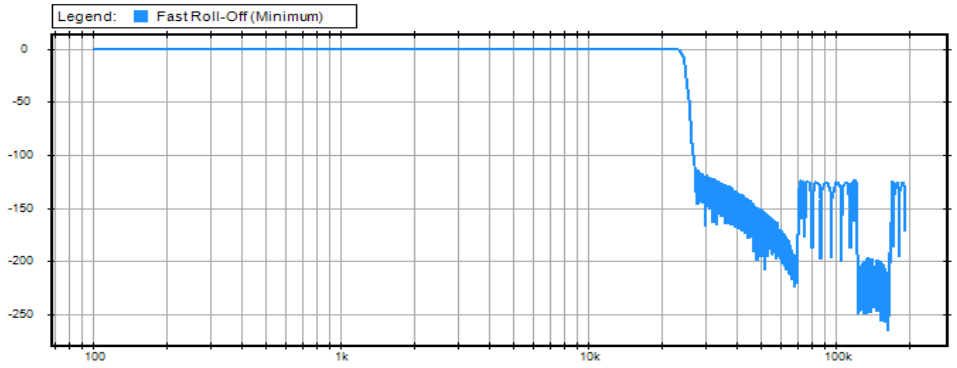
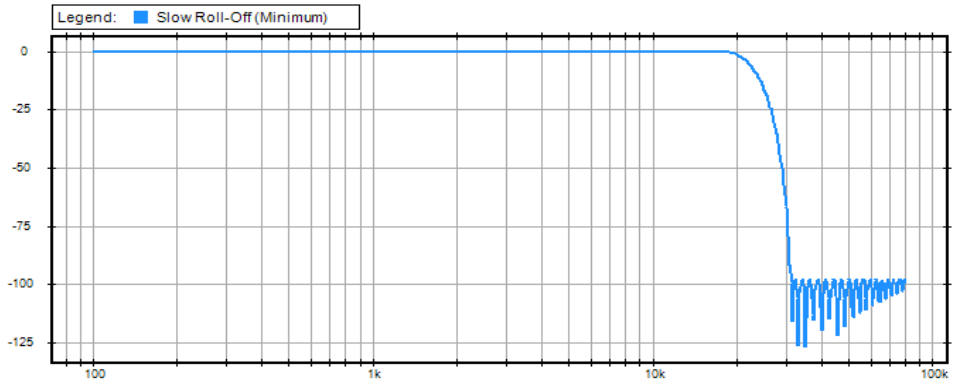
Notes:

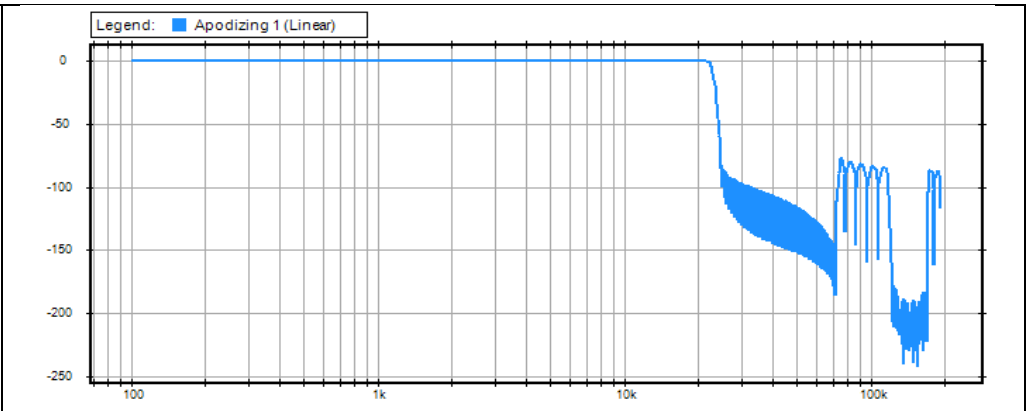
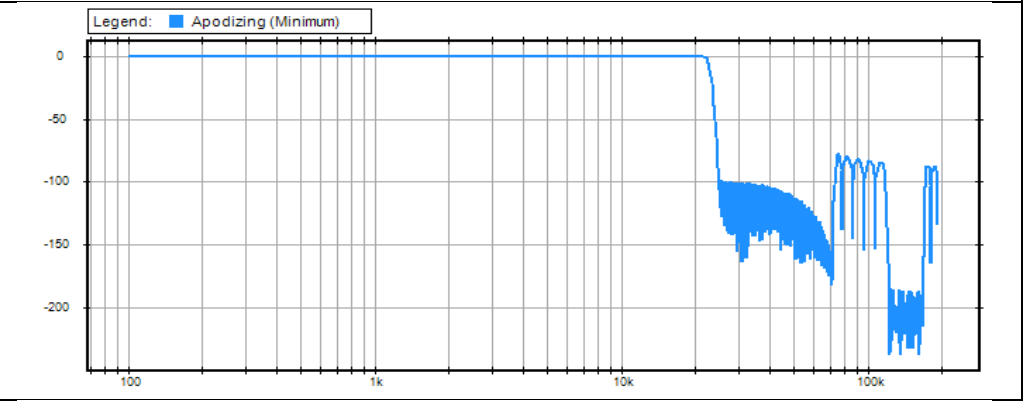
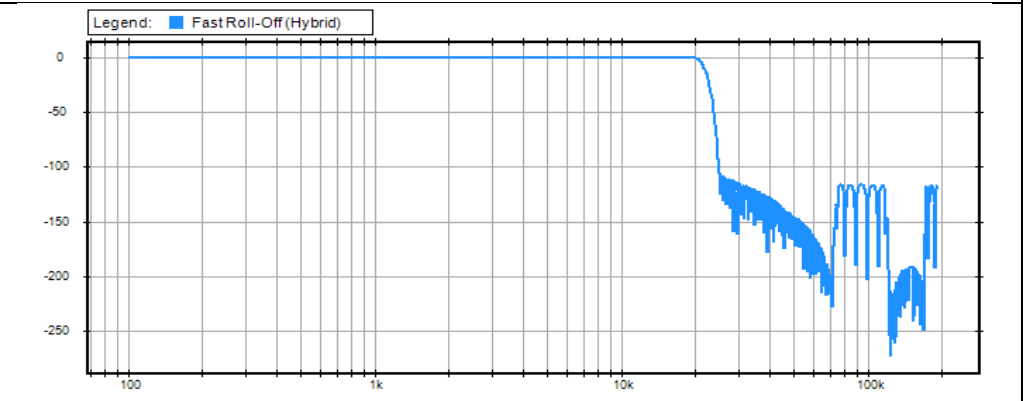
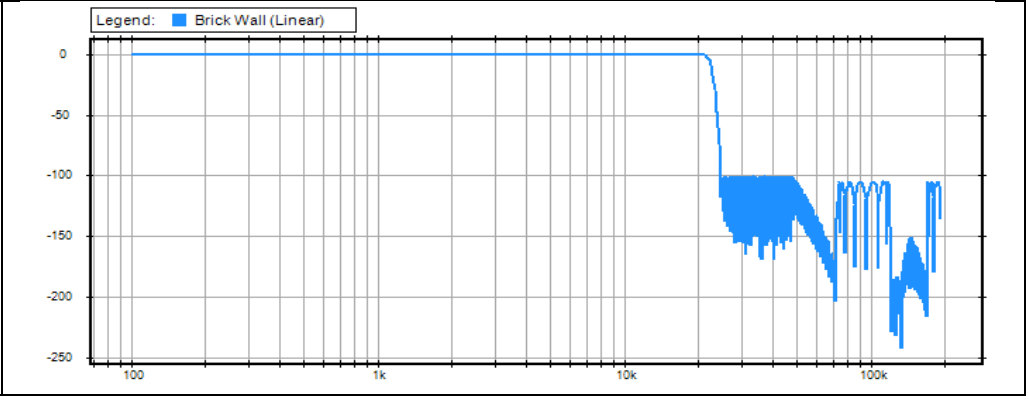
*1. CLK at 128FSR is also supported in Synchronous Mode

*2. Measured between OUT_L and GND, and OUT_R and GND, DAC outputs set to DAC output set to 50/50. See

*3. Automute Enabled, Automute configured for Mute + Ramp-to-ground, Analog Automute, Amp_pdb_ss

PCM Filter Frequency Response

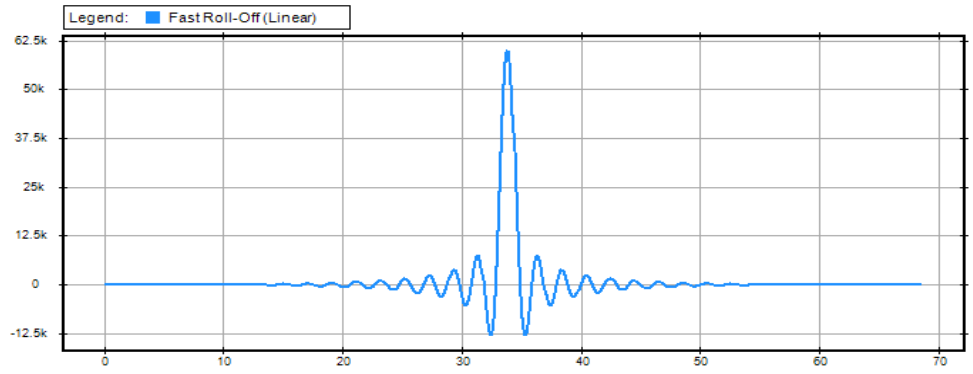
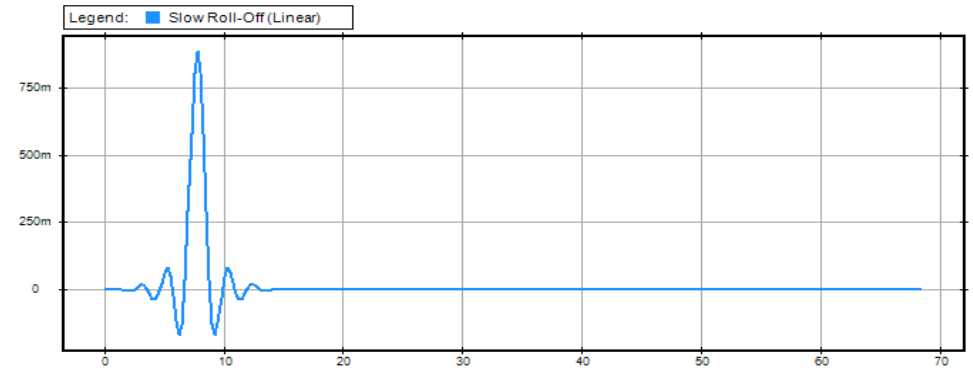
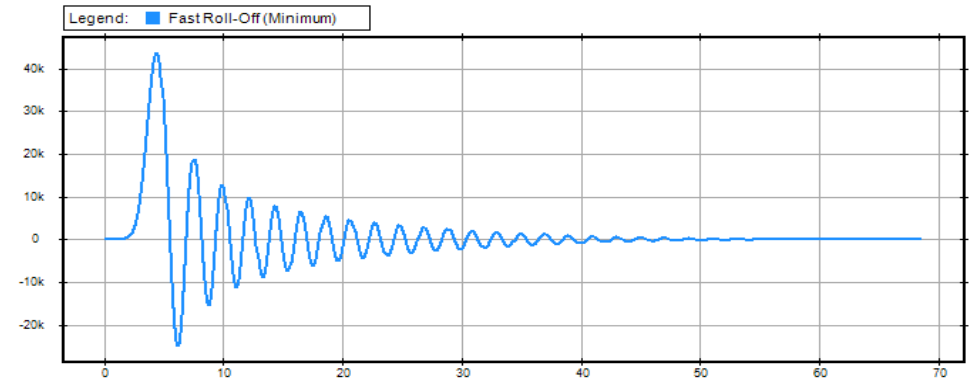
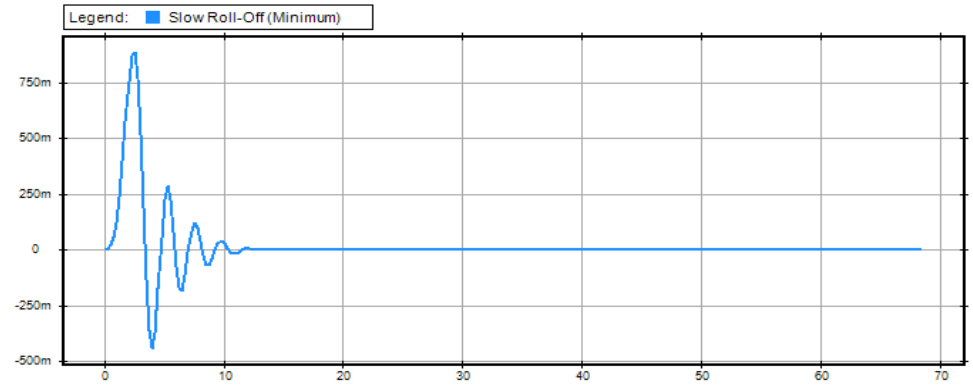
Filter	Response Curve
Linear phase fast roll-off filter (dB)	
Linear phase slow roll-off filter (dB)	
Minimum phase fast roll-off filter (dB)	
Minimum phase slow roll-off filter (dB)	

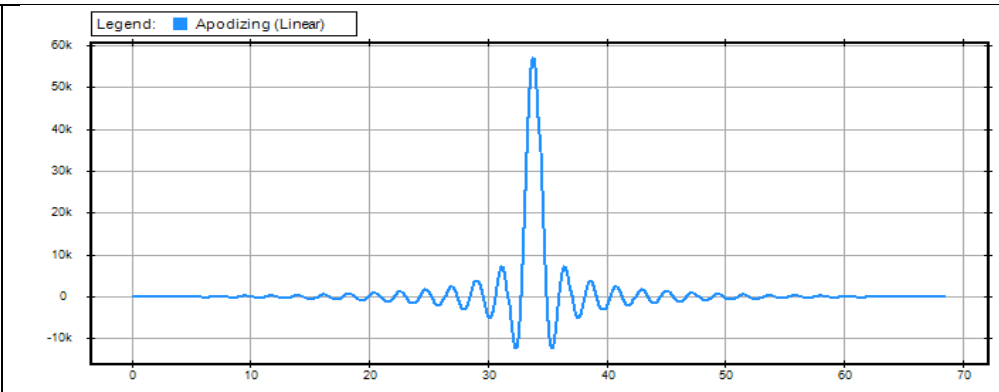
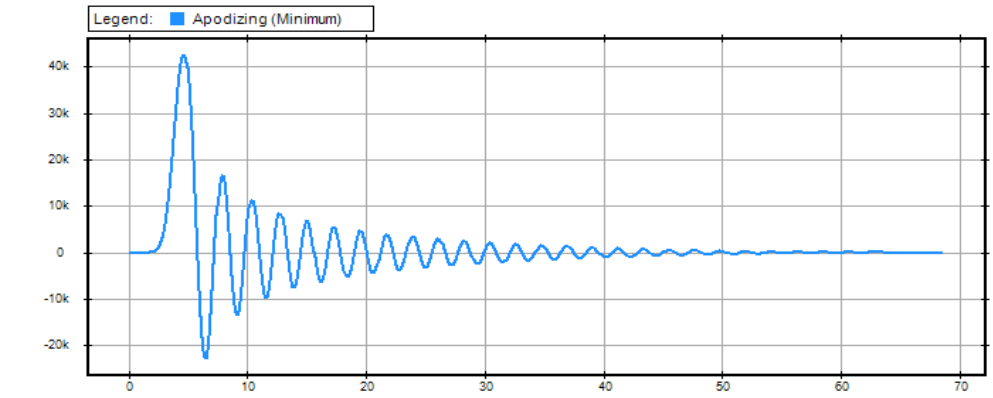
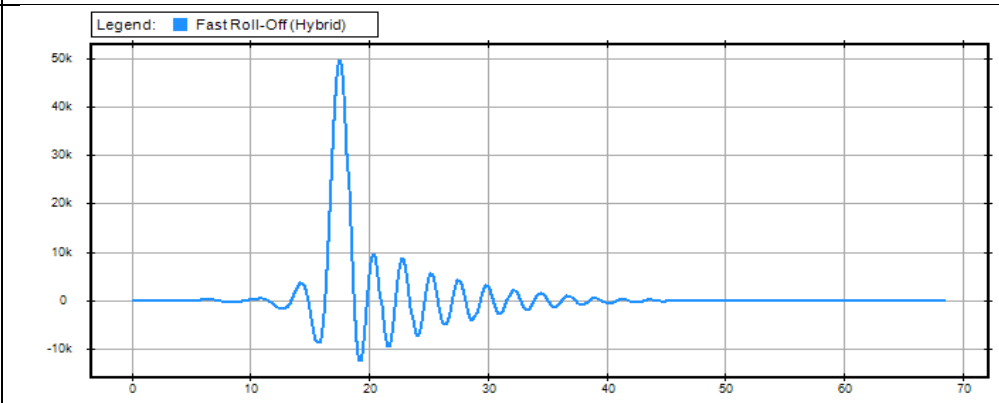
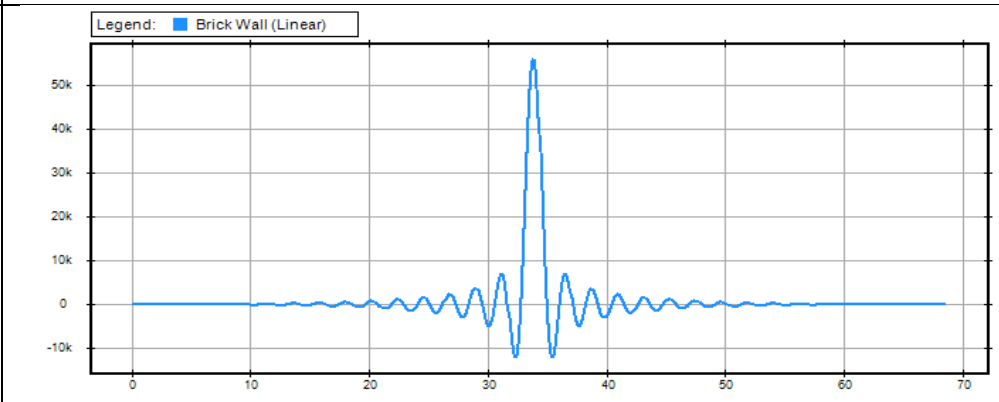
Apodizing fast roll-off filter type 1 (default, dB)	
Apodizing fast roll-off filter type 2 (dB)	
Hybrid fast roll-off filter (dB)	
Brick wall filter (dB)	

Unit: fs (Hz) / 48000

Figure 4. PCM Filter Frequency Response

PCM Filter Impulse Response

Filter	Response Curve
Linear phase fast roll-off filter	
Linear phase slow roll-off filter	
Minimum phase fast roll-off filter	
Minimum phase slow roll-off filter	

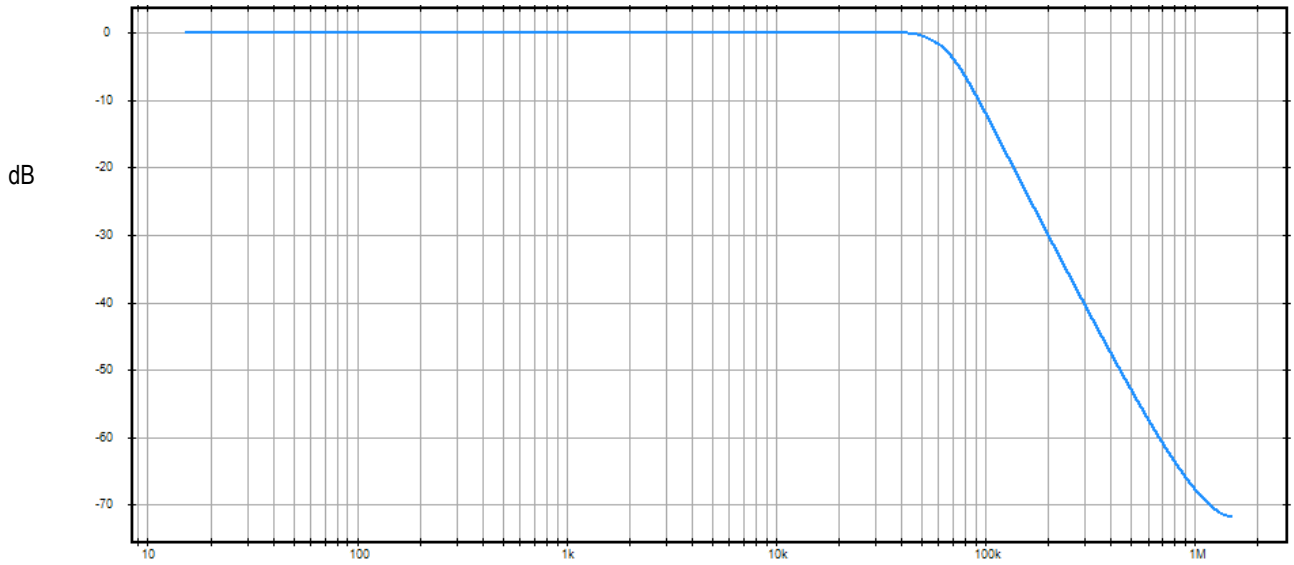
Apodizing fast roll-off filter type 1 (default)	
Apodizing fast roll-off filter type 2	
Hybrid fast roll-off filter	
Brick wall filter	

Unit: 1/fs (s)

Figure 5. PCM Filter Impulse Response

DSD Filter Characteristics

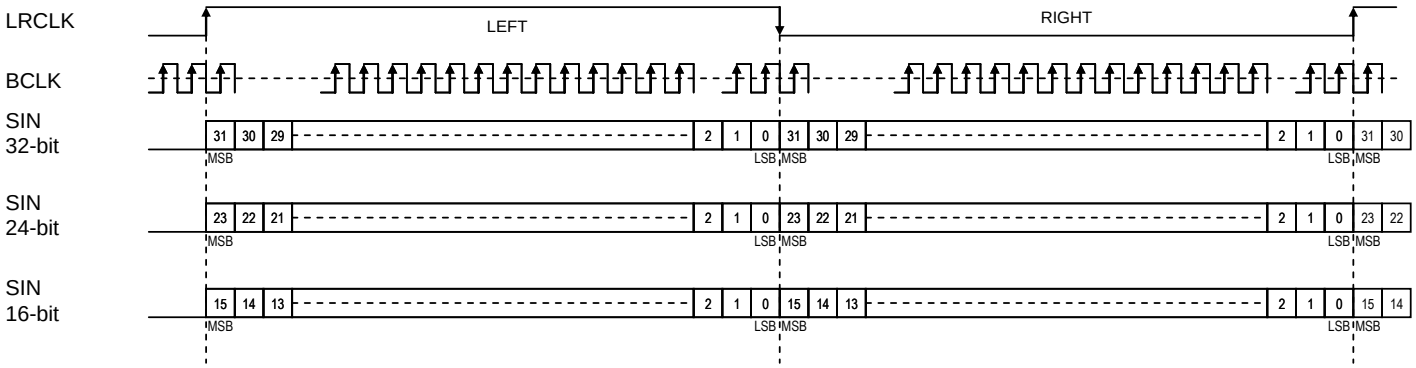
DSD Filter Frequency Response



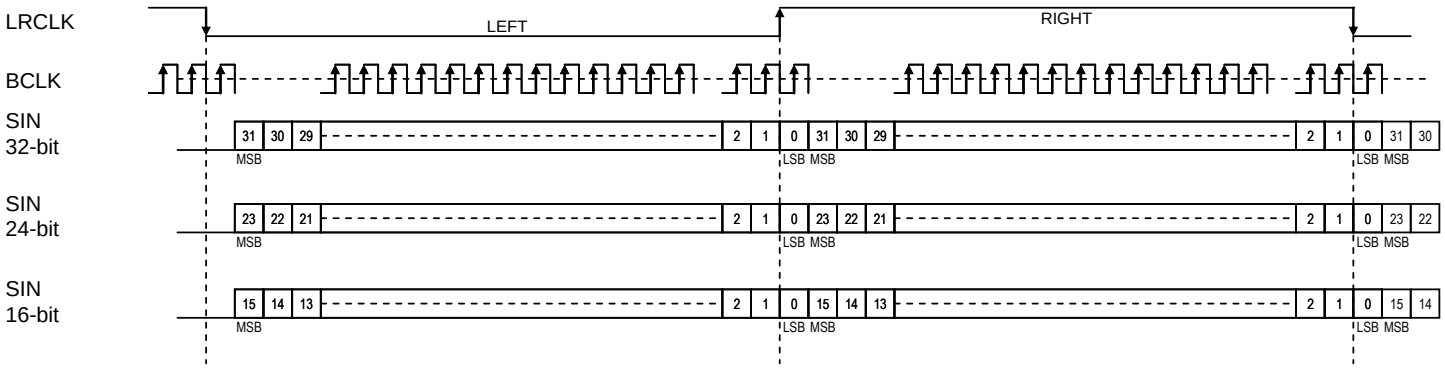
Unit: DATA_CLK (Hz) / 2822400

Audio Interface Formats

Several interface formats are provided so that direct connection to common audio processors is possible. The available formats are shown in the following diagrams. The audio interface format can be set by programming the registers.



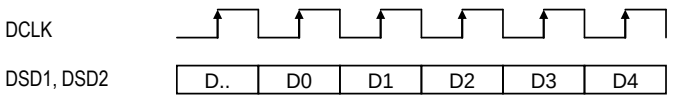
LEFT JUSTIFIED FORMAT



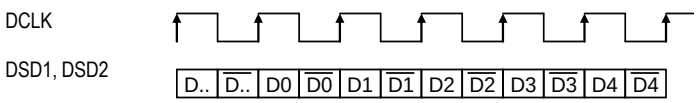
I2S FORMAT

Note: for Left-Justified and I²S formats, the following number of BCLKs is present per (left plus right) frame:

- 16-bit mode: 32 BCLKs
- 24-bit mode: 48 BCLKs
- 32-bit mode: 64 BCLKs



DSD NORMAL MODE



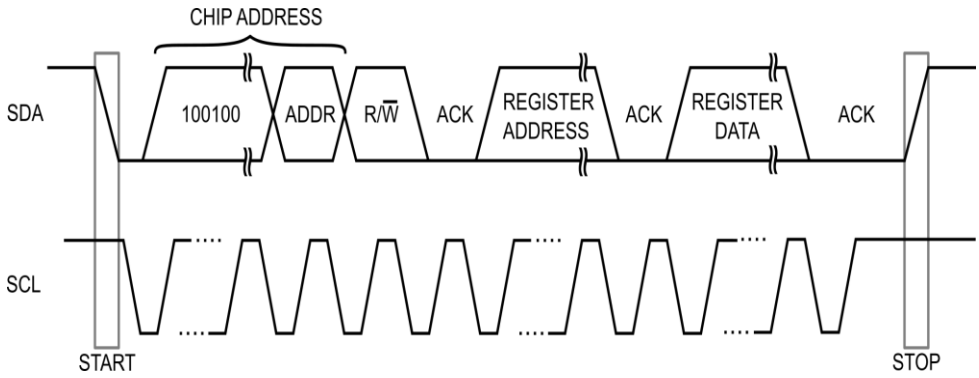
DSD PHASE MODE

Figure 6. Audio Interface Format

Serial Control Interface

The chip registers are programmed via an I²C interface. The diagram below shows the timing for this interface. The chip address can be set to 2 different settings using the ADDR pin.

ADDR	CHIP ADDRESS
0	0x90
1	0x92



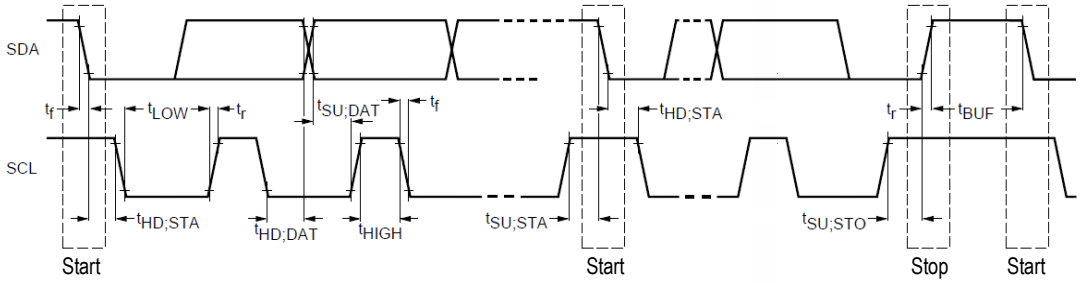


Figure 7. I2C Control Interface

Parameter	Symbol	CLK Constraint	Standard-Mode		Fast-Mode		Unit
			MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}	< CLK/20	0	100	0	400	kHz
START condition hold time	$t_{HD,STA}$		4.0	-	0.6	-	µs
LOW period of SCL	t_{LOW}	>10/CLK	4.7	-	1.3	-	µs
HIGH period of SCL (>10/CLK)	t_{HIGH}	>10/CLK	4.0	-	0.6	-	µs
START condition setup time (repeat)	$t_{SU,STA}$		4.7	-	0.6	-	µs
SDA hold time from SCL falling - All except NACK read - NACK read only	$t_{HD,DAT}$		0 2/CLK	-	0 2/CLK	-	µs s
SDA setup time from SCL rising	$t_{SU,DAT}$		250	-	100	-	ns
Rise time of SDA and SCL	t_r		-	1000		300	ns
Fall time of SDA and SCL	t_f		-	300		300	ns
STOP condition setup time	$t_{SU,STO}$		4	-	0.6	-	µs
Bus free time between transmissions	t_{BUF}		4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b		-	400	-	400	pF

The I2C master clock is affected by the clock gearing. If the auto clock gearing lowers CLK by too much it can cause I2C transactions to fail. See Register 29: GPIO Inversion & Automatic Clock Gearing (0x1D) for clock gearing options.

CLK Requirement	t(SCL high) >=10*t(Clock Gear(CLK)) t(SCL low) >=10*t(Clock Gear(CLK))

The system must ensure this condition can still be met when enabling automatic clock gearing. If the criterion cannot be met for all clock gear settings, then the clock gearing must be limited using Register 29: GPIO Inversion & Automatic Clock Gearing (0x1D).

XIN/MCLK Timing

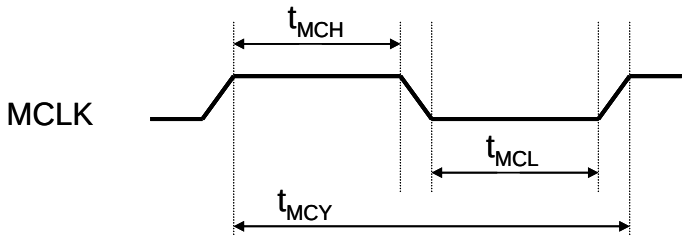
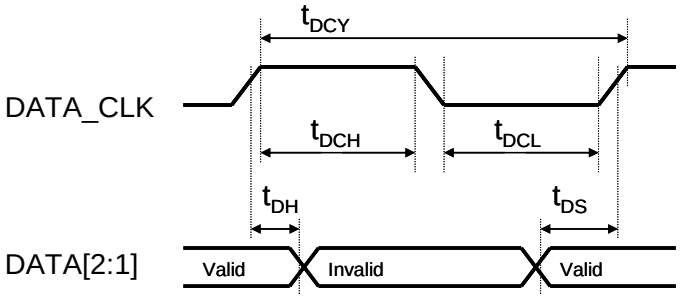


Figure 8. Clock Timing

Parameter	Symbol	Min	Max	Unit
MCLK pulse width high	T_{MCH}	9.0	90	ns
MCLK pulse width low	T_{MCL}	9.0	90	ns
MCLK cycle time	T_{MCY}	20	200	ns
MCLK duty cycle		45:55	55:45	

$$5MHz \leq MCLK \leq 50MHz$$

Audio Interface Timing



Parameter	Symbol	Min	Max	Unit
DATA_CLK pulse width high	t_{DCH}	9.0		ns
DATA_CLK pulse width low	t_{DCL}	9.0		ns
DATA_CLK cycle time	t_{DCY}	20		ns
DATA_CLK duty cycle		45:55	55:45	
DATA set-up time to DATA_CLK rising edge	t_{DS}	4.1		ns
DATA hold time to DATA_CLK rising edge	t_{DH}	2		ns

Figure 9. Audio Interface Timing

Notes:

- Audio data on DATA[2:1] are sampled at the rising edges of DATA_CLK and must satisfy the setup and hold time requirements relative to the rising edge of DATA_CLK
- For DSD Phase mode, the normal data (D0, D1, D2) must satisfy the setup and hold time requirements relative to the rising edge of DATA_CLK. The complimentary data (D0, D1, etc.) will be ignored.

Recommended Power-up Sequence

External Powered Oscillator / MCLK

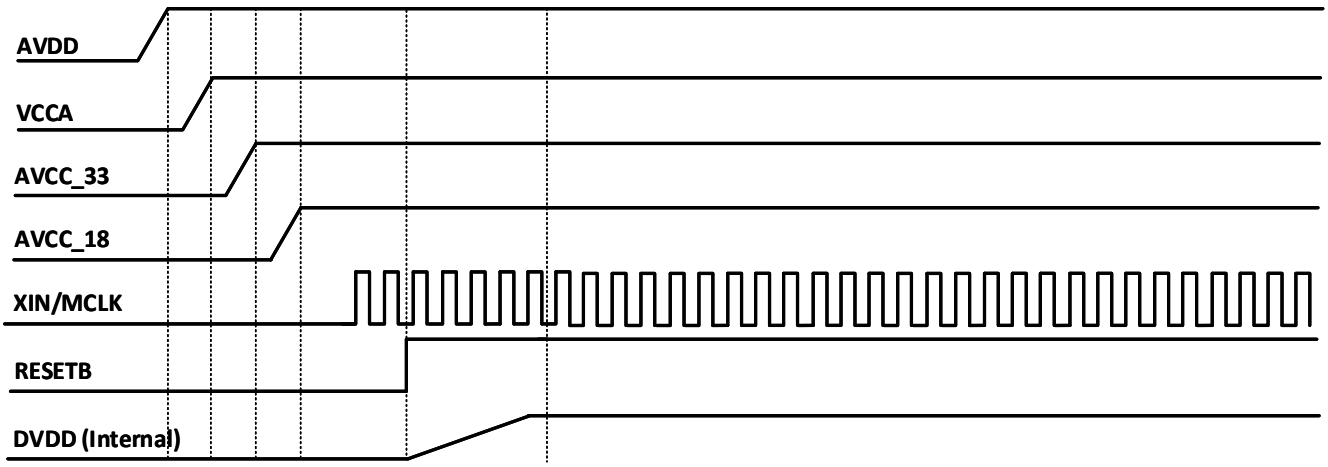


Figure 10. Using external powered oscillator

Crystal

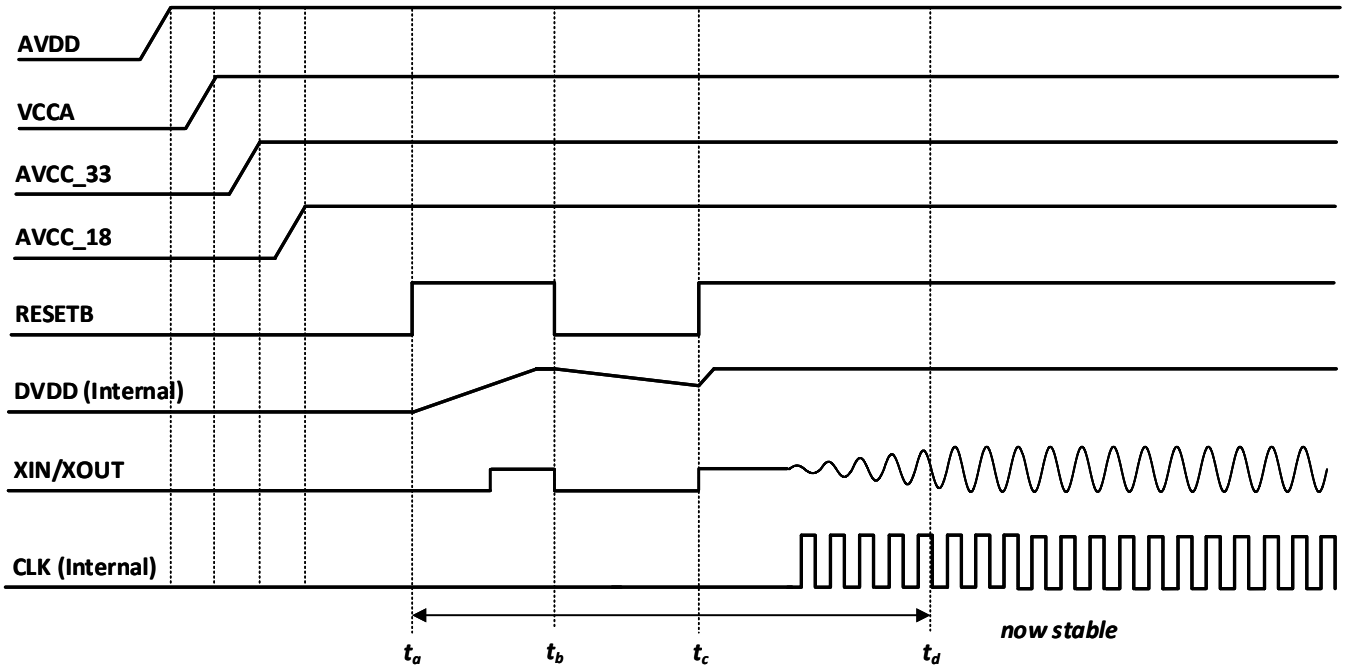


Figure 11. Crystal with internal oscillator

When a crystal is used with internal DVDD, it is possible for core timing requirements to be violated during chip startup. The following measures should be taken to ensure default register values are loaded correctly:

1. Use a small decoupling capacitor at the DVDD pin. 1µF maximum is recommended.
2. Consult the crystal vendor to optimize crystal circuitry. The chip has a 2-stage reset pipeline. If the oscillator starts slowly for any reason, more than two runt-pulses may occur and the reset pipeline will not be sufficient to prevent invalid core timing.

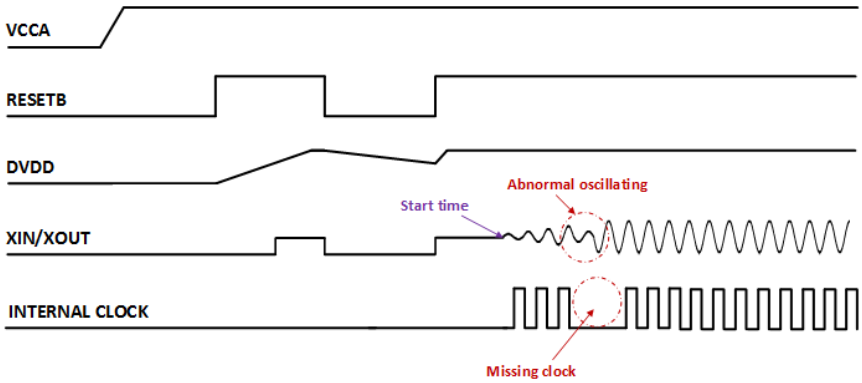


Figure 12. Non-optimal crystal circuitry

3. Perform two hardware resets (RESETB is de-asserted), followed by a software reset.
   For a 1µF DVDD de-coupling capacitor:

$$70\mu s \leq t_b - t_a \leq 100\mu s$$

$$50\mu s \leq t_c - t_b \leq 150\mu s$$ DVDD should not fall below 1V during $t_c - t_b$.

$$t_d - t_a \approx 1.5ms$$

Device Register Map

Address (Hex)	Register	7	6	5	4	3	2	1	0
Read/Write									
0x00	SYSTEM REGISTERS	OSC_DRV				CLK_GEAR		RESERVED	SOFT_RESET
0x01	INPUT SELECTION	SERIAL_LENGTH		SERIAL_MODE		AUTO_SELECT		INPUT_SELECT	
0x02	MIXING & AUTOMUTE CONFIGURATION	AUTOMUTE_CONFIG		ANALOG_ AUTOMUTE	AUTOMUTE_ TIMER_FAST	CH2_MIX_SEL		CH1_MIX_SEL	
0x03	ANALOG VOLUME CONTROL	RESERVED			ANALOG_VOLUME				
0x04	AUTOMUTE _TIME	AUTOMUTE_TIME							
0x05	AUTOMUTE _LEVEL	RESERVED	AUTOMUTE_LEVEL						
0x06	DoP, & VOLUME RAMP RATE	RESERVED				DoP_ENABLE	VOLUME_RATE		
0x07	FILTER BANDWIDTH & SYSTEM MUTE	FILTER_SHAPE			RESERVED	BYPASS _OSF	RESERVED		MUTE
0x08	GPIO1-2 CONFIGURATION	GPIO2_CONFIG				GPIO1_CONFIG			
0x0A	MASTER MODE & SYNC CONFIGURATION	MASTER_ _MODE	MASTER_DIV		128FS_ MODE	LOCK_SPEED			
0x0B	OVERCURRENT PROTECTION	OC_SD_EN	OC_SD_GAIN			RESERVED			
0x0C	ASRC/DPLL BANDWIDTH	DPLL_BW_SERIAL				DPLL_BW_DSD			
0x0D	THD COMPENSATION BYPASS	RESERVED	BYPASS_ THD	RESERVED	MONO_ MODE	RESERVED			
0x0E	SOFT START CONFIGURATION	RESERVED			SOFT_START_TIME				
0x0F	VOLUME CONTROL	VOLUME1							
0x10		VOLUME2							
0x11	MASTER TRIM	MASTER_TRIM							
0x12									
0x13									
0x14									
0x15	GPIO INPUT SELECTION	GPIO_SEL2		GPIO_SEL1		RESERVED			
0x16	THD COMPENSATION C2	THD_COMP_C2							
0x17									
0x18	THD COMPENSATION C3	THD_COMP_C3							
0x19									
0x1A	CHARGE PUMP SOFT START DELAY	CP_SS_DELAY							
0x1B	GENERAL CONFIGURATION	ASRC_EN	RESERVED			CH1_ VOLUME	RESERVED		
0x1D	GPIO INVERSION & AUTO CLOCK GEAR	INVERT_GPIO		RESERVED			AUTO_CLK_ GEAR	MAX_CLK_GEAR	
0x1E	CHARGE PUMP CLOCK	CP_CLK_SEL		CP_CLK_EN		CP_CLK_DIV			
0x1F		CP_CLK_DIV							
0x20	AMPLIFIER CONFIGURATION	RESERVED			AMP_MODE_GPIO		RESERVED	AMP_MODE_DEFAULT	
0x22	PROGRAMMABLE NCO	NCO_NUM							
0x23									
0x24									
0x25									
0x28	PROGRAMMABLE FIR RAM ADDRESS	PROG_COEF_ STAGE	PROG_COEFF_ADDRESS						
0x29	PROGRAMMABLE FIR RAM DATA	PROG_COEFF_DATA							
0x2A									
0x2B									
0x2C	PROGRAMMABLE FIR CONFIGURATION	RESERVED					STAGE2_ EVEN	PROG_ COEFF_WE	PROG_ COEFF_EN
0x31		CLK_GEAR_MIN_THRESH							
0x32		CLK_GEAR_MAX_THRES				CLK_GEAR_MAX_THRES			
0x33		CLK_GEAR_MAX_THRESH							
Read only									
0x40	CHIP_ID							AUTOMUTE_ STATUS	LOCK_ STATUS
0x41	GPIO READBACK	RESERVED				CLK_GEAR_RB		GPIO2	GPIO1
0x42	DPLL NUMBER	DPLL_NUM							

0x43							
0x44							
0x45							
0x48	INPUT SELECTION & AUTOMUTE STATUS	OC_SD_MUTE	AM2, AM1	DoP_STATUS	RESERVED	I2S_ SELECT	DSD_ SELECT
0x49	RAM COEFFICIENT READBACK	PROG_COEFF_OUT					
0x4A							
0x4B							

Table 1. Register Map

Register Settings

Read-Write Registers

Registers 0 - 60 (0x00 - 0x3C) are read-write registers.

Register 0: System Registers (0x00)

Bits	[7:4]	[3:2]	[1]	[0]
Mnemonic	osc_drv	clk_gear	reserved	soft_reset
Default	4'b0000	2'b00	1'b0	1'b0

Bit	Mnemonic	Description
[7:4]	osc_drv	Oscillator drive specifies the bias current to the oscillator pad. • 4'b0000: full bias (default) • 4'b1000: ¾ bias • 4'b1100: ½ bias • 4'b1110: ¼ bias • 4'b1111: shut down the oscillator
[3:2]	clk_gear	Configures a clock divider network that can reduce the power consumption of the chip by reducing the clock frequency supplied to both the digital core and analog stages. • 2'b00: uses CLK = XI(MCLK) (default) • 2'b01: divides CLK = XI(MCLK) by 2 • 2'b10: divides CLK = XI(MCLK) by 4 • 2'b11: divides CLK = XI(MCLK) by 8
[1]	reserved	
[0]	soft_reset	Software configurable hardware reset with the ability to reset the design to its initial power-on configuration. • 1'b0: normal operation (default) • 1'b1: resets the ES9218P to its power-on defaults Note: This register will always read as "1'b0" as the power-on default for this register is "1'b0". A reset can be verified by checking the status of other modified registers.

Register 1: Input selection (0x01)

Bits	[7:6]	[5:4]	[3:2]	[1:0]
Mnemonic	serial_length	serial_mode	auto_select	input_select
Default	2'b10	2'b00	2'b11	2'b00

Bit	Mnemonic	Description
[7:6]	serial_length	Selects how many DATA_CLK pulses exist per data word. • 2'b00: 16-bit data words • 2'b01: 24-bit data words • 2'b10: 32-bit data words (default) • 2'b11: 32-bit data words
[5:4]	serial_mode	Configures the type of serial data. • 2'b00: I2S mode (default) • 2'b01: left-justified mode • 2'b11 or 2'b10: right-justified mode
[3:2]	auto_select	Allows the ES9218P to automatically select between either serial (I2S), or DSD input formats. • 2'b00: disable automatic input decoder and instead use the information provided by register 1[1:0] • 2'b01: automatically select between DSD or serial data • 2'b10: reserved • 2'b11: automatically select between DSD or serial (I2S) data (default)
[1:0]	input_select	Configures the ES9218P to use a particular input decoder if auto_select is disabled. • 2'b00: serial (default) • 2'b01: DSD • 2'b10: auto select • 2'b11: auto select Note: Register 1[3:2] must be set to 2'b00 for input_select to function.

Register 2: Mixing, Serial Data and Automute Configuration (0x02)

Bits	[7:6]	[5]	[4]	[3:2]	[1:0]
Mnemonic	automute_config	analog_automute	automute_timer_fast	ch2_mix_sel	ch1_mix_sel
Default	2'b00	1'b1	1'b1	2'b01	2'b00

Bit	Mnemonic	Description
[7:6]	automute config	Configures the automute state machine, which allows the ES9218P to perform different power saving and sound optimizations. • 2'b00: normal operation (default) • 2'b01: perform a mute when an automute condition is asserted • 2'b10: ramp all channels to ground when an automute condition is asserted • 2'b11: perform a mute and then ramp all channels to ground when an automute condition is asserted Note: Ramping the internal DAC outputs to ground can reduce the power consumption of the ES9218P in some situations. Note: The ramp speed can be changed by using the automute_time, volume_rate and soft_start_rate registers.
[5]	analog_automute	Allows the analog volume control to be driven to -24dB of full scale when an automute condition occurs. • 1'b0: analog volume control is left 'as programmed' when an automute occurs • 1'b1: analog volume control is pushed to -24dB when an automute occurs
[4]	automute_timer_fast	If disabled, the automute time is multiplied by 8, resulting in a longer delay before an automute event is triggered. • 1'b0: automute time is calculated by the regular formula (see Register 4: Automute Time (0x04)) multiplied by 8 • 1'b1: automute time is calculated by the regular formula (default)
[3:2]	ch2_mix_sel	Selects which data is mapped to DAC Right (OUT_R) • 2'b00: ch1 • 2'b01: ch2 (default) • 2'b10: reserved • 2'b11: reserved
[1:0]	ch1_mix_sel	Selects which data is mapped to DAC Left (OUT_L) • 2'b00: ch1 (default) • 2'b01: ch2 • 2'b10: reserved • 2'b11: reserved

Register 3: Analog Volume Control (0x03)

Bits	[7:5]	[4:0]
Mnemonic	reserved	analog_volume
Default	3'd2	5'd24

Bit	Mnemonic	Description
[7:5]	reserved	
[4:0]	analog_volume	This register controls the analog volume which ranges from 0dB to -24dB and transitions in 1dB steps. This register is only valid from 5'd0 to 5'd24. See Analog Volume Control.

Register 4: Automute Time (0x04)

Bits	[7:0]
Mnemonic	automute_time
Default	8'd0

Bit	Mnemonic	Description
[7:0]	automute_time	Configures the amount of time the audio data must remain below the automute_level before an automute condition is flagged. Defaults to 0 which disables automute. $\text{Time in seconds} = \frac{2096896}{DATA\_CLK * automute\_time}$ DATA_CLK should be provided with a unit of Hz

Register 5: Automute Level (0x05)

Bits	[7]	[6:0]
Mnemonic	reserved	automute_level
Default	1'b0	7'd104

Bit	Mnemonic	Description
[7]	reserved	
[6:0]	automute_level	Configures the threshold which the audio must be below before an automute condition is flagged. The level is measured in decibels (dB) and defaults to -104dB. This register works in tandem with Register 4: Automute Time (0x04) to create the automute condition. See Automute for more details.

Register 6: DoP and Volume Ramp Rate (0x06)

Bits	[7:4]	[3]	[2:0]
Mnemonic	reserved	dop_enable	volume_rate
Default	4'b0111	1'b0	3'b010

Bit	Mnemonic	Description
[7:4]	reserved	
[3]	dop_enable	Selects whether the DSD over PCM (DoP) logic is enabled. • 1'b0: disables the DoP logic (default) • 1'b1: enables the DoP logic
[2:0]	volume_rate	Selects a volume ramp rate to use when transitioning between different volume levels. The volume ramp rate is measured in decibels per second (dB/s). $$\text{rate} = \frac{2^{\text{vol\_rate}} * \text{FS}}{512} \text{ dB/s}$$ ***For DoP support, please contact your local FAE.***

Register 7: Filter Bandwidth and System Mute (0x07)

Bits	[7:5]	[4]	[3]	[2:1]	[0]
Mnemonic	filter_shape	reserved	bypass_osf	reserved	mute
Default	3'b100	1'b0	1'b0	2'b00	1'b0

Bit	Mnemonic	Description
[7:5]	filter_shape	Selects the type of filter to use during the 8x FIR interpolation phase. • 3'b000: linear phase fast roll-off filter • 3'b001: linear phase slow roll-off filter • 3'b010: minimum phase fast roll-off filter • 3'b011: minimum phase slow roll-off filter • 3'b100: apodizing fast roll-off filter type 1 (default) • 3'b101: apodizing fast roll-off filter type 2 • 3'b110: hybrid fast roll-off filter • 3'b111: brick wall filter
[4]	reserved	
[3]	bypass_osf	Allows the use of an external 8x upsampling filter, bypassing the internal interpolating FIR filter. • 1'b0: uses the built-in oversampling filter (default) • 1'b1: uses an external upsampling filter, which requires data oversampled by 8x externally
[2:1]	reserved	
[0]	mute	Mutes all 2 channels of the ES9218P. • 1'b0: normal operation (default) • 1'b1: mute both channels

Register 8: GPIO1-2 Configuration (0x08)

Bits	[7:4]	[3:0]
Mnemonic	gpio2_cfg	gpio1_cfg
Default	4'd13	4'd13

Bit	Mnemonic	Description
[7:4]	gpio2_cfg	GPIO 2 configuration bits, value is 4'd0 – 4'd15 • 4'd13: shutdown (default) See GPIO Modes for all configuration options
[3:0]	gpio1_cfg	GPIO 1 configuration bits, value is 4'd0 – 4'd15 • 4'd13: shutdown (default) See GPIO Modes for all configuration options

GPIO Modes

The following table describes the supported values for gpio1_cfg or gpio2_cfg and their function.

gpioX_cfg	Name	I/O Direction	Details
4'd0	Automute Status	Output	Output is high when an automute has been triggered. This signal is analogous to Register 64 (Read-Only): Chip Status (0x40) *automute_status*.
4'd1	Lock Status	Output	Output is high when lock is triggered. This signal is analogous to Register 64 (Read-Only): Chip Status (0x40) *lock_status*.
4'd2	Volume Min	Output	Output is high when all digital volume controls have been ramped to minus full scale. This can occur, for example, if automute is enabled and set to mute the volume.
4'd3	CLK	Output	Output is a buffered CLK signal which can be used to synchronize other devices.
4'd4	Interrupt	Output	Output is high for a variety of interrupts: • Register 64 (Read-Only): Chip Status (0x40) *lock_status* or *automute_status* have changed. Clear by reading register 64. • Any bit in Register 65 (Read-Only): GPIO Readback (0x41) *ocbr* or *ocbl* has gone high. Clear by reading register 65. • Any bit in Register 72 (Read-Only): Input Selection and Automute Status (0x48) *oc_sd_mute* has gone high. Clear by disabling overcurrent protection with Register 11: Overcurrent Protection (0x0B) *oc_sd_en*. See Register 33: Interrupt Mask (0x21) for details on masking these interrupts.
4'd5	Reserved		
4'd6	Reserved		
4'd7	Output 1'b0	Output	Output is forced low.
4'd8	Standard Input	Input	Places the GPIO into a high impedance state, allowing the customer to provide a digital signal and then read that signal back via the I2C from Register 65 (Read-Only): GPIO Readback (0x41).
4'd9	Input Select	Input	Places the GPIO into a high impedance state and allows the customer to toggle the input selection between two modes using either GPIO pin. See Register 21: GPIO Input Selection (0x15) for more information.
4'd10	Mute All	Input	Places the GPIO into a high impedance state. A mute condition can be forced by applying a logic high signal to the GPIO. The mute condition can be reset but applying a logic low signal to the GPIO. This will not reset mute conditions caused by an automute.
4'd11	Amp Mode Select	Input	Activates the amplifier mode set in Register 32: Amplifier Configuration (0x20) when the GPIO is pulled up. This option is only available for GPIO1.
4'd12	Reserved		
4'd13	Shut Down	Input	Shutdown GPIO.
4'd14	Soft Start Complete	Output	Output is high when the DAC output is ramped to ground. The DAC can be ramped to ground via an automute condition when appropriately programmed (see Automute), or via Register 14: Soft Start Configuration (0x0E).
4'd15	Output 1'b1	Output	Output is forced high.

Register 9: Reserved (0x09)

Bits	[7:0]
Mnemonic	reserved
Default	8'd24

Register 10: Master Mode and Sync Configuration (0x0A)

Bits	[7]	[6:5]	[4]	[3:0]
Mnemonic	master_mode	master_div	128fs_mode	lock_speed
Default	1'b0	2'b00	1'b0	4'd2

Bit	Mnemonic	Description
[7]	master_mode	Enables master mode which causes the ES9218P to drive the DATA_CLK and DATA1 signals when in I2S mode. Can also be enabled when in DSD mode to enable DATA_CLK only. • 1'b0: disables master mode (default) • 1'b1: enables master mode
[6:5]	master_div	Sets the frame clock (DATA1) and DATA_CLK frequencies when in master mode. This register is used when in normal synchronous operation. • 2'b00: DATA_CLK frequency = CLK/2 (default) • 2'b01: DATA_CLK frequency = CLK/4 • 2'b10: DATA_CLK frequency = CLK/8 • 2'b11: DATA_CLK frequency = CLK/16 See Master Mode for more details.
[4]	128fs_mode	Disable ASRC and enables synchronous operation: • 1'b0: disables CLK = 128*FSR mode (default) • 1'b1: enables CLK = 128*FSR mode DATA_CLK and CLK must be synchronous and the audio sample rate must be exactly 128*FSR: $\frac{CLK}{FSR} = 128$
[3:0]	lock_speed	Sets the number of audio samples required before the DPLL and ASRC lock to the incoming signal during asynchronous operation. More audio samples give a better initial estimate of the CLK/FSR ratio at the expense of a longer locking interval. • 4'd0: 16384 FS edges • 4'd1: 8192 FS edges • 4'd2: 5461 FS edges (default) • 4'd3: 4096 FS edges • 4'd4: 3276 FS edges • 4'd5: 2730 FS edges • 4'd6: 2340 FS edges • 4'd7: 2048 FS edges • 4'd8: 1820 FS edges • 4'd9: 1638 FS edges • 4'd10: 1489 FS edges • 4'd11: 1365 FS edges • 4'd12: 1260 FS edges • 4'd13: 1170 FS edges • 4'd14: 1092 FS edges • 4'd15: 1024 FS edges

Register 11: Overcurrent Protection (0x0B)

Bits	[7]	[6:4]	[3:0]
Mnemonic	oc_sd_en	oc_sd_gain	reserved
Default	1'b0	3'b000	4'd0

Bit	Mnemonic	Description
[7]	oc_sd_en	Enable an automatic detection circuit to mute the DAC when an overcurrent event is detected. • 1'b0: automatic overcurrent shutdown is disabled (default) • 1'b1: automatic overcurrent shutdown is enabled and will mute the DAC if an overcurrent threshold is crossed and the timeout period expires.
[6:4]	oc_sd_gain	The value added to the OCP timeout counter for each CLK cycle that an overcurrent condition is sensed at the amplifier output. Exact timeout duration is both CLK dependent and signal dependent. Counter is only incremented by this amount once per CLK cycle if the signal exceeds the built-in amplifier output current limit. • 3'd0: A timeout will never occur. Automatic overcurrent shutdown is disabled (default) • 3'd1-3'd7: OCP timeout counter incremental value. Higher values will yield a shorter timeout.
[3:0]	reserved	

See Overcurrent Protection

Register 12: ASRC/DPLL Bandwidth (0x0C)

Bits	[7:4]	[3:0]
Mnemonic	dpll_bw_serial	dpll_bw_dsd
Default	4'd5	4'd10

Bit	Mnemonic	Description
[7:4]	dpll_bw_serial	Sets the bandwidth of the DPLL when operating in I2S/DoP mode. • 4'd0: DPLL Off • 4'd1: Lowest Bandwidth • 4'd2: • 4'd3: • 4'd4: • 4'd5: (default) • 4'd6: • 4'd7: • 4'd8: • 4'd9: • 4'd10: • 4'd11: • 4'd12: • 4'd13: • 4'd14: • 4'd15: Highest Bandwidth
[3:0]	dpll_bw_dsd	Sets the bandwidth of the DPLL when operating in DSD mode. • 4'd0: DPLL Off • 4'd1: Lowest Bandwidth • 4'd2: • 4'd3: • 4'd4: • 4'd5: • 4'd6: • 4'd7: • 4'd8: • 4'd9: • 4'd10: (default) • 4'd11: • 4'd12: • 4'd13: • 4'd14: • 4'd15: Highest Bandwidth

Register 13: THD Compensation Bypass & Mono Mode (0x0D)

Bits	[7]	[6]	[5]	[4]	[3:0]
Mnemonic	reserved	bypass_thd	reserved	mono_mode	reserved
Default	1'b0	1'b1	1'b0	1'b0	4'b0000

Bit	Mnemonic	Description
[7]	reserved	
[6]	bypass_thd	Selects whether to disable the THD compensation logic. THD compensation is disabled by default and can be configured to correct for second and third harmonic distortion. • 1'b0: enable THD compensation • 1'b1: disable THD compensation (default)
[5]	reserved	
[4]	mono_mode	Selects whether mono mode is enabled. Mono mode disables the channel 2 datapath and routes channel 1 to both outputs. This mode will consume less power as nearly half of the datapath is disabled. • 1'b0: disable mono mode (default) • 1'b1: enable mono mode
[3:0]	reserved	

Register 14: Soft Start Configuration (0x0E)

Bits	[7]	[6]	[5]	[4:0]
Mnemonic	soft_start	reserved	soft_start_type	soft_start_time
Default	1'b0	1'b0	1'b0	5'd10

Bit	Mnemonic	Description
[7]	soft_start	Controls the soft start/ramp to ground action. Only functions when the *dig_over_en* bit is set in Register 46: Analog Control Override (0x2E). • 1'b0 Ramps the DAC outputs to ground (default) • 1'b1 Ramps the DAC outputs to AVCC_DAC/2
[6]	reserved	
[5]	soft_start_type	Sets whether the soft start ramp is linear or a quadratic function. • 1'b0: uses the standard soft start ramp (default) • 1'b1: uses a quadratic function for the soft start ramp
[4:0]	soft start time	Sets the amount of time that it takes to perform a DAC soft start ramp. This time affects both ramp ***down*** to ground and ramp ***up*** to mute (AVCC_DAC/2). Values from 0 to 20 are valid. $$\text{time (s)} = 4096 * \frac{2^{(\text{soft\_start\_time}+1)}}{\text{CLK (Hz)}}$$

Register 15-16: Volume Control (0x0F & 0x10)

Bits	[7:0]
Register 15	volume1
Register 16	volume2
Default	8'd80

Bit	Mnemonic	Description
[7:0]	volume1	Volume level setting for Ch1. Default of 8'd80 (-40dB) -0dB to -127.5dB with 0.5dB steps
[7:0]	volume2	Volume level setting for Ch2. Default of 8'd80 (-40dB) -0dB to -127.5dB with 0.5dB steps

Register 17-20: Master Trim (0x11 - 0x14)

Bits	[31:0]
Mnemonic	master_trim
Default	32'h7fffffff

Bit	Mnemonic	Description
[31:0]	master_trim	A 32 bit signed value that sets the 0dB level for all volume controls. Defaults to full-scale (32'h7FFFFFFF).

See Master Trim for more details.

Register 21: GPIO Input Selection (0x15)

Bits	[7:6]	[5:4]	[3:0]
Mnemonic	gpio_sel2	gpio_sel1	reserved
Default	2'b00	2'b00	4'b1101

Bit	Mnemonic	Description
[7:6]	gpio_sel2	Selects which input type will be selected when GPIO# = 1'b1. • 2'd0: serial data (I2S/LJ) (default) • 2'd3: DSD data GPIO needs to be configured as "input select". See Register 8: GPIO1-2 Configuration (0x08).
[5:4]	gpio_sel1	Selects which input type will be selected when GPIO# = 1'b0. • 2'd0: serial data (I2S/LJ) (default) • 2'd3: DSD data GPIO needs to be configured as "input select". See Register 8: GPIO1-2 Configuration (0x08).
[3:0]	reserved	

Note: If both GPIO pins are configured as 4'd9 (Input Select), GPIO1 will have precedence for the input type.

Register 22-23: THD Compensation C2 (0x16 - 0x17)

Bits	[15:0]
Mnemonic	thd_comp_c2
Default	16'd0

Bit	Mnemonic	Description
[15:0]	thd_comp_c2	A 16-bit signed coefficient for correcting for the second harmonic distortion. Defaults to 16'd0.

See THD Compensation for more details.

Register 24-25: THD Compensation C3 (0x18 - 0x19)

Bits	[15:0]
Mnemonic	thd_comp_c3
Default	16'd0

Bit	Mnemonic	Description
[15:0]	thd_comp_c3	A 16-bit signed coefficient for correcting for the third harmonic distortion. Defaults to 16'd0.

See THD Compensation for more details.

Register 26: Charge Pump Soft Start Delay (0x1A)

Bits	[7:0]
Mnemonic	cp_ss_delay
Default	8'd98

Bit	Mnemonic	Description
[7:0]	cp_ss_delay	Configures the delay between the weak charge pump enable and the strong charge pump enable. This delay is to limit the inrush currents of the strong charge pump when powering up. This relationship is not exact because chargepump clock frequency is not guaranteed to be exactly equal to XI(MCLK). It is automatically adjusted to undo the effects of clock gearing. The result is that the chargepump clock rate remains constant with respect to XI(MCLK) even when CLK changes but only to within the truncation error of the chargepump clock divider. $$\text{delay(s)} \approx \frac{256 * \text{cp\_ss\_delay}}{f_{MCLK}}$$ Example: For the default register setting if XI(MCLK) = 25MHz, delay ≈ 1ms. See System Clock XI(MCLK) for the relationship between XI(MCLK) and CLK.

Register 27: General Configuration (0x1B)

Bits	[7]	[6-4]	[3]	[2-0]
Mnemonic	asrc_en	reserved	ch1_volume	reserved
Default	1'b1	3'b101	1'b0	3'b100

Bit	Mnemonic	Description
[7]	asrc_en	Selects whether the ASRC is enabled. Allows for the ASRC to be disabled if the ES9218P is in Master mode or using a synchronous MCLK. • 1'b0: ASRC is disabled • 1'b1: ASRC is used as normal, providing a first order correction on the sample rate converted data (default)
[6:4]	reserved	
[3]	ch1_volume	Allows channel 2 to share the channel 1 volume control. This allows for perfectly syncing up the two channel gains. • 1'b0: allow independent control of both channel 1 and channel volume controls (default) • 1'b1: use the channel 1 volume control for both channel 1 and channel 2
[2:0]	reserved	

Register 28: Reserved (0x1C)

Bits	[7:0]
Mnemonic	reserved
Default	8'd240

Register 29: GPIO Inversion & Automatic Clock Gearing (0x1D)

Bits	[7:6]	[5:3]	[2]	[1:0]
Mnemonic	invert_gpio	reserved	auto_clk_gear	max_clk_gear
Default	2'b00	3'b000	1'b0	2'b00

Bit	Mnemonic	Description
[7:6]	invert_gpio	Allows each GPIO output to be inverted independently. • 2'b00: normal GPIO operation (default) • 2'b01: invert GPIO1 output only • 2'b10: invert GPIO2 output only • 2'b11: invert both GPIO outputs
[5:3]	reserved	
[2]	auto_clk_gear	Decrease/increase the system clock by automatically adjusting the clock gear setting when the clocking requirements reach a programmable threshold. This saves power when running at lower sample rates. • 1'b0: automatic clock gearing is disabled (default) • 1'b1: automatic clock gearing is enabled See Register 49-51: Automatic Clock Gearing Thresholds (0x31 – 0x33) for threshold setting.
[1:0]	max_clk_gear	Sets the maximum allowed divisor (/1, /2, /4, /8) of the system clock that the automatic clock gearing circuitry can implement. This is useful when running at slow clock rates where a clock gear could slow the CLK down below the I2C programming constraints. • 2'b00: sets MCLK/1 as the maximum clock gearing ratio (effectively disabling the automatic clock gearing) (default) • 2'b01: sets MCLK/2 as the maximum clock gearing ratio • 2'b10: sets MCLK/4 as the maximum clock gearing ratio • 2'b11: sets MCLK/8 as the maximum clock gearing ratio See Serial Control Interface for I2C clock requirements.

Register 30-31: Charge Pump Clock (0x1E & 0x1F)

Bits	[15:14]	[13:12]	[11:0]
Mnemonic	cp_clk_sel	cp_clk_en	cp_clk_div
Default	2'b00	2'b00	12'd0

Bit	Mnemonic	Description
[15:14]	cp_clk_sel	Selects which clock will be used as the reference clock for the charge pump (CP) clock. • 2'b00: use CLK as the CP reference clock (default) • 2'b01: use 128*fs as the CP reference clock • 2'b10: use 64*fs as the CP reference clock • 2'b11: use 1*fs as the CP reference clock The chargepump clock frequency is not guaranteed to be exactly equal to XI(MCLK). The *cp_clk_div* setting is automatically adjusted to undo the effects of clock gearing. The result is that the chargepump rate remains constant with respect to XI(MCLK) even when CLK changes but only to within the truncation error of the chargepump clock divider. See System Clock XI(MCLK) for the relationship between XI(MCLK) and CLK.
[13:12]	cp_clk_en	Sets the state of the charge pump clock. • 2'b00: tristate output (default, use internal CP oscillator) • 2'b01: tied to GND • 2'b10: tied to DVDD • 2'b11: cp_clk_sel / cp_clk_div Note: Set cp_clk_div before setting cp_clk_en to 2'b11.
[11:0]	cp_clk_div	Sets the divider ratio for the charge pump clock. f_{CLK} is the frequency of the clock selected by cp_clk_sel. $$f_{CP} = \frac{f_{CLK}}{cp\_clk\_div * 2}$$

Register 32: Amplifier Configuration (0x20)

Bits	[7:5]	[4:3]	[2]	[1:0]
Mnemonic	reserved	amp_mode_gpio	reserved	amp_mode
Default	3'b000	2'b00	1'b0	2'b00

Bit	Mnemonic	Description
[7:5]	reserved	
[4:3]	amp_mode_gpio	Configures the amplifier mode based on GPIO input: • 3'd0: core on (default) • 3'd1: LowFi • 3'd2: HiFi 1VRMS • 3'd3: HiFi 2VRMS GPIO1 pin must be high and Register 8: GPIO1-2 Configuration (0x08) must be configured to Amp Mode Select (4'd11). This option is only available for GPIO1. When configured this way: • GPIO1 HIGH activates the amplifier mode *amp_mode_gpio* • GPIO1 LOW activates the amplifier mode *amp_mode_default*
[2]	reserved	
[1:0]	amp_mode	Configures the amplifier mode • 3'd0: core on (default) • 3'd1: LowFi • 3'd2: HiFi 1VRMS • 3'd3: HiFi 2VRMS

Register 33: Interrupt Mask (0x21)

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	ocr_sd_m	ocl_sd_m	ocr_pos_m	ocl_pos_m	ocr_neg_m	ocr_neg_m	automute_status_m	lock_status_m
Default	1'b0	1'b0	1'b1	1'b1	1'b1	1'b1	1'b0	1'b0

Bit	Mnemonic	Description
[7]	ocr_sd_m	Interrupt mask for *ocr_sd_mute* Register 72 (Read-Only): Input Selection and Automute Status (0x48). • 1'b0: *ocr_sd_mute* bit will not flag an interrupt. (default) • 1'b1: *ocr_sd_mute* bit will flag an interrupt. Clear this interrupt by toggling overcurrent protection disabled-enabled with *oc_sd_en* Register 11: Overcurrent Protection (0x0B).
[6]	ocl_sd_m	Interrupt mask for *ocl_sd_mute* Register 72 (Read-Only): Input Selection and Automute Status (0x48). • 1'b0: *ocl_sd_mute* bit will not flag an interrupt. (default) • 1'b1: *ocl_sd_mute* bit will flag an interrupt Clear this interrupt by toggling overcurrent protection disabled-enabled with *oc_sd_en* Register 11: Overcurrent Protection (0x0B).
[5]	ocr_pos_m	Interrupt mask for *ocbr_pos* Register 65 (Read-Only): GPIO Readback (0x41). • 1'b0: *ocbr_pos* bit will not flag an interrupt • 1b'1: *ocbr_pos* bit will flag an interrupt (default) Clear this interrupt by reading Register 65 (Read-Only): GPIO Readback (0x41).
[4]	ocl_pos_m	Interrupt mask for *ocbl_pos* Register 65 (Read-Only): GPIO Readback (0x41) • 1'b0: *ocbl_pos* bit will not flag an interrupt • 1b'1: *ocbl_pos* bit will flag an interrupt (default) Clear this interrupt by reading Register 65 (Read-Only): GPIO Readback (0x41).
[3]	ocr_neg_m	Interrupt mask for *ocbr_neg* Register 65 (Read-Only): GPIO Readback (0x41). • 1'b0: *ocbr_neg* bit will not flag an interrupt • 1b'1: *ocbr_neg bit will flag an interrupt* (default) Clear this interrupt by reading Register 65 (Read-Only): GPIO Readback (0x41).
[2]	ocl_neg_m	Interrupt mask for *ocbl_neg* Register 65 (Read-Only): GPIO Readback (0x41). • 1'b0: *ocbl_neg* bit will not flag an interrupt • 1b'1: *ocbl_neg* bit will flag an interrupt (default) Clear this interrupt by reading Register 65 (Read-Only): GPIO Readback (0x41).

[1]	automute_status_m	Interrupt mask for *automute_status* Register 64 (Read-Only): Chip Status (0x40). • 1'b0: *automute_status* will not flag an interrupt (default). • 1'b1: *automute_status* will flag an interrupt Clear this interrupt by reading Register 64 (Read-Only): Chip Status (0x40).
[0]	lock_status_m	Interrupt mask for *lock_status* Register 64 (Read-Only): Chip Status (0x40). • 1'b0: *lock_status* will not flag an interrupt (default) • 1'b1: *lock_status* will flag an interrupt Clear this interrupt by reading Register 64 (Read-Only): Chip Status (0x40).

See GPIO Modes to configure a GPIO pin to output these interrupts.

Register 34-37: Programmable NCO (0x22 - 0x25)

Bits	[31:0]
Mnemonic	nco_num
Default	32'd0

Bit	Mnemonic	Description
[31:0]	nco_num	The Numerically Controlled Oscillator (NCO) is an unsigned 32-bit quantity that defines the ratio between CLK and FSR. • 32'd0: disables NCO mode (default) • 32'd#: enables NCO mode The NCO number is related to FSR and CLK by the following equation: $$\text{FSR (raw sample rate)} = \frac{(\text{nco\_num} * \text{CLK})}{2^{32}}$$ This feature is most commonly used to generate arbitrary DATA_CLK frequencies in master mode. See Master Mode for more details. NCO mode also supports synchronous operation in slave mode with a programmable ***CLK***/FSR ratio as long as the following condition is true: $$\frac{\text{CLK}}{\text{FSR}} > 128$$ ***Contact your local FAE regarding DoP master mode support using NCO mode.***

Register 39: Reserved (0x27)

Bits	[7:0]
Mnemonic	reserved
Default	8'd204

Register 40: Programmable FIR RAM Address (0x28)

Bits	[7]	[6:0]
Mnemonic	prog_coeff_stage	prog_coeff_address
Default	1'b0	7'd0

Bit	Mnemonic	Description
[7]	prog_coeff_stage	Selects which stage of the filter to write. • 1'b0: selects stage 1 of the oversampling filter (default) • 1'b1: selects stage 2 of the oversampling filter
[6:0]	prog_coeff_address	Selects the coefficient address when writing custom coefficients for the oversampling filter.

See Programmable FIR filter for more information.

Register 41-43: Programmable FIR RAM Data (0x29 - 0x2B)

Bits	[23:0]
Mnemonic	prog_coeff_data
Default	24'd0

Bit	Mnemonic	Description
[23:0]	coeff_data	A 24bit signed filter coefficient that will be written to the address defined in *prog_coeff_addr*.

See Programmable FIR filter for more information.

Register 44: Programmable FIR Configuration (0x2C)

Bits	[7:3]	[2]	[1]	[0]
Mnemonic	reserved	stage2_even	prog_coeff_we	prog_coeff_en
Default	5'b00000	1'b0	1'b0	1'b0

Bit	Mnemonic	Description
[7:3]	reserved	
[2]	stage2_even	Selects the symmetry of the stage 2 oversampling filter. • 1'b0: uses a sine symmetric filter (27 coefficients) (default) • 1'b1: uses a cosine symmetric filter (28 coefficients)
[1]	prog_coeff_we	Enables writing to the programmable coefficient RAM. • 1'b0: disables write signal to the coefficient RAM (default) • 1'b1: enables write signal to the coefficient RAM
[0]	prog_coeff_en	Enables the custom oversampling filter coefficients. • 1'b0: uses a built-in filter selected by Register 7: Filter Bandwidth and System Mute (0x07) *filter_shape* (default) • 1'b1: uses the coefficients programmed via Register 41-43: Programmable FIR RAM Data (0x29 - 0x2B) *prog_coeff_data*

See Programmable FIR filter for more information.

Register 45: Analog Control Override (0x2D)

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	enaux	areg_pdb	enhpa	cph_ens	cph_enw	apdb	cp_clk_sel	reserved
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bit	Mnemonic	Description
[7]	enaux	Sets the state of the output switch when the digital core has taken control of the switch. The switch can be controlled by the digital by setting ENAUX_OE to 1'b1. • 1'b0: switch is disengaged, allowing the DAC and headphone amplifier to drive the output (default) • 1'b1: switch is engaged, allowing the auxiliary input to drive the output **Note**: The switch should not be engaged when the headphone amplifier is enabled.
[6]	areg_pdb	Enables the analog regulator, which uses the reference voltage enabled by the apdb signal. • 1'b0: analog regulator is disabled (default) • 1'b1: analog regulator is enabled. Note: apdb must be set to 1'b1 for the analog regulator to work correctly
[5]	enhpa	Enables the pre-amplifier for the headphone amplifier. • 1'b0: pre-amplifier is disabled (default) • 1'b1: pre-amplifier is enabled.
[4]	cph_ens	Enables the main charge pump and places it into strong mode. The main charge pump powers the output stage of the headphone amplifier. • 1'b0: main charge pump (strong mode) is disabled (default) • 1'b1: main charge pump (strong mode) is enabled • **Note**: encp_oe must be set to 1'b1 for the digital core to control the charge pump
[3]	cph_enw	Enables the main charge pump and places it into weak mode. The main charge pump powers the output stage of the headphone amplifier. • 1'b0: main charge pump is disabled (default) • 1'b1: main charge pump is enabled • **Note**: encp_oe must be set to 1'b1 for the digital core to control the charge pump
[2]	apdb	Enables the analog reference voltage, which is derived by a bandgap. • 1'b0: analog reference is disabled (default) • 1'b1: analog reference is enabled, which supplies a reference voltage for the analog regulator. This bit must be set prior to enabling the analog regulator (AREG_PDB)
[1]	cp_clk_sel	Disables the internal oscillator for the charge pump and uses a digitally generated clock signal instead. The digitally generated clock signal can be configured via register 30-31. • 1'b0: use the internal oscillator as the charge pump clock (default) • 1'b1: use the digitally generated clock as the charge pump clock
[0]	reserved	

Register 46: Analog Control Override (0x2E)

Bits	***[7]***	***[6:3]***	***[2]***	***[1]***	***[0]***
Mnemonic	dig_over_en	reserved	sel1v	shtoutb	shtinb
Default	1'b0	4'b0000	1'b0	1'b0	1'b0

Bit	Mnemonic	Description
[7]	dig_over_en	Allows the digital core to override the amp_mode settings via the contents of register 45, 46 and 47. • 1'b0: Uses the amp_mode setting to control the analog sections (default). • 1'b1: Allows the digital core to override the amp_mode settings.
[6:3]	reserved	
[2]	sel1v	Drops the digital power supply to 1V, which allows the supply to be driven externally. • 1'b0: Use the internal digital power supply regulator (default). • 1'b1: Lower the internal digital power supply voltage to 1V for use with external 1.2V supply.
[1]	shtoutb	Controls the shunt on the output of the amplifier. • 1'b0: Shunt on the output of the amplifier is engaged, allowing for protection against clicks while configuring the amplifier (default). • 1'b1: Shunt on the output of the amplifier is disengaged, allowing the amplifier to drive an audio signal.
[0]	shtinb	Controls the shunt on the input of the amplifier. • 1'b0: Shunt on the input of the amplifier is engaged, allowing for protection against clicks while configuring the amplifier (default). • 1'b1: Shunt on the input of the amplifier is disengaged.

Register 47: Analog Control Override (0x2F)

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	enfcb	encp_oe	enaux_oe	cpl_ens	cpl_enw	sel3v3_ps	ensm_ps	sel3v3_cph
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bit	Mnemonic	Description
[7]	enfcb	Enables the fast charge of the analog reference. • 1'b0: analog reference will be charged as quickly as possible (default) • 1'b1: analog reference will be charged at a slower rate
[6]	encp_oe	Allows the digital core to override the charge pump settings. • 1'b0: charge pump settings are controlled via the GPIO2 pin (default) • 1'b1: charge pump settings are controlled via the digital override bits
[5]	enaux_oe	Allows the digital core to override the output switch settings. • 1'b0: output switch is controlled via the GPIO2 pin (default) • 1'b1: output switch is controlled via the enaux register
[4]	cpl_ens	Enables the small charge pump and places it into strong mode. The small charge pump powers the pre-amplifier of the headphone amp. • 1'b0: small charge pump (strong mode) is disabled (default) • 1'b1: small charge pump (strong mode) is enabled • **Note**: encp_oe must be set to 1'b1 for the digital core to control the charge pump.
[3]	cpl_enw	Enables the small charge pump and places it into weak mode. The small charge pump powers the pre-amplifier of the headphone amp. • 1'b0: small charge pump (weak mode) is disabled (default) • 1'b1: small charge pump (weak mode) is enabled • **Note**: encp_oe must be set to 1'b1 for the digital core to control the charge pump.
[2]	sel3v3_ps	Configures the voltage of the positive power supply of the output stage. • 1'b0: uses 1.8V for the positive power supply of the output stage (default) • 1'b1: uses 3.3V for the positive power supply of the output stage
[1]	ensm_ps	Allows for a smooth transition between 1.8V and 3.3V on the positive power supply. This bit should be configured to 1'b0 immediately before changing the sel3v3_ps bit. Once sel3v3_ps has been set to the required value, then ensm_ps can be set back to 1'b1 for normal operation. • 1'b0: configure the positive supply for a transition between 1.8V and 3.3V (default) • 1'b1: normal operation
[0]	sel3v3_cph	Configures the voltage of the negative power supply of the output stage. • 1'b0: uses 1.8V for the negative power supply of the output stage (default) • 1'b1: uses 3.3V for the negative power supply of the output stage

Register 48: Analog Control (0x30)

Bits	[7]	[6]	[5:4]	[3]	[2]	[1:0]
Mnemonic	reserved	enhpa_out	Reserved	hpa_hiq	en_sep_thd_comp	reserved
Default	1'b0	1'b0	2'b00	1'b0	1'b0	2'b01

Bit	Mnemonic	Description
[7]	reserved	
[6]	enhpa_out	Enable the headphone amplifier output stage, active high. • 1'b0: disable the headphone output stage (default) • 1'b1: enable the headphone output stage Note: To reduce clicks/pops during power sequencing ENHPA_OUT should be delayed at least 100us after issuing the ENHPA signal.
[5:4]	reserved	
[3]	hpa_hiq	Selects the bias current of the headphone amplifier output stage. • 1'b0: Low output bias current (default). • 1'b1: High output bias current.
[2]	en_sep_thd_comp	Selects either one set or separate sets of THD coefficients are to be used for channel 1 & 2 THD compensation. • 1'b0: one set of coefficients (register 22-25) are used for both channels 1 and 2 (default). • 1'b1: a separate set of coefficients (registers 53-56) are used for channel 2.
[1:0]	reserved	

Register 49-51: Automatic Clock Gearing Thresholds (0x31 – 0x33)

Bits	[23:12]	[11:0]
Mnemonic	clk_gear_max_thresh	clk_gear_min_thresh
Default	12'd220	12'd98

Bit	Mnemonic	Description
[23:12]	clk_gear_max_thresh	Selects the maximum number of ***CLK***/2 pulses per 1fs that must be counted before the clock gear is automatically increased (***CLK*** is slowed down).
[11:0]	clk_gear_min_thresh	Selects the minimum number of ***CLK***/2 pulses per 1fs that must be counted before the clock gear is automatically decreased (***CLK*** is sped up). This value should always be 98 or larger so that the minimum ***CLK*** oversampling factor is achieved.

Note: The Automatic Clock Gearing Thresholds registers must be written from LSB to MSB in their entirety to be latched correctly.

Register 52: Reserved (0x34)

Bits	[7:0]
Mnemonic	Reserved
Default	8'd98

Register 53-54: THD Compensation C2 – Ch.2 (0x35 - 0x36)

Bits	[15:0]
Mnemonic	thd_comp_c2_ch2
Default	16'd0

Bit	Mnemonic	Description
[15:0]	thd_comp_c2_ch2	A 16-bit signed coefficient for correcting for the second harmonic distortion. Defaults to 16'd0. Used for channel 2 only when enable_sep_thd_comp is set. See Register 48: Analog Control (0x30).

See THD Compensation for more details.

Register 55-56: THD Compensation C3 – Ch.2 (0x37 - 0x38)

Bits	[15:0]
Mnemonic	thd_comp_c3_ch2
Default	16'd0

Bit	Mnemonic	Description
[15:0]	thd_comp_c3_ch2	A 16-bit signed coefficient for correcting for the third harmonic distortion. Defaults to 16'd0. Used for channel 2 only when enable_sep_thd_comp is set. See Register 48: Analog Control (0x30).

See THD Compensation for more details.

Register 57: Reserved (0x39)

Bits	[7:0]
Mnemonic	Reserved
Default	8'd16

Register 58: Reserved (0x3A)

Bits	[7:0]
Mnemonic	Reserved
Default	8'd1

Register 59: Reserved (0x3B)

Bits	[7:0]
Mnemonic	Reserved
Default	8'd0

Register 60: Reserved (0x3C)

Bits	[7:0]
Mnemonic	Reserved
Default	8'd0

Read-Only Registers

Registers 64 - 75 (0x40 - 0x4B) are read only registers that can change their default values due to write register settings.

Default values are only valid when the ES9218P is initially brought out of a reset state.

Register 64 (Read-Only): Chip Status (0x40)

Bits	[7:2]	[1]	[0]
Mnemonic	chip_id	automute_status	lock_status
Default	6'b11010X	1'b0	1'b0

Bit	Mnemonic	Description
[7:2]	chip_id	6'b11010x: ES9218P
[1]	automute_status	Indicator for when automute has become active. • 1'b0: automute condition is inactive • 1'b1: automute condition has been flagged and is active
[0]	lock_status	Indicator for when the DPLL is locked (when in slave mode) or 1'b1 when the ES9218P is the master. • 1'b0: DPLL is not locked to the incoming audio sample rate (which could mean that no audio input is present, the lock has not completed, or the ES9218P is unable to lock due to clock jitter or drift) • 1'b1: DPLL is locked to the incoming audio sample rate, or the ES9218P is in master or 128*fs mode

Register 65 (Read-Only): GPIO Readback (0x41)

Bits	[7]	[6]	[5]	[4]	[3:2]	[1]	[0]
Mnemonic	ocbr_pos	ocbl_pos	ocbr_neg	ocbl_neg	clk_gear_rb	gpio2	gpio1
Default	1'b0	1'b0	1'b0	1'b0	2'b00	1'b0	1'b0

Bit	Mnemonic	Description
[7]	ocbr_pos	Indicates instantaneous positive overcurrent condition on the right channel. • 1'b0 No positive overcurrent condition (default) • 1'b1 Positive overcurrent condition at the amplifier output See Overcurrent Protection
[6]	ocbl_pos	Indicates instantaneous positive overcurrent condition on the left channel. • 1'b0 No positive overcurrent condition (default) • 1'b1 Positive overcurrent condition at the amplifier output See Overcurrent Protection
[5]	ocbr_neg	Indicates instantaneous negative overcurrent condition on the right channel. • 1'b0 No negative overcurrent condition (default) • 1'b1 Negative overcurrent condition at the amplifier output See Overcurrent Protection
[4]	ocbl_neg	Indicates instantaneous negative overcurrent condition on the left channel. • 1'b0 No negative overcurrent condition (default) • 1'b1 Negative overcurrent condition at the amplifier output See Overcurrent Protection
[3:2]	clk_gear_rb	Clock gear readback. This register will reflect changes from both manual and automatic clock gearing. • 2'b00: indicates CLK = XI(MCLK) (default) • 2'b01: indicates CLK = XI(MCLK) / 2 • 2'b10: indicates CLK = XI(MCLK) / 4 • 2'b11: indicates CLK = XI(MCLK) / 8
[1]	gpio2	Contains the state of the GPIO2 pin.
[0]	gpio1	Contains the state of the GPIO1 pin.

Registers 66-69 (Read-Only): DPLL Number (0x42 - 0x45)

Bits	[31:0]
Mnemonic	dpll_num
Default	

Bit	Mnemonic	Description
[31:0]	dpll_num	Contains the ratio between the CLK and the audio clock rate once the DPLL has acquired lock. This value is latched on reading the LSB, so register 66 must be read first to acquire the latest DPLL value and avoid data tearing. The value is latched on LSB because the DPLL number can change as the I2C transactions are performed. $$\mathrm{FSR} = \frac{(\mathrm{dpll\_num} * \mathrm{CLK})}{2^{32}}$$

Register 70: Reserved (0x46)

Bits	[7:0]
Mnemonic	Reserved
Default	8'd0

Register 71: Reserved (0x47)

Bits	[7:0]
Mnemonic	Reserved
Default	8'd0

Register 72 (Read-Only): Input Selection and Automute Status (0x48)

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Mnemonic	ocr_sd_mute	ocl_sd_mute	amr	aml	dop_select	reserved	i2s_select	dsd_select
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bit	Mnemonic	Description
[7]	ocr_sd_mute	Indicates when the OCP timeout has expired and an overcurrent event has occurred on the right channel. • 1'b0: No overcurrent condition (default) • 1'b1: Overcurrent condition detected at amplifier output OUT_R. See Overcurrent Protection
[6]	ocl_sd_mute	Indicates when the *oc_sd_gain* OCP timeout has expired and an overcurrent event has occurred on the left channel. • 1'b0: No overcurrent condition (default) • 1'b1: Overcurrent condition detected at amplifier output OUT_L. See Overcurrent Protection
[5]	amr	Automute status of right channel.
[4]	aml	Automute status of left channel.
[3]	dop_select	Contains the status of the DoP decoder. • 1'b0: DoP decoder has not detected a valid DoP signal • 1'b1: DoP decoder has detected a valid DoP signal
[2]	reserved	
[1]	i2s_select	Contains the status of the I2S decoder. • 1'b0: I2S decoder has not found a valid frame clock or bit clock • 1'b1: I2S decoder has detected a valid frame clock and bit clock arrangement
[0]	dsd_select	Contains the status of the DSD decoder. • 1'b0: DSD decoder is not being used • 1'b1: DSD decoder is being used as a fallback option if I2S and DoP have both failed to decode their respective input signals

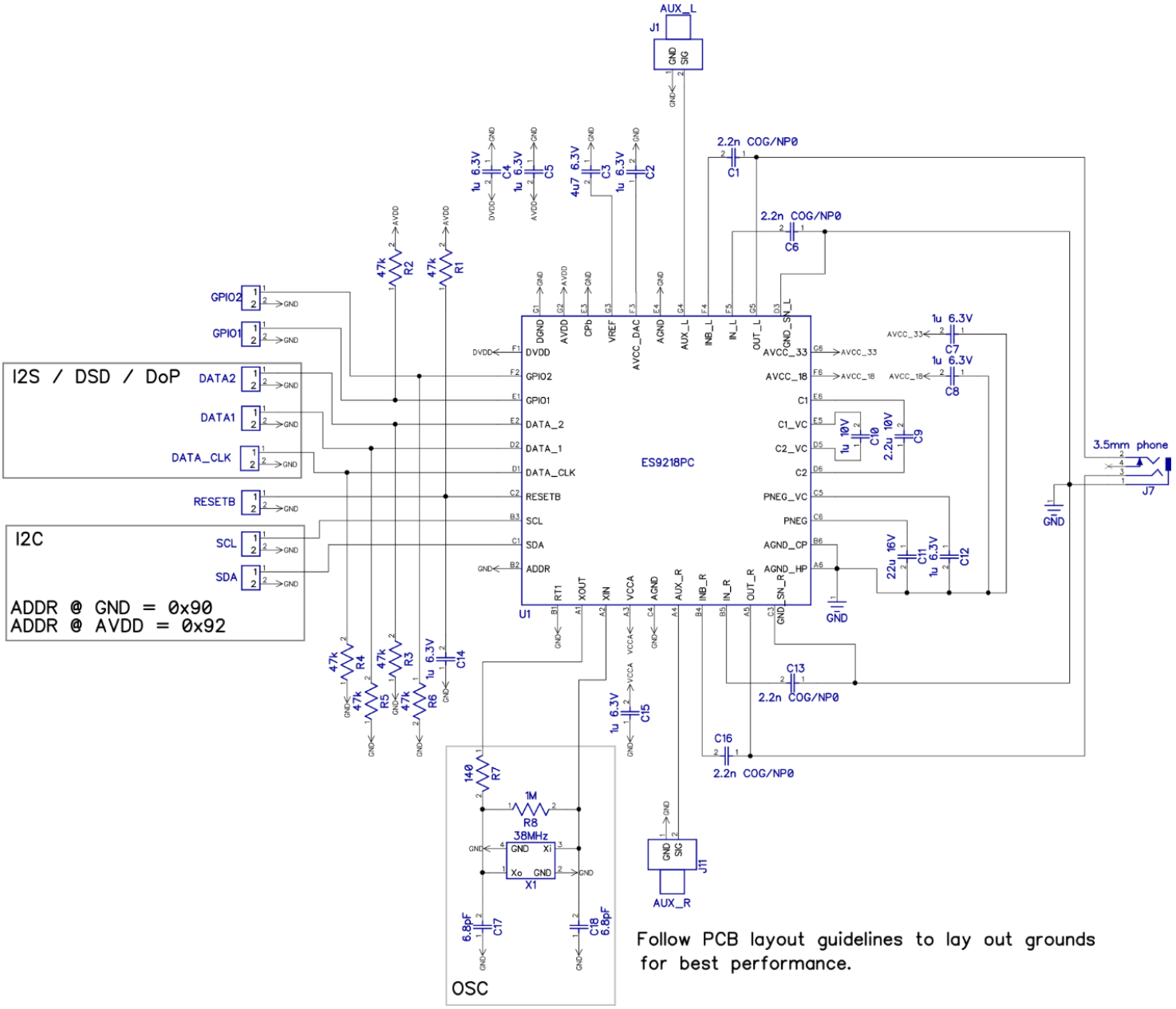
Register 73-75 (Read-Only): RAM Coefficient Readback (0x49 - 0x4B)

Bits	[23:0]
Mnemonic	prog_coeff_out
Default	

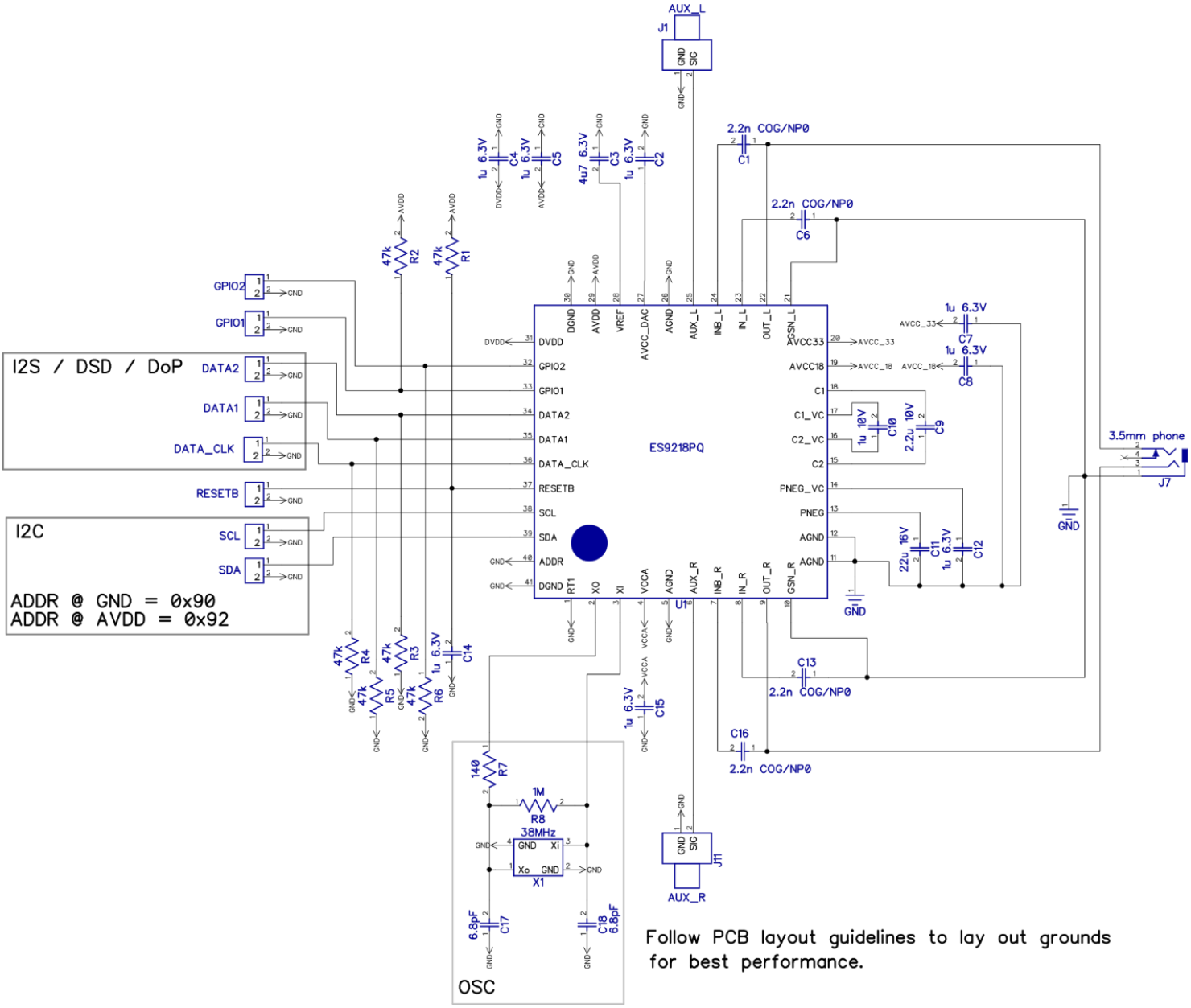
Bit	Mnemonic	Description
[23:0]	prog_coeff_out	A signed 24-bit number matching the data held in the FIR coefficient RAM at *prog_coeff_address*. This register can be used to validate that all RAM coefficients have been written correctly. The RAM address is set via Register 40: Programmable FIR RAM Address (0x28).

See Programmable FIR filter for more information.

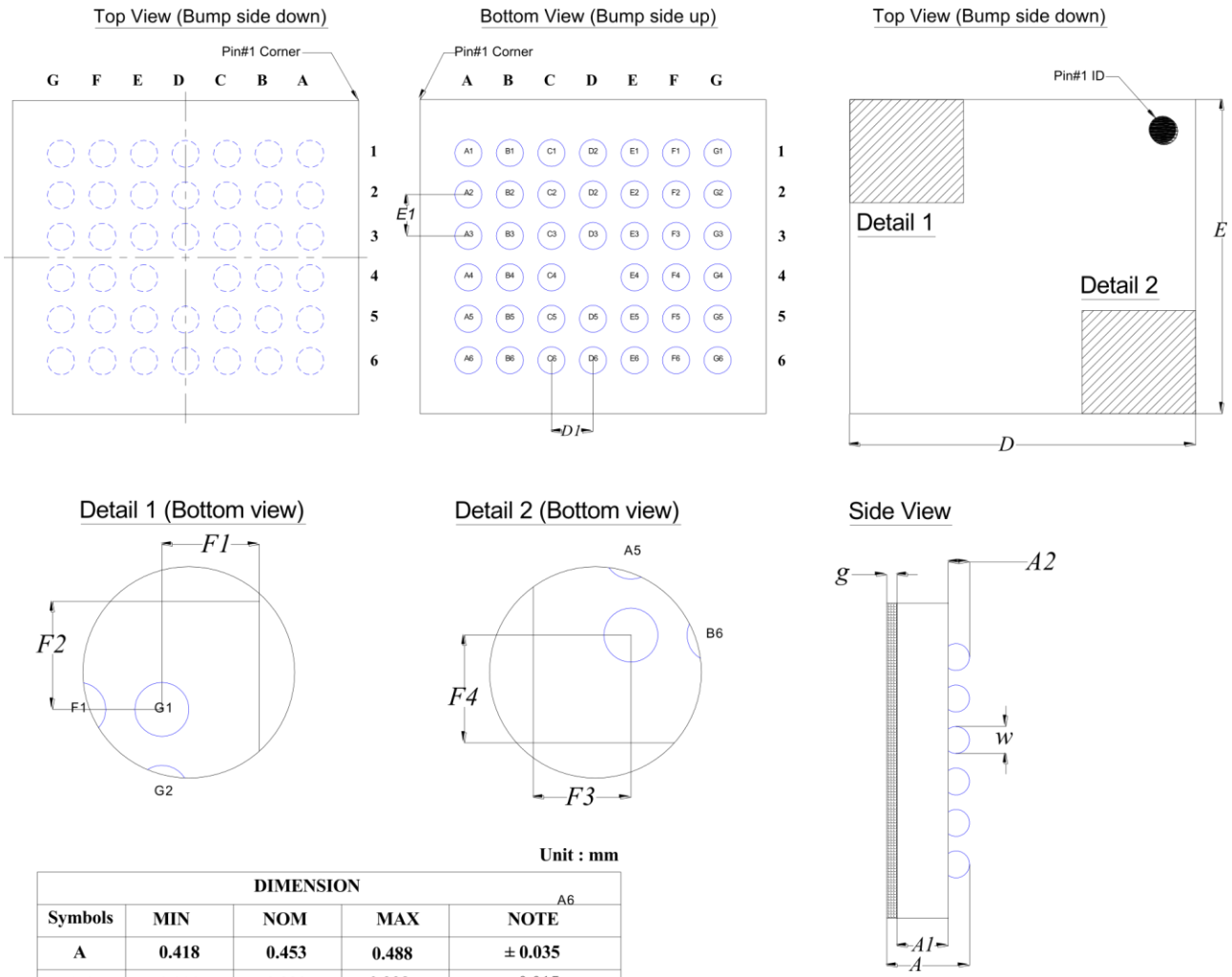
ES9218PC Reference Schematic



ES9218PQ Reference Schematic



41-Ball CSP Mechanical Dimensions



Unit : mm

DIMENSION				
Symbols	MIN	NOM	MAX	NOTE
A	0.418	0.453	0.488	± 0.035
A 1	0.208	0.223	0.238	± 0.015
A 2	0.188	0.205	0.222	± 0.017
D		3.330		± 0.025
E		3.030		± 0.025
D1		0.400		
E1		0.400		
F1		0.465		Ball center to die edge
F2		0.515		Ball center to die edge
F3		0.465		Ball center to die edge
F4		0.515		Ball center to die edge
g	0.022	0.025	0.028	± 0.003
w	0.234	0.260	0.286	± 0.026

Figure 13. ES9218PC Mechanical Dimensions

41-Ball CSP Top View Marking

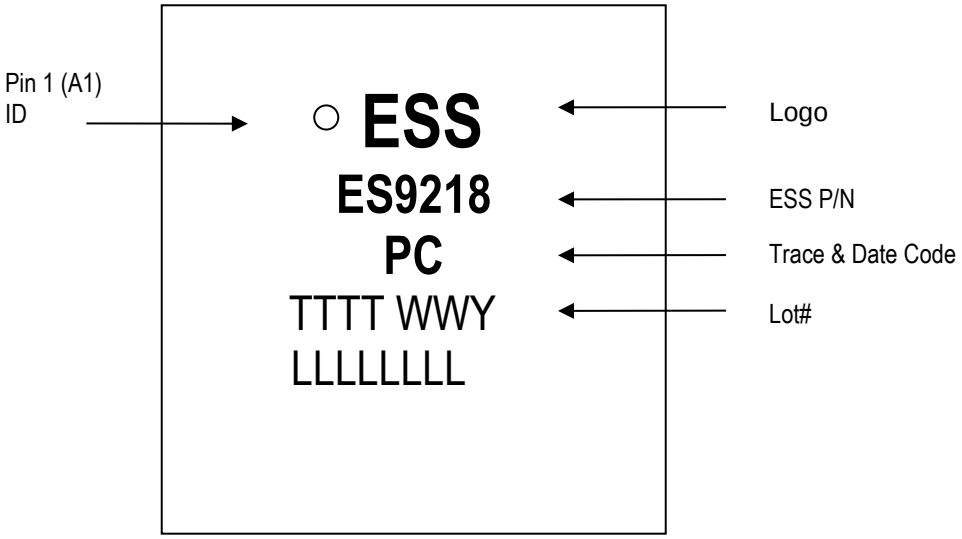
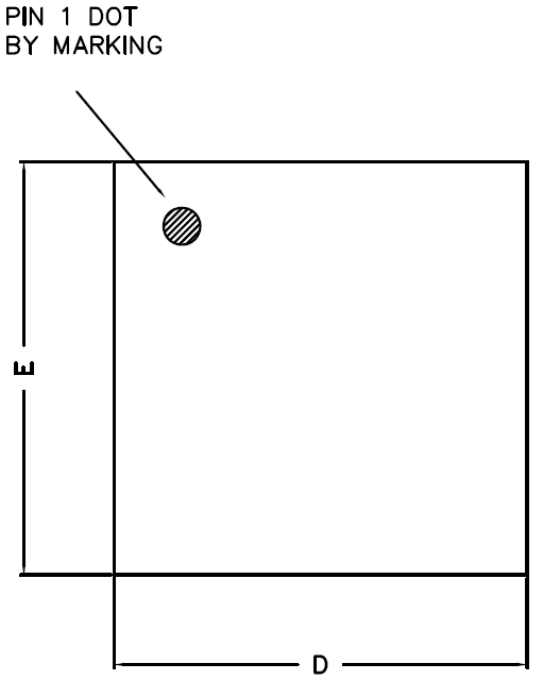


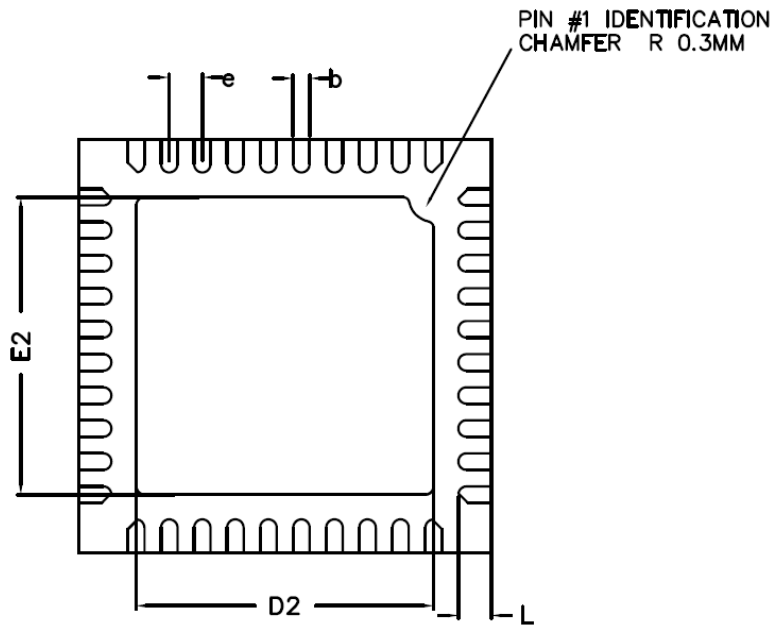
Figure 14. ES9218PC Marking

Marking is subject to change. This drawing is not to scale.

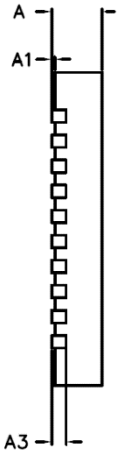
40-Pin QFN Mechanical Dimensions



Top View



Bottom View



Side View

COMMON DIMENSIONS (mm)			
PKG.	W: VERY VERY THIN		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.2 REF.		
D	4.95	5.00	5.05
E	4.95	5.00	5.05
b	0.15	0.20	0.25
L	0.30	0.40	0.50
D2	3.45	3.60	3.70
E2	3.45	3.60	3.70
e	0.4 BSC		

Table 1. Package Dimensions

40-Pin QFN Top View Marking

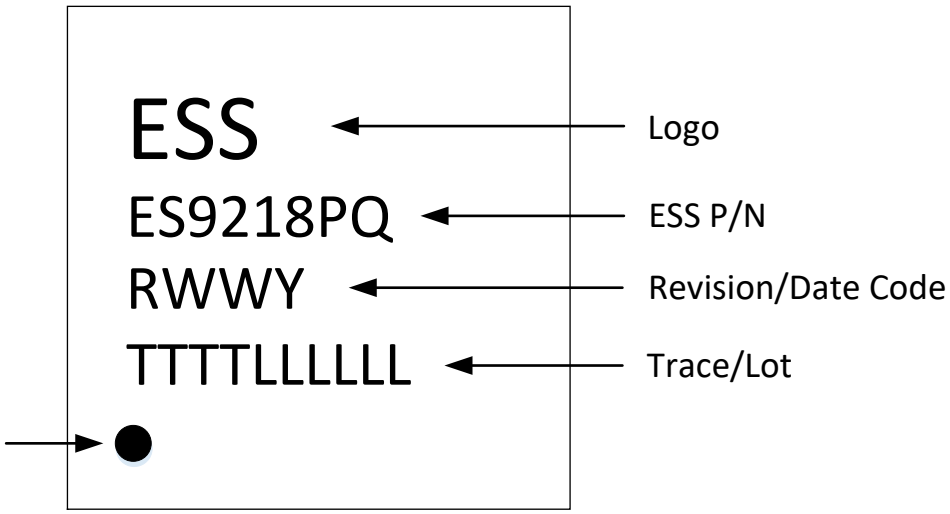


Figure 15. ES9218PQ Marking

Marking is subject to change. This drawing is not to scale.

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.
The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2 Pb-Free Process – Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.
The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used. Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

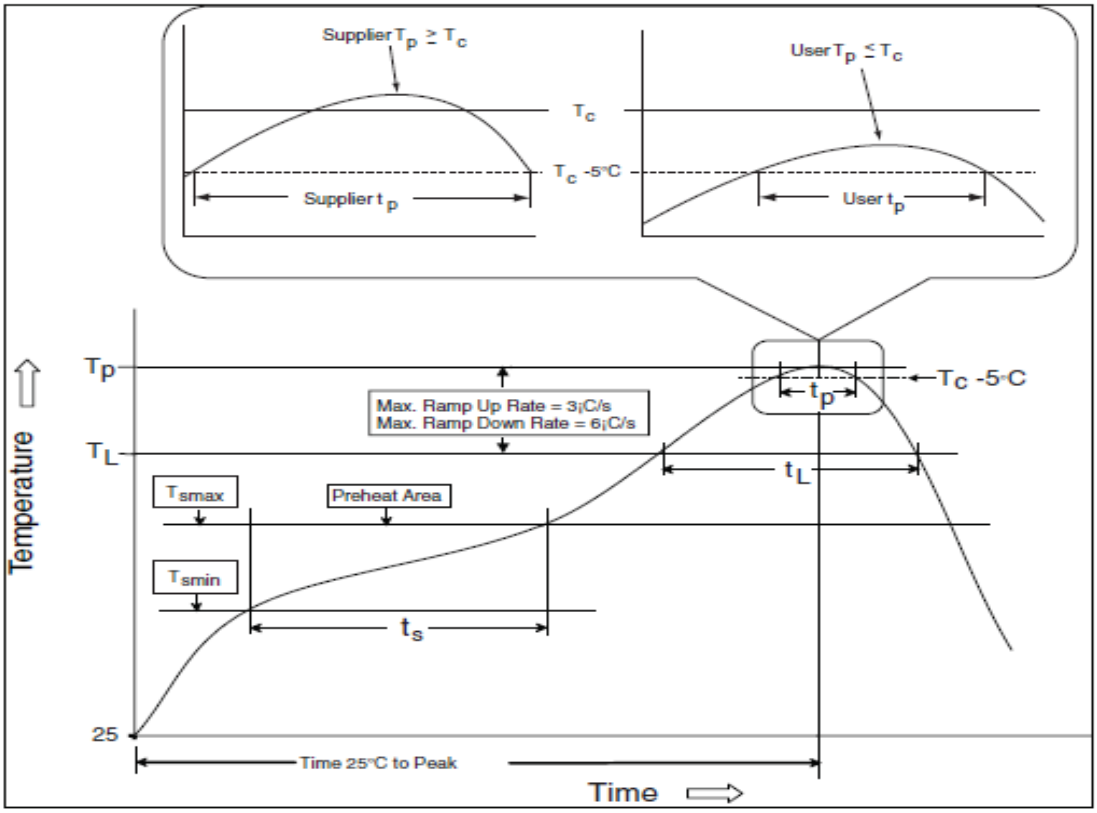


Figure 16. IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350°C no longer than 3 seconds.

RPC-1 Classification reflow profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc), see Figure	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

Note 3: All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).
Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.
Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9218PC	SABRE 32-bit Low Power Stereo DAC with Headphone Amplifier, Analog Volume Control, and Output Switch, on-chip feedback resistors	41-ball CSP
ES9218PQ	SABRE 32-bit Low Power Stereo DAC with Headphone Amplifier, Analog Volume Control, and Output Switch, on-chip feedback resistors	40 pin QFN

Revision History

Current Version 1.9

Rev.	Date	Notes
1.0	November 15, 2016	Initial release
1.1	December 9, 2016	Updated CSP Mechanical Dimensions
1.2	December 13, 2016	Register 8, GPIO Modes - Added OCP interrupts to list of interrupts. Changed name to “Interrupt” from “automute/lock interrupt” Register 11 - oc_sd_mute and oc_sd_gain descriptions Register 33 - Changed from reserved to Interrupt Mask. Added descriptions. Register 65 – Changed from reserved to ocbr and ocbl. Added descriptions. Register 72 - Changed oc_sd_mute description.
1.3	December 14, 2016	Added overcurrent protection to amplifier functional description. Removed notes with duplicate information from Serial Control Interface. Register 7 – Rename Corrected Minimum Phase Fast Roll-Off to Hybrid Fast Roll-Off Register 14 – Changed soft_start from reserved to supported. Register 33 – Separated 2bit registers into 1 bit registers. Register 46 – Corrected register bits and descriptions Register 48 – Changed hpa_hiq from reserved to supported. Register 55-56 – added missing register information. Register 65 – Separated 2 bit registers into 1 bit registers. Added description for clk_gear_rb Register 72 – Separated 2 bit registers into 1 bit registers. Corrected dop_status to dop_select. 41 Ball CSP Top View Marking updated
1.4	March 21, 2017	Added External Powered Oscillator/MCLK diagram, Crystal diagram, and Non-Optimal Crystal Circuitry diagram and explanation to Recommended Power Up Sequence section
1.5	November, 28, 2017	Removed ESS logo from 40-Pin QFN pin diagram.
1.6	February, 2, 2018	Update QUAD DAC™ notation
1.7	November 15, 2018	Added Low Power Audio DAC description, removed Advanced Information
1.8	December 6, 2018	Update Hyperstream® II and Hi Fi ® notations.
1.9	August 22, 2022	Update HQ address