ES9291

Stereo High-Performance SMART CODEC with PowerLine Driver

Product Datasheet

The SABRE® ES9291 High-Performance SMART CODEC is a world class stereo analog-to-digital (ADC) and stereo digital-to-analog (DAC) targeted for professional audio interfaces, very high-quality microphones, live stream media, powered speakers, mixers, recorders and other applications.

The ES9291 is a cost-effective solution that has 2 integrated ADCs & DACs using ESS' patented Hyperstream® IV Architecture, which delivers unprecedented audio sound quality and specifications, including a True DNR of +121dB and a THD+N ratio -110dB per channel. An analog-to-analog direct monitoring path with a mix mode is supported with very low latency. The ES9291 supports I²S/LJ master/slave, TDM I/O and DSD input. The ES9291 includes 8 pre-programmed FIR filters that are complementary to both ADC & DAC.

The ES9291 SMART CODEC incorporates ESS' 2nd generation Audio Signal Processors (ASP2) on both the DAC & ADC data paths. Customers can integrate multi-band PEQs, MIXERs, DRC, AGL, stereo widening, and specialty filters such as RIAA and cross-over filters.

Leveraging ESS' SABRE Intelligence Studio (SI Studio) simplifies programming the ASP2, potentially reducing or eliminating separate DSP requirements. Additional features include a Temperature Sensor and Jack Detection.

The new single-ended PowerLine Driver with an output drive of up to 125mW @ 32Ω is integrated into the ES9291 providing a very high-performance headphone amplifier and line driver for exceeding all application requirements.

FEATURE	DESCRIPTION
+121dB True DNR per channel -110dB THD+N per channel	High-Performance True Dynamic Range and very low distortion
Integrated PowerLine Driver	High-Performance Headphone & Line Driver 125mW output power @ 32Ω with external negative supply (per channel) 70mW output power @ 32Ω with internal negative supply (per channel)
Audio Signal Processor (ASP2) 8 pre-programmed built-in Filters	Presets of digital optimal filters for ADC & DAC ASP2 can be used for custom filters
High Sample Rates	Up to 768kHz PCM (ADC/DAC) & DSD1024 (DAC) in 64FS mode
Integrated Analog PLL	Minimal reduction in performance as compared with external clock, eliminating the need for a powered oscillator
Multiple I/O Formats Available	I²S & TDM inputs/outputs are available, TDM daisy chain is supported, DSD & DoP256 (DAC) input, S/PDIF Stereo output
Digital Volume Control (I²C/SPI) Digital Gain Control (I²C/SPI)	-127 to 0dB (ADC) and -126 to +1dB (DAC) in increments of +0.5dB +0 to +42dB in increments of +6dB for creating maximum gain
I²C, SPI, and Hardware interface control	Configured by microcontroller or other I²C/SPI source, or pins through Hardware Mode for simplification of control, Master SPI Interface integration
Programmable Microphone Bias Supply	Integrated MICBIAS can be programmed from 1.45V-2.8V
Ultra-Low Noise Floor Bandwidth on ADC	200kHz bandwidth enabling higher resolution at higher sample rates
Integrated low noise reference regulators	Reduced BOM cost, PCB area and improved DNR
Low Pin Count Packaging	7mm x 7mm 48 pin QFN

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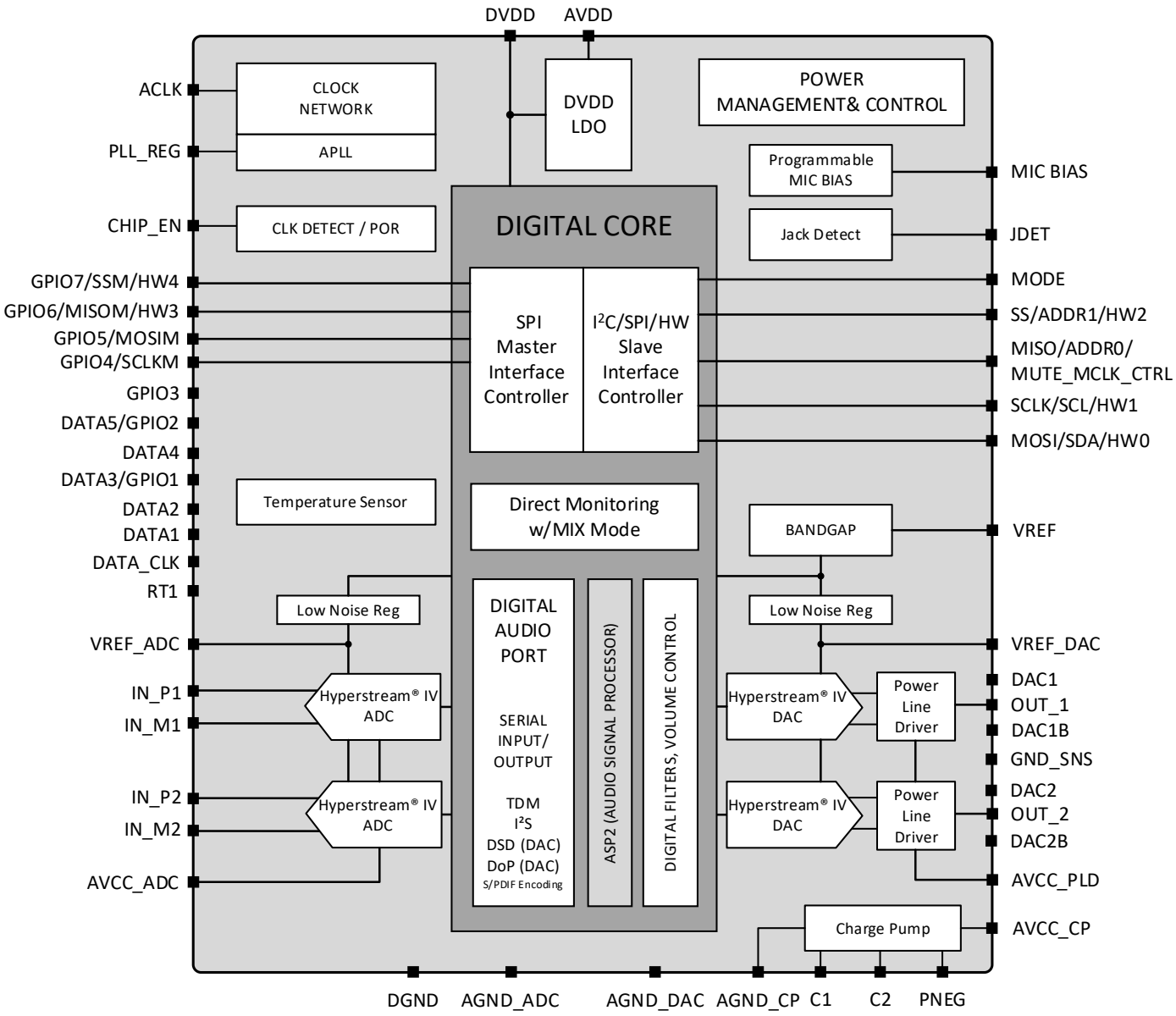


Figure 1 - ES9291 Functional Block Diagram

ES9291 Package

48 QFN Pinout

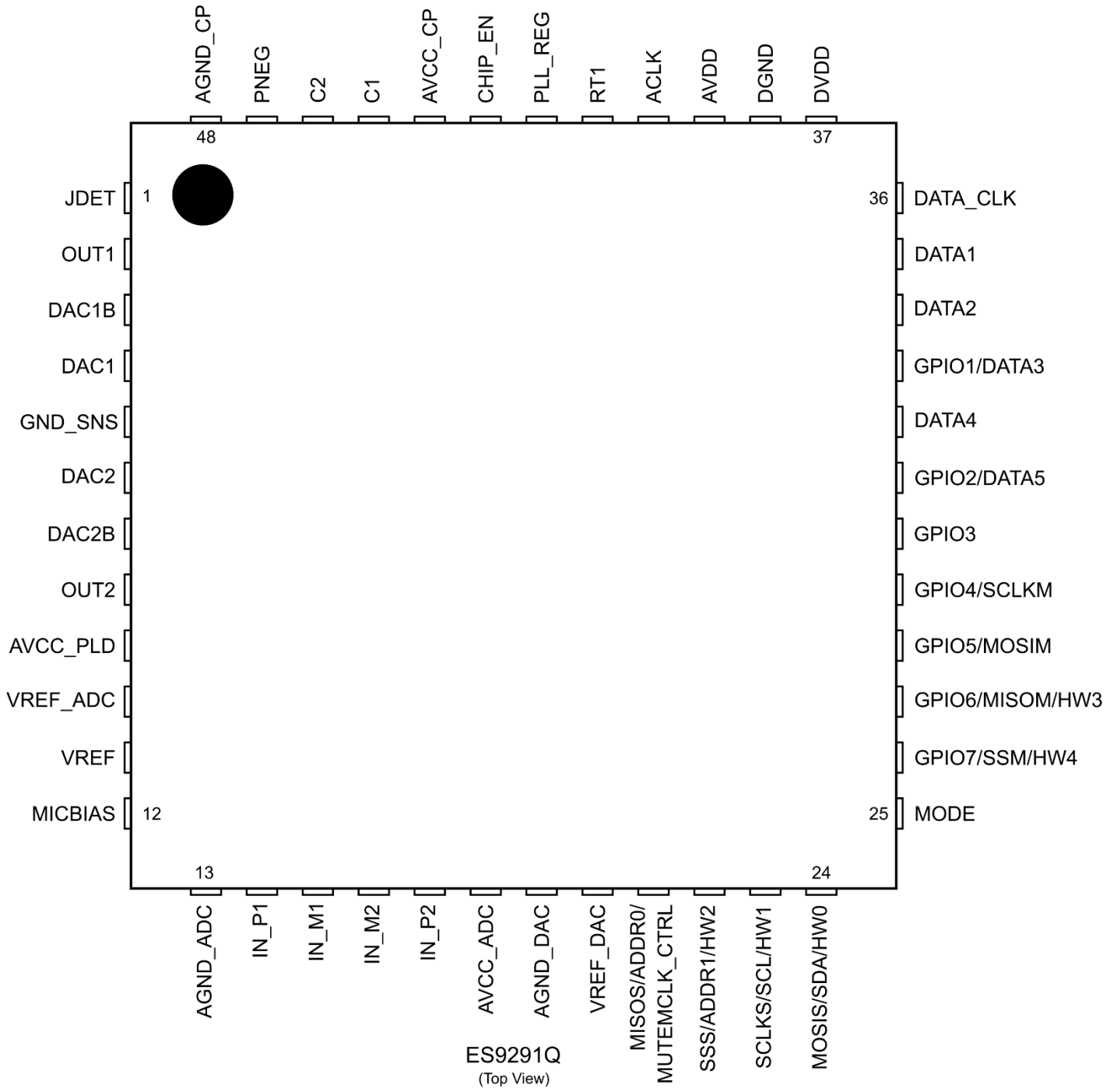


Figure 2 - 48 QFN Pinout

48 QFN Pin List

Pin	Name	Pin Type	Reset State	Pin Description
1	JDET	A I	Power	Jack Detect
2	OUT1	A O	Ground	Power Line Driver Output 1
3	DAC1B	A O	Ground	Channel 1 Line Driver Signal Sense
4	DAC1	A O	Ground	Channel 1 Ground Sense
5	GND_SNS	A I/O	-	Power Line Driver Ground Sense
6	DAC2	A O	Ground	Channel 2 Ground Sense
7	DAC2B	A O	Ground	Channel 2 Line Driver Signal Sense
8	OUT2	A O	Ground	Power Line Driver Output 2
9	AVCC_PLD	Power	Power	3.3V Supply for Power Line Driver
10	VREF_ADC	A I/O	P/D	ADC Reference Voltage
11	VREF	A I/O	P/D	Bandgap Reference Voltage
12	MICBIAS	A I/O	P/D	Low Noise Supply for Microphone Bias, internally generated
13	AGND_DAC	Ground	Ground	Analog Ground for DAC
14	IN_P1	A I	Ground	ADC Channel 1 Differential Positive (+) Input
15	IN_M1	A I	Ground	ADC Channel 1 Differential Negative (-) Input
16	IN_M2	A I	Ground	ADC Channel 2 Differential Negative (-) Input
17	IN_P2	A I	Ground	ADC Channel 2 Differential Positive (+) Input
18	AVCC_ADC	Power	Power	3.3V Supply for ADC
19	AGND_ADC	Ground	Ground	Analog Ground for ADC
20	VREF_DAC	A I/O	P/D	DAC Reference Voltage
21	MISOS	D I/O	HiZ	SPI Main In Sub Out pin (Slave), controlled by MODE
	ADDR0			I²C Address 0 pin, controlled by MODE
	MUTE_MCLK_CTRL			Hardware Mute Control pin, controlled by MODE
22	SSS	D I/O	HiZ	SPI Slave Select pin (Slave), controlled by MODE
	ADDR1			I²C Address 1 pin, controlled by MODE
	HW2			Hardware 2 interface pin, controlled by MODE
23	SCLKS	D I/O	HiZ	SPI Serial Clock pin (Slave), controlled by MODE
	SCL			I²C Serial Clock pin, controlled by MODE
	HW1			Hardware 1 interface pin, controlled by MODE
24	MOSIS	D I/O	HiZ	SPI Main Out Sub In pin (Slave), controlled by MODE
	SDA			I²C Serial Data pin, controlled by MODE
	HW0			Hardware 0 interface pin, controlled by MODE
25	MODE	D I/O	HiZ	I²C/SPI Control selection or HW mode

26	GPIO7	D I/O	HiZ	General I/O 7
	SSM			SPI Slave Select (Master) pin, controlled by MODE
	HW4			Hardware 4 interface pin, controlled by MODE
27	GPIO6	D I/O	HiZ	General I/O 6
	MISOM			SPI Main In Sub Out pin (Master), controlled by MODE
	HW3			Hardware 3 interface pin, controlled by MODE
28	GPIO5	D I/O	HiZ	General I/O 5
	MOSIM			SPI Main Out Sub In pin (Master), controlled by MODE
29	GPIO4	D I/O	HiZ	General I/O 4
	SCLKM			SPI Serial Clock pin (Master), controlled by MODE
30	GPIO3	D I/O	HiZ	General I/O 3
31	GPIO2	D I/O	HiZ	General I/O 2
	DATA5			Serial Data 5
32	DATA4	D I/O	HiZ	Serial Data 4
33	GPIO1	D I/O	HiZ	General I/O 1
	DATA3			Serial Data 3
34	DATA2	D I/O	HiZ	Serial Data 2
35	DATA1	D I/O	HiZ	Serial Data 1
36	DATA_CLK	D I/O	HiZ	Serial Data Clock
37	DVDD	A O	P/D	Digital core supply, internally supplied
38	DGND	Ground	Ground	Digital core ground
39	AVDD	Power	Power	3.3V I/O supply
40	ACLK	Clock I	HiZ	Clock input
41	RT1	D I	HiZ	Reserved. **Must be connected to DGND for normal operation**.
42	PLL_REG	A I/O	P/D	Low Noise Supply for PLL, internally generated
43	CHIP_EN	D I/O	D I/O	Active-High Chip Enable (Defines Reset State)
44	AVCC_CP	Power	Power	3.3V Supply for Charge Pump
45	C1	A I/O	Ground	Charge Pump positive flying capacitor pin
46	C2	A I/O Neg	Ground	Charge Pump negative flying capacitor pin
47	PNEG	A I/O	P/D	Negative Supply for Line Driver, internally generated.
48	AGND_CP	Ground	Ground	Analog Ground for Charge Pump
49	Package Pad	-	-	Electrically connected to internal grounds. **Must** be connected to ground.

Table 1 - 48 QFN Pin List

Configuration Modes

The ES9291 SMART CODEC has 4 control programming modes which are controlled by the state of the MODE pin (Pin 25).

MODE PIN	Configuration
0	I²C Interface
Pull 0	HW control mode (see Hardware Mode Table)
Pull 1	HW control mode (see Hardware Mode Table)
1	SPI Interface

Table 2 - Mode Pin Configuration Options

Design Information

Hardware pins can be configured in 4 different ways. Each pin can be tied-high (1), pulled-high (Pull 1), pulled-low (Pull 0), or tied-low (0). HW0 and HW1 pins are always tied-high or tied-low. These 4 options also apply to MUTE_CTRL.

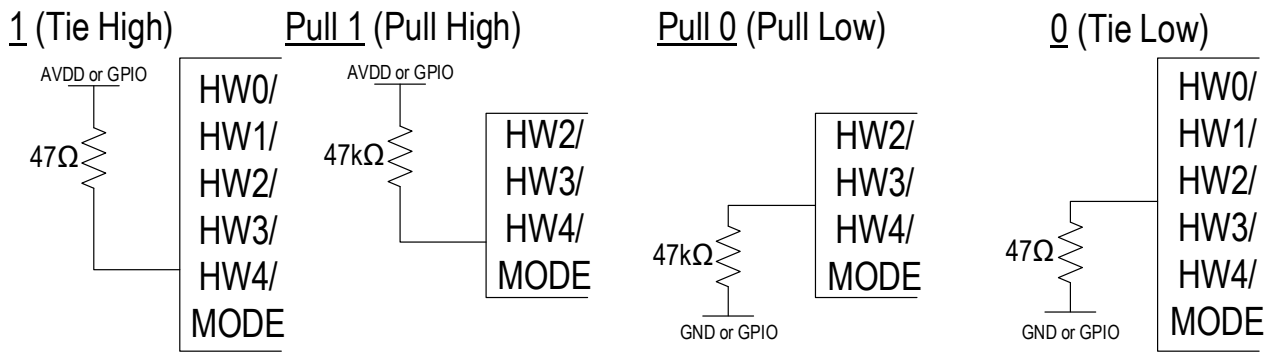


Figure 3 - Example Hardware Mode Pin Configurations

Software Mode

The ES9291 supports a slave I²C or SPI serial communication in software mode. There are two types of registers, read/write registers and read-only registers. Software modes are set when the MODE pin is a 0 (0V) for I²C or a 1 (AVDD) for SPI.

A system clock is not required to read and write registers.

I²C Slave Interface Commands

- MODE (Pin 25) – 0 (Tied-Low)
- Connect per I²C standard
  - SDA (Pin 24)
  - SCL (Pin 23)
  - ADDR0 (Pin 21)
  - ADDR1 (Pin 22)

I²C Address	ADDR1	ADDR0
0x30	GND	GND
0x32	GND	AVDD
0x34	AVDD	GND
0x36	AVDD	AVDD

Table 3 - I²C Addresses

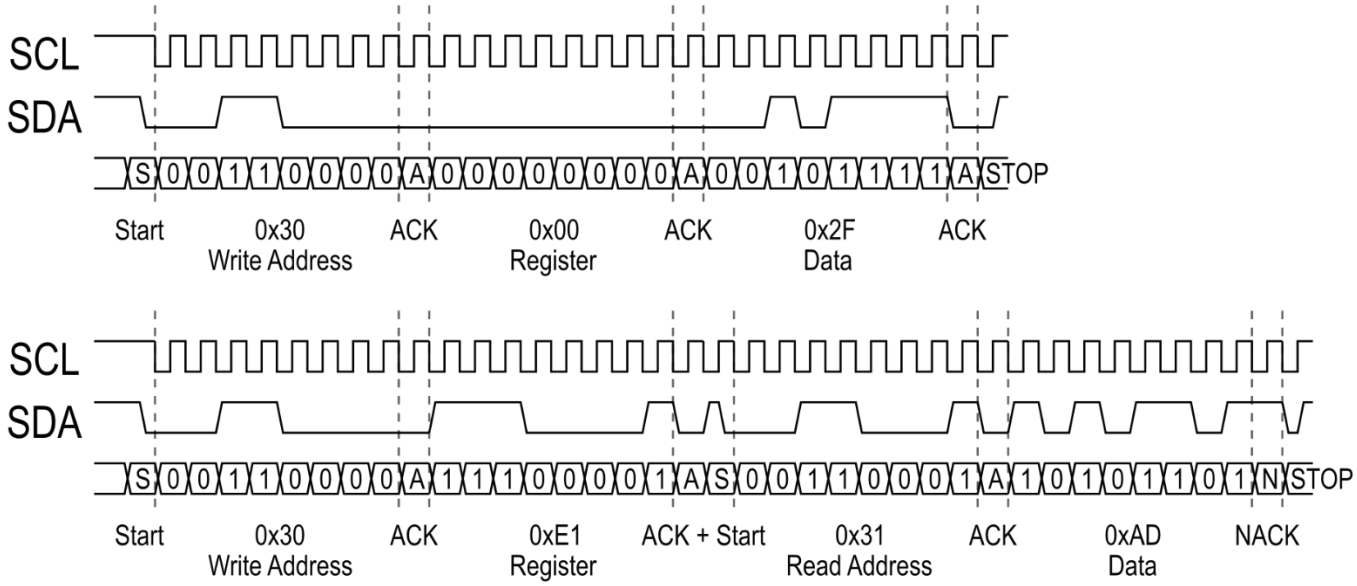


Figure 4 - I²C Write and Read Example

Note: CHIP_ID is 0xAD in Register 225 (0xE1)

SPI Slave Interface Commands

- MODE (Pin 25) - AVDD
- Connect per SPI standard
  - MOSI (Pin 24)
  - SCLK (Pin 23)
  - SS (Pin 22)
  - MISO (Pin 21)

SPI Command	First Byte
Write	0x03
Read	0x01

Table 4 - SPI Commands

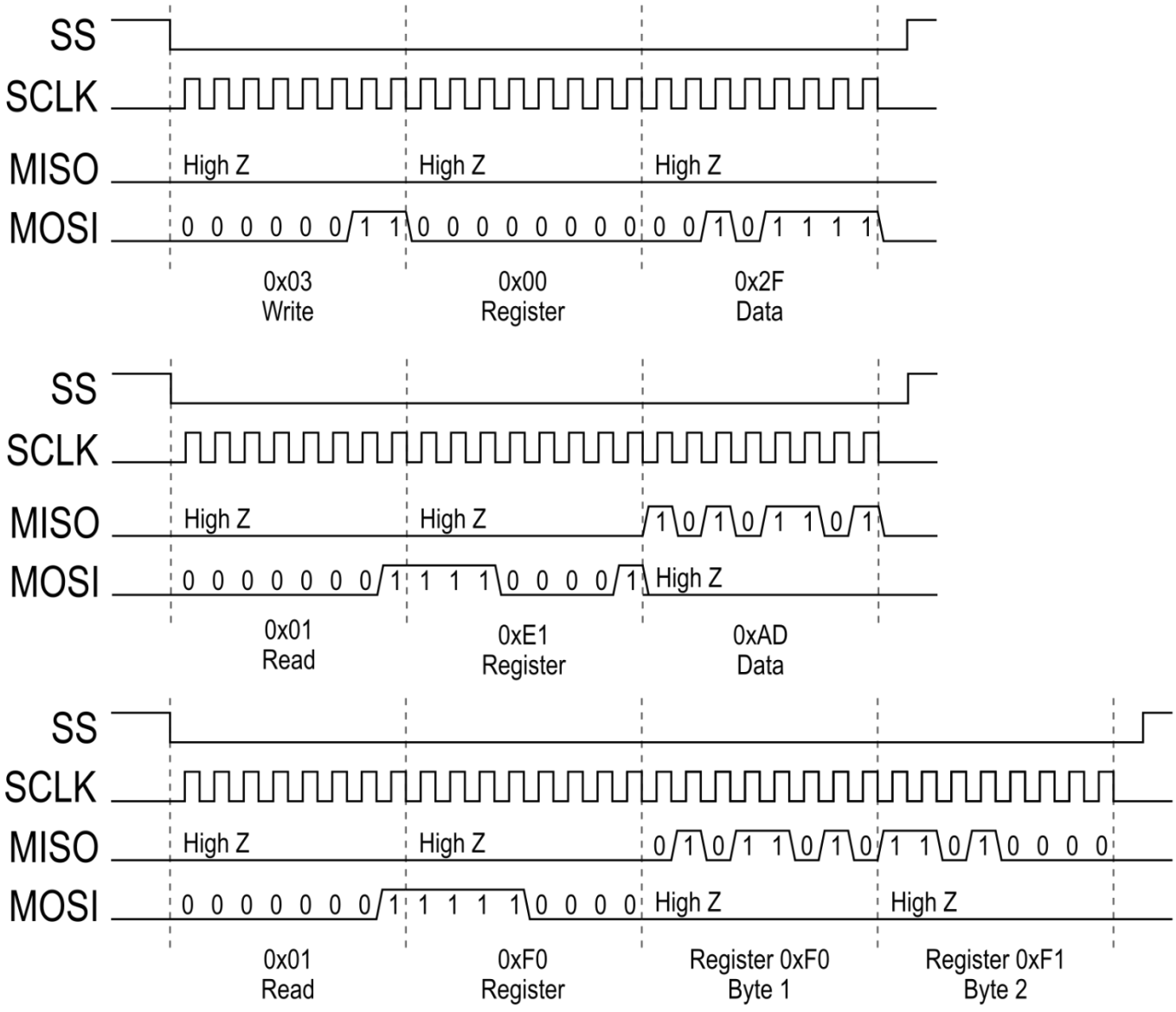


Figure 5 - SPI Single Byte Write, Single Byte Read, and Multi Byte Read Example

Note: CHIP_ID is 0xAD in Register 225 (0xE1)

Hardware Mode

The ES9291 has pre-configured modes that can be set with an external pin configuration. These modes configure the analog to digital converters (ADC) and digital to analog converters (DAC) for different input/output serial data rates and set the mute control. Hardware mode supports analog or stereo digital PDM microphones as inputs. Each hardware mode pin has 4 states that can be found in Design Information.

These modes are set with pins:

- MODE (Pin 25)
- HW0 (Pin 24)
- HW1 (Pin 23)
- HW2 (Pin 22)
- HW3 (Pin 27)
- HW4 (Pin 26)
- GPIO5 (Pin 28)
- MUTE_CTRL (Pin 21)

Recommended Hardware Mode Setup Sequence

The Hardware Mode setup sequence is shown below with all hardware pins being defined after CHIP_EN is asserted.

Note: MUTE_CTRL should be set to muted until the HW mode is finalized and after CHIP_EN is asserted, then it may be set to the correct clock rate and unmuted last. See Mute and MCLK Control for more information.

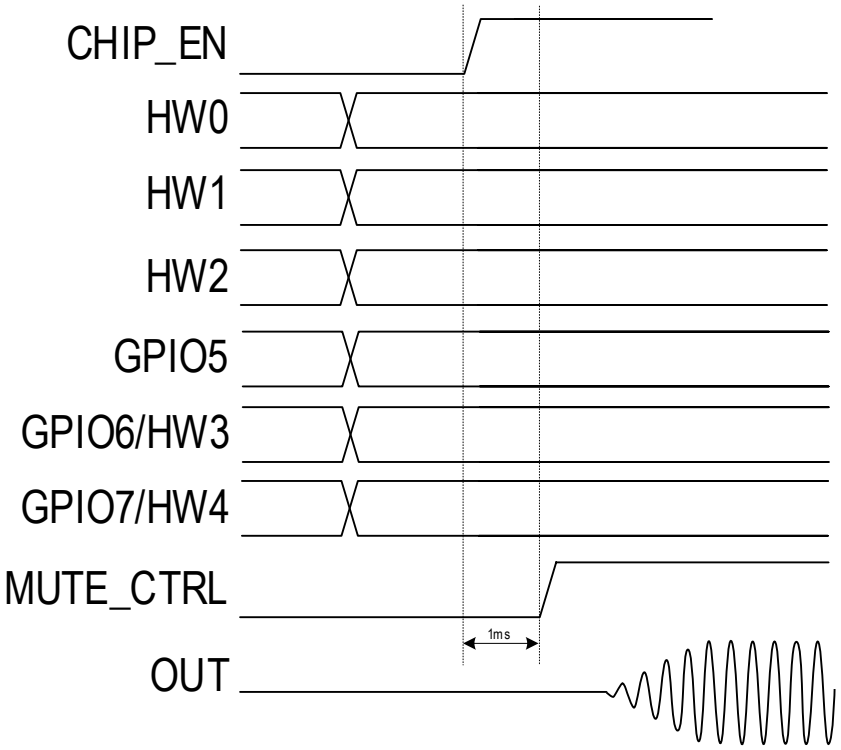


Figure 6 - Hardware Mode Startup Sequence

Hardware Pin Configurations

HW Mode	Description	FS [kHz]	BCK [MHz]	MODE	HW2	HW1	HW0
32-bit PCM Master Modes (Ext MCLK)							
0	I²S with Ext MCLK	MCLK/128	MCLK/2 (64*FS)	Pull 0	0	0	0
1	I²S with Ext MCLK	MCLK/256	MCLK/4 (64*FS)	Pull 0	0	0	1
2	I²S with Ext MCLK	MCLK/512	MCLK/8 (64*FS)	Pull 0	0	1	0
3	I²S with Ext MCLK	MCLK/1024	MCLK/16 (64*FS)	Pull 0	0	1	1
4	LJ with Ext MCLK	MCLK/128	MCLK/2 (64*FS)	Pull 0	Pull 0	0	0
5	LJ with Ext MCLK	MCLK/256	MCLK/4 (64*FS)	Pull 0	Pull 0	0	1
6	LJ with Ext MCLK	MCLK/512	MCLK/8 (64*FS)	Pull 0	Pull 0	1	0
7	LJ with Ext MCLK	MCLK/1024	MCLK/16 (64*FS)	Pull 0	Pull 0	1	1
32-bit PCM Slave Modes (PLL or Ext MCLK)							
8	I²S with Ext MCLK, Auto FS	44.1 ≤ FS ≤ 768	64*FS	Pull 0	Pull 1	0	0
9	I²S with PLL from BCK	48	3.072	Pull 0	Pull 1	0	1
10	I²S with PLL from BCK	96	6.144	Pull 0	Pull 1	1	0
11	I²S with PLL from BCK	192	12.288	Pull 0	Pull 1	1	1
12	LJ with Ext MCLK, Auto FS	44.1 ≤ FS ≤ 768	64*FS	Pull 0	1	0	0
13	LJ with PLL from BCK	48	3.072	Pull 0	1	0	1
14	LJ with PLL from BCK	96	6.144	Pull 0	1	1	0
15	LJ with PLL from BCK	192	12.288	Pull 0	1	1	1
32-bit TDM LJ Slave Modes, Autodetect FS & CH Num							
16	TDM LJ Channel Slots = 1,2	44.1 ≤ FS ≤ 768	Auto (64FS, 128FS, 256FS, 512FS, 1024FS)	Pull 1	0	0	0
17	TDM LJ Channel Slots = 3,4	44.1 ≤ FS ≤ 384	Auto (128FS, 256FS, 512FS, 1024FS)	Pull 1	0	0	1
18	TDM LJ Channel Slots = 5,6	44.1 ≤ FS ≤ 192	Auto (256FS, 512FS, 1024FS)	Pull 1	0	1	0
19	TDM LJ Channel Slots = 7,8	44.1 ≤ FS ≤ 192	Auto (256FS, 512FS, 1024FS)	Pull 1	0	1	1
20	TDM LJ Channel Slots = 9,10	44.1 ≤ FS ≤ 96	Auto (512FS, 1024FS)	Pull 1	Pull 0	0	0
21	TDM LJ Channel Slots = 11,12	44.1 ≤ FS ≤ 96	Auto (512FS, 1024FS)	Pull 1	Pull 0	0	1
22	TDM LJ Channel Slots = 13,14	44.1 ≤ FS ≤ 96	Auto (512FS, 1024FS)	Pull 1	Pull 0	1	0
23	TDM LJ Channel Slots = 15,16	44.1 ≤ FS ≤ 96	Auto (512FS, 1024FS)	Pull 1	Pull 0	1	1
16-bit TDM LJ Slave Modes, Autodetect FS & CH Num							
24	TDM LJ Channel Slots = 1,2	44.1 ≤ FS ≤ 768	Auto (32FS, 64FS, 128FS, 256FS, 512FS)	Pull 1	Pull 1	0	0
25	TDM LJ Channel Slots = 3,4	44.1 ≤ FS ≤ 768	Auto (64FS, 128FS, 256FS, 512FS)	Pull 1	Pull 1	0	1
26	TDM LJ Channel Slots = 5,6	44.1 ≤ FS ≤ 192	Auto (128FS, 256FS, 512FS)	Pull 1	Pull 1	1	0
27	TDM LJ Channel Slots = 7,8	44.1 ≤ FS ≤ 192	Auto (128FS, 256FS, 512FS)	Pull 1	Pull 1	1	1
28	TDM LJ Channel Slots = 9,10	44.1 ≤ FS ≤ 96	Auto (256FS, 512FS)	Pull 1	1	0	0
29	TDM LJ Channel Slots = 11,12	44.1 ≤ FS ≤ 96	Auto (256FS, 512FS)	Pull 1	1	0	1
30	TDM LJ Channel Slots = 13,14	44.1 ≤ FS ≤ 96	Auto (256FS, 512FS)	Pull 1	1	1	0
31	TDM LJ Channel Slots = 15,16	44.1 ≤ FS ≤ 96	Auto (256FS, 512FS)	Pull 1	1	1	1

GPIO Functions in Hardware Mode

The ES9291 supports specific functions through the GPIO pins in hardware modes. The tables below show the available controls in hardware modes. These include the DACs Automute, Filter Select, ADC DC Block, Gain, Mic Bias, and Input Select. These functions are supported in hardware mode.

Supported HW Modes	HW4 (Pin 26)	DAC Automute	ADC DC Block
All	0	Disabled	Disabled
	Pull 0	Disabled	Enabled
	Pull 1	Enabled	Disabled
	1	Enabled	Enabled

Table 5 - DAC Automute and ADC DC Block control with HW4

Supported HW Modes	HW3 (Pin 27)	DAC Filter Select	Daisy Chain Toggle
0 – 15	0 / Pull 0	Filter 1 Minimum Phase	-
	Pull 1 / 1	Filter 3 Linear Phase Fast Roll-Off	-
16-31	0	Filter 1 Minimum Phase	Parallel
	Pull 0		Daisy Chain
	Pull 1	Filter 3 Linear Phase Fast Roll-Off	Parallel
	1		Daisy Chain

Table 6 - DAC Filter and Daisy Chain control with HW3

GPIO5 (Pin 28)	ADC Input	GPIO4 (Pin 29)	GPIO3 (Pin 30)	ADC Gain	Mic Bias
0	Analog	0	0	+0dB	Disabled
		0	1	+18dB	Enabled (2.85V)
		1	0	+24dB	Enabled (2.85V)
		1	1	+30dB	Enabled (2.85V)
1	PDM Microphone[1]	PDM_MIC_DATA [I]	PDM_MIC_CLK[O]	-	-

Table 7 - ADC Input Select, Gain, and Mic Bias control with GPIO5/4/3

[1] PDM Microphone is not available when using a 45.158MHz/49.152MHz MCLK when the MCLK/FS ratio <= 128

Mute and MCLK Control

Set MUTE_MCLK_CTRL (Pin 21) to mute the output while in Hardware Mode:

HW MUTE Control (Pin 21)	Condition	MCLK
0	Mute	24.576MHz
1	Unmute	24.576MHz
Pull 0	Mute	49.152MHz
Pull 1	Unmute	49.152MHz

Table 8 - Mute and MCLK Control in Hardware Mode

Note: If MUTE_MCLK_CTRL (Pin 21) is set to the incorrect MCLK rate, the ADC may have less output performance.

Digital Features

The ES9291 SMART CODEC integrates several digital features including multiple Input/Output audio formats, an SPI Master interface, a TDM Encoder daisy chain mode, pre-programmed digital filters, and programmable GPIOs. The ADC digital signal path and the DAC digital signal path can pass audio through both paths alongside monitoring the signal with Direct Monitoring.

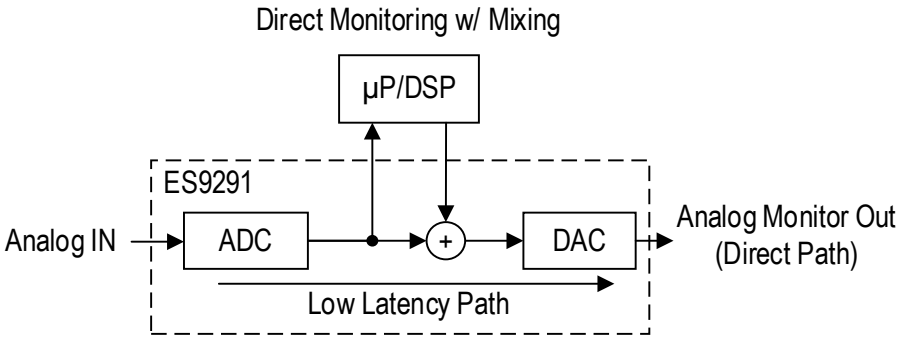


Figure 7 - Direct Monitoring Path

Audio Input/Output Formats

The ES9291 SMART CODEC supports multiple audio serial input and output data formats and are selected through either Software or Hardware modes.

The ES9291 DAC/Powerline datapath supports PCM, DSD, PDM, and DoP input formats and is selected using Register 3[2:1] INPUT_DATA_FORMAT_SEL in software mode. The corresponding format ENABLE_[data format]_DECODE bit in Register 2 must also be set.

The ES9291 ADC analog datapath supports PCM and S/PDIF output formats along with Analog/PDM microphone input formats. The ADC's PCM output is enabled with Register 2[0] ENABLE_TDM_ENCODE, and the S/PDIF output be set with GPIO configuration registers. The PDM microphone can be configured using Register 18-20.

Note: In software mode, the ADC and DAC must be turned on together during initial startup. Hardware mode automatically sets this configuration.

The formats include:

- PCM
  - Slave and master mode is 16, 24, 32 – bit widths
  - I²S and Left-Justified (LJ)
  - Sample rates up to 768kHz (64fs mode)
  - Channel mapping
- TDM
  - Up to 32 slots including daisy chain mode
  - Slave mode in hardware mode. Slave and master modes in software mode
  - LJ Format in hardware modes, I²S or LJ in software modes
  - Channel mapping
- DSD
  - Slave and master modes in software mode
  - Sample rates from DSD64 (2.8224Mbits/s, 64x44.1kHz) to DSD512
  - Channel mapping
- DoP (DSD over PCM)
  - Slave and master modes in software mode
  - Sample rates from DoP64 to DoP256
  - Channel mapping
- PDM
  - Slave and master modes in software mode
  - Sample rates from PDM64 to PDM512
- S/PDIF
  - Stereo 2 Channel Output
  - Input Selection
  - Sample rates up to 192kHz
- PDM Microphone Input
  - Master mode in hardware and software mode
  - Sample rates from PDM64 to PDM512

PCM/TDM Encoder

The ES9291 integrates a 2 channel 1 line PCM/TDM Encoder whose output has a maximum word width of 32-bits (default) and a maximum bit depth of 32-bit (default). The encoder allows for I²S, LJ, and TDM output streams.

The PCM/TDM Encoder can support up to 32 different slots and each channel for the ADC can be mapped to any of the 32 slots.

Note: The PCM/TDM Encoder and PCM/TDM Decoder share the same formatting registers settings.

PCM/TDM Encoder Formatting Registers

- Register 2[0] ENABLE_TDM_ENCODE = 1'b1
- Register 9[6] AUTO_CH_DETECT
- Register 9[4:0] TDM_CH_NUM
- Register 10[6] NOISE_FLOOR_SHAPE_16BIT
- Register 10[5:4] TDM_WORD_WIDTH
- Register 10[3:2] TDM_BIT_DEPTH
- Register 10[1] TDM_VALID_EDGE
- Register 10[0] TDM_LJ

ADC TDM Mapping Registers

- Register 11[4:0] TDM_ENC_SLOT_SEL_CH1
- Register 12[4:0] TDM_ENC_SLOT_SEL_CH2

ADC Daisy Chain Registers

- Register 15[7] TDM_ENC_DAISY_CHAIN
- Register 15[4:0] TMD_ENC_DATA_LATCH_ADJ

PCM/TDM Decoder

The ES9291 integrates a 2 channel 1 line PCM/TDM Decoder whose input has a maximum word width of 32-bits (default) and a maximum bit depth of 32-bit (default). The decoder allows for I²S, LJ, and TDM input streams.

The PCM/TDM Decoder can support up to 32 different slots and each channel for the DAC can be mapped to any of the 32 slots.

Note: The PCM/TDM Encoder and PCM/TDM Decoder share the same formatting registers settings.

PCM/TDM Decoder Formatting Registers

- Register 2[4] ENABLE_TDM_DECODE = 1'b1
- Register 3[2:1] INPUT_DATA_FORMAT_SEL = 2'b00
- Register 9[6] AUTO_CH_DETECT
- Register 9[4:0] TDM_CH_NUM
- Register 10[6] NOISE_FLOOR_SHAPE_16BIT
- Register 10[5:4] TDM_WORD_WIDTH
- Register 10[3:2] TDM_BIT_DEPTH
- Register 10[1] TDM_VALID_EDGE
- Register 10[0] TDM_LJ

DAC TDM Mapping Registers

- Register 13[4:0] TDM_DEC_SLOT_SEL_CH1
- Register 14[4:0] TDM_DEC_SLOT_SEL_CH2

DAC Daisy Chain Registers

- Register 16[7] TDM_DEC_DAISY_CHAIN
- Register 16[4:0] TDM_DEC_DATA_LATCH_ADJ

PCM (I²S, LJ) Format

PCM includes I²S and LJ with 2 channels/slots per data line. The ADC outputs can be mapped to any slot/channel of the PCM encoder output data (DATA2) using TDM_ENC_SLOT_SEL_CHx. The PCM decoder routes any slot/channel of the PCM input data (DATA4) to the DACs using TDM_DEC_SLOT_SEL_CHx.

Pin Name	Function	Direction	Description
DATA_CLK	PCM BCLK	[I/O]	PCM Clock (Bit Clock), Master or Slave
DATA1	PCM WS	[I/O]	PCM WS (Word Select/Frame Select), Master or Slave
DATA2	PCM ENC DATA1	[O]	PCM Data Output from ADC (Encoder)
DATA4	PCM DEC DATA1	[I]	PCM Data Input for DAC (Decoder)

Table 9 - PCM Pin Connections

Note: The PCM Decoder supports Right Justified (RJ) format in software mode for a single device.

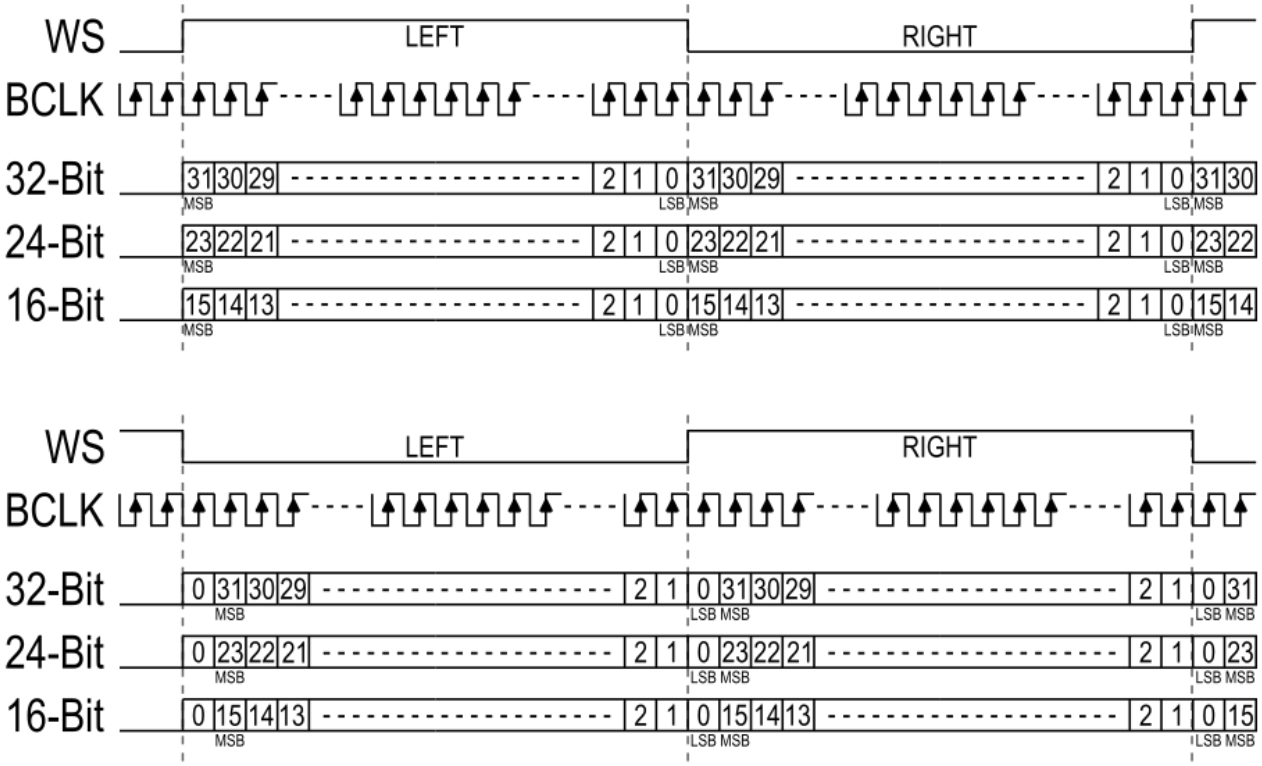


Figure 8 - LJ (top) & I²S (bottom) for 32, 24, and 16-bit Word Widths

TDM Format

The ES9291 supports TDM format, allowing more than 2 channels/slots to be transmitted and received on a data line, up to a maximum of 32 channels. Supported formats are TDM4 (4ch), TDM8 (8ch), TDM16 (16ch) and TDM32 (32ch). The ADC outputs can be mapped to any slot of the TDM output data (DATA2) using TDM_ENC_SLOT_SEL_CHx. The DACs can choose any slot/channel of the TDM input data (DATA4) using TDM_DEC_SLOT_SEL_CHx.

Data is latched on the positive edge of BCLK.

Pin Name	Function	Direction	Description
DATA_CLK	TDM BCLK	[I/O]	TDM Clock, Master or Slave
DATA1	TDM WS	[I/O]	TDM WS, Master or Slave
DATA2	TDM ENC DATA1	[O]	TDM Encoder DATA1 (default)
GPIO1/DATA3	TDM ENC DAISY	[I]	TDM Encoder Daisy Chain Pin
DATA4	TDM DEC DATA1	[I]	TDM Decoder DATA1 (default)
GPIO2/DATA5	TDM DEC DAISY	[O]	TDM Decoder Daisy Chain Pin

Table 10 - TDM Pin Connections

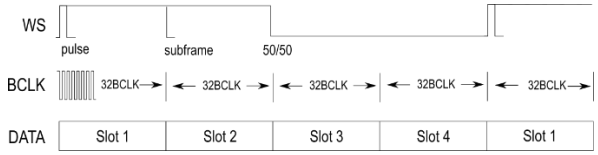


Figure 9 - TDM4 Mode

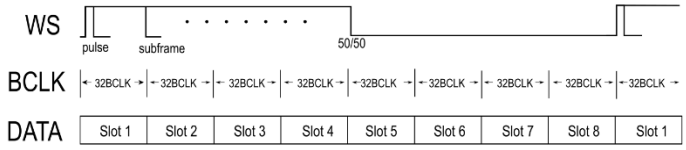


Figure 10 - TDM8 Mode

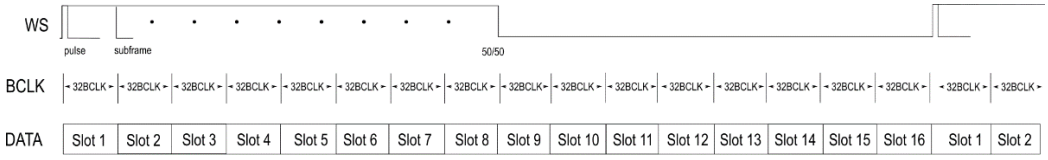


Figure 11 - TDM16 Mode

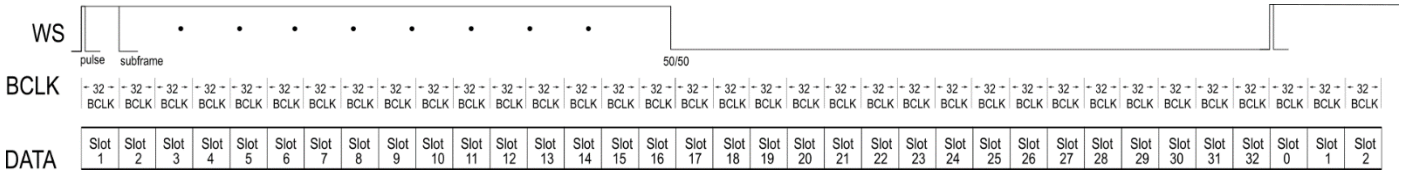


Figure 12 - TDM32 Mode

DSD Decoder

The ES9291 features a DSD Decoder input to the DAC Datapath with a single clock line and dual data lines. Each DSD source can be remapped to any DAC channel by using the remapping registers.

Note: When decoding DSD, the DAC must be muted prior to any instance where a DC signal is present on the DATA pins (e.g., stopping the data to switch to TDM/PCM format). This can be done with Register 90[1:0] DAC_MUTE_CHx.

DSD Decoder Registers

- Register 2[6] ENABLE_DSD_DECODE = 1'b1
- Register 3[2:1] INPUT_DATA_FORMAT_SEL = 2'b10

DSD Channel Remapping Registers

- Register 17[4] DSD_LINE_SEL_CH1
- Register 17[5] DSD_LINE_SEL_CH2

DSD Format

DSD Pin Connections:

Pin Name	Function	Description
DATA_CLK	DSD CLK	DSD Clock
DATA4	DSD CH1	DSD DATA Channel 1
DATA5	DSD CH2	DSD DATA Channel 2

Table 11 - DSD Pin Connections

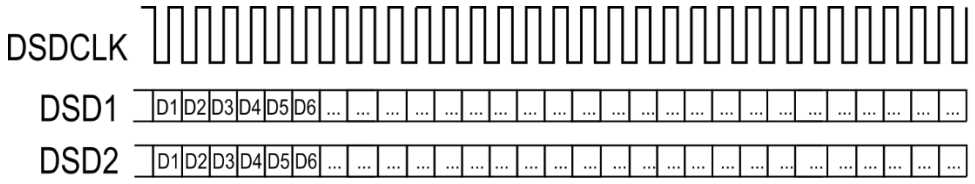


Figure 13 - DSD Format, 1-bit stream

DoP Decoder

The ES9291 integrates a DoP (DSD over PCM) Decoder that converts the DSD over PCM data into DSD internally following the rest of the internal DSD data path including the Automute, and DSD FIR and Volume blocks. The channels can be remapped by using the PCM/TDM Decoders Mapping Registers.

DoP Decoder Registers

- Register 2[5] ENABLE_DOP_DECODE
- Register 2[4] ENABLE_TDM_DECODE
- Register 10[5:4] TDM_WORD_WIDTH
- Register 10[3:2] TDM_BIT_DEPTH
- Register 10[0] TDM_LJ

PCM/TDM Decoder Mapping Registers

- Register 13[4:0] TDM_DEC_SLOT_SEL_CH1
- Register 14[4:0] TDM_DEC_SLOT_SEL_CH2

The PCM/TDM Decoder must be enabled and set up for a 24- or 32-bit word width and bit depth when using the DoP Decoder. I2S and LJ are supported for the PCM format. When using a 32-bit word width the 8 LSBs are dropped when decoding.

DoP Format

DoP Encodes 16 bits of DSD data into a 24-bit PCM frame, with the 8 most significant bits containing the DSD marker. The marker alternates between 0x05 and 0xFA every sample. The DSD data is inserted into the frame such that the oldest bit is in the t_0 position.

Pin Name	Function	Description
DATA_CLK	DoP BCLK	DoP Clock (Bit Clock), Master or Slave
DATA1	DoP WS	DoP WS (Word Select/Frame Select), Master or Slave
DATA4	DoP DATA1	DoP Data Channel 1 & 2 (default)

Table 12 - DoP Pin Connections

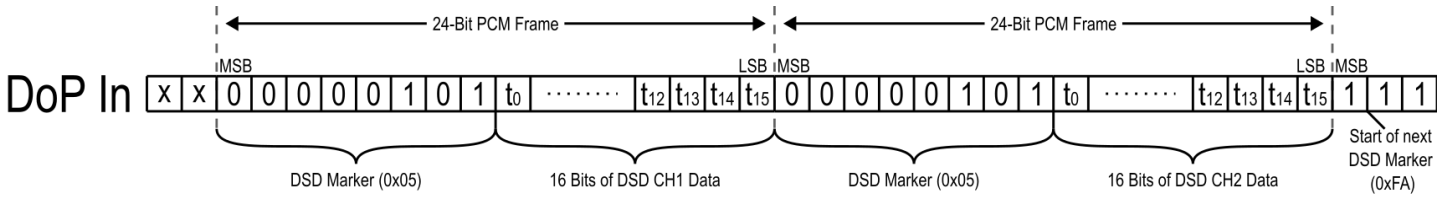


Figure 14 - DoP Format

PDM Microphone Decoder (Microphone Input to ADC)

The ES9291's ADC path can receive input audio from a PDM Microphone using the integrated Master PDM Microphone Decoder. To use the PDM signal as a replacement for the analog input in software mode, PDM_MIC_IN_SEL must be set. PDM Microphone Input is also supported in hardware modes, see GPIO Functions in Hardware Mode for more information.

Note: PDM_CLK_DIV will follow AUTO_FS_DETECT if enabled and should be set to 7'd3 (default) for a 22.5792MHz/24.576MHz MCLK and 7'd7 for a 45.1584MHz/49.152MHz MCLK to ensure the PDM clock output is 3.072MHz (typical PDM Microphone frequency).

Note: PDM_CLK_DIV must not be set to 0 if running a 45.1584/49.152MHz MCLK.

PDM Decoder Registers

- Register 3[6] ENABLE_PDM_MIC_DECODE = 1'b1
- Register 19[2] PDM_MIC_SAMPLE_EDGE
- Register 19[1] PDM_MIC_DATA_PHASE
- Register 19[0] PDM_MIC_IN_SEL
- Register 20[6:0] MCLK_PDM_MIC_DIV

PDM Decoder (DAC Input)

The ES9291's DAC path can also receive input audio from a PDM source using the PDM Decoder. The Decoders input can be remapped by using the DSD Channel Mapping registers.

Note: If a one sample phase shift is present between channels, invert PDM_DEC_SAMPLE_EDGE to resolve the shift.

PDM Decoder Registers

- Register 2[7] ENABLE_PDM_DECODE = 1'b1
- Register 3[2:1] INPUT_DATA_FORMAT_SEL = 2'b11
- Register 18[2] PDM_DEC_SAMPLE_EDGE
- Register 18[1] PDM_DEC_DATA_PHASE
- Register 18[0] PDM_DEC_2X_GAIN_EN

PDM Format

In PDM mode, there is a single PDM clock line and multiple PDM data lines containing two channels of data each. The channels can be swapped by setting the respective DATA_PHASE register.

Pin Name	Function	Description
DATA_CLK	PDM DEC CLK	PDM Clock
DATA4	PDM DEC DATA 1	PDM Encoder DATA Channels 1 & 2

Table 13 - Slave PDM Decoder Pin Connections

Pin Name	Function	Description
GPIO3	PDM MIC CLK	PDM Microphone Clock
GPIO4	PDM MIC DATA 1	PDM Microphone Input DATA Channels 1 & 2

Table 14 - PDM Decoder (Microphone Input) Pin Connections

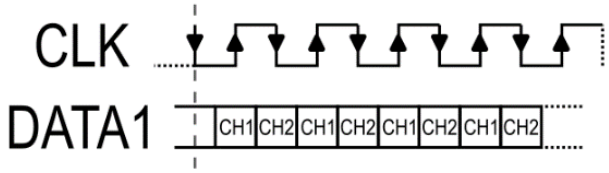


Figure 15 - PDM 2 Channel Format

S/PDIF Encoder

The ES9291 features a stereo auxiliary S/PDIF Encoder that can output the pair of channels sourced from two paths selected with SPDIF_DATA_SOURCE. The input to the encoder can be taken from the output of the ADC Gain block or from the output of the DACs PCM/TDM Decoder allowing for a fully digital bit-perfect PCM/TDM to S/PDIF conversion. This allows the ES9291 to have an Analog to S/PDIF or a Bit-Perfect Digital to S/PDIF path which can be output of any GPIO pin, see GPIO Configuration for more information.

The S/PDIF Encoder is auxiliary from the PCM/TDM Encoder, with the ability to be enabled with ENABLE_SPDIF_ENCODE while the PCM/TDM Encoder is running.

The S/PDIF Encoder includes the ability to customize the 40-bits (5 bytes) of channel status bits one byte at a time by setting SPDIF_CS_BYTE_ADDR and SPDIF_CS_BYTE_DATA then toggling SPDIF_CS_WE to latch the single byte in the status bits.

S/PDIF Encoder Registers

- Register 3[7] ENABLE_SPDIF_ENCODE = 1'b1
- Register 21[0] SPDIF_DATA_SOURCE
- Register 22[7] SPDIF_CS_WE
- Register 22[2:0] SPDIF_CS_BYTE_ADDR
- Register 23 SPDIF_CS_BYTE_DATA

SPI Master Interface

The ES9291 features an SPI master interface. The interface is primarily for programming an ASP2 program quickly from a SPI Flash device at high-speed clock rates (up to MCLK/2). The ES9291 can use the SPI Master Interface as a generic I²C to SPI Transcoder. This allows the SPI Master to interface with a wide array of devices like flash memories, shift registers, and other SPI slave programmable ESS devices. The SPI master interface makes use of the GPIOs in the following table.

GPIO #	SPI Master Function
GPIO7	SS Master (SSM) or Chip Select Master (CSM)
GPIO6	MISO Master (MISOM)
GPIO5	MOSI Master (MOSIM)
GPIO4	SCLK Master (SCLKM)

Table 15 - SPI Master Interface GPIO Connections

There are three registers related to using the SPI master interface and one bit to ensure it is disconnected from the ASP2:

- Register 131 [3] ASP_PROG_SOURCE_SEL should be set low to disconnect the SPI master interface from the ASP2 programming interface.
- Register 173 SPI_MASTER_CONFIG is used to start and end SPI transmissions and set the SPI master clock.
    - [7:4] SPI_M_PULSE_WIDTH – sets the SPI clock frequency
    - [3] SPI_M_EN – Enables the SPI Master interface
    - [2] SPI_M_MODE – Switches the SPI master between Mode 0 (default) and Mode 3
    - [1] SPI_M_SEND_BYTE – Used to manually send/receive SPI bytes.
    - [0] SPI_M_START – Starts and SPI transaction, pulls SSM (GPIO8) low
- Register 174 SPI_MASTER_DATA_OUT contains the data byte to be sent from the SPI master interface.
- Register 252 SPI_MASTER_DATA_IN contains the data byte received by the SPI master interface.

When the chip is powered on or reset the chip select output (GPIO7) will be set low by default. When Register 173 [3] SPI_M_EN is set high, enabling the SPI master interface, the chip select will output high.

As the SPI master interface is designed to communicate with an SPI Flash device, it is very efficient at reading or writing long blocks of data. However, to simultaneously read and write data for a generic application requires a specific sequence of register commands.

SPI Write

Writing data on the SPI bus requires 2+n write-register commands where n is the number of bytes to be sent in one SPI transaction. To efficiently write data to an SPI flash Register 173 [1] SPI_M_SEND_BYTE must remain low for automatic SPI data output. Each time Register 174 SPI_M_DATA_OUT is written during an SPI transaction the data will automatically be sent out of the SPI master interface at the end of the write-register command.

A single byte SPI transmission would be sequenced as follows:

1. Setup Register 173 SPI MASTER CONFIG
   - [7:4] SPI_M_PULSE_WIDTH sets the SPI clock speed
   - [3] SPI_M_EN = 1'b1 enables the SPI master
   - [2] SPI_M_MODE selects between SPI modes 0 and 3
   - [1] SPI_M_SEND_BYTE = 1'b0 for automatic operation
   - [0] SPI_M_START prepares the SPI master interface to initiate an SPI transmission.
2. Write a byte of data to Register 174. This will automatically start the SPI transaction.
   - After receiving the write-register command the chip select output (GPIO7) is set low after 2 MCLK cycles.
   - The SPI clock will begin half an SPI clock cycle plus one MCLK cycle after the chip select is set low.
   - The SPI master interface will output the 8 bits of data and afterwards the SPI clock will remain idle, and the chip select low.
3. Resetting Register 173 [0] SPI_M_START low will end the SPI transaction by setting the chip select high.

To write multiple bytes of data in one SPI transaction repeat step 2 for each byte. As an example, the following sequence will write a 16-bit value to a specified address in the SPI Flash to be used as a version identifier for an ASP program.

```
void I²C_WriteFlash(uint32_t addr, uint16_t data)
{
  I²C_WriteReg(173, 0x19);  // Start SPI
  I²C_WriteReg(174, 0x06);  // Write Enable Command
  I²C_WriteReg(173, 0x18);  // End SPI

  I²C_WriteReg(173, 0x19);  // Start SPI
  I²C_WriteReg(174, 0x02);  // Page Program Command

  I²C_WriteReg(174, addr >> 16);  // 24-bit Address
  I²C_WriteReg(174, addr >> 8);
  I²C_WriteReg(174, addr);

  I²C_WriteReg(174, data >> 8);  // 16-bit Data
  I²C_WriteReg(174, data);

  I²C_WriteReg(173, 0x18);  // End SPI
}
```

SPI Read

The data byte received on the SPI master interface is stored in Register 252 SPI_MASTER_DATA_IN. The last byte of data stored can be read back at any time with a read-register command. Sequential SPI reads can be efficiently performed by automatically triggering after each read-register command while the Register 173 [1] SPI_M_SEND_BYTE bit remains low. In this configuration when Register 252 is readback the data currently in it will be transmitted on the I²C or SPI slave interfaces and immediately after the read-register command finishes the SPI master interface will automatically trigger another sequence of 8 bits to load in the next byte of data. During a read-register command whatever data is already stored in Register 174 SPI_MASTER_DATA_OUT will be output again for each read-register command on Register 252.

The following example sequence reads a 16-bit value from a specified address in an SPI Flash.

```
uint16_t I²C_ReadFlash(uint32_t addr)
{
  I²C_WriteReg(173, 0x19);  // Start SPI
  I²C_WriteReg(174, 0x03);  // Read Data Command

  I²C_WriteReg(174, addr >> 16);  // 24-bit Address
  I²C_WriteReg(174, addr >> 8);
  I²C_WriteReg(174, addr);

  I²C_WriteReg(174, 0x00);       // Dummy data to load in first byte from SPI Flash
  uint8_t x1 = I²C_ReadReg(252); // Reads first byte from ES98x3QPRO and then loads second byte form SPI Flash
  I²C_WriteReg(173, 0x18);       // End SPI
  uint8_t x2 = I²C_ReadReg(252); // Reads second byte from ES9841

  return (x1 << 8 | x2);  // Return 16-bit data
}
```

SPI Simultaneous Read and Write

In the default automatic mode, it is not possible to write new data while the data is being read back on the I²C or SPI slave interfaces. This is not an issue with the SPI flash chips which the SPI master interface is intended to be used with. However, there is way to sequence the commands to be able to both read and write data at the same time without the automatic sequencing:

1. While the SPI master is not currently active, load the first byte of data into Register 174
2. Enable the SPI output with Register 173 and set bit [1] high to begin the SPI transaction and output the first byte of data
3. While Register 173 [1] remains high, the first data byte received can be readback (Register 252) without automatically triggering another byte sequence
4. The second byte of data to be transmitted can then be loaded into Register 174, again without automatically triggering a byte sequence.
5. Then Register 173 [1] must be set low and back high again to trigger the next SPI sequence. The sequence will immediately follow the write-register command setting that bit high.
6. Afterwards the data received can be readback from Register 252 and the next byte loaded into Register 174 again.
7. To end the SPI transaction set Register 173 [0] low and the chip select will immediately be set high.

As long as Register 173 [1] is high, data can be written and read from the SPI master interface without automatically triggering the SPI master output. Any time the bit is set high the SPI master interface will output the data currently in Register 174 and replace the data in readback Register 252. This process to manually read and write takes four read/write register commands for each byte of data to be transmitted on the SPI master interface.

```
I²C_WriteReg(174, 0x03); // Load first data byte
I²C_WriteReg(173, 0x1B); // Start SPI
I²C_ReadReg(252);        // Read first data byte

I²C_WriteReg(174, 0x12); // Load second data byte
I²C_WriteReg(173, 0x19); // Toggle Send Byte bit
I²C_WriteReg(173, 0x1B);
I²C_ReadReg(252);        // Read second data byte

I²C_WriteReg(173, 0x18); // End SPI
```

SPI Serial Flash Control & Shift Register Control

The ES9291s SPI Master Interface can interact with a multitude of SPI Devices such as Serial Flash Controls and Shift Registers.

SPI Serial Flash can be used to store the programmable instructions and coefficients for the ASP2. The programming will change depending on the specific architecture of the SPI flash and the MCU used to send the instructions. For an application note on the ASP2, please ask your FAE or Distributor for availability.

The SPI Master Interface can also be used to interact with shift registers, effectively adding a serial to parallel converter to the ES9291.

For more information on the SPI Master Interface and its applications please ask your FAE or Distributor for the Application Note.

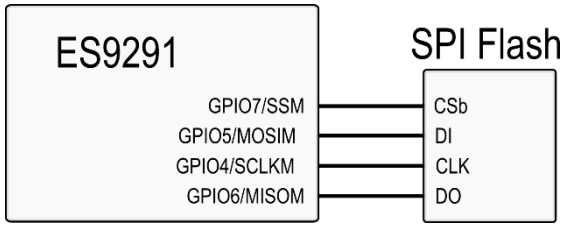


Figure 16 - Example SPI Flash Schematic

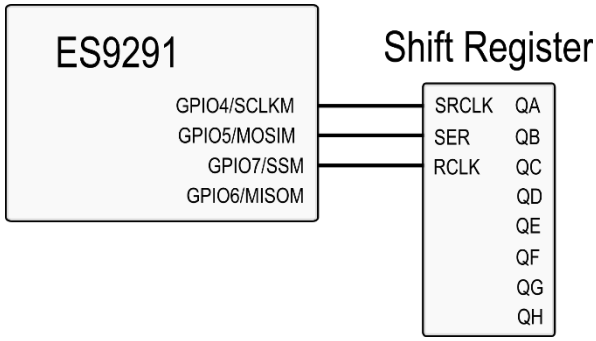


Figure 17 - Example SPI Shift Register Schematic

ASP2 (Audio Signal Processor)

The ES9291 SMART CODEC incorporates 2 of the 2nd generation ESS Audio Signal Processors (ASP2) that allow customers to integrate their preferred audio algorithms by using ESS' proprietary SABRE Intelligence Studio (SI Studio) graphical software tool. The ADC and DAC ASP2s can be programmed with different instruction sets and coefficients, allowing for independent operation of each path.

The ES9291's ASP2 is a very versatile Audio Signal Processor that can allow up to 512 instructions per sample depending on sample rate. It has a 32-bit internal data path with real-time operation. The ASP2 can be programmed using the slave I²C, slave SPI interfaces or with the SPI master interface with an optional external SPI Flash memory for very fast program loading and for storing multiple configuration programs.

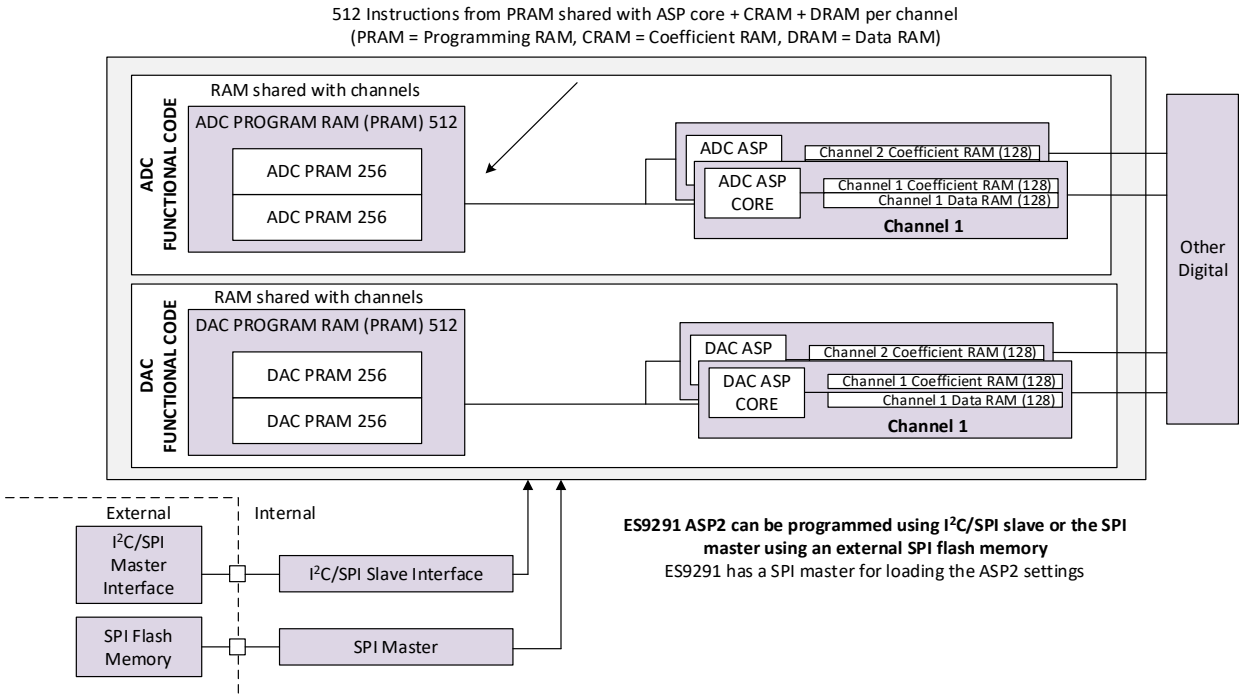


Figure 18 - ASP2 Overview

The ASP2 can be programmed to represent (among others):

- High-efficiency IIR/Biquad filters
- Mixers
- Parametric Equalizers (PEQ), including 25 band PEQs
- Multi-band Dynamic Range Compression (DRC) operations
- Automatic Gain Limiters (AGL)
- Specialty filters including Crossovers & RIAA Equalization pre-emphasis filters
- Stereo Widening
- Audio Expansion and Compression

The integration of the ASP2 into the datapath alleviates processing requirements on the system processor and helps simplify system design.

The ES9291's ASP2 can be programmed using ESS' proprietary SABRE Intelligence Studio (SI Studio) graphical software tool. For more information on the ASP2 or SI Studio tool, please contact your local ESS FAE or distributor for availability.

Advanced Mixing

In addition, the ES9291 allows for inter-path mixing by using the ASP2's Input3. Each path (ADC and DAC) can mix their audio into the other path's ASP2 by using the Pre or Post ASP2 mix point as an input. This allows for advanced mixing between the ADC and DAC paths.

In addition to cross path mixing, Input3 can input status flags from GPIOs by setting ASP_(ADC/DAC)_IN3_SEL_CHx = 1'b1. The respective GPIO must be free to use, ie not currently in use by any encoder, decoder, or transcoder.

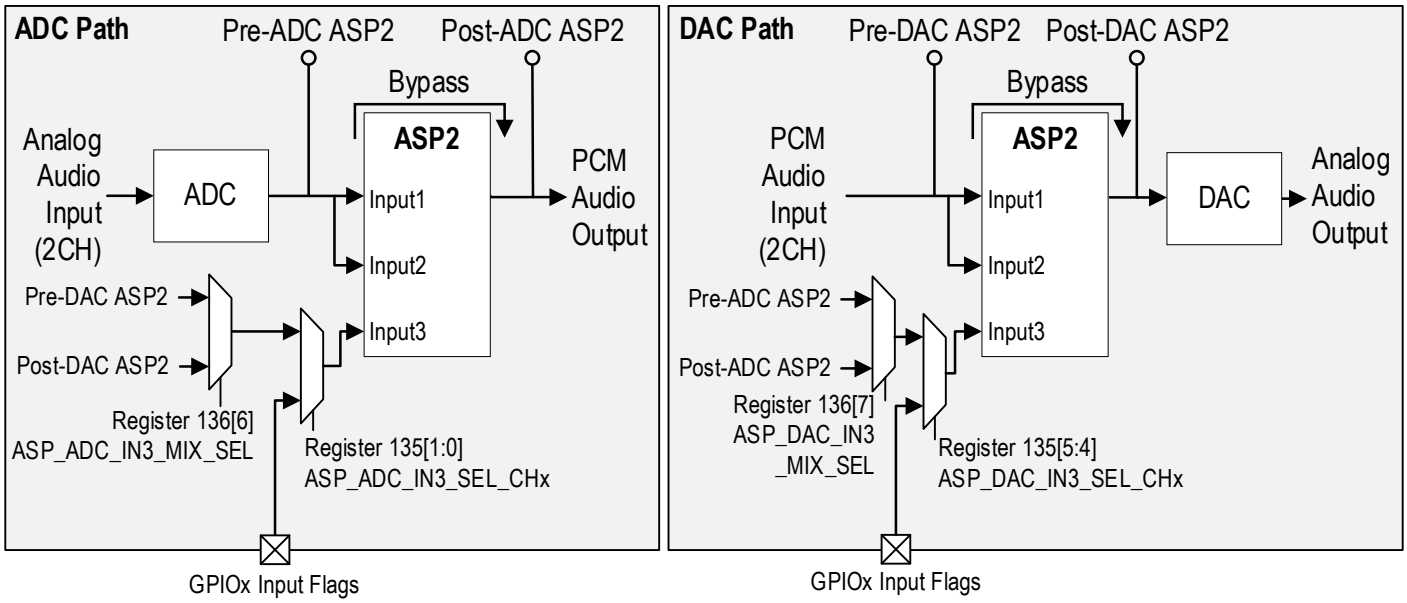


Figure 19 - ES9291 ASP2 Advanced Mixing

Advanced Mixing Registers

- Register 135[5:4] ASP_DAC_IN3_SEL_CHx
- Register 135[1:0] ASP_ADC_IN3_SEL_CHx
- Register 136[7] ASP_DAC_IN3_MIX_SEL
- Register 136[6] ASP_ADC_IN3_MIX_SEL

ADC Digital Signal Path

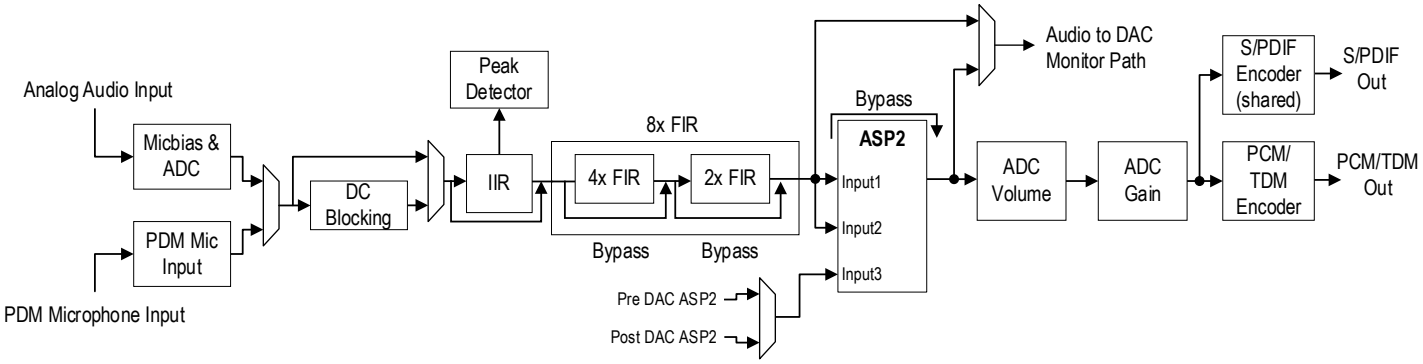


Figure 20 - ADC Digital Signal Path

Mic Bias

The ES9291 integrates a Microphone Bias for using Analog microphones as one of the ADC's analog inputs. The bias' voltage can be set using the following registers:

Mic Bias Registers

- Register 82[6] MB_VR_BYPB
- Register 82[3] MB_EN
- Register 82[2:0] MB_VR_SET

DC Blocking

The integrated DC Blocking filter exhibits a high cutoff frequency (-3dB @ 0.25Hz).

DC Blocking Registers

- Register 66[5, 4] DC_BLOCK_EN_CHx

ADC IIR

The IIR filter can be bypassed using Register 64[2:0] ADC_BYPASS_IIR

ADC 8x FIR

Selection of the 8x Interpolation filter is chosen from 8 pre-programmed filter shapes. For more information on filters see ADC: PCM Filter Latency.

ADC 8x FIR Registers

- Register 64[7:5] ADC_FILTER_SHAPE
- Register 64[4] ADC_BYPASS_FIR2X
- Register 64[3] ADC_BYPASS_FIR4X

Peak Detector

Peak Detector Enable Registers

- Register 75[0,1] PEAK_DETECT_EN_CHx

Peak Flag GPIO Registers

- Register 58[0] ADC_DET_FLAG_SEL = 1'b0
- Register 58[1] ADC_LIVE_FLAG_EN
- Register 58[2] GPIO_AND_PEAK_DET
- Register 58[4] GPIO_OR_PEAK_DET
- Register 58[6] ADC_FLAG_CH_SEL

Peak Flag Latching and Readback Registers

- Register 76[6] LOCK_PEAK_VALUE
- Register 237 [2, 3] PEAK_FLAG_LAT_CHx
- Register 237[0, 1] PEAK_FLAG_CHx
- Register 238-241 PEAK_LEVEL_CHx

Peak Flag Decay Rate and Threshold Registers

- Register 76[4:0] PEAK_DECAY_RATE
- Register 77-78 PEAK_THRESH_CHx

$$N(t) = N_0 exp\left(\frac{-MCLK\_24M * t}{2^{decay\_rate+9}}\right)$$

$$N(t) = N_0 - \frac{20 * MCLK\_24M * t}{ln(10) * 2^{decay\_rate+9}}[dB]$$

$$\frac{dN}{dt} = -\frac{N * MCLK\_24M}{2^{decay\_rate+9}}[1/s]$$

$$\text{threshold [dB]} = 20 \cdot \log10\left(\left(\frac{PEAK\_THRESH\_CHx}{2^8 - 1}\right)\right)$$

N_0: Initial Level
N(t): Level
decay_rate = Reg 76[4:0]PEAK_DECAY_RATE
MCLK_24M = 22.5792/24.576MHz
(Reg 5[4] MCLK_24M_DIV2 must be set if using a 45.1584/49.152MHz MCLK)

ADC Volume

The ADC Volume Control is intended for use during audio playback. Each channel can be digitally attenuated from +1dB to -126dB in 0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME UP RAMP RATE and VOLUME DOWN RAMP RATE registers.

ADC Volume Registers

- Register 67 ADC VOLUME CH1
- Register 68 ADC VOLUME CH2
- Register 24 VOLUME UP RAMP RATE
- Register 25 VOLUME DOWN RAMP RATE

ADC Gain

The ES9291 has an additional digital gain that can be added through registers. Settings for +0dB to +42dB in +6dB steps are available.

ADC Gain Registers

- Register 69[6:4] ADC_DIGITAL_GAIN_CH2
- Register 69[2:0] ADC_DIGITAL_GAIN_CH1

DAC Digital Signal Path

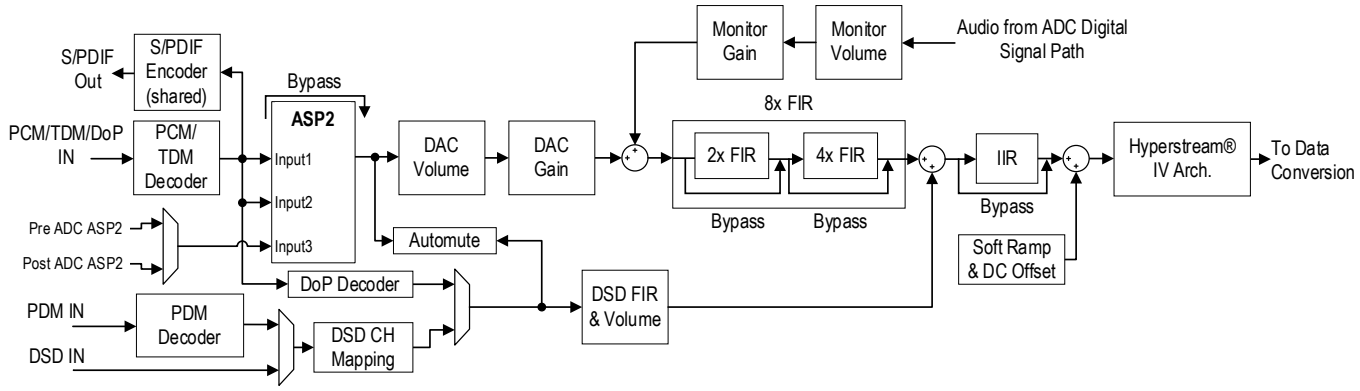


Figure 21 - DAC Digital Signal Path

Automute

In HW Mode Automute is controlled by the state of the HW4 pin (Pin 26), the pin must be in the "Pull 1" or "1" state to enable Automute.

The DAC in the ES9291 features an automute that triggers when the signal is below the specified level for longer than the specified time. The automute will disengage when the signal is above the specified off value for the same amount of time.

The DSD path also has its own automute that will check for the DSD mute pattern.

Note: Automute will not engage if the Direct Monitor is running.

$$Time[s] = \frac{2^{18}}{AUTOMUTE\_TIME * FS}$$

$$Level[dB] = \frac{20 * log_{10}(AUTOMUTE\_LEVEL)}{(2^{16} - 1) * 2^{7}}$$

DAC PCM Automute Registers

- Register 94[1:0] AUTOMUTE_EN_CHx
- Register 95-96[10:0] AUTOMUTE_TIME
- Register 97-98 AUTOMUTE_LEVEL
- Register 99-100 AUTOMUTE_OFF_LEVEL

DAC DSD Automute Registers

- Register 95-96[14] DSD_DC_AM_EN
- Register 95-96[13] DSD_MUTE_AM_EN

DAC Volume

The DAC Volume Control is intended for use during audio playback. Each channel can be digitally attenuated from -126dB to +1dB in +0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME UP RAMP RATE and VOLUME DOWN RAMP RATE registers.

DAC Volume Registers

- Register 84 DAC VOLUME CH1
- Register 85 DAC VOLUME CH2
- Register 24 VOLUME UP RAMP RATE
- Register 25 VOLUME DOWN RAMP RATE

DAC Gain

The ES9291 has an additional digital gain that can be added through registers. Settings for +0dB to +42dB in 6dB steps are available.

DAC Gain Registers

- Register 88[6:4] DAC_DIGITAL_GAIN_CH2
- Register 88[2:0] DAC_DIGITAL_GAIN_CH1

DAC 8x FIR

Selection of the 8x interpolation filter is chosen from 8 pre-programmed filters. The 2x and 4x filter can be bypassed individually or together. For more information on filters see the Pre-Programmed Digital Filters section.

DAC FIR Registers

- Register 83[2:0] DAC_FILTER_SHAPE
- Register 83[3] BYPASS_FIR2X
- Register 83[4] BYPASS_FIR4X

DAC IIR

The IIR filter can be bypassed using Register 83[5] BYPASS_IIR

Soft Ramp & DC Offset

The ES9291 saves power by ramping to ground during a normal mute condition. This includes automute, register mute, and GPIO mute.

A DC offset can be added to the CH1 datapath signal in 100uV increments.

Note: The Soft Ramp Time has a maximum value of 4'd12.

Soft Ramp & DC Offset Registers

- Register 91[5] MUTE_RAMP_TO_GROUND
- Register 91[4:0] SOFT_RAMP_TIME
- Register 92-93 DC_OFFSET

$$\text{Soft Ramp Time [s]} = \frac{2^{16} \cdot 2^{\text{SOFT\_RAMP\_TIME}}}{MCLK \cdot 2^{\sim\text{MCLK\_24M\_DIV2}}}$$

Direct Monitor Volume

Signals from the ADC digital path can be passed into the DAC digital path using the Direct Monitor, either individually to their respective channels or in a mono configuration where both ADC channels will be passed to the DAC channel. The audio will be taken from either the Pre or Post ASP path indicated in the ADC Digital Signal Path, configured with DIR_MON_ADC_SEL.

The Direct Monitor Volume Control is intended for use during audio playback. Each channel can be digitally attenuated from +1dB to -126dB in 0.5dB steps. When a new volume level is set, the attenuation circuit will ramp softly to the new level at a rate specified in the VOLUME UP RAMP RATE and VOLUME DOWN RAMP RATE registers.

Monitor Volume Registers

- Register 86 DIRECT MONITOR VOLUME CH1
- Register 87 DIRECT MONITOR VOLUME CH2
- Register 89[5:4] DIR_MON_MONO_CHx
- Register 89[3:2] DIR_MON_VOL_PHASE_INV_CHx
- Register 90[1:0] DIR_MON_MUTE_CHx
- Register 91[6] DIR_MON_ADC_SEL

Note: Using the Direct Monitor will disable Automute functionality.

Direct Monitor Gain

The Direct Monitor uses the same gain settings as the ADC Gain does.

Monitor Gain Registers

- Register 69[6:4] ADC_DIGITAL_GAIN_CH2
- Register 69[2:0] ADC_DIGITAL_GAIN_CH1

GPIO Configuration

GPIO_CONFIG	Function	I/O Direction
0	Analog Outputs Off	Shutdown
1	Mute DAC Channels	Input
2	Clock Valid Flag	Output
3	PLL Locked Flag	Output
4	DAC Minimum Volume Flag	Output
5	DAC Automute Status	Output
6	DAC Soft Ramp Done Flag	Output
7	ADC Detection Flags	Output
8	OR of Status Bits	Output
9	S/PDIF Stream	Output
10	PWM Signal	Output
11	ASP Status Flags In	Input
12	ASP Status Flags Out	Output
13	Output 1'b0	Output
14	Reserved	-
15	Jack Detect Flag	Output

Table 16 - GPIO Configuration

GPIOx Default states:

GPIO1-8: Analog Shutdown

Analog Outputs Off

The GPIO is shutdown and has no functionality.

Mute DAC Channels

Mute both DAC channels and Direct Monitor.

Clock Valid Flag

Outputs HIGH if a MCLK source is detected. Outputs LOW when clock is removed or not present.

Relevant Registers

- Register 7[0] CLK_FAULT_DET_EN must be asserted for the clock valid flag to operate.

PLL Locked Flag

Outputs HIGH if the PLL is locked.

Relevant Registers

- Register 7[1] FORCE_PLL_LOCK must be 1'b0 to see the status of the PLL, else this flag will output HIGH.

DAC Minimum Volume Flag

Outputs HIGH when the DAC is muted. This can occur from manual muting, automuting, and setting volume to 0xFF.

Relevant Registers

- Register 59[0] GPIO_AND_VOL_MIN sets the output to be the logical AND of both channels' mute flags.
- Register 59[3] GPIO_OR_VOL_MIN sets the output to be the logical OR of both channels' mute flags.
- Register 59[6] DAC_FLAG_CH_SEL selects which of the individual DAC channel flags to output.

DAC Automute Status

Outputs HIGH when the DACs automute condition is met.

Relevant Registers

- Register 59[1] GPIO_AND_AUTOMUTE sets the output to be the logical AND of both channels' automute flags.
- Register 59[4] GPIO_OR_AUTOMUTE sets the output to be the logical OR of both channels' automute flags.
- Register 59[6] DAC_FLAG_CH_SEL selects which of the DAC channel flags to output.

DAC Soft Ramp Done Flag

Outputs HIGH when the DAC is neither ramping up nor down.

Relevant Registers

- Register 59[2] GPIO_AND_SS_RAMP sets the output to be the logical AND of both channels' automute flags.
- Register 59[5] GPIO_OR_SS_RAMP sets the output to be the logical OR of both channels' automute flags.
- Register 59[6] DAC_FLAG_CH_SEL selects which of the DAC channel flags to output.

ADC Detection Flag

Outputs the selected ADC Peak Detector and Overload flags. The live or latched version of the flags can be output, by default this will output the latched peak detector flag.

Relevant Registers

- Register 58[0] ADC_DET_FLAG_SEL determines which flag is output from the GPIO
- Register 58[1] ADC_LIVE_FLAG_EN allows the live version of the flag to be output from the GPIO
- Register 58[2] GPIO_AND_PEAK_DET sets the GPIO output to be the logical AND of all channels ADC Peak flags
- Register 58[3] GPIO_AND_OVERLOAD sets the GPIO output to be the logical AND of all channels ADC Overload flags
- Register 58[4] GPIO_OR_PEAK_DET sets the GPIO output to be the logical OR of all channels ADC Peak flags
    - Overrides GPIO_AND_PEAK_DET
- Register 58[5] GPIO_OR_OVERLOAD sets the GPIO output to be the logical OR of all channels ADC Overload flags
    - Overrides GPIO_AND_OVERLOAD_DET
- Register 58[6] ADC_FLAG_CH_SEL will output the flag of a specific channel is all GPIO_AND_xx and GPIO_OR_xx are 1'b0

OR of Status Bits

Bitwise OR of all masked status bits. This includes the JDET, ADC Overload, and Peak Detect flags.

Relevant Registers

- Register 30 STATUS BITS MASK
- Register 31 STATUS BITS CLEAR

S/PDIF Stream

Outputs the S/PDIF stream from the S/PDIF Encoder.

PWM Signal

Outputs a configurable PWM signal. The frequency and duty cycle of the PWM signal can be calculated with the following equations:

$$frequency\ [Hz] = \frac{MCLK}{PWM\_FREQ + 1}$$

$$Duty\ Cycle\ [\%] = \left(\frac{PWM\_COUNT}{PWM\_FREQ + 1}\right) \times 100$$

Relevant Registers

- Register 60 PWM_COUNT
- Register 61-62 PWM_FREQ

ASP Status Flags In

Connects the GPIO inputs to the ASP2 core, for use in the ASP2 program. Connects to ASP2 core Input3, with a per-core mux controlling whether the core receives the GPIO inputs or the TDM decoder signal. The mux is controlled with Register 135[5:4, 1:0] ASP_(DAC/ADC)_IN3_SEL_CHx.

ASP Status Flags Out

Connects the ASP2 core to the GPIO outputs, allowing flags set by the ASP2 program to be read externally. The selected core is determined by Register

Output 1'b0

Outputs a constant 1'b0. Invert to output a constant 1'b1.

Jack Detect Flag

Outputs 1'b1 when a headphone jack is detected. Requires Register 7[7] JDET_EN = 1'b1.

Pre-Programmed Digital Filters

The ES9291 has 8 pre-programmed digital filters. The latency for each filter reduces (scales) with increasing sample rates. (See Register 64[7:5] ADC_FILTER_SHAPE and Register 83[2:0] DAC_FILTER_SHAPE for configuration)

#	Filter	Description
1	Minimum Phase (default)	Version 2 of minimum phase fast roll-off (#6) with less ripple and more image rejection
2	Linear Phase Apodizing Fast Roll-Off	Full image rejection by FS/2 to avoid any aliasing, with smooth roll-off starting before 20k.
3	Linear Phase Fast Roll-Off	Sabre legacy filter, optimized for image rejection @ 0.55FS
4	Linear Phase Fast Roll-Off Low-Ripple	Sabre legacy filter, optimized for in-band ripple
5	Linear Phase Slow Roll-Off	Sabre legacy filter, optimized for lower latency, but symmetric impulse response
6	Minimum Phase Fast Roll-Off	Low latency, minimal pre ringing and low passband ripple, image rejection @ 0.55FS
7	Minimum Phase Slow Roll-Off	Lowest latency at the cost of image rejection
8	Minimum Phase Fast Roll-Off Low Dispersion	Provides a nice balance of the low latency of minimum phase filters and the low dispersion of linear phase filters. Minimal pre-ringing is added to achieve the low dispersion in the audio band.

Table 17 - Pre-Programmed Digital Filter Descriptions

Note: Minimum phase filters are asymmetric filters that work to minimize the pre-echo of the filter, while still maintaining an excellent frequency response and they peak earlier than linear phase filters, resulting in a lower group delay. Minimum phase filters usually feature zero cycles of pre-echo, which can result in improved audio quality.

ADC: PCM Filter Latency

The following table shows the simulated latency of each filter across different sample rates. Measurements were taken from the external impulse response prior to being down sampled to 1FS. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Filter Shape \ Frequency [kHz]	44.1 / 48	88.2 / 96	176.4 / 192	352.8 / 384
Minimum Phase (default)	5.31 / FS	5.50 / FS	5.74 / FS	6.36 / FS
Linear Phase Apodizing Fast Roll-Off	35.06 / FS	35.25 / FS	35.62 / FS	36.23 / FS
Linear Phase Fast Roll-Off	35.31 / FS	35.50 / FS	35.75 / FS	36.36 / FS
Linear Phase Fast Roll-Off Low-Ripple	34.94 / FS	35.13 / FS	35.37 / FS	35.98 / FS
Linear Phase Slow Roll-Off	7.94 / FS	8.12 / FS	8.37 / FS	8.86 / FS
Minimum Phase Fast Roll-Off	5.44 / FS	5.50 / FS	5.87 / FS	6.48 / FS
Minimum Phase Slow Roll-Off	4.31 / FS	4.50 / FS	4.74 / FS	5.36 / FS
Minimum Phase Slow Roll-Off Low Dispersion	6.19 / FS	6.25 / FS	6.62 / FS	7.23 / FS

Table 18 - ADC: PCM Filter Latency

ADC: PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-100.4 dB	0.55 FS			Hz
Group Delay		2.90/FS		9.23/FS	s
Flatness (ripple)	0.0030				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41 FS	Hz
Stop band	-108.9 dB	0.50 FS			Hz
Group Delay			33.25/FS		s
Flatness (ripple)	0.0033				dB

Linear Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-115.5 dB	0.55 FS			Hz
Group Delay			33.38/FS		s
Flatness (ripple)	0.0037				dB

Linear Phase Fast Roll-Off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-82.53 dB	0.55 FS			Hz
Group Delay			33/FS		s
Flatness (ripple)	0.0021				dB

Linear Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.46 FS	Hz
Stop band	-85.02 dB	0.75 FS			Hz
Group Delay			6.05/FS		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 FS	Hz
Stop band	-101.2 dB	0.55 FS			Hz
Group Delay		2.95/FS		9.42/FS	s
Flatness (ripple)	0.0048				dB

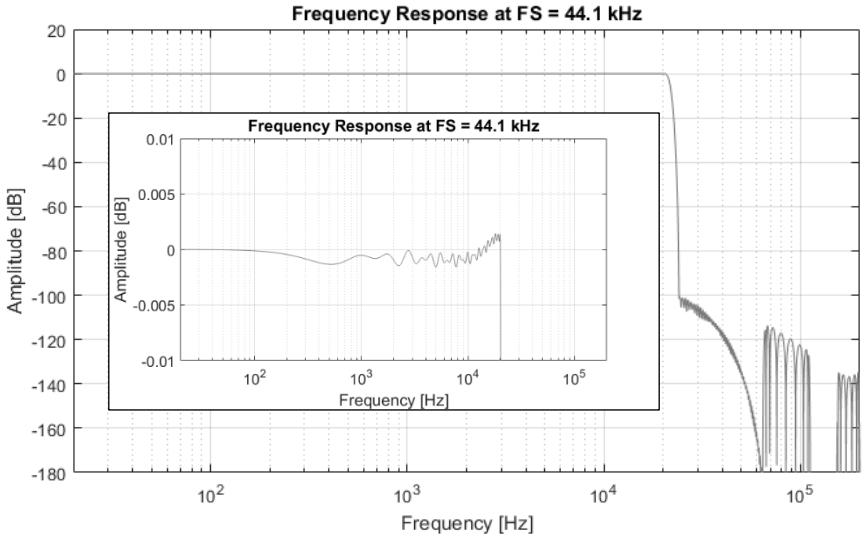
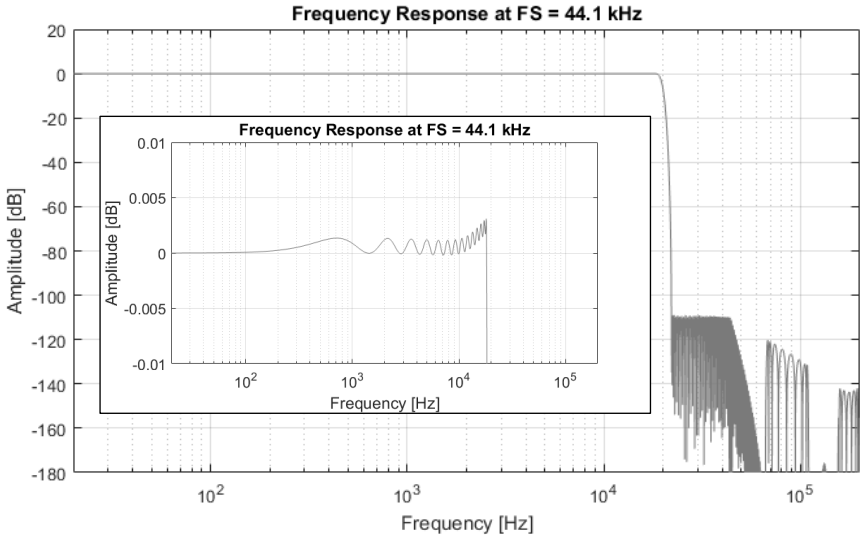
Minimum Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 FS	Hz
Stop band	-90.34 dB	0.80 FS			Hz
Group Delay		2.03/FS		3.51/FS	s
Flatness (ripple)					dB

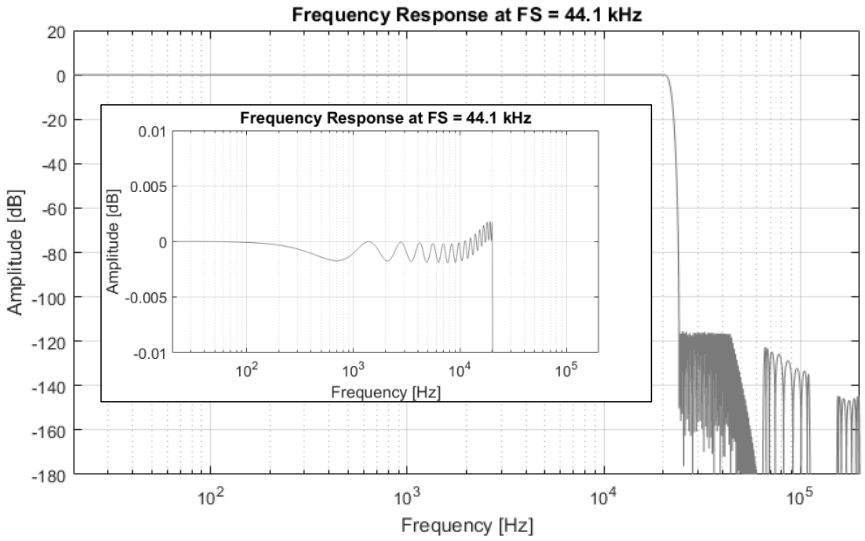
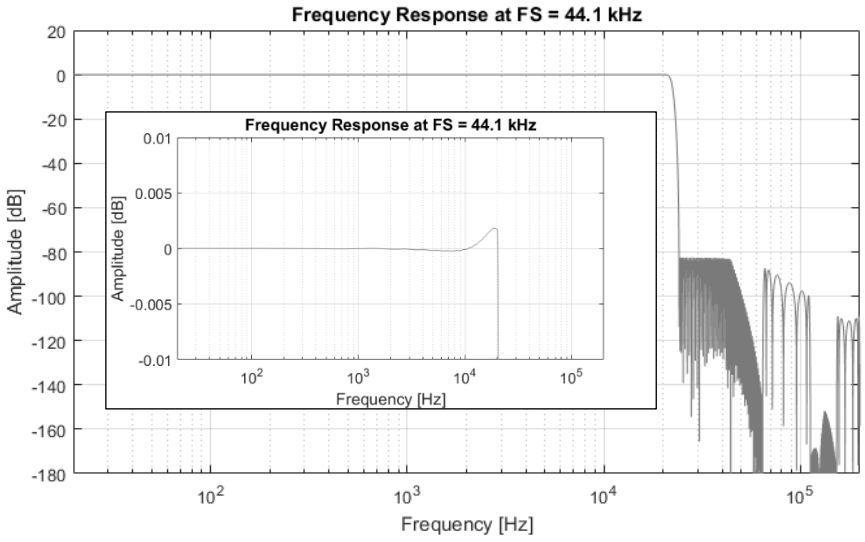
Minimum Phase Slow Roll-Off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.45 FS	Hz
Stop band	-98.8 dB	0.82 FS			Hz
Group Delay		4.12/FS		4.38/FS	s
Flatness (ripple)					dB

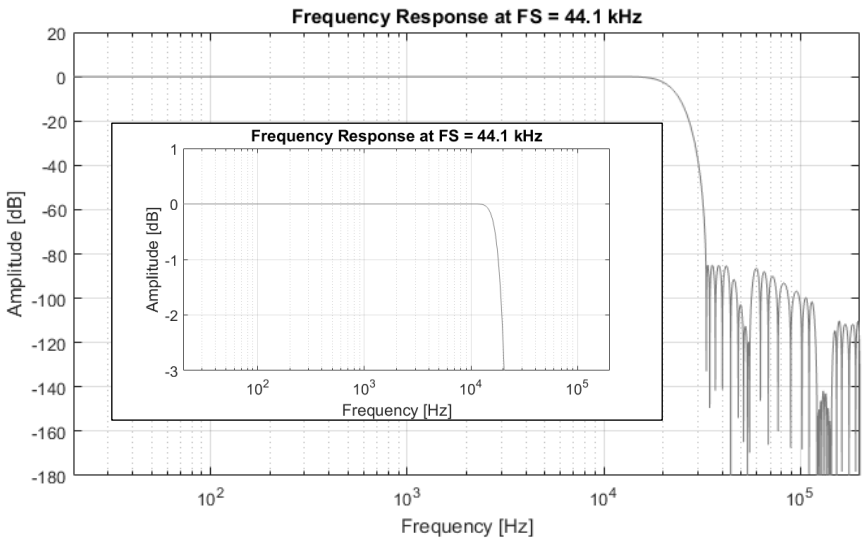
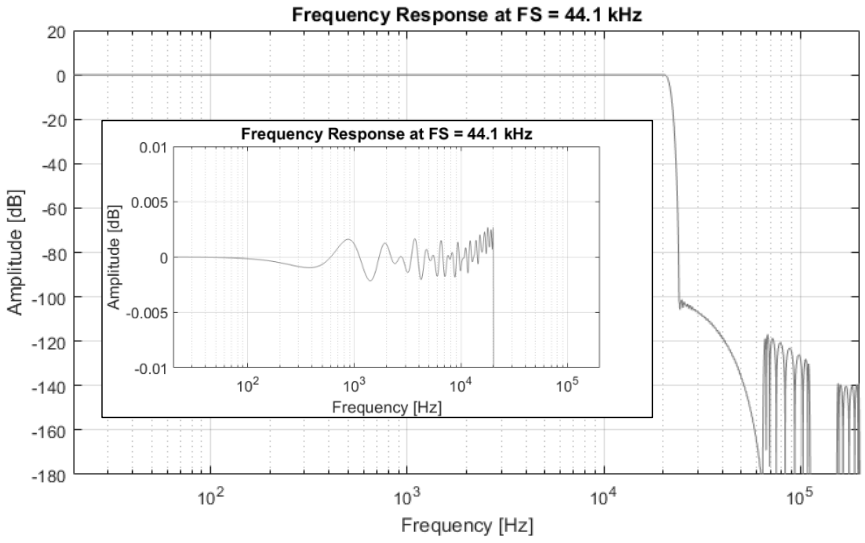
Table 19 - ADC: PCM Filter Properties

ADC: PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

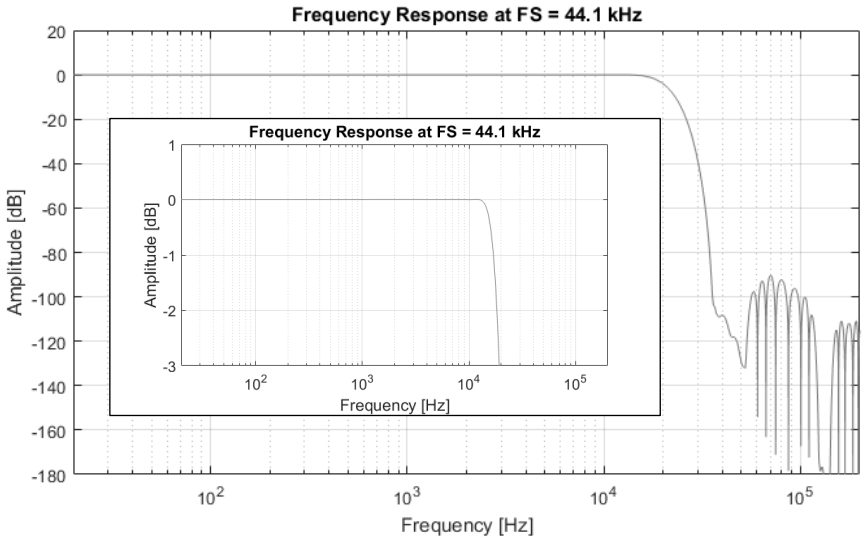
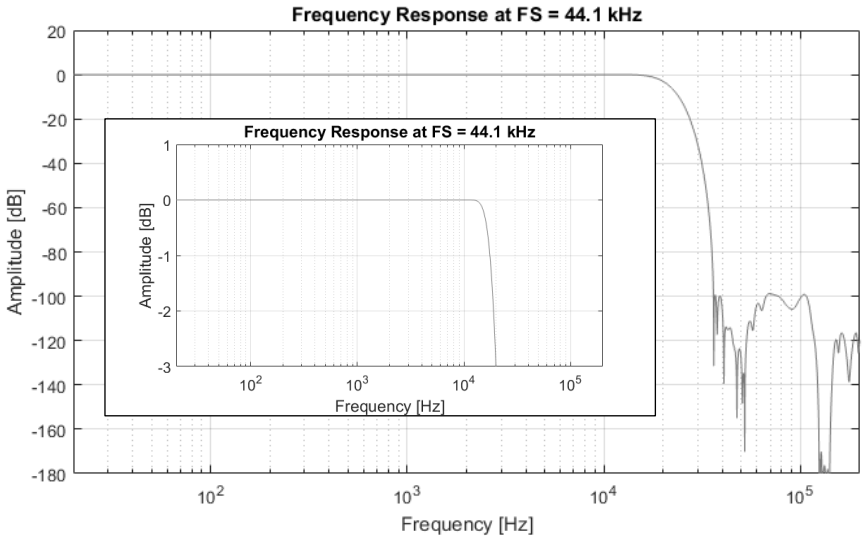
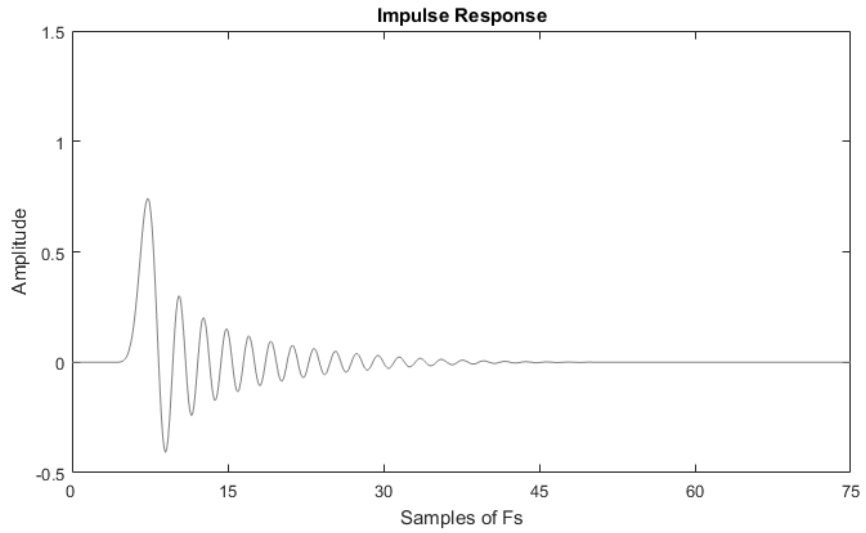
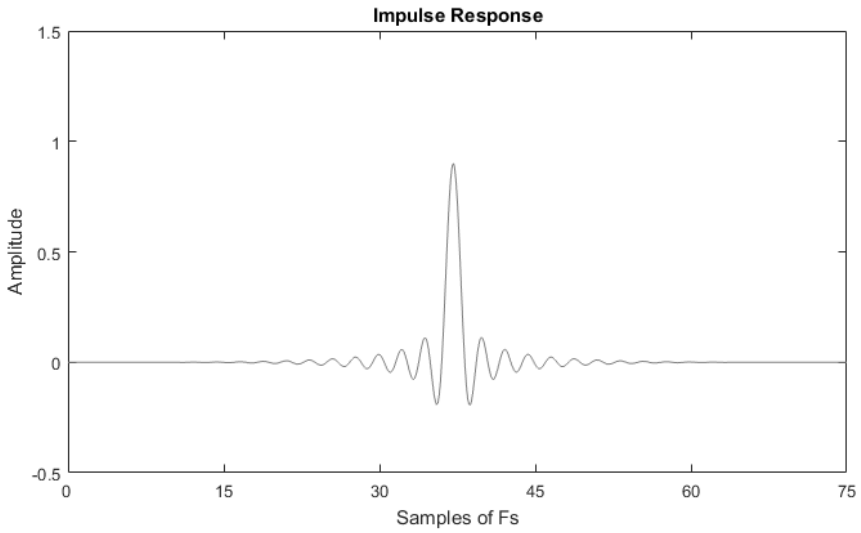
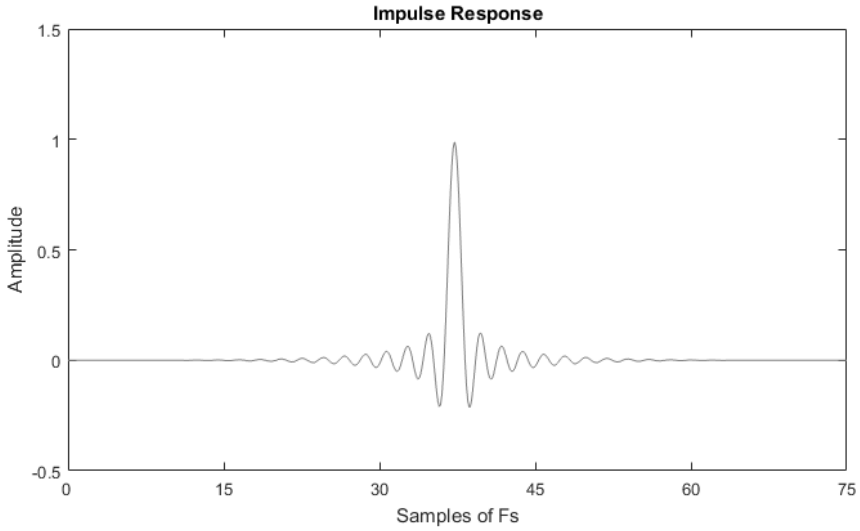
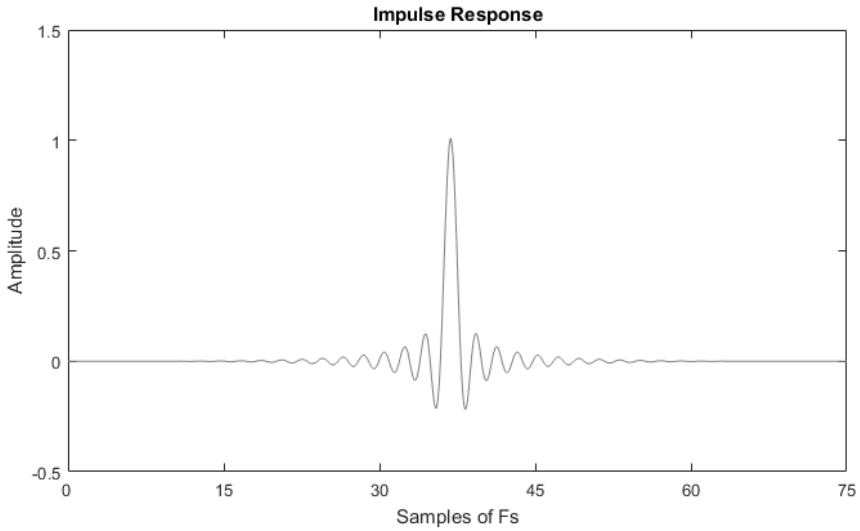
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

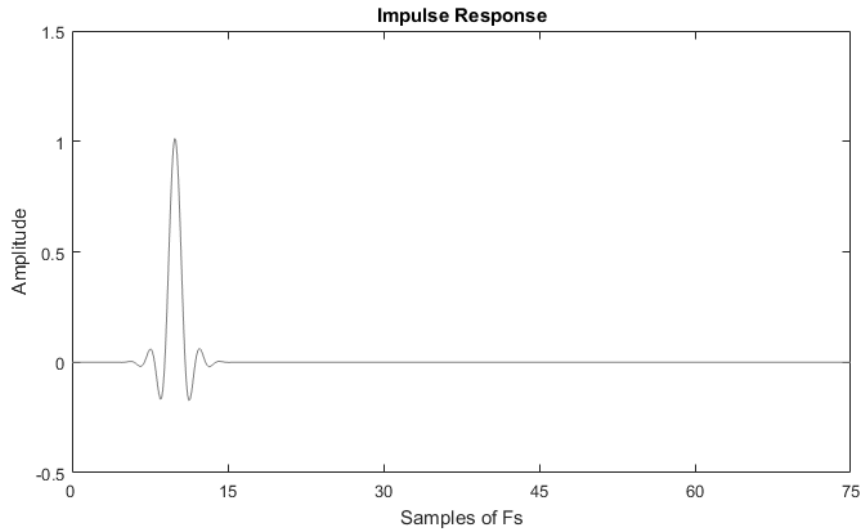
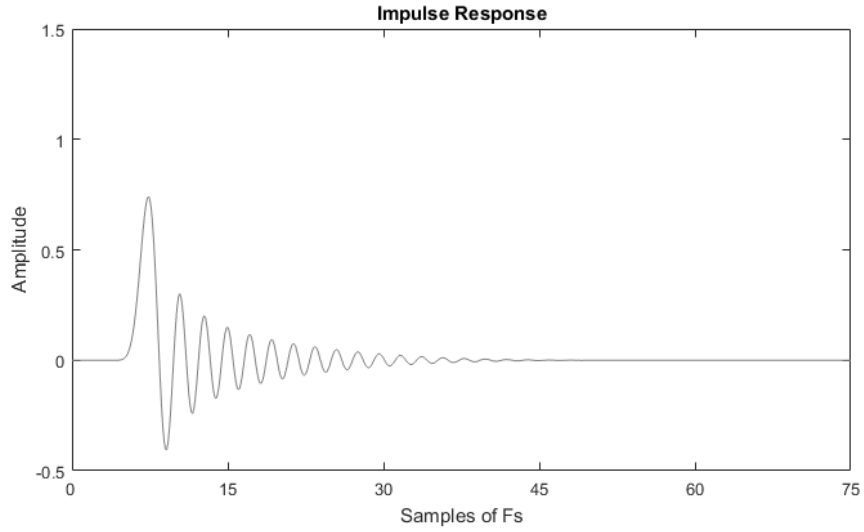
Table 20 - ADC: PCM Filter Frequency Response

ADC: PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They show the decimation path prior to down-sampling to 1FS and are scaled accordingly. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

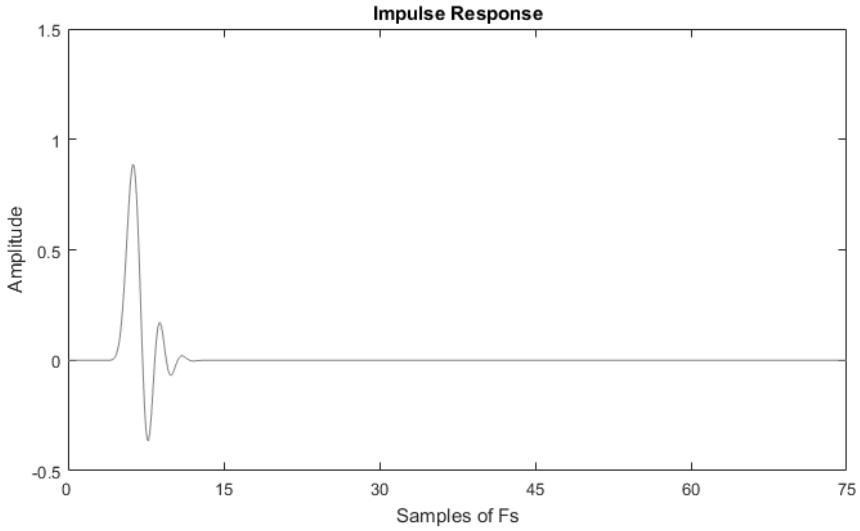
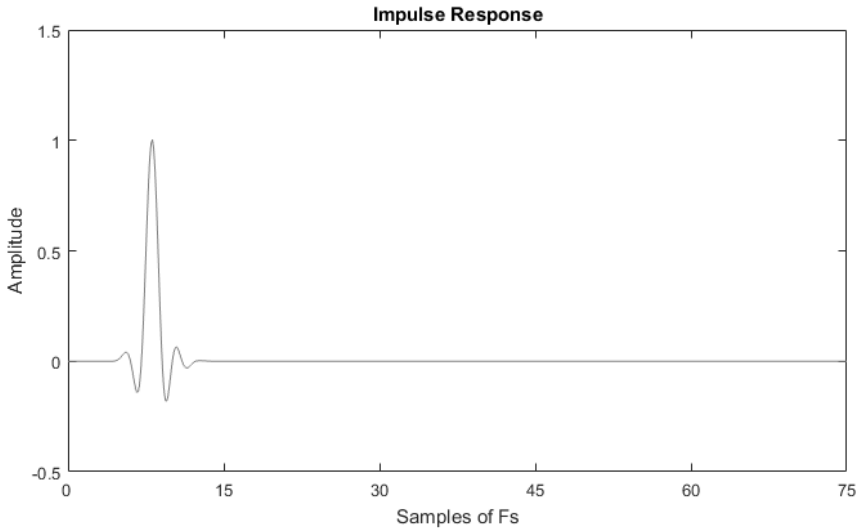
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 21 - ADC : PCM Filter Impulse Response

ADC: 64FS Mode

ADC: Minimum Phase 64FS Mode Latency

The following table shows the simulated latency at 705.6kHz sampling rate and is very similar at 768kHz. Measurements were taken from the external impulse response prior to being down sampled to 1FS. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay(us) @ FS = 705.6 kHz
Minimum Phase Double Rate	5.93 / FS

Table 22 - ADC: Minimum Phase 64FS Latency

ADC: Minimum Phase 64FS Properties

Minimum Phase 64FS Mode					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	-3 dB			0.44 FS	Hz
Stop band	-68.35 dB	0.68 FS			Hz
Group Delay		1.43/FS		3.45/FS	s
Flatness (ripple)					dB

Table 23 - ADC: Minimum Phase 64FS Properties

ADC: Minimum Phase 64FS Frequency Response

This filter gets selected automatically when MCLK/FS = 64. The following frequency response was obtained from software simulations with a sample rate of 705.6kHz

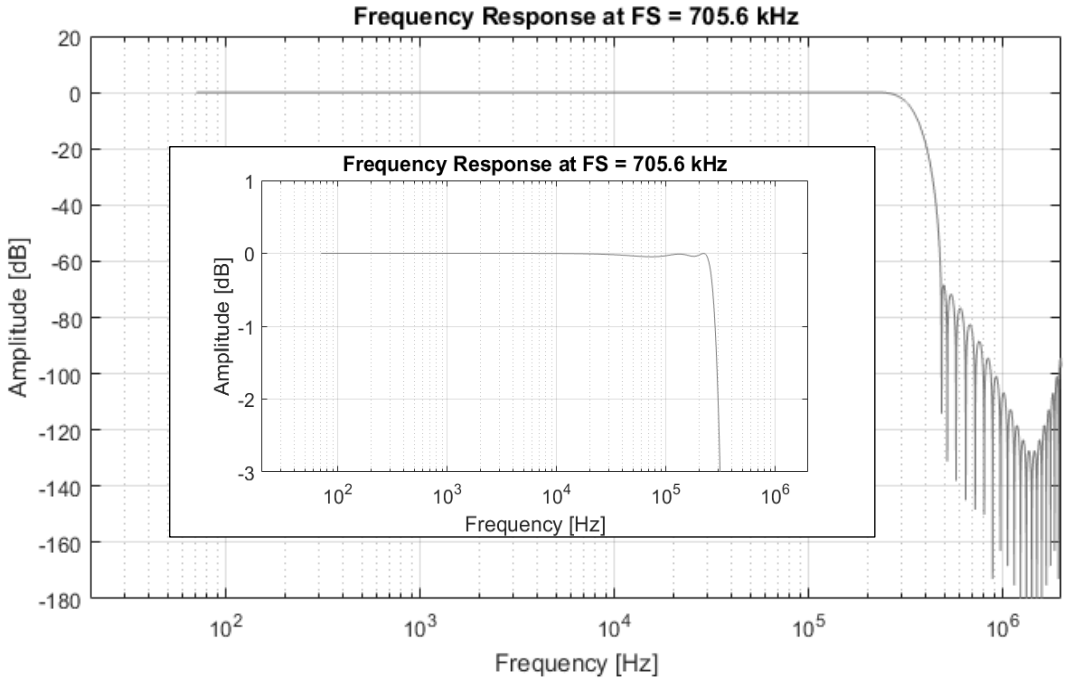


Figure 22 - ADC: Minimum Phase 64FS Frequency Response

ADC: Minimum Phase 64FS Impulse Response

The following impulse responses were obtained from software simulations of these filters. They show the decimation path prior to down-sampling to 1FS and are scaled accordingly. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

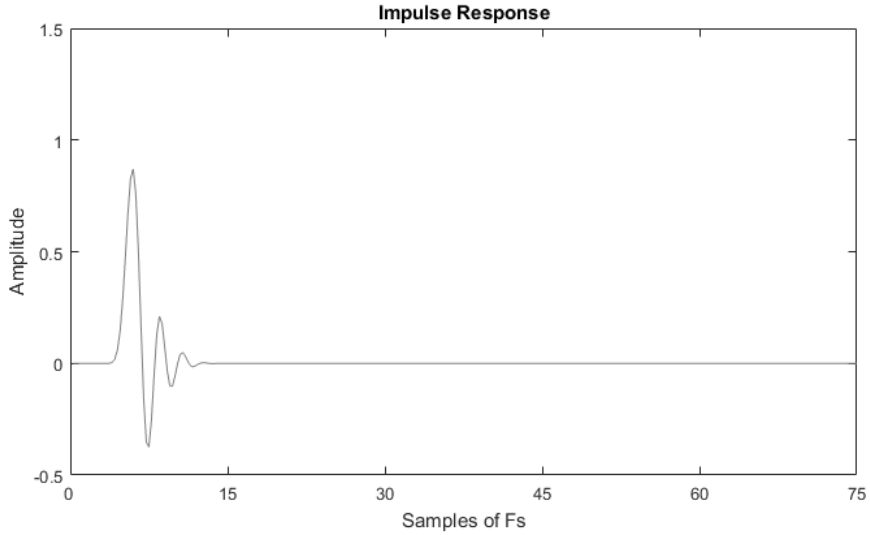


Figure 23 - ADC: Minimum Phase 64FS Impulse Response

DAC: PCM Filter Latency

The following table shows the simulated latency of each filter. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency will reduce (scale) with sampling rate.

Filter Shape \ Frequency [kHz]	44.1 / 48	88.2 / 96	176.4 / 192	352.8 / 384
Minimum Phase (default)	5.78 / FS	5.79 / FS	5.79 / FS	5.80 / FS
Linear Phase Apodizing Fast Roll-Off	35.15 / FS	35.16 / FS	35.16 / FS	35.17 / FS
Linear Phase Fast Roll-Off	35.77 / FS	35.78 / FS	35.78 / FS	35.80 / FS
Linear Phase Fast Roll-Off Low-Ripple	33.71 / FS	33.72 / FS	33.72 / FS	33.73 / FS
Linear Phase Slow Roll-Off	8.21 / FS	8.22 / FS	8.22 / FS	8.23 / FS
Minimum Phase Fast Roll-Off	5.78 / FS	5.79 / FS	5.79 / FS	5.80 / FS
Minimum Phase Slow Roll-Off	4.81 / FS	4.82 / FS	4.82 / FS	4.84 / FS
Minimum Phase Slow Roll-Off Low Dispersion	6.67 / FS	6.68 / FS	6.68 / FS	6.70 / FS

Table 24 - DAC: PCM Filter Latency

DAC: PCM Filter Properties

Minimum Phase					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-96.06 dB	0.55 x fs			Hz
Group Delay		2.90/fs		9.01/fs	s
Flatness (ripple)	0.0013				dB

Linear Phase Apodizing					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.41 x fs	Hz
Stop band	-104.6 dB	0.50 x fs			Hz
Group Delay			32.81/fs		s
Flatness (ripple)	0.0028				dB

Linear Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.45 x fs	Hz
Stop band	-106.8 dB	0.55 x fs			Hz
Group Delay			33.81/fs		s
Flatness (ripple)	0.0032				dB

Linear Phase Fast Roll-Off Low Ripple					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-88.79 dB	0.55 x fs			Hz
Group Delay			31.37/fs		s
Flatness (ripple)	0.0013				dB

Linear Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.44 x fs	Hz
Stop band	-90.49 dB	0.75 x fs			Hz
Group Delay			5.87/fs		s
Flatness (ripple)					dB

Minimum Phase Fast Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band				0.46 x fs	Hz
Stop band	-97.64 dB	0.55 x fs			Hz
Group Delay		2.91/fs		9.14/fs	s
Flatness (ripple)	0.0024				dB

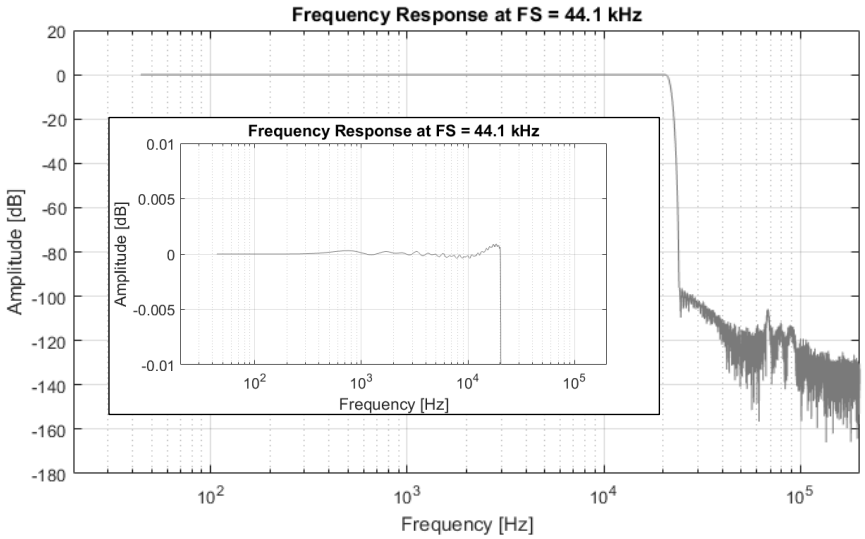
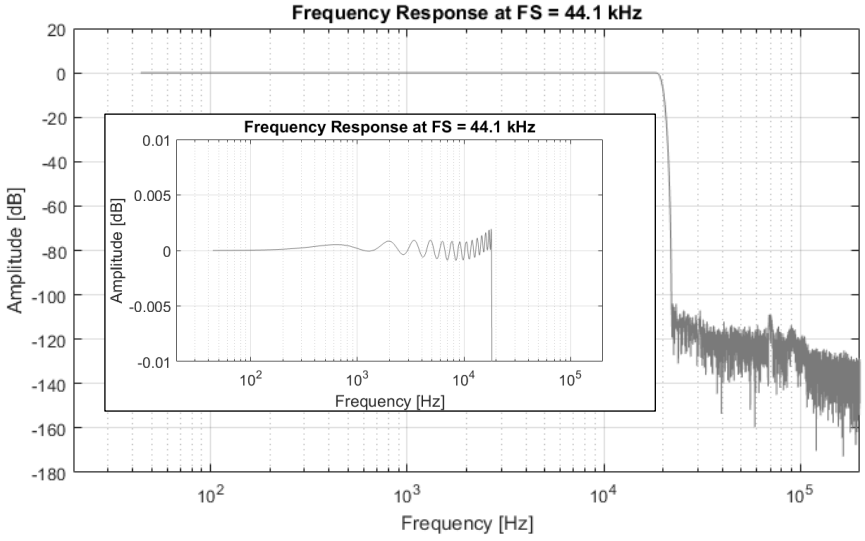
Minimum Phase Slow Roll-Off					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.43 x fs	Hz
Stop band	-90.94 dB	0.80 x fs			Hz
Group Delay		2.08/fs		3.56/fs	s
Flatness (ripple)					dB

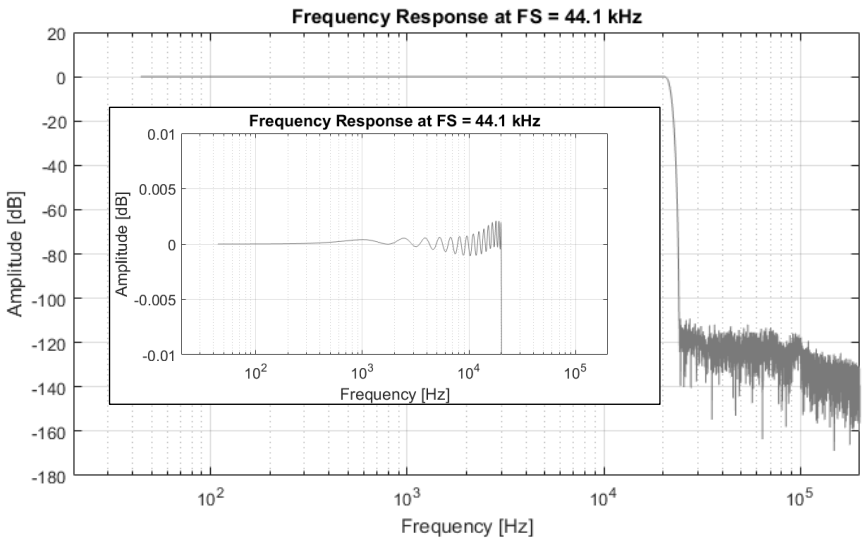
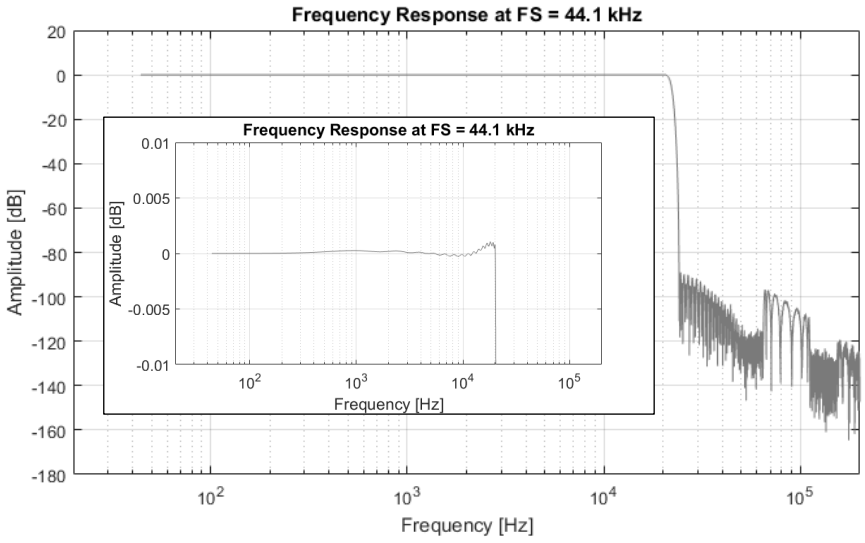
Minimum Phase Slow Roll-Off Low Dispersion					
Parameter	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
Pass band	-3 dB			0.45 x fs	Hz
Stop band	-98.56 dB	0.82 x fs			Hz
Group Delay		4.21/fs		4.42/fs	s
Flatness (ripple)					dB

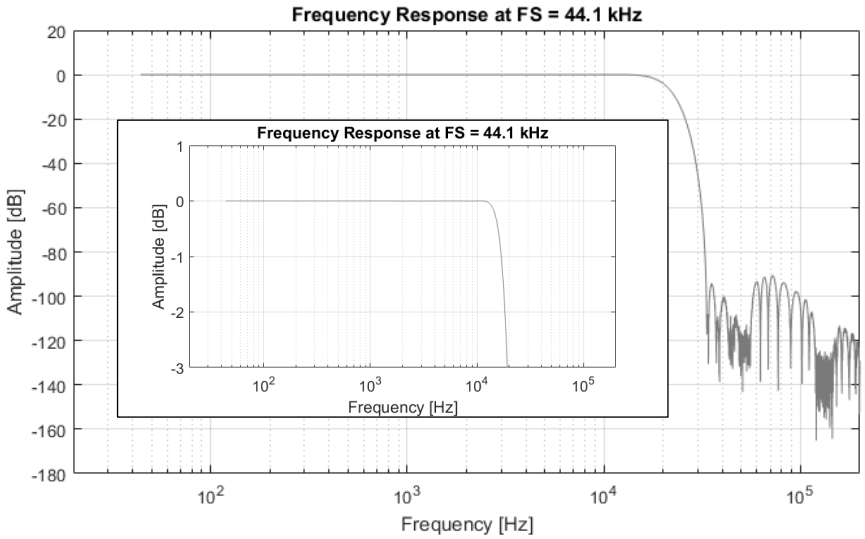
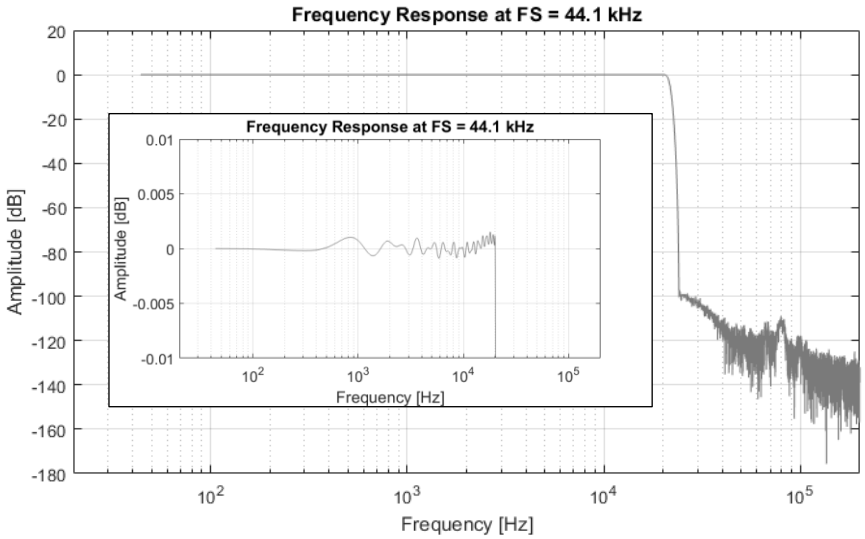
Table 25 - DAC: PCM Filter Properties

DAC: PCM Filter Frequency Response

The following frequency responses were obtained from software simulations of these filters. Simulation sample rate is 44.1kHz.

Filter	Frequency Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

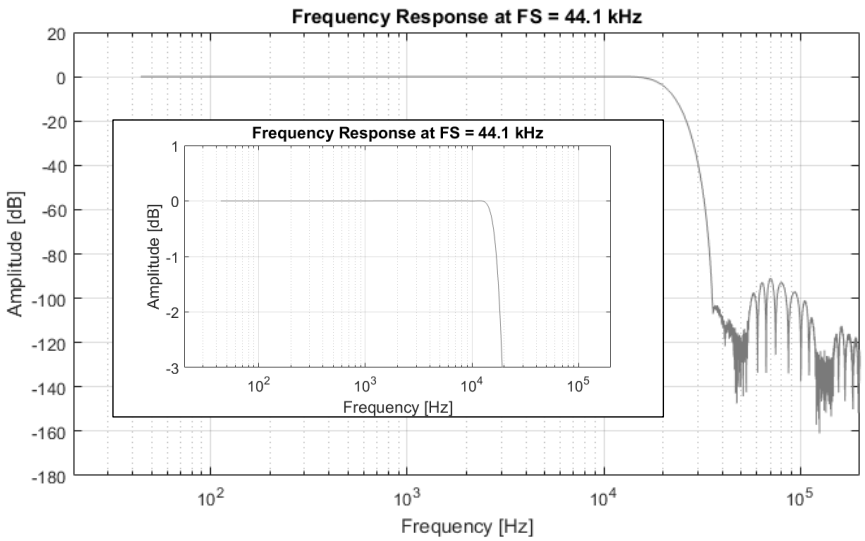
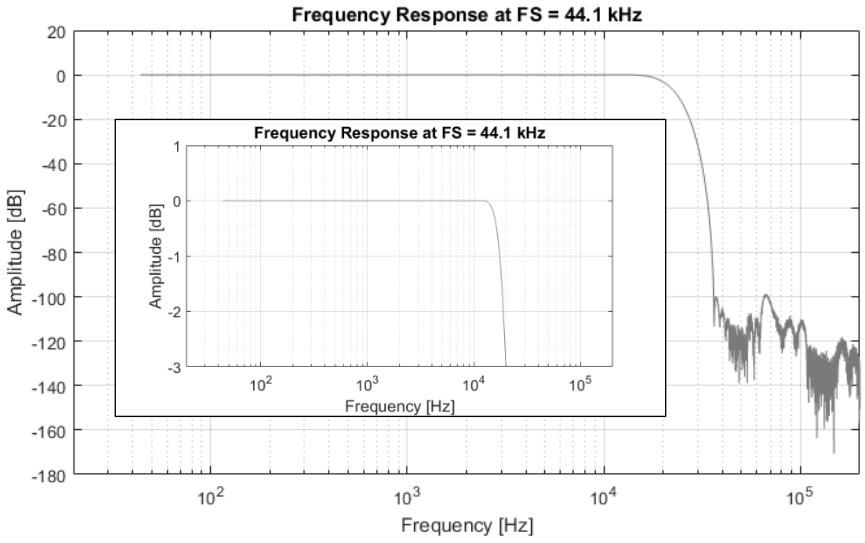
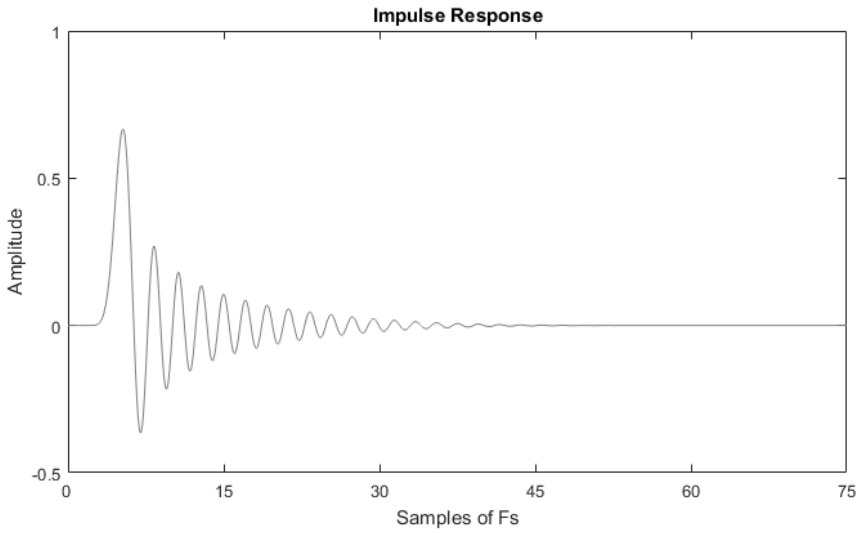
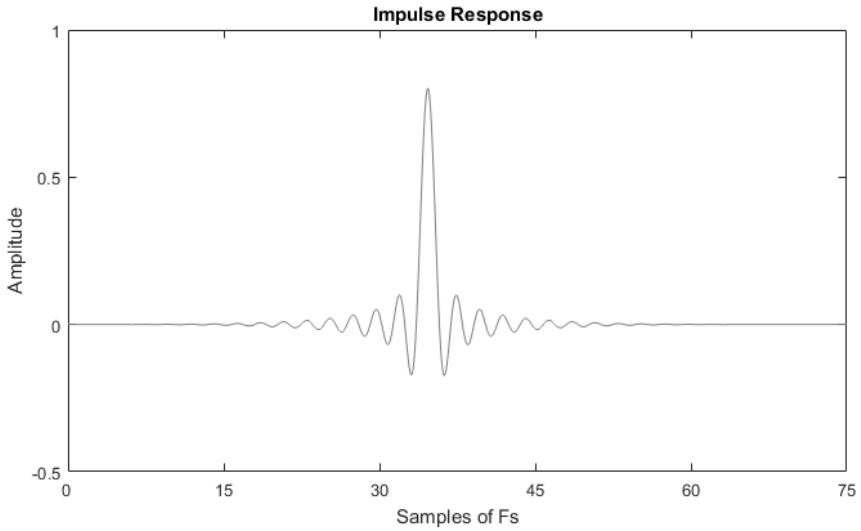
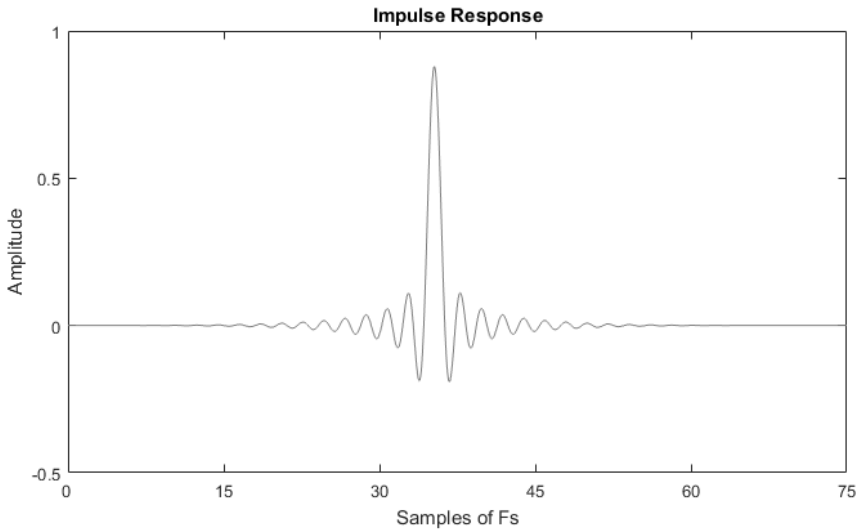
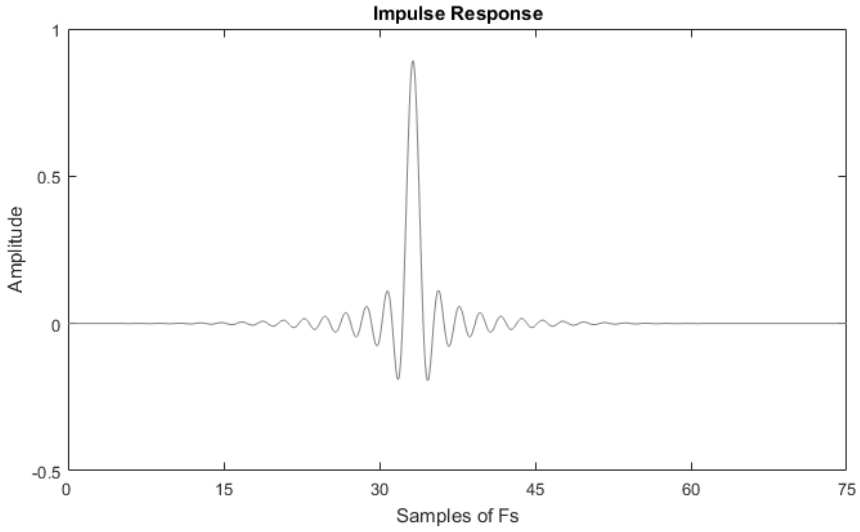
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

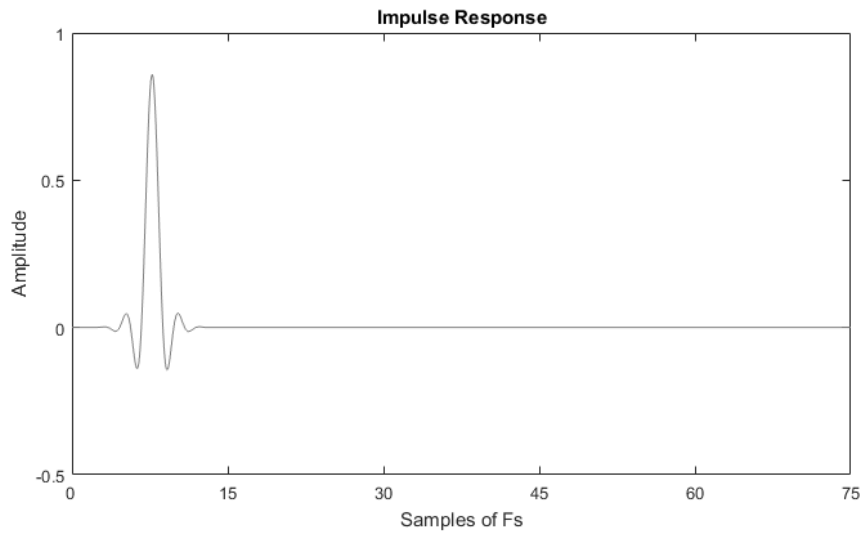
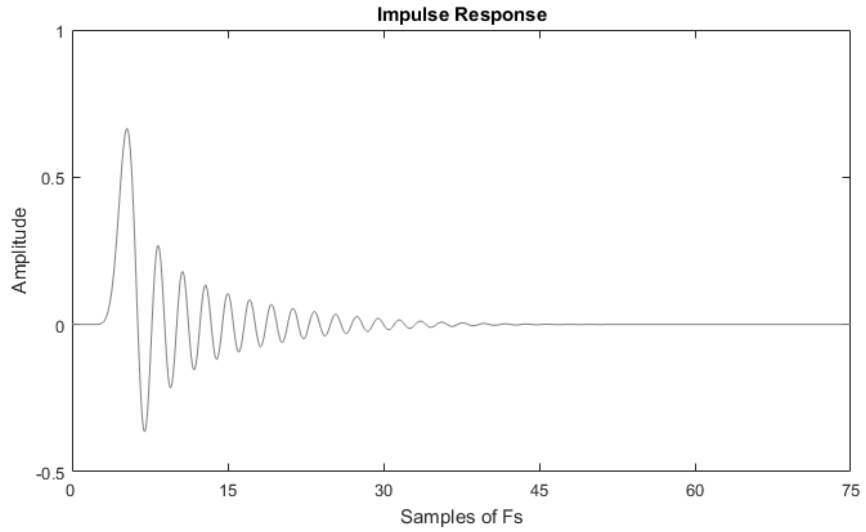
Table 26 - DAC: PCM Filter Frequency Response

DAC: PCM Filter Impulse Response

The following impulse responses were obtained from software simulations of these filters. They were measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

Filter	Impulse Response
Minimum Phase	
Linear Phase Apodizing	

Linear Phase Fast Roll-Off	
Linear Phase Fast Roll-Off Low Ripple	

Linear Phase Slow Roll-Off	
Minimum Phase Fast Roll-Off	

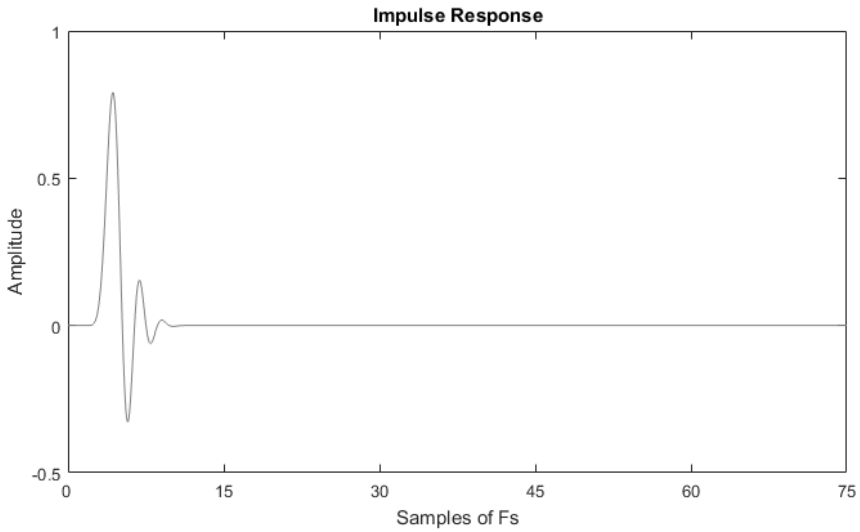
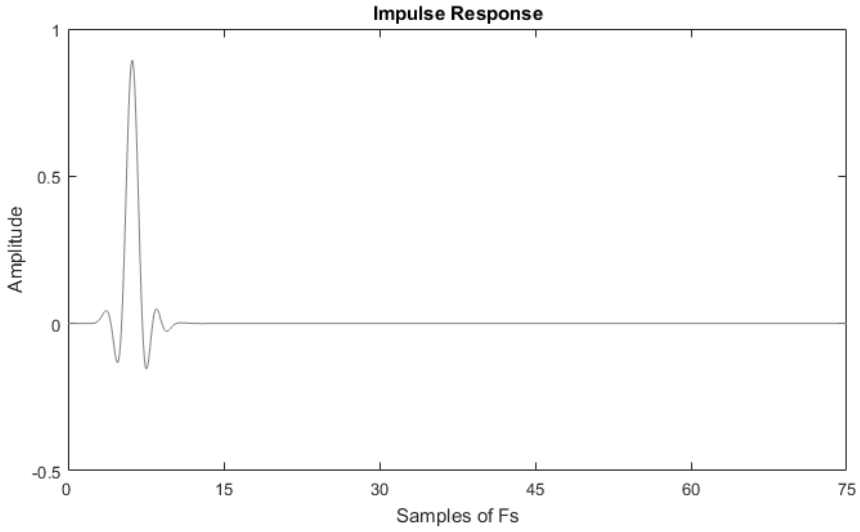
Minimum Phase Slow Roll-Off	
Minimum Phase Slow Roll-Off Low Dispersion	

Table 27 - DAC: PCM Filter Impulse Response

DAC: 64FS Mode

DAC: Minimum Phase 64FS Mode Latency

The following table shows the simulated latency at 705.6kHz sampling rate and is very similar at 768kHz. Measurements were taken from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize the data stream. Latency delay will reduce (scale) with sampling rate.

Digital Filter	Delay(us) @ FS = 705.6 kHz
Minimum Phase Double Rate	3.61 / FS

Table 28 - DAC: Minimum Phase 64FS Latency

DAC: Minimum Phase 64FS Properties

Minimum Phase 64FS Mode					
Parameter	Conditions	MIN	TYP	MAX	UNIT
Pass band	-3 dB			0.45 x fs	Hz
Stop band	-61.31 dB	0.68 x fs			Hz
Group Delay		1.54/fs		2.35/fs	s
Flatness (ripple)					dB

Table 29 - DAC: Minimum Phase 64FS Properties

DAC: Minimum Phase 64FS Frequency Response

This filter gets selected automatically when MCLK/FS = 64. The following frequency response was obtained from software simulations with a sample rate of 705.6kHz

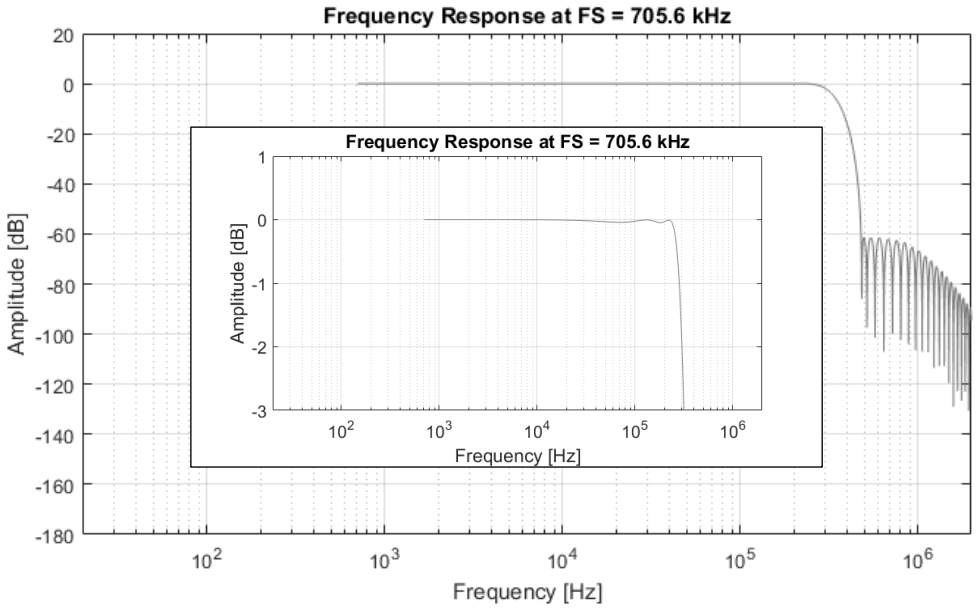


Figure 24 - DAC: Minimum Phase 64FS Frequency Response

DAC: Minimum Phase 64FS Impulse Response

The following impulse responses were obtained from software simulations of these filters. They were measured from the external impulse response. The extra sample delay to get the data encoded accounts for external processing time to serialize data stream.

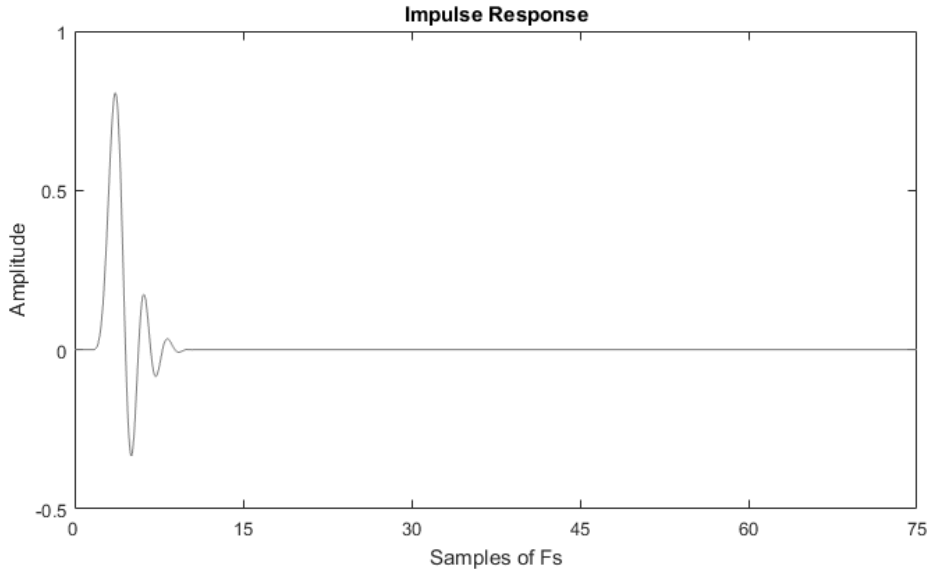


Figure 25 - DAC: Minimum Phase 64FS Impulse Response

Sample Rate Calculation

Acquiring the real time sample rate from the ES9291 can be accomplished using Register 232 AUTO FS READ.

Auto fs detect (Register 1[0] AUTO_FS_DETECT = 1'b1) must be set.

The below equation calculates the current auto detected sample rate by using a combination of register readback states.

$$FS\ [Hz] = \frac{Y * MCLK}{(X+1) * \left(\frac{128}{2^Z}\right)}$$

Variables

- {X}: Register 232[5:0] MCLK_128FS_DIV_AUTO
- {Y}: Register 232[6] MCLK_128FS_HALF_DIV_AUTO
  - 1'b0: Y=1
  - 1'b1: Y=2
- {Z}: Register 232[7] EN_64FS_MODE_AUTO
- MCLK: Master Clock rate

Example

For this example, let the variables be as follows:
X = 7, Y = 1, Z = 0, MCLK = 49.152 [MHz]

$$FS\ [Hz] = \frac{1 * 49.152MHz}{(7+1) * \left(\frac{128}{2^0}\right)} = \frac{49.152MHz}{8 * 128} = 48kHz$$

Daisy Chain

The ES9291 supports connecting multiple devices together in a daisy chain configuration. Up to 16 devices can be daisy chained together to output data onto any of the 32 channels in a TDM data line. The DACs Daisy Chain has a digital input on DATA3 from the previous chip and will append its data onto the line and output on GPIO2 for the next chip down the chain. At the same time, the ADCs Daisy Chain has a digital input on GPIO1 from the previous chip and will append its data onto the line and output on DATA2. See Application Note for more information.

Note: GPIO1 on the last ES9291 of the Daisy Chain must be set to zero by tied to ground through a 47Ω resistor.

Data Path	Output Pin	Input Pin
DAC	GPIO2/DATA5	DATA4
ADC	DATA2	GPIO1/DATA3

Table 30 - Daisy Chain Pins

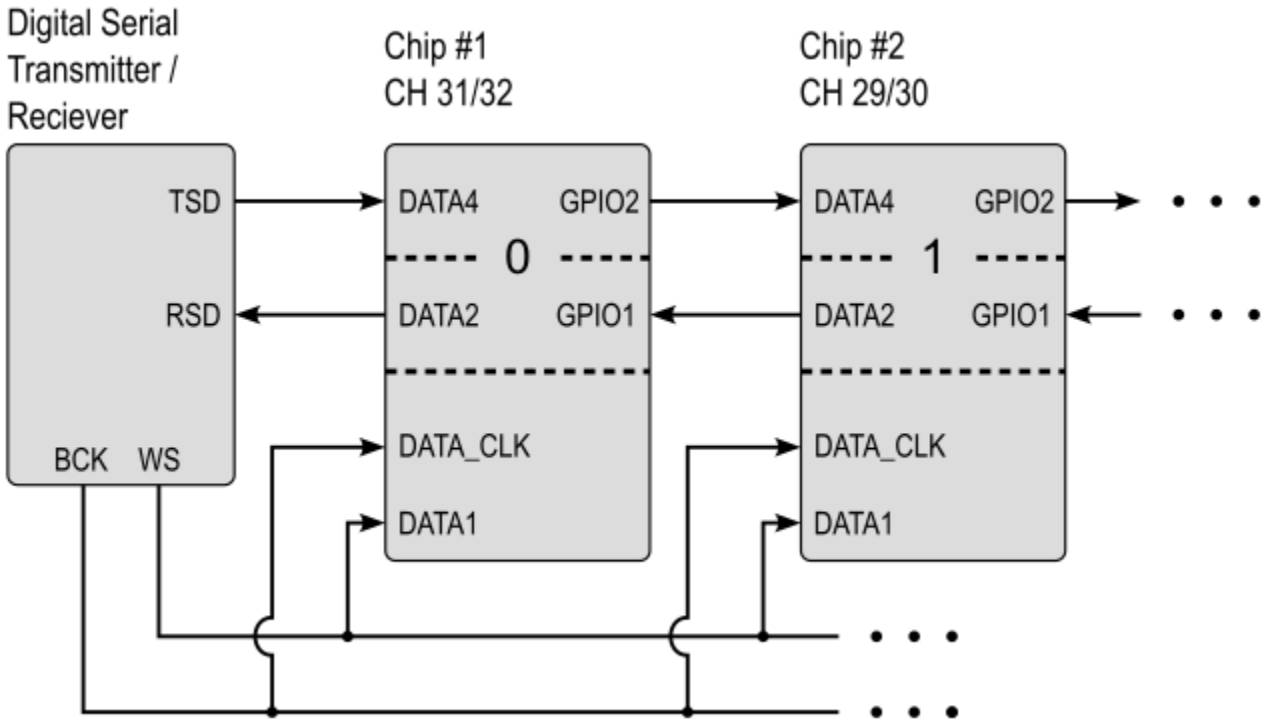


Figure 26 - Daisy Chain Configuration

THD Compensation

The ES9291 has integrated ADC and DAC THD Compensation to add or correct second and third harmonics that may be present on the output signal. The compensation is controlled by two 16-bit coefficients for the ADC Datapath located in Registers 71-74 and two 12-bit coefficients for the DAC Datapath located in Registers 101-104.

The following equation displays how the second and third order harmonics are affected by the C2 and C3 values:

$$output = x + c2 * x^2 + c3 * x^3$$

ADC THD Compensation Coefficient Registers

- Registers 71-72: ADC THD COMP C2
  - This register's value is internally XORed with 16'hFFFC
- Registers 73-74: ADC THD COMP C3
  - This register's value is internally XORed with 16'hFFE2

DAC THD Compensation Coefficient Registers

- Registers 101-102: DAC THD COMP C2
  - This register's value is internally XORed with 12'h222
- Registers 103-104: DAC THD COMP C3
  - This register's value is internally XORed with 12'h030

Analog Features

APLL

The ES9291 has a built in Analog PLL (APLL) for generating frequencies that are unavailable externally. For an application note on the APLL, please ask your FAE or distributor for availability.

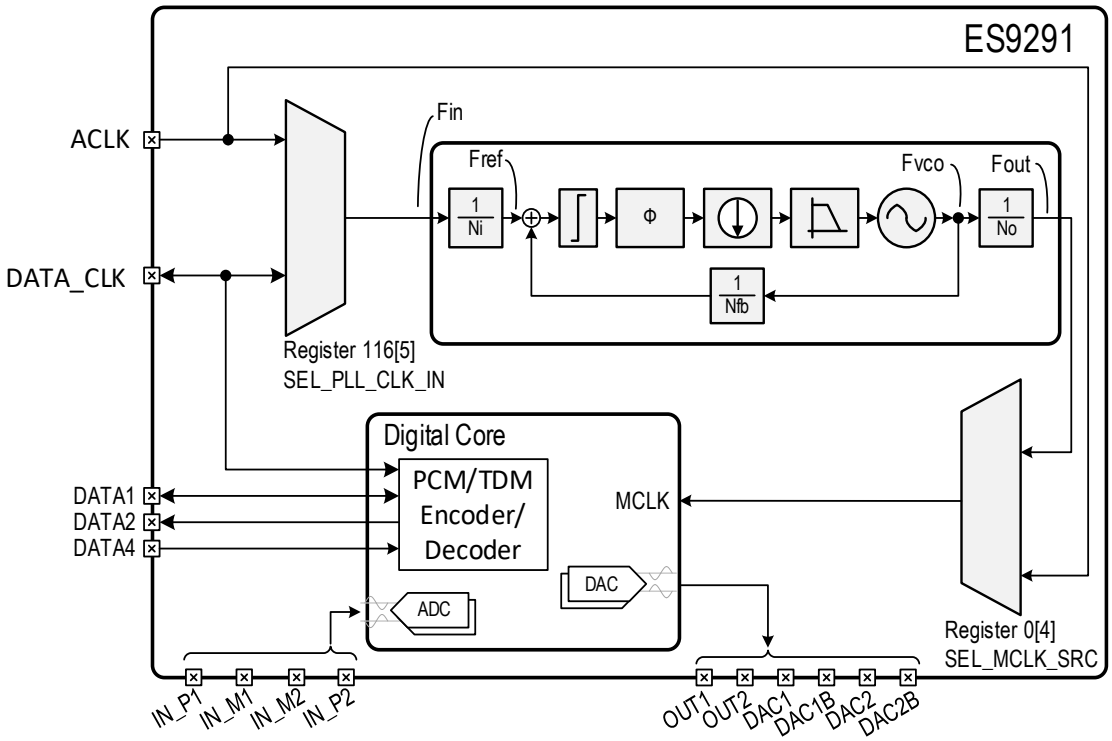


Figure 27 - Functional Block Diagram of ES9291 APLL

The input clock (F_{in}) source to the APLL is chosen between ACLK or DATA_CLK with Register 116[5] SEL_PLL_CLK_IN. The MCLK source to the chip is chosen between the APLLs output or the ACLK pin with Register 0[4] SEL_MCLK_SRC.

For calculation of the PLL frequency output, use the following formulas:

$$F_{ref} = \left(\frac{F_{in}}{N_i}\right) \qquad F_{vco} = \left(\frac{F_{in}}{N_i}\right) * N_{fb} \qquad N_{fb} = \frac{2^{25}}{FBDIV} \qquad F_{out} = \left(\frac{F_{in}}{N_i}\right) * \frac{N_{fb}}{N_o}$$

Where:

a. FBDIV is a 24-bit number
b. PLL frequency range requirements:
    a. Fref requirement: 2.5MHz < Fref < 13 MHz
    b. Fvco requirement: 90MHz < Fvco < 110MHz
    c. Fout requirement: 22.5792/24.576MHz & 45.1584/49.152Mhz
c. Ni = input divider
    - Accessible from Reg 122-124[8:0], PLL_CLK_IN_DIV
d. No = output divider
    - Accessible from Reg 122-12415:12], PLL_CLK_OUT_DIV
e. Nfb = feedback divider
    - Accessible from Reg 119-121[23:0], PLL_CLK_FB_DIV
        - Note: Toggle Reg 122-124[9] PLL_FB_DIV_LOAD to load PLL_CLK_FB_DIV value

44.1kHz Base Rates (SYNC Slave Mode)							
FS (kHz)	**DATA_CLK (MHz)**	**Ni**	**Fref (MHz)**	**FBDIV**	**Fvco (MHz)**	**No**	**Fout (MHz)**
32-Bit Frame							
352.8	22.5792	2	11.2896	4194304	90.3168	4	22.5792
176.4	11.2896	1	11.2896	4194304	90.3168	4	22.5792
88.2	5.6448	1	5.6448	2097152	90.3168	4	22.5792
44.1	2.8224	1	2.8224	1048576	90.3168	4	22.5792
16-Bit Frame							
352.8	11.2896	1	11.2896	4194304	90.3168	4	22.5792
176.4	5.6448	1	5.6448	2097152	90.3168	4	22.5792
88.2	2.8224	1	2.8224	1048576	90.3168	4	22.5792
44.1	1.4112	1	1.4112	524288	90.3168	4	22.5792

Table 31 - APLL Divider Values for 44.1kHz Base Rates

48kHz Base Rates (SYNC Slave Mode)							
FS (kHz)	**DATA_CLK (MHz)**	**Ni**	**Fref (MHz)**	**FBDIV**	**Fvco (MHz)**	**No**	**Fout (MHz)**
32-Bit Frame							
384	24.576	2	12.288	4194304	98.304	4	24.576
192	12.288	1	12.288	4194304	98.304	4	24.576
96	6.144	1	6.144	2097152	98.304	4	24.576
48	3.072	1	3.072	1048576	98.304	4	24.576
16-Bit Frame							
384	12.288	1	12.288	4194304	98.304	4	24.576
192	6.144	1	6.144	2097152	98.304	4	24.576
96	3.072	1	3.072	1048576	98.304	4	24.576
48	1.536	1	1.536	524288	98.304	4	24.576

Table 32 - APLL Divider Values for 48kHz Base Rates

Jack Detect

The ES9291 features Jack Detection that has a status indicator (flag) when it detects the presence of headphone jack tip. This indicator can be masked onto the GPIO pins as well as readback via a register.

Jack Detect Registers

- Register 7[7] JDET_EN
- Register 30[6] MASK_JDET
- Register 31[6] CLEAR_JDET
- Register 234[2] JDET_FLAG

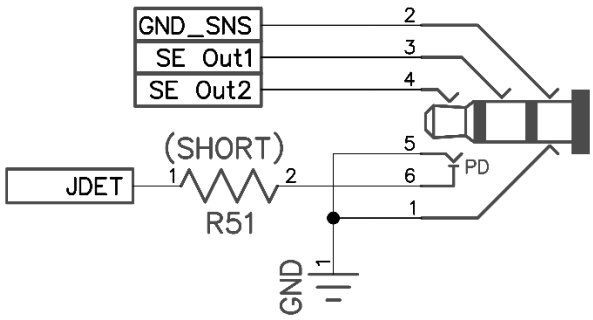


Figure 28 - Recommended Jack Detect Schematic

Temperature Sensor

The ES9291 integrates a temperature sensor that can be readback at any time. The equation to convert the register value to temperature (˚C) is as follows:

$$\text{Temperature } [^{\circ}\text{C}] = \text{TS\_DATA} * 3.2151 - 247$$

Temperature Sensor Registers

- Register 7[6] TSENSE_EN
- Register 235 TSENSE_DATA

Mic-Bias

The integrated Mic Bias can be set to varying voltages between 1.45V and 2.85V (default). See Registers for more list of available values.

Mic Bias Registers

- Register 82[6] MB_VR_BYPB
- Register 82[3] MB_EN
- Register 82[2:0] MB_VR_SET

Charge Pump

The ES9291 features an integrated Charge Pump that generates the required -3.3V (PNEG) for the “ground centered” Power Line Driver, on pin 47 (PNEG). To achieve higher output power for high loads, an external negative supply is required. When using an external negative supply ensure the internal Charge Pump is disabled with CP_NS_EXT = 1’b1.

The Charge Pump will automatically shut down, saving power, when a mute condition is detected. This function can be disabled with CP_MUTE_PD_EN = 1’b0.

The charge pump clock must be 705.6kHz/768kHz for 44.1kHz/48kHz sample rate families, respectively. This is set by default when using a 22.5792/24.576MHz or 45.1584/49.152MHz MCLK and setting MCLK_24M_DIV2 appropriately. If another MCLK frequency is used, the below equation can be used to calculate the required CP_CLK_DIV to achieve the required CP_CLK rate.

$$\text{CP\_CLK [Hz]} = \frac{\text{MCLK}}{2^{\text{MCLK\_24M\_DIV2}} \cdot (\text{CP\_CLK\_DIV} + 1)}$$

Charge Pump Registers

- Register 5[4] MCLK_24M_DIV2
- Register 111[1] CP_NS_EXT
- Register 111[0] CP_MUTE_PD_EN
- Register 112 CP_CLK_DIV

PowerLine Driver

The ES9291 PowerLine Driver is a very low-noise audio driver that delivers clean, high-fidelity sound to both line outputs, headphones and other applications. It is designed for wide dynamic range and solid current drive, it ensures clear, reliable audio across various loads.

With a $2V_{rms}$ line level output and the capability to output 70mW with the internal charge pump and up to 125mW per channel with an external negative supply, the PowerLine Driver is a versatile output stage.

Absolute Maximum Ratings

PARAMETER	RATING
Positive Supply Voltage • AVCC_CP • AVCC_PLD • AVDD • AVCC_ADC • DVDD (Internally generated) • PNEG (Internally generated)	 • -0.3 to +3.7V with respect to ground • -0.3 to +3.7V with respect to ground • -0.3 to +3.7V with respect to ground • -0.3 to +3.7V with respect to ground • -0.3 to +1.4V with respect to ground • -3.5V with respect to ground
Storage Temperature	-65ºC to +150ºC
Operating Junction Temperature	+125ºC
Voltage Range for Digital Input Pins	-0.3V to AVDD (nom) +0.3V

Table 33 - Absolute Maximum Ratings

WARNING: Stresses beyond those listed here may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied.

ESD Ratings

ESD Standard	Rating
Human Body Model (HBM), ANSI/ESDA/JEDEC JS-001	2kV
Charge Device Model (CDM), ANSI/ESDA/JEDEC JS-002	500V

Table 344 - ESD Ratings

WARNING: Electrostatic Discharge (ESD) can damage this device. Proper procedures must be followed to avoid ESD when handling this device.

IO Electrical Characteristics

PARAMETER	SYMBOL	MINIMUM	MAXIMUM	UNIT
High-level input voltage	VIH	(AVDD / 2) + 0.2		V
Low-level input voltage	VIL		1.61	V
High-level output voltage	VOH	AVDD – 0.2		V
Low-level output voltage	VOL		0.2	V

Table 35 - I/O Electrical Characteristics

Switching Characteristics

Parameter	Notes	Min.	Typ.	Max.	Unit
MCLK[1]					
Frequency		22.5792	-	49.152	MHz
Duty Cycle		45	-	55	%
PCM Mode[2]					
WS Frequency[3] (Word Select Clock)		MCLK/1024	-	MCLK/128	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	TDM_WORD_WIDTH)* (TDM_CH_NUM+1)*WS	MCLK	MHz
WS Frequency (Word Select Clock)	64FS Mode[4]	352.8	MCLK/64	768	kHz
BCLK Frequency (Bit Clock)		22.5792	MCLK	49.152	MHz
TDM Mode					
WS Frequency (Word Select Clock)	TDM4	MCLK/1024	-	MCLK/128	kHz
	TDM8		-	MCLK/256	kHz
	TDM16		-	MCLK/512	kHz
	TDM32		-	MCLK/1024	kHz
BCLK Frequency (Bit Clock)		(16*2*WS)	(TDM_WORD_WIDTH)* (TDM_CH_NUM+1)*WS	MCLK	MHz
DSD Mode					
DSD Clock Frequency		2.8224		MCLK/2	MHz

Table 36 - Switching Characteristics

[1] MCLK must be synchronous to the digital audio clock.

[2] In hardware mode, only 32-bit word widths are supported for both PCM, 32-bit and 16-bit for TDM.

[3] The sample rate of 256kHz at 49MHz MCLK is unsupported.

[4] 64FS mode is for 705.6/768kHz with 45.1584/49.152MHz or 352.8/384kHz with 22.5792/24.576MHz.

Timing Characteristics

Master Clock (MCLK) and Bit-Clock (BCK) Timing

The ES9291 has a phase relationship requirement between MCLK (Master Clock) and BCK (Bit-Clock). The internal clock for the ADC (MCLK_24M) is derived from the provided MCLK. In slave mode, the ES9291 requires the BCK transition to be outside a specific range of the MCLK period. This is due to the synchronization circuitry that aligns the output samples with the input clocks. The table below specifies the amount of time required between the bit clock transition and the MCLK falling edge.

45.1584/49.152MHz

With a 45.1584/49.152MHz MCLK, the MCLK Rising to BCK time (t_{MRB}) must be either less than t_{MRB1} or greater than t_{MRB2}.

$$t_{MRB} \leq t_{MRB1}$$

$$OR$$

$$t_{MRB} \geq t_{MRB2}$$

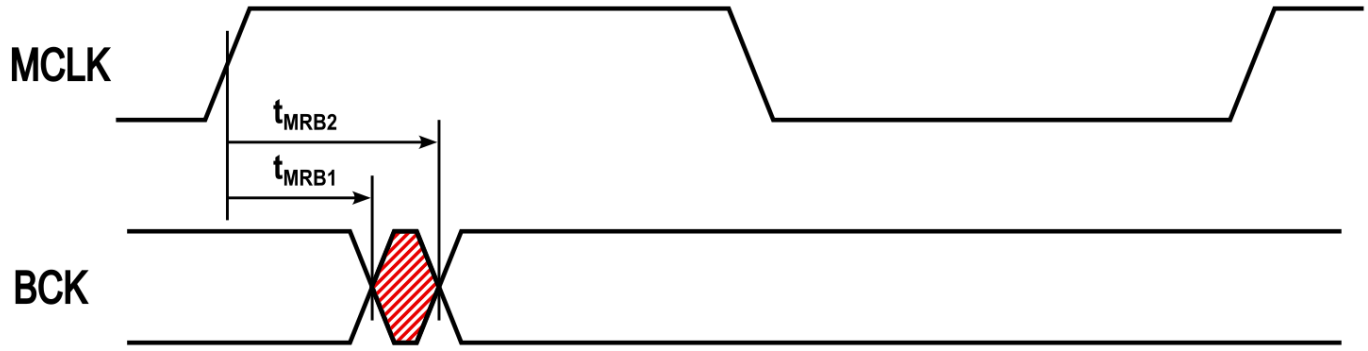


Figure 29 - 45/49M MCLK with BCK Phase Relationship

	Symbol	MCLK [MHz]	Minimum	Maximum	Unit
MCLK "↑" to BCK	t_{MRB2}	49.152 / 45.1584	6.2	-	ns
MCLK "↑" to BCK	t_{MRB1}		-	4.9	ns

Figure 30 - Timing Relationship for 45/49M MCLK & BCK

Bit-Clock (BCK) and Word-Select (WS) Timing

Master Mode

For maximum flexibility the Master BCK and WS generated can be inverted with Register 8[3] MASTER_WS_INVERT and Register 8[2] MASTER_BCK_INVERT respectively.

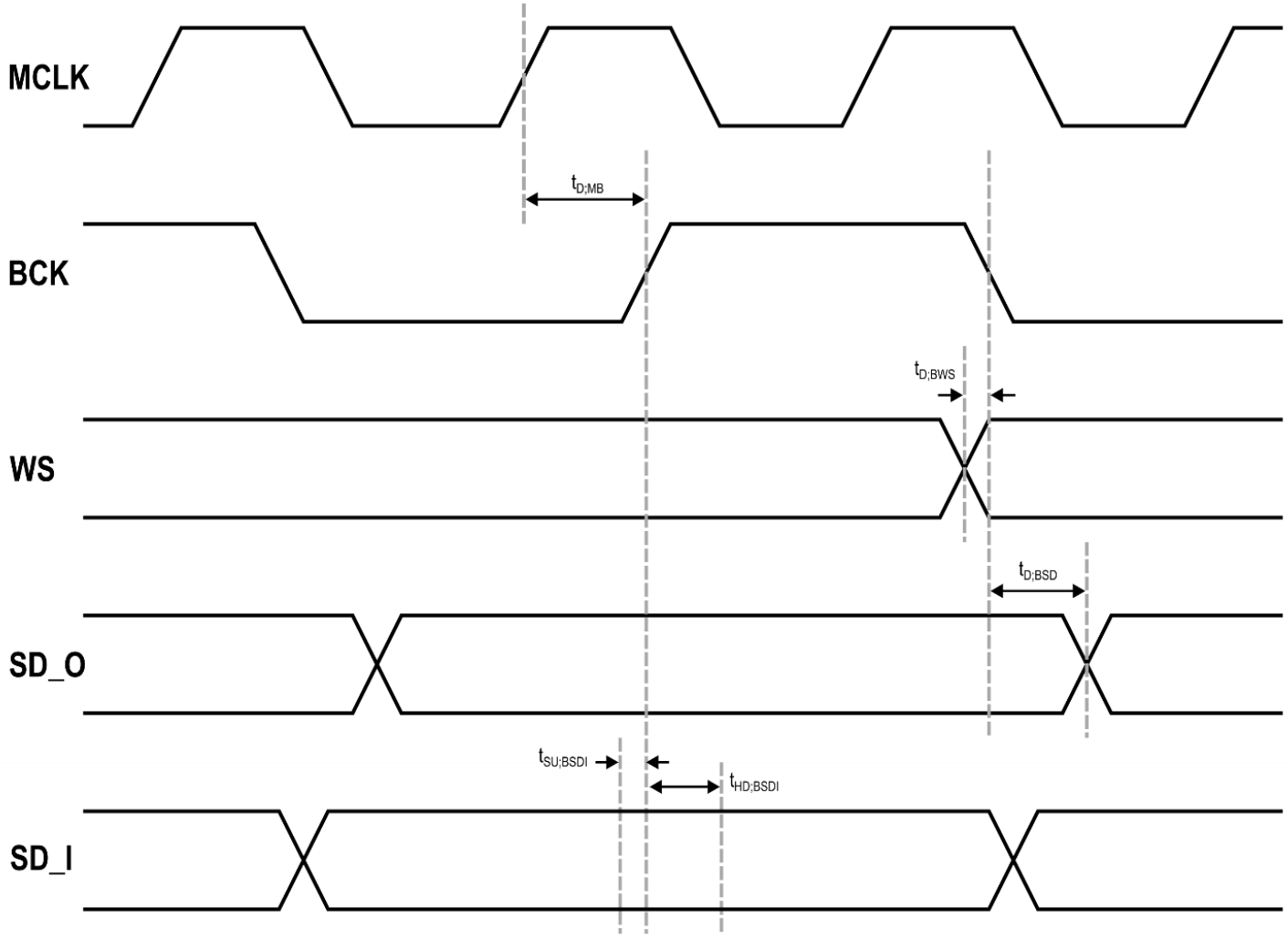


Figure 31 – Master Mode TDM Timing Diagram

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK-to-BCK output delay	$t_{D;MB}$	7.50	-	14.24	ns
BCK-to-WS output delay	$t_{D;BWS}$	0.18	-	0.57	ns
BCK-to-DATAx output delay	$t_{D;BSD}$	4.27	-	7.99	ns
BCK-to-SD_I setup time	$t_{SU;BSDI}$	-0.74	-	-	ns
BCK-to-SD_I hold time	$t_{HD;BSDI}$	1.05	-	-	ns

Table 37 – Master Mode TDM Interface Timings

Slave Mode

In this diagram SD_O is the output data lines from the PCM/TDM Encoder and SD_I is the input data for the TDM Daisy Chain and the PCM/TDM Decoder. The setup and hold times for SD_I and WS are equivalent.

For maximum flexibility the input Slave BCK can be inverted with Register 8[7] SLAVE_BCK_INV.

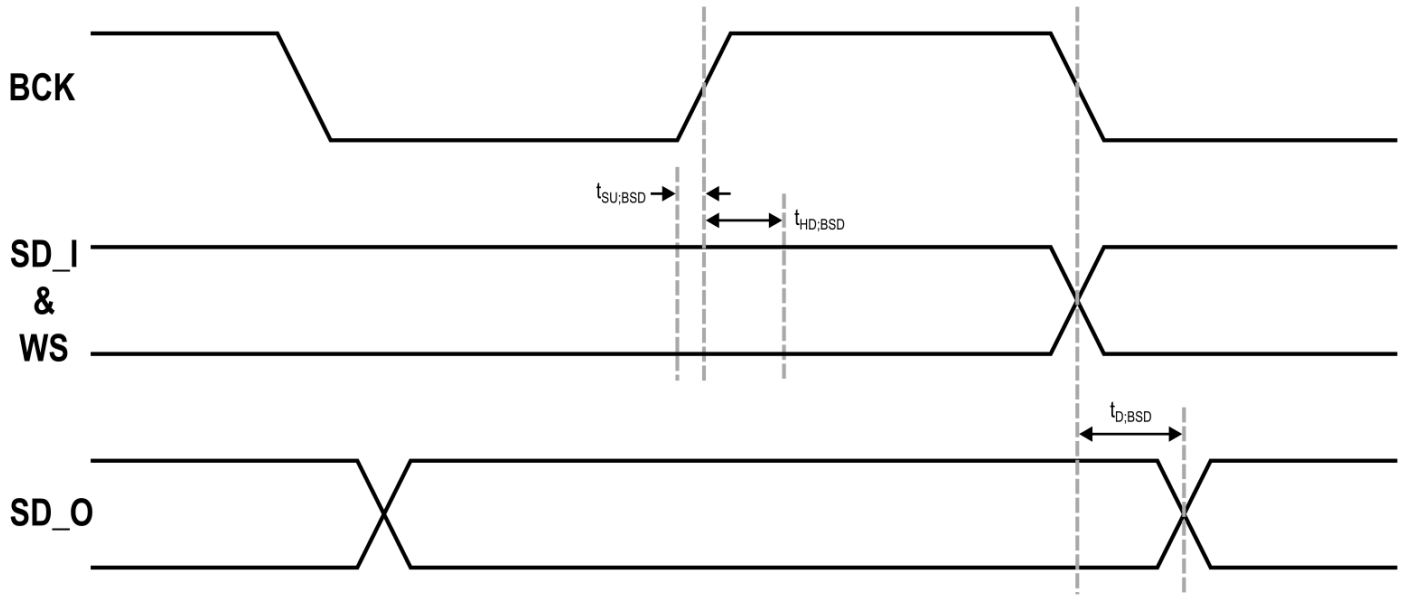


Figure 32 – Slave Mode TDM Timing Diagram

Parameter	Symbol	Min.	Typ.	Max.	Unit
BCK-to-WS setup time	$t_{SU;BSD}$	0	-	-	ns
BCK-to-WS hold time	$t_{HD;BSD}$	3	-	-	ns
BCK-to-DATAx output delay	$t_{D;BSD}$	4.27	-	-	ns

Table 38 – Slave Mode TDM Interface Timings

I²C Slave Interface Timing

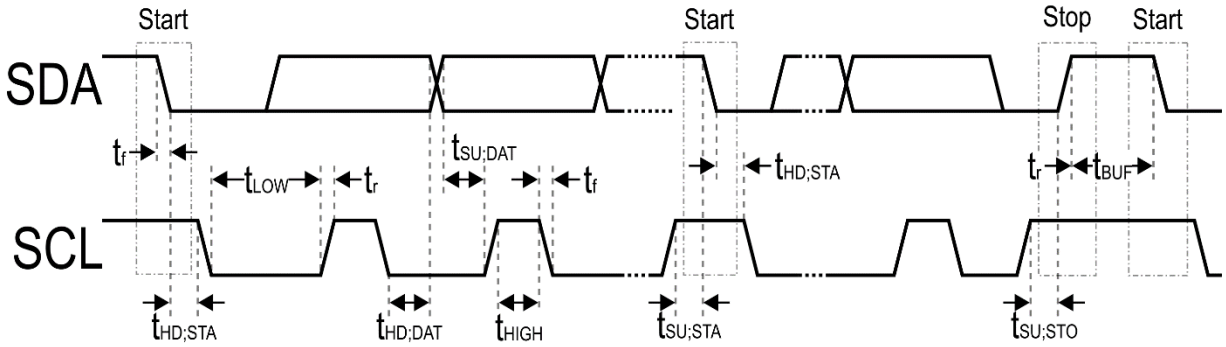


Figure 33 - I²C Slave Control Interface Timing

Parameter	Symbol	Standard-Mode			Unit
		MIN	TYP	MAX	
SCL Clock Frequency	f_{SCL}	-	-	1	MHz
START condition hold time	$t_{HD;STA}$	4	-	-	ns
LOW period of SCL	t_{LOW}	96	-	-	ns
HIGH period of SCL (>10/CLK)	t_{HIGH}	96	-	-	ns
START condition setup time (repeat)	$t_{SU;STA}$	216	-	-	ns
SDA hold time from SCL falling	$t_{HD;DAT}$	1	-	-	ns
SDA setup time from SCL rising	$t_{SU;DAT}$	180	-	-	ns
Rise time of SDA and SCL	t_r	-	180	-	ns
Fall time of SDA and SCL	t_f	15	-	-	ns
STOP condition setup time	$t_{SU;STO}$	1	-	-	ns
Bus free time between transmissions	t_{BUF}	192	-	-	ns
Capacitive load for each bus line	C_b	-	-	70	pF

Table 39 - I²C Slave/Synchronous Slave Interface Timing Definitions

SPI Slave Interface Timing

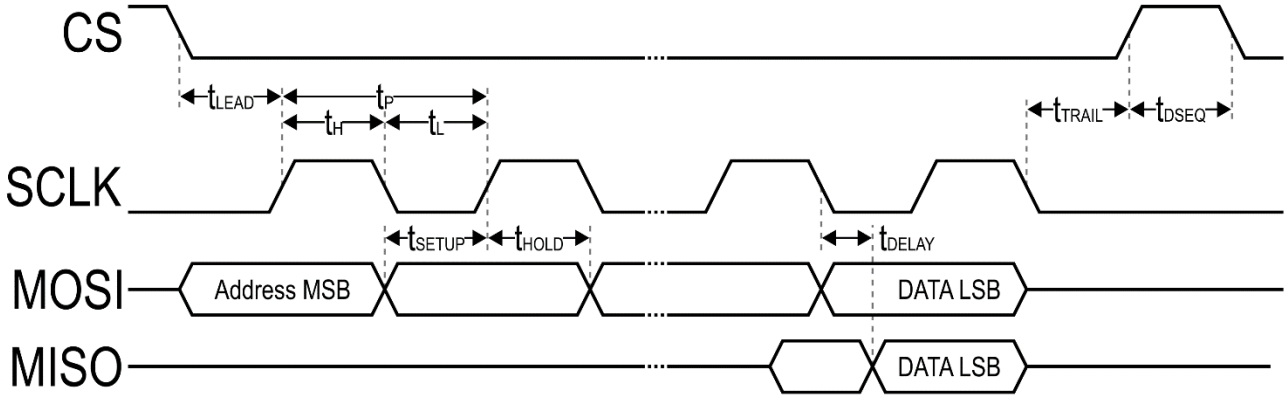


Figure 34 - SPI Slave Interface Timing

Parameter	Symbol	Min [ns]	Max [ns]
CS Lead Time (SCLK rising edge)	t_{LEAD}	2	-
CS Trail Time (SCLK falling edge)	t_{TRAIL}	2	-
MOSI Data Setup Time	t_{SETUP_MOSI}	5	-
MOSI Data Hold Time	t_{HOLD_MOSI}	7	-
SCLK-MISO Delay Time	t_{DELAY_MISO}	-	12
SCLK Period	t_{P_SCLK}	40	-
SCLK High Pulse Duration	t_{H_SCLK}	8	-
SCLK Low Pulse Duration	t_{L_SCLK}	8	-
Sequential Transfer Delay	t_{DSEQ}	40	-

Table 40 - SPI Slave Interface Timing

Recommended Operating Conditions

Table 42 shows the recommended operating conditions for ES9291.

PARAMETER	SYMBOL	CONDITIONS
Operating Temperature	T_A	-20°C to +85°C
AVCC_CP		+3.3V ± 5%
AVDD		+3.3V ± 5%
AVCC_ADC		+3.3V ± 5%
AVCC_PLD		+3.3V ± 5%
PNEG		Internal -3.3V
PLL_REG		Internal 1.8V
DVDD		Internal 1.2V
VREF		Internal 2.85V
MICBIAS		Internal 1.45V - 2.75V
VREF_DAC		Internal 2.85V
VREF_ADC		Internal 2.85V

Table 41 - Recommended Operating Conditions

Recommended Power Up/Down Sequence

It is recommended for powering up that AVDD turns on ~200us before AVCC_CP and AVCC_ADC turn on. For powering down, first make sure CHIP_EN is low, then AVCC_CP, AVCC_ADC and AVCC_PLD, then finally AVDD.

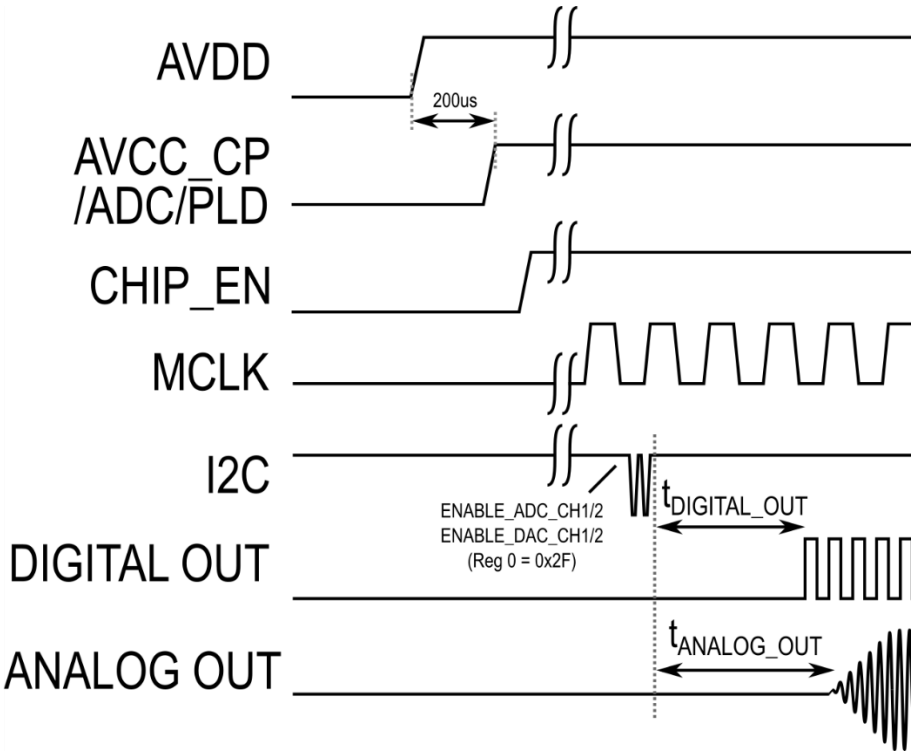


Figure 35 - Recommended Power Up Sequence

$$t_{digital\_out}[s] = \left(3 + \frac{900000}{2^{\sim MCLK\_24M\_DIV2}}\right) * \left(\frac{1}{MCLK}\right) \approx 18.3ms$$

$$t_{analog\_out}[s] = \left(2 + \frac{950000 + 2^{16+SOFT\_RAMP\_TIME}}{2^{\sim MCLK2\_24M\_DIV2}}\right) * \left(\frac{1}{MCLK}\right) + \frac{4}{FS} \approx 30ms\ @\ 48kHz$$

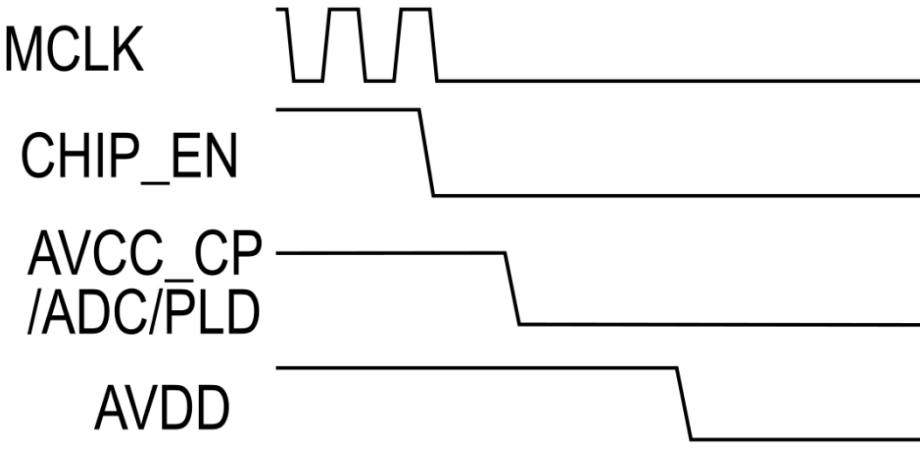


Figure 36 - Recommended Power Down Sequence

Power Consumption

Test Conditions (unless otherwise noted)
T_A = 25ºC, AVCC_ADC = AVCC_CP = AVCC_PLD= AVDD = +3.3V,
ADC: 1.8Vrms Differential Input.
DAC: 0dBFS Digital Input.
AVDD supply includes DVDD current.

Parameter	Min	Typ.	Max	Unit
Standby (CHIP_EN=0)				
AVCC_ADC		<1		µA
AVCC_CP		<1		µA
AVCC_PLD		<1		µA
AVDD		<1		µA

HW Mode 8, 16 (I²S / TDM LJ Slave 32-bit), MCLK = 24.576MHz				
AVCC_ADC		8		mA
AVCC_CP		10.9		mA
AVCC_PLD		23.1		mA
AVDD for HW8/HW16, Fs=24kHz		12.7		mA
AVDD for HW8/HW16, Fs=48kHz		15		mA
AVDD for HW8/HW16, Fs=96kHz		18.6		mA
AVDD for HW8/HW16, Fs=192kHz		26.4		mA

Table 42 - Power Consumption

Note: Current consumption can be reduced by externally supplying DVDD with 1.2V to decrease AVDD current.

Performance

Test Conditions 1 (unless otherwise noted)
T_A = 25ºC, AVCC_ADC = AVCC_PLD = AVCC_CP = AVDD = +3.3V, fs = 48kHz, HW mode, 49.152MHz clock, 1kHz input.

Note: Performance numbers were measured using the ESS ES9291 1v0 evaluation board.

Parameter			Min	Typ.	Max	Unit
ADC Analog Input Characteristics						
Resolution					32	Bit
Differential Input Voltage (IN_P to IN_M)	0dBFS output			2		V_{rms}
Input DC Common Mode				VREF_ADC/2		V_{dc}
Stereo THD+N Ratio (+5dBV differential input, -1dBFS output)	fs=48kHz	BW=20Hz-20kHz		-110		dB
	fs=96kHz	BW=20Hz-40kHz		-107		dB
	fs=192kHz	BW=20Hz-80kHz		-104		dB
Stereo Dynamic Range (2mVrms differential input, -60dBFS output)	A-weighted			+121		dB
Input Impedance				780±15%		Ω

Table 43 - ES9291 ADC Performance

Parameter			Min	Typ.	Max	Unit
DAC Analog Output Characteristics						
Resolution					32	Bit
Output Voltage	0dBFS input			2		V_{rms}
Stereo THD+N Ratio (0dBFS input, single ended output)	fs=48kHz BW=20Hz-20kHz	2Vrms,10kΩ		-110		dB
		65mW, 32Ω[1]		-102		dB
		120mW, 32Ω[2]		-102		dB
	fs=96kHz BW=20Hz-40kHz	2Vrms,10kΩ		-107		dB
	fs=192kHz BW=20Hz-80kHz	2Vrms,10kΩ		-104		dB
Stereo Dynamic Range (-60dBFS input, single ended output)	A-weighted	2mVrms		+121		dB
Output Impedance				<1		Ω
Max Output Power (per channel)	Internal Charge Pump	<1% THD+N Ratio		70		mW
	External Negative Supply			125		mW

Table 44 - ES9291 DAC Performance

[1] For heavy load cases that require near maximum output power, ensure both AVCC_PLD and AVCC_CP are at or above 3.3V by +5%

[2] 120mW output into 32Ω requires an external negative supply.

Register Overview

A system clock is not required to access registers.

Read/Write Register Addresses

Registers 0-174 (0x00 - 0xAE) are read and write registers.

Read-Only Register Addresses

Register 224-252 (0xE0 - 0xFC) are read only registers.

Multi-Byte Registers

Multi-Byte registers must be written from LSB to MSB. Data is latched when MSB is written.
Multi-Byte registers must be read from LSB to MSB. Data is latched when LSB is read.
MSB is always stored in the highest register address.

Register Map

Addr (Hex)	Addr (Dec)	Register	7	6	5	4	3	2	1	0
0x00	0	SYS CONFIG	SOFT_RESET	RESERVED	EN_MCLK_IN	SEL_MCLK_SRC	ENABLE_DAC_CH2	ENABLE_DAC_CH1	ENABLE_ADC_CH2	ENABLE_ADC_CH1
0x01	1	FS CONFIG	RESERVED			ADC_MONO_MODE	RESERVED	ENABLE_64FS_MODE	AUTO_FS_DETECT_BLOCK_64FS	AUTO_FS_DETECT
0x02	2	ENCODER CONFIG	ENABLE_PDM_DECODE	ENABLE_DSD_DECODE	ENABLE_DOP_DECODE	ENABLE_TDM_DECODE	RESERVED			ENABLE_TDM_ENCODE
0x03	3	INPUT & OUTPUT SELECT	ENABLE_SPDIF_ENCODE	ENABLE_PDM_MIC_DECODE	RESERVED			INPUT_DATA_FORMAT_SEL		RESERVED
0x04	4	FRONT-END CLOCK CONTROL	RESERVED	MCLK_128FS_HALF_DIV	MCLK_128FS_DIV					
0x05	5	BACK-END CLOCK CONTROL	RESERVED			MCLK_24M_DIV2	RESERVED			
0x06	6	MASTER CLK CONFIG	MASTER_DCLK_DIV							
0x07	7	MISC CLOCK CONFIG	JDET_EN	TSENSE_EN	RESERVED		ENABLE_WS_MONITOR	ENABLE_BCK_MONITOR	FORCE_PLL_LOCK	CLK_FAULT_DET_EN
0x08	8	MASTER MODE CONFIG	SLAVE_BCK_INVERT	RESERVED	MASTER_WS_CLK_PHASE	MASTER_WS_PULSE_MODE	MASTER_WS_INVERT	MASTER_BCK_INVERT	DSD_MASTER_MODE_EN	PCM_MASTER_MODE_EN
0x09	9	TDM CONFIG 1	RESERVED	AUTO_CH_DETECT	RESERVED	TDM_CH_NUM				
0x0A	10	TDM CONFIG 2	RESERVED	NOISE_FLOOR_SHAPE_16BIT	TDM_WORD_WIDTH		TDM_BIT_DEPTH		TDM_VALID_EDGE	TDM_LJ
0x0B	11	TDM ENC CH1 SLOT CONFIG	RESERVED			TDM_ENC_SLOT_SEL_CH1				
0x0C	12	TDM ENC CH2 SLOT CONFIG	RESERVED			TDM_ENC_SLOT_SEL_CH2				
0x0D	13	TDM DEC CH1 SLOT CONFIG	RESERVED			TDM_DEC_SLOT_SEL_CH1				
0x0E	14	TDM DEC CH2 SLOT CONFIG	RESERVED			TDM_DEC_SLOT_SEL_CH2				
0x0F	15	TDM ENC DAISY CHAIN	TDM_ENC_DAISY_CHAIN	RESERVED		TDM_ENC_DATA_LATCH_ADJ				
0x10	16	TDM DEC DAISY CHAIN	TDM_DEC_DAISY_CHAIN	RESERVED		TDM_DEC_DATA_LATCH_ADJ				
0x11	17	DSD MAPPING	RESERVED		DSD_LINE_SEL_CH2	DSD_LINE_SEL_CH1	RESERVED			
0x12	18	PDM I/O CONFIG	RESERVED	PDM_DEC_SAMPLE_EDGE	PDM_DEC_DATA_PHASE	PDM_DEC_2X_GAIN_EN	RESERVED			
0x13	19	PDM MIC CONFIG	RESERVED					PDM_MIC_SAMPLE_EDGE	PDM_MIC_DATA_PHASE	PDM_MIC_IN_SEL
0x14	20	PDM MIC CLK SELECT	RESERVED	PDM_MIC_CLK_DIV						
0x15	21	S/PDIF DATA SELECT	RESERVED							SPDIF_DATA_SOURCE
0x16	22	S/PDIF CS ADDR	SPDIF_CS_WE		RESERVED			SPDIF_CS_BYTE_ADDR		
0x17	23	S/PDIF CS DATA	SPDIF_CS_BYTE_DATA							
0x18	24	VOLUME UP RAMP RATE	VOL_RAMP_RATE_UP							
0x19	25	VOLUME DOWN RAMP RATE	VOL_RAMP_RATE_DOWN							
0x1A	26	VOLUME RAMP SPEED	RESERVED							VOL_RAMP_SPEED_SEL
0x1B-0x1D	27-29	RESERVED	RESERVED							
0x1E	30	STATUS BITS MASK	RESERVED	MASK_JDET	RESERVED		MASK_ADC_OVERLOAD_CH2	MASK_ADC_OVERLOAD_CH1	MASK_PEAK_DET_CH2	MASK_PEAK_DET_CH1
0x1F	31	STATUS BITS CLEAR	RESERVED	CLEAR_JDET	RESERVED		CLEAR_ADC_OVERLOAD_CH2	CLEAR_ADC_OVERLOAD_CH1	CLEAR_PEAK_DET_CH2	CLEAR_PEAK_DET_CH1
0x20-0x30	32-48	RESERVED	RESERVED							
0x31	49	GPIO1/2 CONFIG	GPIO2_CFG				GPIO1_CFG			
0x32	50	GPIO3/4 CONFIG	GPIO4_CFG				GPIO3_CFG			
0x33	51	GPIO5/6 CONFIG	GPIO6_CFG				GPIO5_CFG			
0x34	52	GPIO7/8 CONFIG	RESERVED				GPIO7_CFG			
0x35	53	GPIO INPUT ENABLE	RESERVED	GPIO7_SDB	GPIO6_SDB	GPIO5_SDB	GPIO4_SDB	GPIO3_SDB	GPIO2_SDB	GPIO1_SDB
0x36	54	GPIO OUTPUT ENABLE	RESERVED	GPIO7_OE	GPIO6_OE	GPIO5_OE	GPIO4_OE	GPIO3_OE	GPIO2_OE	GPIO1_OE
0x37	55	GPIO INVERT	RESERVED	GPIO7_INV	GPIO6_INV	GPIO5_INV	GPIO4_INV	GPIO3_INV	GPIO2_INV	GPIO1_INV
0x38	56	GPIO WEAK KEEPER	RESERVED	GPIO7_WK_EN	GPIO6_WK_EN	GPIO5_WK_EN	GPIO4_WK_EN	GPIO3_WK_EN	GPIO2_WK_EN	GPIO1_WK_EN
0x39	57	GPIO READ	RESERVED	GPIO7_READ	GPIO6_READ	GPIO5_READ	GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ
0x3A	58	GPIO ADC FLAG CONFIG	RESERVED	ADC_FLAG_CH_SEL	GPIO_OR_OVERLOAD	GPIO_OR_PEAK_DET	GPIO_AND_OVERLOAD	GPIO_AND_PEAK_DET	ADC_UNLAT_FLAG_EN	ADC_DET_FLAG_SEL
0x3B	59	GPIO DAC FLAG CONFIG	RESERVED	DAC_FLAG_CH_SEL	GPIO_OR_SS_RAMP	GPIO_OR_AUTOMUTE	GPIO_OR_VOL_MIN	GPIO_AND_SS_RAMP	GPIO_AND_AUTOMUTE	GPIO_AND_VOL_MIN
0x3C	60	PWM COUNT	PWM_COUNT							
0x3D	61	PWM FREQUENCY	PWM_FREQ							
0x3E	62		PWM_FREQ							
0x3F	63	ADC NEGATION	RESERVED						ADC_NEG_SEL_CH2	ADC_NEG_SEL_CH1
0x40	64	ADC FIR FILTER	ADC_FILTER_SHAPE			ADC_BYPASS_FIR2X	ADC_BYPASS_FIR4X	ADC_BYPASS_IIR		
0x41	65	RESERVED	RESERVED							

0x42	66	DC BLOCKING	RESERVED		DC_BLOCK_EN_CH2	DC_BLOCK_EN_CH1	RESERVED		
0x43	67	ADC VOLUME CH1	ADC_VOLUME_CH1						
0x44	68	ADC VOLUME CH2	ADC_VOLUME_CH2						
0x45	69	ADC DIGITAL GAIN	RESERVED	ADC_DIGITAL_GAIN_CH2			RESERVED	ADC_DIGITAL_GAIN_CH1	
0x46	70	ADC PHASE INVERSION	RESERVED					ADC_VOL_PHASE_INV_CH2	ADC_VOL_PHASE_INV_CH1
0x47	71	ADC THD COMP C2	ADC_THD_COMP_C2						
0x48	72		ADC_THD_COMP_C2						
0x49	73	ADC THD COMP C3	ADC_THD_COMP_C3						
0x4A	74		ADC_THD_COMP_C3						
0x4B	75	PEAK DETECT ENABLE	RESERVED					PEAK_DETECT_EN_CH2	PEAK_DETECT_EN_CH1
0x4C	76	PEAK DETECT CONFIG	RESERVED	LOCK_PEAK_VALUE	RESERVED	PEAK_DECAY_RATE			
0x4D	77	PEAK THRESHOLDS	PEAK_THRESH_CH1						
0x4E	78		PEAK_THRESH_CH2						
0x4F-0x51	79-81	RESERVED	RESERVED						
0x52	82	MIC BIAS	RESERVED	MB_VR_BYPB	RESERVED		MB_EN	MB_VR_SET	
0x53	83	DAC FILTER CONFIG	RESERVED		DAC_BYPASS_IIR	DAC_BYPASS_FIR4X	DAC_BYPASS_FIR2X	DAC_FILTER_SHAPE	
0x54	84	DAC VOLUME CH1	DAC_VOLUME_CH1						
0x55	85	DAC VOLUME CH2	DAC_VOLUME_CH2						
0x56	86	DIRECT MONITOR VOLUME CH1	DIR_MON_VOL_CH1						
0x57	87	DIRECT MONITOR VOLUME CH2	DIR_MON_VOL_CH2						
0x58	88	DAC DIGITAL GAIN	RESERVED	DAC_DIGITAL_GAIN_CH2			RESERVED	DAC_DIGITAL_GAIN_CH1	
0x59	89	DAC PHASE INVERSION	RESERVED		DIR_MON_MONO_CH2	DIR_MON_MONO_CH1	DIR_MON_VOL_PHASE_INV_CH2	DIR_MON_VOL_PHASE_INV_CH1	DAC_VOL_PHASE_INV_CH2	DAC_VOL_PHASE_INV_CH1
0x5A	90	DAC MUTE	RESERVED		DIR_MON_MUTE_CH2	DIR_MON_MUTE_CH1	RESERVED		DAC_MUTE_CH2	DAC_MUTE_CH1
0x5B	91	SOFT RAMP CONFIG	RESERVED	DIR_MON_ADC_SEL	MUTE_RAMP_TO_GROUND	SOFT_RAMP_TIME			
0x5C	92	DC OFFSET	DC_OFFSET_CH1						
0x5D	93		DC_OFFSET_CH2						
0x5E	94	AUTOMUTE ENABLE	RESERVED					AUTOMUTE_EN_CH2	AUTOMUTE_EN_CH1
0x5F	95	AUTOMUTE TIME	AUTOMUTE_TIME						
0x60	96		RESERVED	DSD_DC_AM_EN	DSD_MUTE_AM_EN	RESERVED	AUTOMUTE_TIME		
0x61	97	AUTOMUTE LEVEL	AUTOMUTE_LEVEL						
0x62	98		AUTOMUTE_LEVEL						
0x63	99	AUTOMUTE OFF LEVEL	AUTOMUTE_OFF_LEVEL						
0x64	100		AUTOMUTE_OFF_LEVEL						
0x65	101	DAC THD COMP C2	DAC_THD_COMP_C2						
0x66	102		RESERVED				DAC_THD_COMP_C2		
0x67	103	DAC THD COMP C3	DAC_THD_COMP_C3						
0x68	104		RESERVED				DAC_THD_COMP_C3		
0x69-0x6E	105-110	RESERVED	RESERVED						
0x6F	111	CHARGE PUMP CONFIG	RESERVED					CP_EXT_NS	CP_MUTE_PD_EN
0x70	112	CHARGE PUMP CLOCK DIV	CP_CLK_DIV						
0x71-0x73	113-115	RESERVED	RESERVED						
0x74	116	PLL CLOCK SELECT	RESERVED	PLL_CLK_PHASE_INV	SEL_PLL_CLK_IN	RESERVED	EN_PLL_CLK_IN	RESERVED	
0x75	117	PLL VCO & CP	RESERVED				PLL_CP_EN	PLL_VCO_EN	PLL_CLKSMP_EN	PLL_DIG_RSTB
0x76	118	PLL REGULATOR	RESERVED				PLL_REG_EN	PLL_REG_LN	RESERVED	
0x77	119	PLL FEEDBACK DIV	PLL_CLK_FB_DIV						
0x78	120		PLL_CLK_FB_DIV						
0x79	121		PLL_CLK_FB_DIV						
0x7A	122	PLL IN & OUT DIV	PLL_CLK_IN_DIV						
0x7B	123		PLL_CLK_OUT_DIV				RESERVED	PLL_FB_DIV_LOAD	PLL_CLK_IN_DIV
0x7C-0x82	124-130	RESERVED	RESERVED						
0x83	131	ASP CONTROL	ASP_DAC_CORE_EN	ASP_DAC_MEM_FLUSH	ASP_SPI_FLASH_REG_RUN	RESERVED	ASP_PROG_SOURCE_SEL	ASP_ADC_MEM_FLUSH	ASP_PROG_EN	ASP_ADC_CORE_EN
0x84	132	ASP BYPASS	RESERVED		ASP_DAC_BYPASS_CH2	ASP_DAC_BYPASS_CH1	RESERVED		ASP_ADC_BYPASS_CH2	ASP_ADC_BYPASS_CH1
0x85	133	RESERVED	RESERVED						
0x86	134	ASP PAIRED MODE	RESERVED		ASP_DAC_PAIRED_MODE	ASP_ADC_PAIRED_MODE	RESERVED		ASP_CORE_READ_SEL	
0x87	135	ASP INPUT3 SELECT	RESERVED		ASP_DAC_IN3_SEL_CH2	ASP_DAC_IN3_SEL_CH1	RESERVED		ASP_ADC_IN3_SEL_CH2	ASP_ADC_IN3_SEL_CH1

0x88	136	ASP PRAM WRITE EN	ASP_DAC_IN3_MIX_SEL	ASP_ADC_IN3_MIX_SEL	RESERVED						ASP_DAC_PRAM_WE	ASP_ADC_PRAM_WE
0x89	137	ASP COEFF DATA WRITE EN	RESERVED		ASP_DAC_COEFF_DATA_WE_CH2	ASP_DAC_COEFF_DATA_WE_CH1	RESERVED				ASP_ADC_COEFF_DATA_WE_CH2	ASP_ADC_COEFF_DATA_WE_CH1
0x8A	138	ASP PROG MEM ADDR	ASP_PROG_MEM_ADDR									
0x8B	139	ASP PROG MEM DATA	ASP_PROG_MEM_DATA									
0x8C	140		ASP_PROG_MEM_DATA									
0x8D	141		ASP_PROG_MEM_DATA									
0x8E	142		ASP_PROG_MEM_DATA									
0x8F	143	DMA DATA2	DMA_DATA2									
0x90	144		DMA_DATA2									
0x91	145		DMA_DATA2									
0x92	146		DMA_DATA2									
0x93	147	DMA DATA3	DMA_DATA3									
0x94	148		DMA_DATA3									
0x95	149		DMA_DATA3									
0x96	150		DMA_DATA3									
0x97	151	DMA DATA4	DMA_DATA4									
0x98	152		DMA_DATA4									
0x99	153		DMA_DATA4									
0x9A	154		DMA_DATA4									
0x9B	155	DMA DATA5	DMA_DATA5									
0x9C	156		DMA_DATA5									
0x9D	157		DMA_DATA5									
0x9E	158		DMA_DATA5									
0x9F	159	DMA DATA6	DMA_DATA6									
0xA0	160		DMA_DATA6									
0xA1	161		DMA_DATA6									
0xA2	162		DMA_DATA6									
0xA3	163	DMA DATA7	DMA_DATA7									
0xA4	164		DMA_DATA7									
0xA5	165		DMA_DATA7									
0xA6	166		DMA_DATA7									
0xA7	167	DMA DATA8	DMA_DATA8									
0xA8	168		DMA_DATA8									
0xA9	169		DMA_DATA8									
0xAA	170		DMA_DATA8									
0xAB	171	DMA CORE MASK	RESERVED		DMA_DAC_CORE_MASK_CH2	DMA_DAC_CORE_MASK_CH1	RESERVED				DMA_ADC_CORE_MASK_CH2	DMA_ADC_CORE_MASK_CH1
0xAC	172	DMA WRITE EN	DMA_DATA8_WE	DMA_DATA7_WE	DMA_DATA6_WE	DMA_DATA5_WE	DMA_DATA4_WE	DMA_DATA3_WE			DMA_DATA2_WE	DMA_DATA1_WE
0xAD	173	SPI MASTER CONFIG	SPI_M_PULSE_WIDTH				SPI_M_EN	SPI_M_MODE			SPI_M_SEND_BYTE	SPI_M_START
0xAE	174	SPI MASTER DATA OUT	SPI_M_DATA_O									
0xE0	224	CODEC VALIDITY READ	RESERVED		INPUT_DATA_FORMAT_SEL_OVR		DOP_DEC_VALID	TDM_DEC_VALID			TDM_ENC_VALID	PLL_LOCKED
0xE1	225	CHIP ID	CHIP_ID									
0xE2-0xE7	226-231	RESERVED	RESERVED									
0xE8	232	AUTO FS READ	EN_64FS_MODE_AUTO	MCLK_128FS_HALF_DIV_AUTO	MCLK_128FS_DIV_AUTO							
0xE9	233	CLOCK VALIDITY	RATIO_VALID	BCK_INVALID	WS_INVALID	AUTO_CH_NUM						
0xEA	234	JACK DETECT READBACK	RESERVED					JDET_READ	RESERVED			
0xEB	235	TEMP SENSE READ	TSENSE_DATA									
0xEC	236	GPIO READBACK	RESERVED	GPIO7_R	GPIO6_R	GPIO5_R	GPIO4_R	GPIO3_R	GPIO2_R	GPIO1_R		
0xED	237	ADC CLIP DETECT FLAGS	ADC_OVERLOAD_FLAG_LAT_CH2	ADC_OVERLOAD_FLAG_LAT_CH1	ADC_OVERLOAD_FLAG_CH2	ADC_OVERLOAD_FLAG_CH1	PEAK_FLAG_LAT_CH2	PEAK_FLAG_LAT_CH1	PEAK_FLAG_CH2	PEAK_FLAG_CH1		
0xEE	238	PEAK CH1 READ	PEAK_LEVEL_CH1									
0xEF	239		PEAK_LEVEL_CH1									
0xF0	240	PEAK CH2 READ	PEAK_LEVEL_CH2									
0xF1	241		PEAK_LEVEL_CH2									
0xF2	242	DAC STATUS FLAGS	SS_RAMP_DOWN_CH2	SS_RAMP_DOWN_CH1	SS_RAMP_UP_CH2	SS_RAMP_UP_CH1	AUTOMUTE_CH2	AUTOMUTE_CH1	VOL_MIN_CH2	VOL_MIN_CH1		
0xF3-0xF4	243-244	RESERVED	RESERVED									
0xF5	245	SPI MASTER BUSY	SPI_M_ASP_PROG_BUSY	RESERVED								
0xF6-0xFB	246-251	RESERVED	RESERVED									
0xFC	252	SPI MASTER DATA IN	SPI_M_DATA_I									

Table 45 - Register Map

Register Listing

System Registers

Register 0: SYS CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b1	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	SOFT_RESET	Performs soft reset to digital core, resetting registers to their power-on defaults. Note: When performing a Soft Reset, write 0xA0 to Register 0 to ensure EN_MCLK_IN = 1'b1.
[6]	RESERVED	N/A
[5]	EN_MCLK_IN	Enables clock inputs to the digital core. • 1'b0: Disabled • 1'b1: Enabled (default)
[4]	SEL_MCLK_SRC	Selects digital core and ADC clock source when EN_MCLK_IN is set. • 1'b0: ACLK1 (default) • 1'b1: PLL_CLK
[3]	ENABLE_DAC_CH2	Enables the DAC CH2 interpolation path. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	ENABLE_DAC_CH1	Enables the DAC CH1 interpolation path. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	ENABLE_ADC_CH2	Enables the ADC CH2 decimation path. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ENABLE_ADC_CH1	Enables the ADC CH1 decimation path. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 1: FS CONFIG

Bits	[7:5]	[4]	[3]	[2]	[1]	[0]
Default	3'b000	1'b0	1'd0	1'b0	1'b0	1'b1

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4]	ADC_MONO_MODE	Enables ADC mono mode, summing CH1 and CH2 onto the CH1 path. • 1'b0: Disabled (default) • 1'b1: Enabled
[3]	RESERVED	N/A
[2]	ENABLE_64FS_MODE	Enables 64FS mode for 768k sample rate. • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	AUTO_FS_DETECT_BLOCK_64FS	Block AUTO_FS_DETECT from transitioning to 64FS mode when the detected MCLK/MCLK_128FS ratio is 64. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	AUTO_FS_DETECT	Automatically determine optimal MCLK/MCLK_128FS ratio, from detected FS. • 1'b0: Disabled, use MCLK_128FS_DIV to set ratio. • 1'b1: Enabled, overrides MCLK_128FS_DIV (default)

Register 2: ENCODER CONFIG

Bits	[7]	[6]	[5]	[4]	[3:1]	[0]
Default	1'b0	1'b0	1'b0	1'b1	3'd0	1'b1

Bits	Mnemonic	Description
[7]	ENABLE_PDM_DECODE	Enables PDM decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ENABLE_DSD_DECODE	Enables DSD decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[5]	ENABLE_DOP_DECODE	Enables DoP decoding. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	ENABLE_TDM_DECODE	Enables the PCM/TDM decoding clock. • 1'b0: Disabled • 1'b1: Enabled (default)
[3:1]	RESERVED	N/A
[0]	ENABLE_TDM_ENCODE	Enables the PCM/TDM encoding clock. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 3: INPUT & OUTPUT SELECT

Bits	[7]	[6]	[5:3]	[2:1]	[0]
Default	1'b0	1'b0	3'd0	2'b00	1'b0

Bits	Mnemonic	Description
[7]	ENABLE_SPDIF_ENCODE	Enables the S/PDIF encoding clock. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ENABLE_PDM_MIC_DECODE	Enables PDM microphone decoding clock. • 1'b0: Disabled (default) • 1'b1: Enabled
[5:3]	RESERVED	N/A
[2:1]	INPUT_DATA_FORMAT_SEL	Select which digital input format to use. • 2'b00: PCM (default) • 2'b01: DoP • 2'b10: DSD • 2'b11: PDM
[0]	RESERVED	N/A

Register 4: FRONT-END CLOCK CONTROL

Bits	[7]	[6]	[5:0]
Default	1'd0	1'b0	6'd3

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	MCLK_128FS_HALF_DIV	• 1'b0: Divide by SELECT_ADC_NUM + 1 (default) • 1'b1: Divide by half of SELECT_ADC_NUM + 1 Note: Can only produce half of an odd number divide
[5:0]	MCLK_128FS_DIV	Whole number divide value + 1 for MCLK_128FS (MCLK/divide_value). • 6'd0: Whole number divide value + 1 = 1 • 6'd3: Whole number divide value + 1 = 4 (default)

Register 5: BACK-END CLOCK CONTROL

Bits	[7:5]	[4]	[3:0]
Default	3'b000	1'b0	4'b1000

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4]	MCLK_24M_DIV2	Sets the rate of MCLK_24M as well as the analog ADC_CLK, relative to MCLK. Both clocks must be running at 22.5792 MHz or 24.576 MHz. • 1'b0: Rate = MCLK (default) • 1'b1: Rate = MCLK/2
[3:0]	RESERVED	N/A

Register 6: MASTER CLK CONFIG

Bits	[7:0]
Default	8'd7

Bits	Mnemonic	Description
[7:0]	MASTER_DCLK_DIV	Master mode DCLK and WS generation clock divider. Whole number divide value + 1 for CLK_BCK_WS_GEN (MCLK/divide_value).

Register 7: MISC CLOCK CONFIG

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	2'b00	1'b1	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7]	JDET_EN	Enable jack detection. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	TSENSE_EN	Enable temperature sensor. • 1'b0: Disabled (default) • 1'b1: Enabled
[5:4]	RESERVED	N/A
[3]	ENABLE_WS_MONITOR	Enable WS monitor, used to detect the validity of the WS signal. WS is considered invalid if BCK/WS > 1024. • 1'b0: Disabled • 1'b1: Enabled (default)
[2]	ENABLE_BCK_MONITOR	Enable BCK monitor, used to detect the validity of the BCK signal. BCK is considered invalid if MCLK/BCK > 256. • 1'b0: Disabled • 1'b1: Enabled (default)
[1]	FORCE_PLL_LOCK	Clock locking status control with PLL_LOCKED. • 1'b0: clock locking status is determined by PLL_LOCKED • 1'b1: Ignore PLL_LOCKED signal, set lock status to 1'b1
[0]	CLK_FAULT_DET_EN	Enable the clock detection circuit, sets the CLK_AVALID signal. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 8: MASTER MODE CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'd0	1'b1	1'b0	1'b0	1'b1	1'd0	1'b0

Bits	Mnemonic	Description
[7]	SLAVE_BCK_INVERT	Inverts the BCK input on DATA_CLK. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[6]	RESERVED	N/A
[5]	MASTER_WS_CLK_PHASE	Determines the CLK_BCK edge DATA_WS (GPIO2) is output on, in master mode. • 1'b0: Negative edge • 1'b1: Positive edge (default) Note: MASTER_BCK_INVERT inverts this logic.
[4]	MASTER_WS_PULSE_MODE	When enabled, master WS is a 1 BCK pulse signal instead of a 50% duty cycle signal. • 1'b0: 50% duty cycle WS signal (default) • 1'b1: Pulse WS signal
[3]	MASTER_WS_INVERT	Inverts master WS output on DATA1. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[2]	MASTER_BCK_INVERT	Inverts master BCK output on DATA_CLK. • 1'b0: Non-inverted • 1'b1: Inverted (default)
[1]	DSD_MASTER_MODE_EN	Enables DSD master mode, generating DCLK • 1'b0: Disabled, slave mode (default) • 1'b1: Enabled
[0]	PCM_MASTER_MODE_EN	Enables PCM master mode, generating BCK and WS. • 1'b0: Disabled, slave mode (default) • 1'b1: Enabled

Register 9: TDM CONFIG 1

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'b0	1'b0	5'd1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	AUTO_CH_DETECT	Automatically determine the number of TDM channels in a sample, based on the BCK/WS ratio. • 1'b0: Disabled, use TDM_CH_NUM to set channels (default) • 1'b1: Enabled, overrides TDM_CH_NUM Note: Only active in TDM slave mode.
[5]	RESERVED	N/A
[4:0]	TDM_CH_NUM	Sets number of channels in each frame. • 5'd0: 1 channel • 5'd1: 2 channels (default) • 5'd31: 32 channels

Register 10: TDM CONFIG 2

Bits	[7]	[6]	[5:4]	[3:2]	[1]	[0]
Default	1'd0	1'b0	2'b00	2'b00	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	NOISE_FLOOR_SHAPE_16BIT	Sets the shape of the 16-bit PCM/TDM noise floor. • 1'b0: 1st order noise shaping (default) • 1'b1: Flat noise shaping
[5:4]	TDM_WORD_WIDTH	Sets the width, in bits, of one data word / subframe. A subframe is a frame divided by the number of channels. • 2'b00: 32-bits (default) • 2'b01: 24-bits • 2'b10: 16-bits
[3:2]	TDM_BIT_DEPTH	Sets the bit depth, number of data bits, in one data word / subframe. • 2'b00: 32-bit (default) • 2'b01: 24-bit • 2'b10: 16-bit
[1]	TDM_VALID_EDGE	Sets which WS edge the frame starts on. • 1'b0: Frame starts on negedge of WS (default) • 1'b1: Frame starts on posedge of WS
[0]	TDM_LJ	Sets left-justified mode. • 1'b0: One BCK period delay (default) • 1'b1: Left-justified

Register 11: TDM ENC CH1 SLOT CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_ENC_SLOT_SEL_CH1	Selects which TDM channel slot is filled by the CH1 data. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 12: TDM ENC CH2 SLOT CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_ENC_SLOT_SEL_CH2	Selects which TDM channel slot is filled by the CH2 data. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 13: TDM DEC CH1 SLOT CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd0

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_DEC_SLOT_SEL_CH1	Selects which TDM channel slot is latched into CH1. • 5'd0: Slot 1 (default) • 5'd31: Slot 32

Register 14: TDM DEC CH2 SLOT CONFIG

Bits	[7:5]	[4:0]
Default	3'd0	5'd1

Bits	Mnemonic	Description
[7:5]	RESERVED	N/A
[4:0]	TDM_DEC_SLOT_SEL_CH2	Selects which TDM channel slot is latched into CH2. • 5'd0: Slot 1 • 5'd1: Slot 2 (default) • 5'd31: Slot 32

Register 15: TDM ENC DAISY CHAIN

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	TDM_ENC_DAISY_CHAIN	Enables TDM encoder daisy chain mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[6:5]	RESERVED	N/A
[4:0]	TDM_ENC_DATA_LATCH_ADJ	Adjusts the position of the MSB within each TDM slot by TDM_DATA_LATCH_ADJ clock cycles. • 5'd0: Normal position • 5'd1-31: Data output TDM_ENC_DATA_LATCH_ADJ BCKs early

Register 16: TDM DEC DAISY CHAIN

Bits	[7]	[6:5]	[4:0]
Default	1'b0	2'd0	5'd0

Bits	Mnemonic	Description
[7]	TDM_DEC_DAISY_CHAIN	Enables TDM decoder daisy chain mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[6:5]	RESERVED	N/A
[4:0]	TDM_DEC_DATA_LATCH_ADJ	Adjusts the position of the MSB within each TDM slot by TDM_DATA_LATCH_ADJ clock cycles. DAC data sampling is delayed from the normal position. • 5'd0: Normal position • 5'd1-31: DAC_TDM_DATA_LATCH_ADJ BCKs delay before sampling data

Register 17: DSD MAPPING

Bits	[7:6]	[5]	[4]	[3:0]
Default	2'd0	1'b1	1'b0	4'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	DSD_LINE_SEL_CH2	Selects the source for the DAC CH2 DSD data. • 1'b0: DATA4 • 1'b1: DATA5 (default)
[4]	DSD_LINE_SEL_CH1	Selects the source for the DAC CH1 DSD data. • 1'b0: DATA4 (default) • 1'b1: DATA5
[3:0]	RESERVED	N/A

Register 18: PDM I/O CONFIG

Bits	[7]	[6]	[5]	[4]	[3:0]
Default	1'd0	1'b1	1'b0	1'b0	4'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	PDM_DEC_SAMPLE_EDGE	Sets the edge of DATA_CLK where the PDM sample increments. • 1'b0: Rising edge • 1'b1: Falling edge (default)
[5]	PDM_DEC_DATA_PHASE	Selects the CH input edges of the PDM decoder. • 1'b0: CH1 on the rising edge of DATA_CLK, CH2 on the falling edge (default) • 1'b1: CH2 on the rising edge of DATA_CLK, CH1 on the falling edge
[4]	PDM_DEC_2X_GAIN_EN	Sets the overall datapath gain of the PDM decoder path. • 1'b0: 1x gain (default) • 1'b1: 2x gain
[3:0]	RESERVED	N/A

Register 19: PDM MIC CONFIG

Bits	[7:3]	[2]	[1]	[0]
Default	5'd0	1'b1	1'b0	1'b0

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2]	PDM_MIC_SAMPLE_EDGE	Sets the edge of PDM_CLK where the PDM sample increments. • 1'b0: Rising edge • 1'b1: Falling edge (default)
[1]	PDM_MIC_DATA_PHASE	Selects the CH output edges of the PDM encoder. • 1'b0: CH1 on the rising edge of DCLK, CH2 on the falling edge (default) • 1'b1: CH2 on the rising edge of DCLK, CH1 on the falling edge
[0]	PDM_MIC_IN_SEL	Selects the input to the ADC datapath. • 1'b0: Analog input to datapath (default) • 1'b1: PDM input to datapath

Register 20: PDM MIC CLK SELECT

Bits	[7]	[6:0]
Default	1'b0	7'd3

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:0]	PDM_MIC_CLK_DIV	Frequency divider for the PDM microphone clock, PDM_CLK. Overidden by AUTO_FS_DETECT, sets PDM_MIC_CLK_DIV = MCLK_128FS_DIV_AUTO[3:0]. • 7'd0: 2 * (PDM_MIC_CLK_DIV + 1) = DIV2 • 7'd3: 2 * (PDM_MIC_CLK_DIV + 1) = DIV8 (default) $\text{PDM\_CLK [Hz]} = \frac{\text{MCLK}}{2 \cdot (\text{PDM\_MIC\_CLK\_DIV} + 1)}$

Register 21: S/PDIF DATA SELECT

Bits	[7:1]	[0]
Default	7'd0	1'b0

Bits	Mnemonic	Description
[7:1]	RESERVED	N/A
[0]	SPDIF_DATA_SOURCE	Selects the data source for the S/PDIF encoder. • 1'b0: Output of the pcm_vol block (default) • 1'b1: Output of the TDM decoder Note: The TDM decoder output is bit perfect.

Register 22: S/PDIF CS ADDR

Bits	[7]	[5:3]	[2:0]
Default	1'b0	4'd0	3'd0

Bits	Mnemonic	Description
[7]	SPDIF_CS_WE	Write enable for the S/PDIF channel status bits. Writes the SPDIF_CS_DATA to the byte at address SPDIF_CS_BYTE_SEL. Toggle high-low to perform a write.
[5:3]	RESERVED	N/A
[2:0]	SPDIF_CS_BYTE_ADDR	Byte of the 40-bit S/PDIF Channel Status to write to.

Register 23: S/PDIF CS DATA

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	SPDIF_CS_BYTE_DATA	Data to write into the 40-bit S/PDIF Channel Status.

Register 24: VOLUME UP RAMP RATE

Bits	[7:0]
Default	8'h20

Bits	Mnemonic	Description
[7:0]	VOL_RAMP_RATE_UP	Linear step size from current volume to target volume, represented as a fraction of full-scale. $\text{ramp\_step[inc/sample]} = \frac{\text{VOL\_RAMP\_RATE\_UP}}{2^{12}}$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h20: Default • 8'hFF: Fastest change

Register 25: VOLUME DOWN RAMP RATE

Bits	[7:0]
Default	8'h20

Bits	Mnemonic	Description
[7:0]	VOL_RAMP_RATE_DOWN	Linear step size from current volume to target volume, represented as a fraction of full-scale. $\text{ramp\_step[dec/sample]} = \frac{\text{VOL\_RAMP\_RATE\_DOWN}}{2^{12}}$ • 8'h00: Instant change • 8'h01: Slowest change • 8'h20: Default • 8'hFF: Fastest change

Register 26: VOLUME RAMP SPEED

Bits	[7:1]	[0]
Default	7'd0	1'b0

Bits	Mnemonic	Description
[7:1]	RESERVED	N/A
[0]	VOL_RAMP_SPEED_SEL	Select the range of ramp rates. • 1'b0: 85ms to 334us (default) • 1'b1: 682ms to 2.70ms

Register 29-27: RESERVED

Register 30: STATUS BITS MASK

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'd0	1'b0	2'b00	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	MASK_JDET	Masks the latched Jack Detect status bit. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[5:4]	RESERVED	N/A
[3]	MASK_ADC_OVERLOAD_CH2	Masks the latched ADC_OVERLOAD status bit on ADC CH2. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[2]	MASK_ADC_OVERLOAD_CH1	Masks the latched ADC_OVERLOAD status bit on ADC CH1. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[1]	MASK_PEAK_DET_CH2	Masks the latched PEAK_FLAG status bit on ADC CH2. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled
[0]	MASK_PEAK_DET_CH1	Masks the latched PEAK_FLAG status bit on ADC CH1. • 1'b0: Status bit masked (default) • 1'b1: Status bit enabled

Register 31: STATUS BITS CLEAR

Bits	[7]	[6]	[5:4]	[3]	[2]	[1]	[0]
Default	1'd0	1'b0	2'b00	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	CLEAR_JDET	Clears the latched Jack Detect status bit. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[5:4]	RESERVED	N/A
[3]	CLEAR_ADC_OVERLOAD_CH2	Clears the latched ADC_OVERLOAD status bit on ADC CH2. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[2]	CLEAR_ADC_OVERLOAD_CH1	Clears the latched ADC_OVERLOAD status bit on ADC CH1. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[1]	CLEAR_PEAK_DET_CH2	Clears the latched PEAK_FLAG status bit on ADC CH2. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared
[0]	CLEAR_PEAK_DET_CH1	Clears the latched PEAK_FLAG status bit on ADC CH1. • 1'b0: Status bit held if asserted (default) • 1'b1: Status bit cleared

Register 48-32: RESERVED

GPIO Registers

Register 49: GPIO1/2 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO2_CFG	Configure GPIO2 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC Detection flag – output • 4'd8: OR of Status Bits – output • 4'd9: S/PDIF Stream – output • 4'd10: PWM signal – output • 4'd11: ASP Status – Input • 4'd12: ASP Status – Output • 4'd13: Output 0 – output • 4'd14: Reserved • 4'd15: JDET Flag – output
[3:0]	GPIO1_CFG	Configure GPIO1 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC Detection flag – output • 4'd8: OR of Status Bits – output • 4'd9: S/PDIF Stream – output • 4'd10: PWM signal – output • 4'd11: ASP Status – Input • 4'd12: ASP Status – Output • 4'd13: Output 0 – output • 4'd14: Reserved • 4'd15: JDET Flag – output

Register 50: GPIO3/4 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO4_CFG	Configure GPIO4 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC Detection flag – output • 4'd8: OR of Status Bits – output • 4'd9: S/PDIF Stream – output • 4'd10: PWM signal – output • 4'd11: ASP Status – Input • 4'd12: ASP Status – Output • 4'd13: Output 0 – output • 4'd14: Reserved • 4'd15: JDET Flag – output
[3:0]	GPIO3_CFG	Configure GPIO3 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC Detection flag – output • 4'd8: OR of Status Bits – output • 4'd9: S/PDIF Stream – output • 4'd10: PWM signal – output • 4'd11: ASP Status – Input • 4'd12: ASP Status – Output • 4'd13: Output 0 – output • 4'd14: Reserved • 4'd15: JDET Flag – output

Register 51: GPIO5/6 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	GPIO6_CFG	Configure GPIO6 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC Detection flag – output • 4'd8: OR of Status Bits – output • 4'd9: S/PDIF Stream – output • 4'd10: PWM signal – output • 4'd11: ASP Status – Input • 4'd12: ASP Status – Output • 4'd13: Output 0 – output • 4'd14: Reserved • 4'd15: JDET Flag – output
[3:0]	GPIO5_CFG	Configure GPIO5 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC Detection flag – output • 4'd8: OR of Status Bits – output • 4'd9: S/PDIF Stream – output • 4'd10: PWM signal – output • 4'd11: ASP Status – Input • 4'd12: ASP Status – Output • 4'd13: Output 0 – output • 4'd14: Reserved • 4'd15: JDET Flag – output

Register 52: GPIO7/8 CONFIG

Bits	[7:4]	[3:0]
Default	4'd0	4'd0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3:0]	GPIO7_CFG	Configure GPIO7 functionality. • 4'd0: Analog outputs off – shutdown (default) • 4'd1: Mute DAC Channels – input • 4'd2: Clock valid flag – output • 4'd3: PLL locked flag – output • 4'd4: DAC Minimum Volume flag – output • 4'd5: DAC Automute status – output • 4'd6: DAC Soft Ramp Done flag – output • 4'd7: ADC Detection flag – output • 4'd8: OR of Status Bits – output • 4'd9: S/PDIF Stream – output • 4'd10: PWM signal – output • 4'd11: ASP Status – Input • 4'd12: ASP Status – Output • 4'd13: Output 0 – output • 4'd14: Reserved • 4'd15: JDET Flag – output

Register 53: GPIO INPUT ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	GPIO7_SDB	• 1'b0: GPIO7 input disabled (default) • 1'b1: GPIO7 input enabled
[5]	GPIO6_SDB	• 1'b0: GPIO6 input disabled (default) • 1'b1: GPIO6 input enabled
[4]	GPIO5_SDB	• 1'b0: GPIO5 input disabled (default) • 1'b1: GPIO5 input enabled
[3]	GPIO4_SDB	• 1'b0: GPIO4 input disabled (default) • 1'b1: GPIO4 input enabled
[2]	GPIO3_SDB	• 1'b0: GPIO3 input disabled (default) • 1'b1: GPIO3 input enabled
[1]	GPIO2_SDB	• 1'b0: GPIO2 input disabled (default) • 1'b1: GPIO2 input enabled
[0]	GPIO1_SDB	• 1'b0: GPIO1 input disabled (default) • 1'b1: GPIO1 input enabled

Register 54: GPIO OUTPUT ENABLE

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	GPIO7_OE	• 1'b0: Tristate GPIO7 output (default) • 1'b1: GPIO7 output enabled
[5]	GPIO6_OE	• 1'b0: Tristate GPIO6 output (default) • 1'b1: GPIO6 output enabled
[4]	GPIO5_OE	• 1'b0: Tristate GPIO5 output (default) • 1'b1: GPIO5 output enabled
[3]	GPIO4_OE	• 1'b0: Tristate GPIO4 output (default) • 1'b1: GPIO4 output enabled
[2]	GPIO3_OE	• 1'b0: Tristate GPIO3 output (default) • 1'b1: GPIO3 output enabled
[1]	GPIO2_OE	• 1'b0: Tristate GPIO2 output (default) • 1'b1: GPIO2 output enabled
[0]	GPIO1_OE	• 1'b0: Tristate GPIO1 output (default) • 1'b1: GPIO1 output enabled

Register 55: GPIO INVERT

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	GPIO7_INV	Invert the GPIO7 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[5]	GPIO6_INV	Invert the GPIO6 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[4]	GPIO5_INV	Invert the GPIO5 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[3]	GPIO4_INV	Invert the GPIO4 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[2]	GPIO3_INV	Invert the GPIO3 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[1]	GPIO2_INV	Invert the GPIO2 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	GPIO1_INV	Invert the GPIO1 input and output. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 56: GPIO WEAK KEEPER

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	GPIO7_WK_EN	• 1'b0: GPIO7 weak keeper disabled (default) • 1'b1: GPIO7 weak keeper enabled
[5]	GPIO6_WK_EN	• 1'b0: GPIO6 weak keeper disabled (default) • 1'b1: GPIO6 weak keeper enabled
[4]	GPIO5_WK_EN	• 1'b0: GPIO5 weak keeper disabled (default) • 1'b1: GPIO5 weak keeper enabled
[3]	GPIO4_WK_EN	• 1'b0: GPIO4 weak keeper disabled (default) • 1'b1: GPIO4 weak keeper enabled
[2]	GPIO3_WK_EN	• 1'b0: GPIO3 weak keeper disabled (default) • 1'b1: GPIO3 weak keeper enabled
[1]	GPIO2_WK_EN	• 1'b0: GPIO2 weak keeper disabled (default) • 1'b1: GPIO2 weak keeper enabled
[0]	GPIO1_WK_EN	• 1'b0: GPIO1 weak keeper disabled (default) • 1'b1: GPIO1 weak keeper enabled

Register 57: GPIO READ

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	GPIO7_READ	• 1'b0: GPIO7 input readback disabled (default) • 1'b1: Allows readback of GPIO7 input
[5]	GPIO6_READ	• 1'b0: GPIO6 input readback disabled (default) • 1'b1: Allows readback of GPIO6 input
[4]	GPIO5_READ	• 1'b0: GPIO5 input readback disabled (default) • 1'b1: Allows readback of GPIO5 input
[3]	GPIO4_READ	• 1'b0: GPIO4 input readback disabled (default) • 1'b1: Allows readback of GPIO4 input
[2]	GPIO3_READ	• 1'b0: GPIO3 input readback disabled (default) • 1'b1: Allows readback of GPIO3 input
[1]	GPIO2_READ	• 1'b0: GPIO2 input readback disabled (default) • 1'b1: Allows readback of GPIO2 input
[0]	GPIO1_READ	• 1'b0: GPIO1 input readback disabled (default) • 1'b1: Allows readback of GPIO1 input

Register 58: GPIO ADC FLAG CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b1	1'b1	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	ADC_FLAG_CH_SEL	Outputs a specific channel's flag if the corresponding GPIO_AND and GPIO_OR are not set. • 1'b0: Outputs status/flag from CH1 • 1'b1: Outputs status/flag from CH2
[5]	GPIO_OR_OVERLOAD	Sets the GPIO_CFG "ADC Dectection Flag" output as the bitwise OR of all channel statuses. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is (|adc_overload_flag) (default)
[4]	GPIO_OR_PEAK_DET	Sets the GPIO_CFG "ADC Detection Flag" output as the bitwise OR of all channel statuses. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is (|adc_peak_flag) (default)
[3]	GPIO_AND_OVERLOAD	Sets the GPIO_CFG "ADC Detection Flag" output as the bitwise AND of all channel statuses. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is (&adc_overload_flag) Note: Overridden by GPIO_OR_OVERLOAD
[2]	GPIO_AND_PEAK_DET	Sets the GPIO_CFG "ADC Detection Flag" output as the bitwise AND of all channel statuses. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is (&adc_peak_flag) Note: Overridden by GPIO_OR_PEAK_DET
[1]	ADC_UNLAT_FLAG_EN	Set the ADC detection flags to use the unlatched value, instead of the latched value. • 1'b0: Latched flags (default) • 1'b1: Unlatched flags
[0]	ADC_DET_FLAG_SEL	Selects which ADC detection flag to output when gpio_cfg is set to "ADC Detection Flag". • 1'b0: Peak Detect Flag (default) • 1'b1: ADC Overload Flag

Register 59: GPIO DAC FLAG CONFIG

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'd0	1'b0	1'b0	1'b0	1'b0	1'b1	1'b1	1'b1

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	DAC_FLAG_CH_SEL	Outputs a specific channel's flag if the corresponding GPIO_AND and GPIO_OR are not set. • 1'b0: Outputs status/flag from CH1 • 1'b1: Outputs status/flag from CH2
[5]	GPIO_OR_SS_RAMP	Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise OR of both channel's flags. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is (|ss_full_ramp)
[4]	GPIO_OR_AUTOMUTE	Sets the GPIO_CFG "Automute Status" output as the bitwise OR of both channel's statuses. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is (|automute)
[3]	GPIO_OR_VOL_MIN	Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise OR of both channel's flags. • 1'b0: Disabled (default) • 1'b1: Enabled, GPIO_CFG output is (|vol_min)
[2]	GPIO_AND_SS_RAMP	Sets the GPIO_CFG "Soft Ramp Done" flag output as the bitwise AND of both channel's flags. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is (&ss_full_ramp) (default) Note: Overridden by GPIO_OR_SS_RAMP.
[1]	GPIO_AND_AUTOMUTE	Sets the GPIO_CFG "Automute Status" output as the bitwise AND of both channel's statuses. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is (&automute) (default) Note: Overridden by GPIO_OR_AUTOMUTE.
[0]	GPIO_AND_VOL_MIN	Sets the GPIO_CFG "Minimum Volume" flag output as the bitwise AND of both channel's flags. • 1'b0: Disabled • 1'b1: Enabled, GPIO_CFG output is (&vol_min) (default) Note: Overridden by GPIO_OR_VOL_MIN.

Register 60: PWM COUNT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	PWM_COUNT	8-bit value for the number of MCLK periods the PWM signal is high. • 8'h00: Disabled (default) • 8'h01: Minimum • 8'hFF: Maximum

Register 62-61: PWM FREQUENCY

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	PWM_FREQ	16-bit value for the frequency of the PWM signal. • 16'h0000: Disabled (default) • 16'h0001: Minimum • 16'hFFFF: Maximum $\text{frequency [Hz]} = \frac{\text{MCLK}}{\text{PWM\_FREQ} + 1}$ $\text{Duty Cycle [\%]} = \left(\frac{\text{PWM\_COUNT}}{\text{PWM\_FREQ} + 1}\right) \cdot 100$

ADC Registers

Register 63: ADC NEGATION

Bits	[7:2]	[1]	[0]
Default	6'b000000	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	ADC_NEG_SEL_CH2	Inverts data input from the CH2 analog ADC. • 1'b0: No inversion (default) • 1'b1: Inverts input data
[0]	ADC_NEG_SEL_CH1	Inverts data input from the CH1 analog ADC. • 1'b0: No inversion (default) • 1'b1: Inverts input data

Register 64: ADC FIR FILTER

Bits	[7:5]	[4]	[3]	[2:0]
Default	3'd0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:5]	ADC_FILTER_SHAPE	Selects the 8x decimation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase fast roll-off apodizing • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion
[4]	ADC_BYPASS_FIR2X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_2x
[3]	ADC_BYPASS_FIR4X	• 1'b0: Non-bypass (default) • 1'b1: Bypass DFir_4x
[2:0]	ADC_BYPASS_IIR	Bypass IIR Filter. • 3'b000: Non-bypass (default) • 3'b111: Bypass IIR • Others: Reserved

Register 65: RESERVED

Register 66: DC BLOCKING

Bits	[7:6]	[5]	[4]	[3:0]
Default	2'd0	1'b1	1'b1	4'b0010

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	DC_BLOCK_EN_CH2	Enable the CH2 DC blocking filter on audio datapath. • 1'b0: Bypass DC blocking filter • 1'b1: Use DC blocking filter (default)
[4]	DC_BLOCK_EN_CH1	Enable the CH1 DC blocking filter on audio datapath. • 1'b0: Bypass DC blocking filter • 1'b1: Use DC blocking filter (default)
[3:0]	RESERVED	N/A

Register 67: ADC VOLUME CH1

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	ADC_VOLUME_CH1	CH1 volume. 0dB to -127dB, 0.5dB steps. • 8'h00: 0dB (default) • 8'hFE: -127dB • 8'hFF: Mute

Register 68: ADC VOLUME CH2

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	ADC_VOLUME_CH2	CH2 volume. 0dB to -127dB, 0.5dB steps. • 8'h00: 0dB (default) • 8'hFE: -127dB • 8'hFF: Mute

Register 69: ADC DIGITAL GAIN

Bits	[7]	[6:4]	[3]	[2:0]
Default	1'd0	3'd0	1'd0	3'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:4]	ADC_DIGITAL_GAIN_CH2	ADC CH2 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd1: +6dB • 3'd2: +12dB • 3'd3: +18dB • 3'd4: +24dB • 3'd5: +30dB • 3'd6: +36dB • 3'd7: +42dB
[3]	RESERVED	N/A
[2:0]	ADC_DIGITAL_GAIN_CH1	ADC CH1 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd1: +6dB • 3'd2: +12dB • 3'd3: +18dB • 3'd4: +24dB • 3'd5: +30dB • 3'd6: +36dB • 3'd7: +42dB

Register 70: ADC PHASE INVERSION

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	ADC_VOL_PHASE_INV_CH2	Inverts the phase of VOLUME_CH2. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	ADC_VOL_PHASE_INV_CH1	Inverts the phase of VOLUME_CH1. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 72-71: ADC THD COMP C2

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	ADC_THD_COMP_C2	A 16-bit signed coefficient for correcting for the ADC 2nd harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$ Note: Register value is internally XOR'd with 16'hFFFC

Register 74-73: ADC THD COMP C3

Bits	[15:0]
Default	16'h0000

Bits	Mnemonic	Description
[15:0]	ADC_THD_COMP_C3	A 16-bit signed coefficient for correcting for the ADC 3rd harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$ Note: Register value is internally XOR'd with 16'hFFE2

Register 75: PEAK DETECT ENABLE

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	PEAK_DETECT_EN_CH2	Enables the ADC CH2 peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	PEAK_DETECT_EN_CH1	Enables the ADC CH1 peak detector. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 76: PEAK DETECT CONFIG

Bits	[7]	[6]	[5]	[4:0]
Default	1'd0	1'b0	1'b0	5'd10

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	LOCK_PEAK_VALUE	Locks the current peak detector values, for reading back. • 1'b0: Peak detector value can update (default) • 1'b1: Peak detector value locked
[5]	RESERVED	N/A
[4:0]	PEAK_DECAY_RATE	Sets the speed at which the peak detector value will decay when greater than the input signal. • 5'd0: Instant decay • 5'd1: Fastest decay • 5'd10: Default value • 5'd22: Slowest decay • Others: Reserved

Register 78-77: PEAK THRESHOLDS

Bits	[15:8]	[7:0]
Default	8'hFF	8'hFF

Bits	Mnemonic	Description
[15:8]	PEAK_THRESH_CH2	Threshold value to trigger the PEAK_FLAG in the CH2 peak detector. Triggers if the input signal > PEAK_THRESH_CH2. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{threshold [dB]} = 20 \cdot \log10\left(\frac{\text{PEAK\_THRESH\_CH2}}{2^8 - 1}\right) + 0.56$
[7:0]	PEAK_THRESH_CH1	Threshold value to trigger the PEAK_FLAG in the CH1 peak detector. Triggers if the input signal > PEAK_THRESH_CH1. • 8'h01: -48dB • 8'hFF: 0dB (default) $\text{threshold [dB]} = 20 \cdot \log10\left(\frac{\text{PEAK\_THRESH\_CH1}}{2^8 - 1}\right) + 0.56$

Register 81-79: RESERVED

Register 82: MIC BIAS

Bits	[7]	[6]	[5:4]	[3]	[2:0]
Default	1'b0	1'b0	2'b00	1'b0	3'b010

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	MB_VR_BYPB	Bypass the MICBIAS reference voltage select. • 1'b0: 2.85V (default) • 1'b1: Determined by MB_VR_SET
[5:4]	RESERVED	N/A
[3]	MB_EN	Enables the MICBIAS. • 1'b0: Disabled (default) • 1'b1: Enabled
[2:0]	MB_VR_SET	Set mic bias voltage. • 3'b000: 1.45V • 3'b001: 2.55V • 3'b010: 2.65V (default) • 3'b011: 2.75V • 3'b100: 1.65V • 3'b101: 1.75V • 3'b110: 1.85V • 3'b111: 1.95V

DAC Registers

Register 83: DAC FILTER CONFIG

Bits	[7:6]	[5]	[4]	[3]	[2:0]
Default	2'd0	1'b0	1'b0	1'b0	3'd0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	DAC_BYPASS_IIR	Bypass the IIR filter. • 1'b0: Non-bypassed (default) • 1'b1: Bypassed
[4]	DAC_BYPASS_FIR4X	Bypass the 4X FIR filter. • 1'b0: Non-bypassed (default) • 1'b1: Bypassed
[3]	DAC_BYPASS_FIR2X	Bypass the 2X FIR filter. • 1'b0: Non-bypassed (default) • 1'b1: Bypassed
[2:0]	DAC_FILTER_SHAPE	Selects the 8x interpolation FIR filter shape. • 3'd0: Minimum phase (default) • 3'd1: Linear phase fast roll-off apodizing • 3'd2: Linear phase fast roll-off • 3'd3: Linear phase fast roll-off low ripple • 3'd4: Linear phase slow roll-off • 3'd5: Minimum phase fast roll-off • 3'd6: Minimum phase slow roll-off • 3'd7: Minimum phase slow roll-off low dispersion

Register 84: DAC VOLUME CH1

Bits	[7:0]
Default	8'h02

Bits	Mnemonic	Description
[7:0]	DAC_VOLUME_CH1	DAC CH1 volume. +1dB to -126dB, 0.5dB steps • 8'h00: +1dB • 8'h02: 0dB (default) • 8'hFE: -126dB • 8'hFF: Mute

Register 85: DAC VOLUME CH2

Bits	[7:0]
Default	8'h02

Bits	Mnemonic	Description
[7:0]	DAC_VOLUME_CH2	DAC CH2 volume. +1dB to -126dB, 0.5dB steps • 8'h00: +1dB • 8'h02: 0dB (default) • 8'hFE: -126dB • 8'hFF: Mute

Register 86: DIRECT MONITOR VOLUME CH1

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	DIR_MON_VOL_CH1	Volume of ADC CH1 direct monitor signal added into DAC CH1. +1dB to -126dB, 0.5dB steps. • 8'h00: +1dB • 8'h02: 0dB • 8'hFE: -126dB • 8'hFF: -inf dB (default)

Register 87: DIRECT MONITOR VOLUME CH2

Bits	[7:0]
Default	8'hFF

Bits	Mnemonic	Description
[7:0]	DIR_MON_VOL_CH2	Volume of ADC CH2 direct monitor signal added into DAC CH2. +1dB to -126dB, 0.5dB steps. • 8'h00: +1dB • 8'h02: 0dB • 8'hFE: -126dB • 8'hFF: -inf dB (default)

Register 88: DAC DIGITAL GAIN

Bits	[7]	[6:4]	[3]	[2:0]
Default	1'd0	3'd0	1'd0	3'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6:4]	DAC_DIGITAL_GAIN_CH2	ADC CH2 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd1: +6dB • 3'd2: +12dB • 3'd3: +18dB • 3'd4: +24dB • 3'd5: +30dB • 3'd6: +36dB • 3'd7: +42dB
[3]	RESERVED	N/A
[2:0]	DAC_DIGITAL_GAIN_CH1	ADC CH1 gain boost. +0dB to +42dB, +6dB steps. • 3'd0: +0dB (default) • 3'd1: +6dB • 3'd2: +12dB • 3'd3: +18dB • 3'd4: +24dB • 3'd5: +30dB • 3'd6: +36dB • 3'd7: +42dB

Register 89: DAC PHASE INVERSION

Bits	[7:6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	2'd0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	DIR_MON_MONO_CH2	Adds both ADC direct monitor signals onto the CH2 DAC datapath. Both signals are controlled by the CH2 volume and mute controls. • 1'b0: Disabled, CH2 ADC monitored on CH2 DAC (default) • 1'b1: Enabled, CH1 ADC & CH2 ADC monitored on CH2 DAC
[4]	DIR_MON_MONO_CH1	Adds both ADC direct monitor signals onto the CH1 DAC datapath. Both signals are controlled by the CH1 volume and mute controls. • 1'b0: Disabled, CH1 ADC monitored on CH1 DAC (default) • 1'b1: Enabled, CH1 ADC & CH2 ADC monitored on CH1 DAC
[3]	DIR_MON_VOL_PHASE_INV_CH2	Inverts the phase of DIR_MON_VOL_CH2. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[2]	DIR_MON_VOL_PHASE_INV_CH1	Inverts the phase of DIR_MON_VOL_CH1. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[1]	DAC_VOL_PHASE_INV_CH2	Inverts the phase of DAC_VOLUME_CH2. • 1'b0: Non-inverted (default) • 1'b1: Inverted
[0]	DAC_VOL_PHASE_INV_CH1	Inverts the phase of DAC_VOLUME_CH1. • 1'b0: Non-inverted (default) • 1'b1: Inverted

Register 90: DAC MUTE

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'd0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	DIR_MON_MUTE_CH2	Mutes the CH2 ADC direct monitor signal. • 1'b0: Normal operation (default) • 1'b1: Direct monitor signal muted
[4]	DIR_MON_MUTE_CH1	Mutes the CH1 ADC direct monitor signal. • 1'b0: Normal operation (default) • 1'b1: Direct monitor signal muted
[3:2]	RESERVED	N/A
[1]	DAC_MUTE_CH2	Mutes the CH2 DAC datapath, will not mute the monitor signal. • 1'b0: Normal CH2 operation (default) • 1'b1: Mute CH2 DAC
[0]	DAC_MUTE_CH1	Mutes the CH1 DAC datapath, will not mute the monitor signal. • 1'b0: Normal CH1 operation (default) • 1'b1: Mute CH1 DAC

Register 91: SOFT RAMP CONFIG

Bits	[7]	[6]	[5]	[4:0]
Default	1'b0	1'b0	1'b1	5'd3

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	DIR_MON_ADC_SEL	Selects the Direct Monitor source, from the ADC datapath. • 1'b0: Pre-ASP, minimizes delay (default) • 1'b1: Post-ASP
[5]	MUTE_RAMP_TO_GROUND	• 1'b0: When ramped to min volume during normal mute, do not soft ramp to ground • 1'b1: When ramped to min volume during normal mute, soft ramp to ground for power saving (default) normal mute includes: automute, mute by register, mute by GPIO
[4:0]	SOFT_RAMP_TIME	Sets the amount of time that it takes to perform a soft start ramp. This time affects both ramp to ground and ramp to AVCC/2. Valid from 0 to 12. $\text{Time [s]} = \frac{2^{16} \cdot 2^{\text{SOFT\_RAMP\_TIME}}}{MCLK \cdot 2^{\sim\text{MCLK\_24M\_DIV2}}}$

Register 93-92: DC OFFSET

Bits	[15:8]	[7:0]
Default	8'h00	8'h00

Bits	Mnemonic	Description
[15:8]	DC_OFFSET_CH2	Signed 8-bit DC offset value added to the CH2 datapath signal, 100 uV/step. • 8'hFF: -12.7mV DC Offset • 8'h00: 0mV DC Offset (default) • 8'h7F: 12.7mV DC Offset
[7:0]	DC_OFFSET_CH1	Signed 8-bit DC offset value added to the CH1 datapath signal, 100 uV/step. • 8'hFF: -12.7mV DC Offset • 8'h00: 0mV DC Offset (default) • 8'h7F: 12.7mV DC Offset

Register 94: AUTOMUTE ENABLE

Bits	[7:2]	[1]	[0]
Default	6'd0	1'b1	1'b1

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	AUTOMUTE_EN_CH2	Enables CH2 automute. • 1'b0: Disabled • 1'b1: Enabled (default)
[0]	AUTOMUTE_EN_CH1	Enables CH1 automute. • 1'b0: Disabled • 1'b1: Enabled (default)

Register 96-95: AUTOMUTE TIME

Bits	[15]	[14]	[13]	[12:11]	[10:0]
Default	1'd0	1'b1	1'b1	2'd0	11'h0F

Bits	Mnemonic	Description
[15]	RESERVED	N/A
[14]	DSD_DC_AM_EN	Enables the DSD DC automute detection. • 1'b0: Disabled • 1'b1: Enabled (default)
[13]	DSD_MUTE_AM_EN	Enables the DSD automute condition, if a DSD mute pattern is detected. • 1'b0: Disabled • 1'b1: Enabled (default)
[12:11]	RESERVED	N/A
[10:0]	AUTOMUTE_TIME	Configures the amount of time in seconds the audio must remain below AUTOMUTE_LEVEL before an automute condition is flagged. • 11'h000: Disabled • 11'h001: Slowest • 11'h00F: Default • 11'h7FF: Fastest $\text{Time [s]} = \frac{2^{18}}{\text{AUTOMUTE\_TIME} \cdot FS}$

Register 98-97: AUTOMUTE LEVEL

Bits	[15:0]
Default	16'h0008

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_LEVEL	The threshold which the audio must be below before an automute condition is flagged. • 16'h0001: -138dB • 16'h0008: -120dB (default) • 16'hFFFF: -42dB $\text{level [dB]} = 20 \cdot \log10\left(\frac{\text{AUTOMUTE\_LEVEL}}{(2^{16}-1)\cdot 2^{7}}\right)$

Register 100-99: AUTOMUTE OFF LEVEL

Bits	[15:0]
Default	16'h000A

Bits	Mnemonic	Description
[15:0]	AUTOMUTE_OFF_LEVEL	The threshold which the audio must be above before the automute condition is immediately cleared. • 16'h0001: -138dB • 16'h000A: -118dB (default) • 16'hFFFF: -42dB $\text{level [dB]} = 20 \cdot \log10\left(\frac{\text{AUTOMUTE\_OFF\_LEVEL}}{(2^{16}-1)\cdot 2^{7}}\right)$

Register 102-101: DAC THD COMP C2

Bits	[15:12]	[11:0]
Default	4'd0	12'h000

Bits	Mnemonic	Description
[15:12]	RESERVED	N/A
[11:0]	DAC_THD_COMP_C2	A 12-bit signed coefficient for correcting for the DAC 2nd harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$ Note: Register value is internally XOR'd with 12'h222

Register 104-103: DAC THD COMP C3

Bits	[15:12]	[11:0]
Default	4'd0	12'h000

Bits	Mnemonic	Description
[15:12]	RESERVED	N/A
[11:0]	DAC_THD_COMP_C3	A 12-bit signed coefficient for correcting for the DAC 3rd harmonic distortion. $output = x + c2 \cdot x^2 + c3 \cdot x^3$ Note: Register value is internally XOR'd with 12'h030

Register 110-105: RESERVED

Register 111: CHARGE PUMP CONFIG

Bits	[7:2]	[1]	[0]
Default	6'b000010	1'b0	1'b1

Bits	Mnemonic	Description
[7:2]	RESERVED	N/A
[1]	CP_EXT_NS	Disables the DAC Charge Pump, negative voltage supplied externally. • 1'b0: Charge Pump enabled (default) • 1'b1: Charge Pump disabled
[0]	CP_MUTE_PD_EN	Charge pump state control when the DAC mutes. • 1'b0: Keep charge pump on when DAC mutes • 1'b1: Turn off charge pump when DAC mutes (default)

Register 112: CHARGE PUMP CLOCK DIV

Bits	[7:0]
Default	8'd31

Bits	Mnemonic	Description
[7:0]	CP_CLK_DIV	Specifies the clk divider for the CP clock source. $\text{CP\_CLK [Hz]} = \frac{\text{MCLK}}{2^{\text{MCLK\_24M\_DIV2}} \cdot (\text{CP\_CLK\_DIV} + 1)}$

Register 115-113: RESERVED

PLL Registers

Register 116: PLL CLOCK SELECT

Bits	[7]	[6]	[5]	[4]	[3]	[2:0]
Default	1'b0	1'b0	1'b1	1'd0	1'b0	3'd0

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	PLL_CLK_PHASE_INV	Digital/analog DAC clock invert phase enable. • 1'b0: Digital/analog DAC clocks have inverted phase (default) • 1'b1: Digital/analog DAC clocks have the same phase
[5]	SEL_PLL_CLK_IN	Selects PLL input clock source when EN_PLL_CLK_IN is set. • 1'b0: ACLK • 1'b1: DCLK (default)
[4]	RESERVED	N/A
[3]	EN_PLL_CLK_IN	Allows SEL_PLL_CLK_IN to select PLL input clocks. • 1'b0: Disables SEL_PLL_CLK_IN (default) • 1'b1: Enables SEL_PLL_CLK_IN
[2:0]	RESERVED	N/A

Register 117: PLL VCO & CP

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'b0011	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	PLL_CP_EN	Enables/disables the PLL charge pump. • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	PLL_VCO_EN	Enables/disables the PLL voltage-controlled oscillator (VCO). • 1'b0: Disabled (default) • 1'b1: Enabled
[1]	PLL_CLKSMP_EN	Power Down the PLL circuitry. • 1'b0: PLL Block disabled (default) • 1'b1: PLL Block enabled
[0]	PLL_DIG_RSTB	Resets the Digital core of the PLL.

Register 118: PLL REGULATOR

Bits	[7:4]	[3]	[2]	[1:0]
Default	4'd0	1'b0	1'b1	2'b10

Bits	Mnemonic	Description
[7:4]	RESERVED	N/A
[3]	PLL_REG_EN	Power down the PLL regulator. • 1'b0: Disable the PLL regulator (default) • 1'b1: Enable the PLL regulator
[2]	PLL_REG_LN	Select low noise reference for HV regulator. • 1'b0: Disabled (default) • 1'b1: Enabled
[1:0]	RESERVED	N/A

Register 121-119: PLL FEEDBACK DIV

Bits	[23:0]
Default	24'h100000

Bits	Mnemonic	Description
[23:0]	PLL_CLK_FB_DIV	Sets the PLL clock feedback divider (Nfb). • 24'h000000: Reserved • 24'h100000: Default • 24'hn: Divide by 2^25/n

Register 124-122: PLL IN & OUT DIV

Bits	[23:16]	[15:12]	[11:10]	[9]	[8:0]
Default	8'b00010000	4'd3	2'd0	1'b1	9'd0

Bits	Mnemonic	Description
[23:16]	RESERVED	N/A
[15:12]	PLL_CLK_OUT_DIV	Sets the PLL clock output divider (No). • 4'd0: Reserved • 4'd3: Divide by 4. (default) • 4'dn: Divide by (n + 1).
[11:10]	RESERVED	N/A
[9]	PLL_FB_DIV_LOAD	Write 1'b1 then write 1'b0 to load CLK_FB_DIV.
[8:0]	PLL_CLK_IN_DIV	Sets the PLL clock input divider (Ni). • 9'd0: Reserved (default) • 9'dn: Divide by (n + 1).

Register 130-125: RESERVED

ASP Registers

Register 131: ASP CONTROL

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b1	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ASP_DAC_CORE_EN	Enables programmed DAC ASP functionality. • 1'b0: Disabled (default) • 1'b1: Enabled
[6]	ASP_DAC_MEM_FLUSH	Flushes the DAC ASP memories, clearing any existing programming. Requires ASP_DAC_CORE_EN to not be set.
[5]	ASP_SPI_FLASH_REG_RUN	Toggle to transfer a byte of data from the I2C registers over the SPI master interface.
[4]	RESERVED	N/A
[3]	ASP_PROG_SOURCE_SEL	Selects which interface programs the ASP. • 1'b0: I2C programming (default) • 1'b1: SPI master programming
[2]	ASP_ADC_MEM_FLUSH	Flushes the ADC ASP memories, clearing any existing programming. Requires ASP_ADC_CORE_EN to not be set.
[1]	ASP_PROG_EN	Enables ASP programming. Programmed functionality overridden. • 1'b0: Programming disabled (default) • 1'b1: Programming enabled
[0]	ASP_ADC_CORE_EN	Enables programmed ASP functionality. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 132: ASP BYPASS

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'd0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	ASP_DAC_BYPASS_CH2	Bypasses the DAC ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[4]	ASP_DAC_BYPASS_CH1	Bypasses the DAC ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[3:2]	RESERVED	N/A
[1]	ASP_ADC_BYPASS_CH2	Bypasses the ADC ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed
[0]	ASP_ADC_BYPASS_CH1	Bypasses the ADC ASP core, but leaves it running. • 1'b0: Un-bypassed (default) • 1'b1: Bypassed

Register 133: RESERVED

Register 134: ASP PAIRED MODE

Bits	[7:6]	[5]	[4]	[3:2]	[1:0]
Default	2'd0	1'b0	1'b0	2'b0	2'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	ASP_DAC_PAIRED_MODE	Enables the DAC ASP core paired mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	ASP_ADC_PAIRED_MODE	Enables the ADC ASP core paired mode. • 1'b0: Disabled (default) • 1'b1: Enabled
[3:2]	RESERVED	N/A
[1:0]	ASP_CORE_READ_SEL	Determines the ASP core connected to the GPIOs • 2'd0: ADC CH1 (default) • 2'd1: ADC CH2 • 2'd2: DAC CH1 • 2'd3: DAC CH2

Register 135: ASP INPUT3 SELECT

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'd0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	ASP_DAC_IN3_SEL_CH2	Selects DAC CH2 ASP core input3 connection. • 1'b0: ADC CH2 data (default) • 1'b1: GPIO Input flags
[4]	ASP_DAC_IN3_SEL_CH1	Selects DAC CH1 ASP core input3 connection. • 1'b0: ADC CH1 data (default) • 1'b1: GPIO Input flags
[3:2]	RESERVED	N/A
[1]	ASP_ADC_IN3_SEL_CH2	Selects ADC CH2 ASP core input3 connection. • 1'b0: DAC CH2 data (default) • 1'b1: GPIO Input flags
[0]	ASP_ADC_IN3_SEL_CH1	Selects ADC CH1 ASP core input3 connection. • 1'b0: DAC CH1 data (default) • 1'b1: GPIO Input flags

Register 136: ASP PRAM WRITE EN

Bits	[7]	[6]	[5:2]	[1]	[0]
Default	1'b0	1'b0	4'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	ASP_DAC_IN3_MIX_SEL	Selects the data point for the DAC ASP core input3 connection. • 1'b0: Pre-ASP ADC datapath (default) • 1'b1: Post-ASP ADC datapath
[6]	ASP_ADC_IN3_MIX_SEL	Selects the data point for the ADC ASP core input3 connection. • 1'b0: Pre-ASP DAC datapath (default) • 1'b1: Post-ASP DAC datapath
[5:2]	RESERVED	N/A
[1]	ASP_DAC_PRAM_WE	Enables writing to the DAC ASP's program (PRAM) memory. Memory shared between all DAC ASP cores. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ASP_ADC_PRAM_WE	Enables writing to the ADC ASP's program (PRAM) memory. Memory shared between all ADC ASP cores. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 137: ASP COEFF DATA WRITE EN

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'd0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	ASP_DAC_COEFF_DATA_WE_CH2	Enables writing to the DAC CH2 ASP core's coefficient (CRAM) and data (DRAM) memories. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	ASP_DAC_COEFF_DATA_WE_CH1	Enables writing to the DAC CH1 ASP core's coefficient (CRAM) and data (DRAM) memories. • 1'b0: Disabled (default) • 1'b1: Enabled
[3:2]	RESERVED	N/A
[1]	ASP_ADC_COEFF_DATA_WE_CH2	Enables writing to the ADC CH2 ASP core's coefficient (CRAM) and data (DRAM) memories. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	ASP_ADC_COEFF_DATA_WE_CH1	Enables writing to the ADC CH1 ASP core's coefficient (CRAM) and data (DRAM) memories. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 138: ASP PROG MEM ADDR

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	ASP_PROG_MEM_ADDR	Selects the address of the programmable memories when programming the ASP. If writing to the CRAM or DRAM ASP_PROG_MEM_ADDR[7] selects the momory accessed. • 1'b0: DRAM • 1'b1: CRAM When ASP programming is disabled, acts as the DMA_ADDR offset.

Register 142-139: ASP PROG MEM DATA

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	ASP_PROG_MEM_DATA	32-bit data written to the programmable memories at address ASP_PROG_MEM_ADDR. The memory written depends on which write enable is toggled. If writing to PRAM, use ASP_PROG_RAM_WE, and the data format is {insn[i + 256], insn[i]}. If writing to CRAM or DRAM, use ASP_COEFF_DATA_WE_CHx. When ASP programming is disabled, control acts as the DMA_DATA1 element.

Register 146-143: DMA DATA2

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA2	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 1.

Register 150-147: DMA DATA3

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA3	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 2.

Register 154-151: DMA DATA4

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA4	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 3.

Register 158-155: DMA DATA5

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA5	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 4.

Register 162-159: DMA DATA6

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA6	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 5.

Register 166-163: DMA DATA7

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA7	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 6.

Register 170-167: DMA DATA8

Bits	[31:0]
Default	32'd0

Bits	Mnemonic	Description
[31:0]	DMA_DATA8	32-bit coefficient stack data written to the ASP core coeff stack at address ASP_DMA_ADDR + 7.

Register 171: DMA CORE MASK

Bits	[7:6]	[5]	[4]	[3:2]	[1]	[0]
Default	2'd0	1'b0	1'b0	2'd0	1'b0	1'b0

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5]	DMA_DAC_CORE_MASK_CH2	Masks the DAC CH2 ASP core, allowing it to update the core's coeff stack with the DMA values. • 1'b0: Disabled (default) • 1'b1: Enabled
[4]	DMA_DAC_CORE_MASK_CH1	Masks the DAC CH1 ASP core, allowing it to update the core's coeff stack with the DMA values. • 1'b0: Disabled (default) • 1'b1: Enabled
[3:2]	RESERVED	N/A
[1]	DMA_ADC_CORE_MASK_CH2	Masks the ADC CH2 ASP core, allowing it to update the core's coeff stack with the DMA values. • 1'b0: Disabled (default) • 1'b1: Enabled
[0]	DMA_ADC_CORE_MASK_CH1	Masks the ADC CH1 ASP core, allowing it to update the core's coeff stack with the DMA values. • 1'b0: Disabled (default) • 1'b1: Enabled

Register 172: DMA WRITE EN

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7]	DMA_DATA8_WE	DMA DATA8 write enable, loads into CRAM[DMA_ADDR+7]. Toggle to 1'b0 before updating DMA_DATA8 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[6]	DMA_DATA7_WE	DMA DATA7 write enable, loads into CRAM[DMA_ADDR+6]. Toggle to 1'b0 before updating DMA_DATA7 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[5]	DMA_DATA6_WE	DMA DATA6 write enable, loads into CRAM[DMA_ADDR+5]. Toggle to 1'b0 before updating DMA_DATA6 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[4]	DMA_DATA5_WE	DMA DATA5 write enable, loads into CRAM[DMA_ADDR+4]. Toggle to 1'b0 before updating DMA_DATA5 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[3]	DMA_DATA4_WE	DMA DATA4 write enable, loads into CRAM[DMA_ADDR+3]. Toggle to 1'b0 before updating DMA_DATA4 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[2]	DMA_DATA3_WE	DMA DATA3 write enable, loads into CRAM[DMA_ADDR+2]. Toggle to 1'b0 before updating DMA_DATA3 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[1]	DMA_DATA2_WE	DMA DATA2 write enable, loads into CRAM[DMA_ADDR+1]. Toggle to 1'b0 before updating DMA_DATA2 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active
[0]	DMA_DATA1_WE	DMA DATA1 write enable, loads into CRAM[DMA_ADDR]. Toggle to 1'b0 before updating DMA_DATA1 or DMA_ADDR. • 1'b0: DMA load inactive (default) • 1'b1: DMA load active

Register 173: SPI MASTER CONFIG

Bits	[7:4]	[3]	[2]	[1]	[0]
Default	4'd0	1'b0	1'b0	1'b0	1'b0

Bits	Mnemonic	Description
[7:4]	SPI_M_PULSE_WIDTH	Sets the master SCLK frequency. $\text{SCLK [Hz]} = \frac{\text{MCLK}}{2 \cdot \text{SPI\_M\_PULSE\_WIDTH}}$
[3]	SPI_M_EN	Enable the SPI Master • 1'b0: Disabled (default) • 1'b1: Enabled
[2]	SPI_M_MODE	SPI Mode • 1'b0: Mode 0 (default) • 1'b1: Mode 3
[1]	SPI_M_SEND_BYTE	Triggers the SPI master to send the current byte in SPI_M_DATA_O to the slave device. • 1'b0: Do not send byte (default) • 1'b1: Send byte to SPI slave device
[0]	SPI_M_START	Start/stop SPI master transactions. • 1'b0: Transactions stopped (default) • 1'b1: Transactions started

Register 174: SPI MASTER DATA OUT

Bits	[7:0]
Default	8'h00

Bits	Mnemonic	Description
[7:0]	SPI_M_DATA_O	Data byte to send over the SPI master interface.

Readback Registers

Register 224: CODEC VALIDITY READ

Bits	[7:6]	[5:4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-

Bits	Mnemonic	Description
[7:6]	RESERVED	N/A
[5:4]	INPUT_DATA_FORMAT_SEL_OVR	Readback of the current input data format. Either the manual value, or the result of AUTO_DATA_FORMAT_SEL if enabled. • 2'd0: PCM • 2'd1: DoP • 2'd2: DSD • 2'd3: PDM
[3]	DOP_DEC_VALID	DoP decoder valid flag.
[2]	TDM_DEC_VALID	TDM decoder valid flag.
[1]	TDM_ENC_VALID	TDM encoder valid flag.
[0]	PLL_LOCKED	PLL locked flag.

Register 225: CHIP ID

Bits	[7:0]
Default	8'hAD

Bits	Mnemonic	Description
[7:0]	CHIP_ID	• ES9291: 0xAD

Register 231-226: RESERVED

Register 232: AUTO FS READ

Bits	[7]	[6]	[5:0]
Default	-	-	-

Bits	Mnemonic	Description
[7]	EN_64FS_MODE_AUTO	Result {Z} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic, running the device in 64FS mode. • 1'b0: 64FS disabled • 1'b1: 64FS enabled
[6]	MCLK_128FS_HALF_DIV_AUTO	Result {Y} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic. • 1'b0: MCLK_128FS is an integer multiple of MCLK, Y = 1. • 1'b1: MCLK_128FS is a (X+1)*0.5 multiple of MCLK, Y = 2.
[5:0]	MCLK_128FS_DIV_AUTO	Result {X} of the automatic sample rate detect (reg0[3] AUTO_FS_DETECT) logic. $\text{FS [Hz]} = \frac{Y \cdot MCLK}{(X+1) \cdot \left(\frac{128^Z}{2}\right)}$

Register 233: CLOCK VALIDITY

Bits	[7]	[6]	[5]	[4:0]
Default	-	-	-	-

Bits	Mnemonic	Description
[7]	RATIO_VALID	Validity of the MCLK/MCLK_128FS ratio. • 1'b0: Invalid ratio • 1'b1: Valid ratio
[6]	BCK_INVALID	Validity of the BCK signal, requires BCK_MONITOR to be enabled.
[5]	WS_INVALID	Validity of the WS signal, requires WS_MONITOR to be enabled.
[4:0]	AUTO_CH_NUM	Automatic TDM channel number tuning result.

Register 234: JACK DETECT READBACK

Bits	[7:3]	[2]	[1:0]
Default	-	-	-

Bits	Mnemonic	Description
[7:3]	RESERVED	N/A
[2]	JDET_READ	Jack detection output. • 1'b0: No detection • 1'b1: Tip detected
[1:0]	RESERVED	N/A

Register 235: TEMP SENSE READ

Bits	[7:0]
Default	-

Bits	Mnemonic	Description
[7:0]	TSENSE_DATA	Temperature sensor readback. Temperature [°C] = (TS_DATA · 3.2151) − 247.27

Register 236: GPIO READBACK

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	RESERVED	N/A
[6]	GPIO7_R	GPIO7 input readback.
[5]	GPIO6_R	GPIO6 input readback.
[4]	GPIO5_R	GPIO5 input readback.
[3]	GPIO4_R	GPIO4 input readback.
[2]	GPIO3_R	GPIO3 input readback.
[1]	GPIO2_R	GPIO2 input readback.
[0]	GPIO1_R	GPIO1 input readback.

Register 237: ADC CLIP DETECT FLAGS

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	ADC_OVERLOAD_FLAG_LAT_CH2	Latched CH2 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded Note: Requires Reg 33[5] to clear flag.
[6]	ADC_OVERLOAD_FLAG_LAT_CH1	Latched CH1 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded Note: Requires Reg 33[4] to clear flag.
[5]	ADC_OVERLOAD_FLAG_CH2	Unlatched CH2 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded
[4]	ADC_OVERLOAD_FLAG_CH1	Unlatched CH1 ADC modulator overload flag. • 1'b0: No overload • 1'b1: ADC modulator overloaded
[3]	PEAK_FLAG_LAT_CH2	Latched CH1 ADC peak detector flag. • 1'b0: CH2 input signal ≤ PEAK_THRESH_CH2 • 1'b1: CH2 input signal > PEAK_THRESH_CH2 Note: Requires reg26-27[13] STATUS_CLEAR_CH2_PEAK_LATCH to clear flag.
[2]	PEAK_FLAG_LAT_CH1	Latched CH2 ADC peak detector flag. • 1'b0: CH1 input signal ≤ PEAK_THRESH_CH1 • 1'b1: CH1 input signal > PEAK_THRESH_CH1 Note: Requires reg26-27[12] STATUS_CLEAR_CH1_PEAK_LATCH to clear flag.
[1]	PEAK_FLAG_CH2	Unlatched CH2 ADC peak detector flag. • 1'b0: CH2 input signal ≤ PEAK_THRESH_CH2 • 1'b1: CH2 input signal > PEAK_THRESH_CH2
[0]	PEAK_FLAG_CH1	Unlatched CH1 ADC peak detector flag. • 1'b0: CH1 input signal ≤ PEAK_THRESH_CH1 • 1'b1: CH1 input signal > PEAK_THRESH_CH1

Register 239-238: PEAK CH1 READ

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	PEAK_LEVEL_CH1	ADC CH1 peak detector value readback. $\text{Peak [dB]} = 20 \cdot \log10\left(\frac{\text{PEAK\_LEVEL\_CH1}}{2^{16}-1}\right) + 0.56$

Register 241-240: PEAK CH2 READ

Bits	[15:0]
Default	-

Bits	Mnemonic	Description
[15:0]	PEAK_LEVEL_CH2	ADC CH2 peak detector value readback. $\text{Peak [dB]} = 20 \cdot \log10\left(\frac{\text{PEAK\_LEVEL\_CH2}}{2^{16}-1}\right) + 0.56$

Register 242: DAC STATUS FLAGS

Bits	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Default	-	-	-	-	-	-	-	-

Bits	Mnemonic	Description
[7]	SS_RAMP_DOWN_CH2	Unlatched CH2 DAC soft ramped down flag.
[6]	SS_RAMP_DOWN_CH1	Unlatched CH1 DAC soft ramped down flag.
[5]	SS_RAMP_UP_CH2	Unlatched CH2 DAC soft ramped up flag.
[4]	SS_RAMP_UP_CH1	Unlatched CH1 DAC soft ramped up flag.
[3]	AUTOMUTE_CH2	Unlatched CH2 DAC automute status flag.
[2]	AUTOMUTE_CH1	Unlatched CH1 DAC automute status flag.
[1]	VOL_MIN_CH2	Unlatched CH2 DAC minimum volume flag.
[0]	VOL_MIN_CH1	Unlatched CH1 DAC minimum volume flag.

Register 243: RESERVED

Register 245-244: SPI MASTER BUSY

Bits	[15]	[14:0]
Default	-	-

Bits	Mnemonic	Description
[15]	SPI_M_ASP_PROG_BUSY	State of the SPI master bus, during the automated ASP programming. • 1'b0: SPI master bus idle • 1'b1: SPI master bus busy
[14:0]	RESERVED	N/A

Register 251-246: RESERVED

Register 252: SPI MASTER DATA IN

Bits	[7:0]
Default	-

Bits	Mnemonic	Description
[7:0]	SPI_M_DATA_I	Byte of data read from the SPI slave device.

ES9291 Reference Schematic

Hardware (HW) Mode

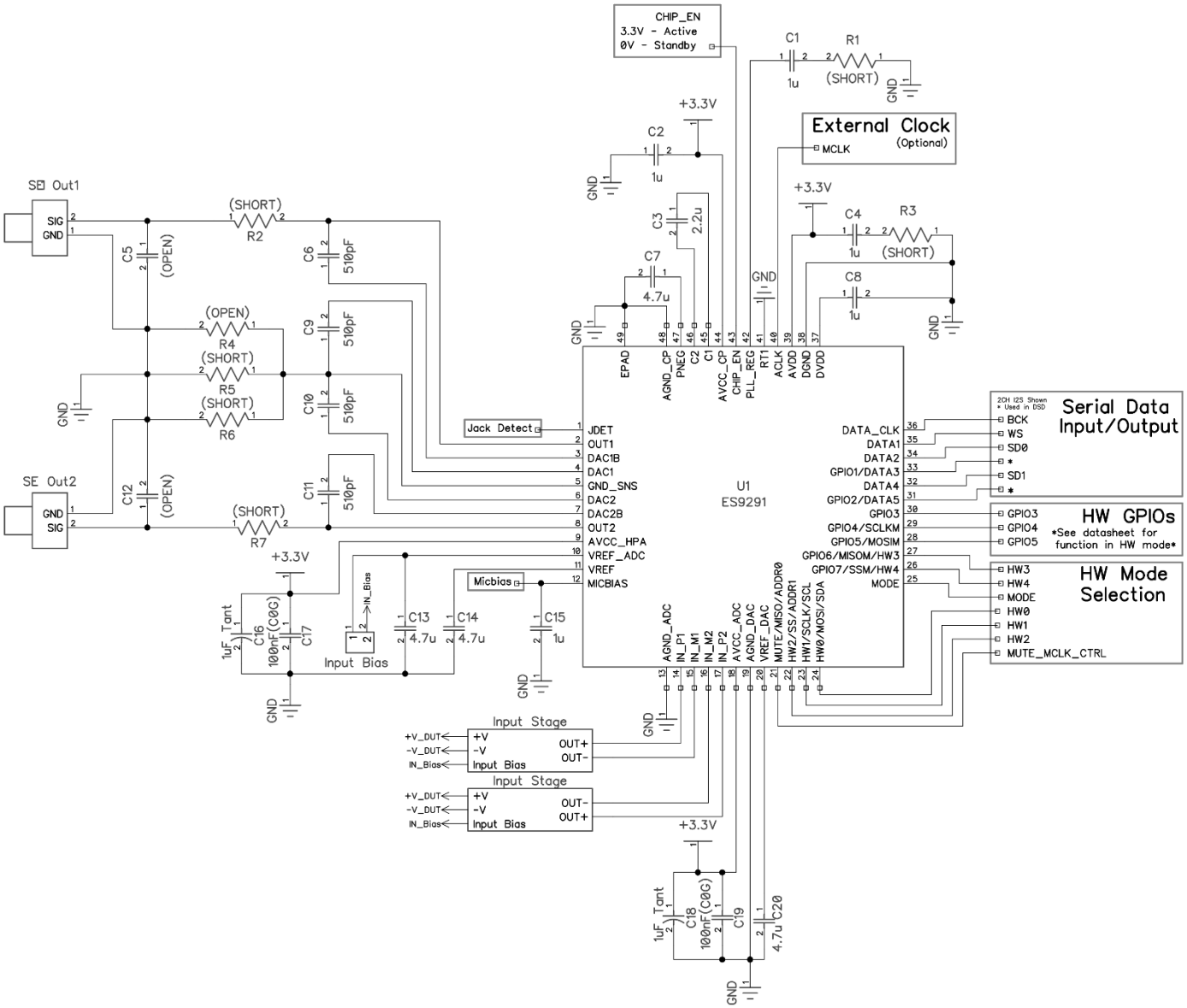


Figure 37 - ES9291 Hardware Mode Reference Schematic

Note: The ES9291 48QFN package has an exposed pad (Pin 49) that must be connected to ground.

Software (SW) Mode

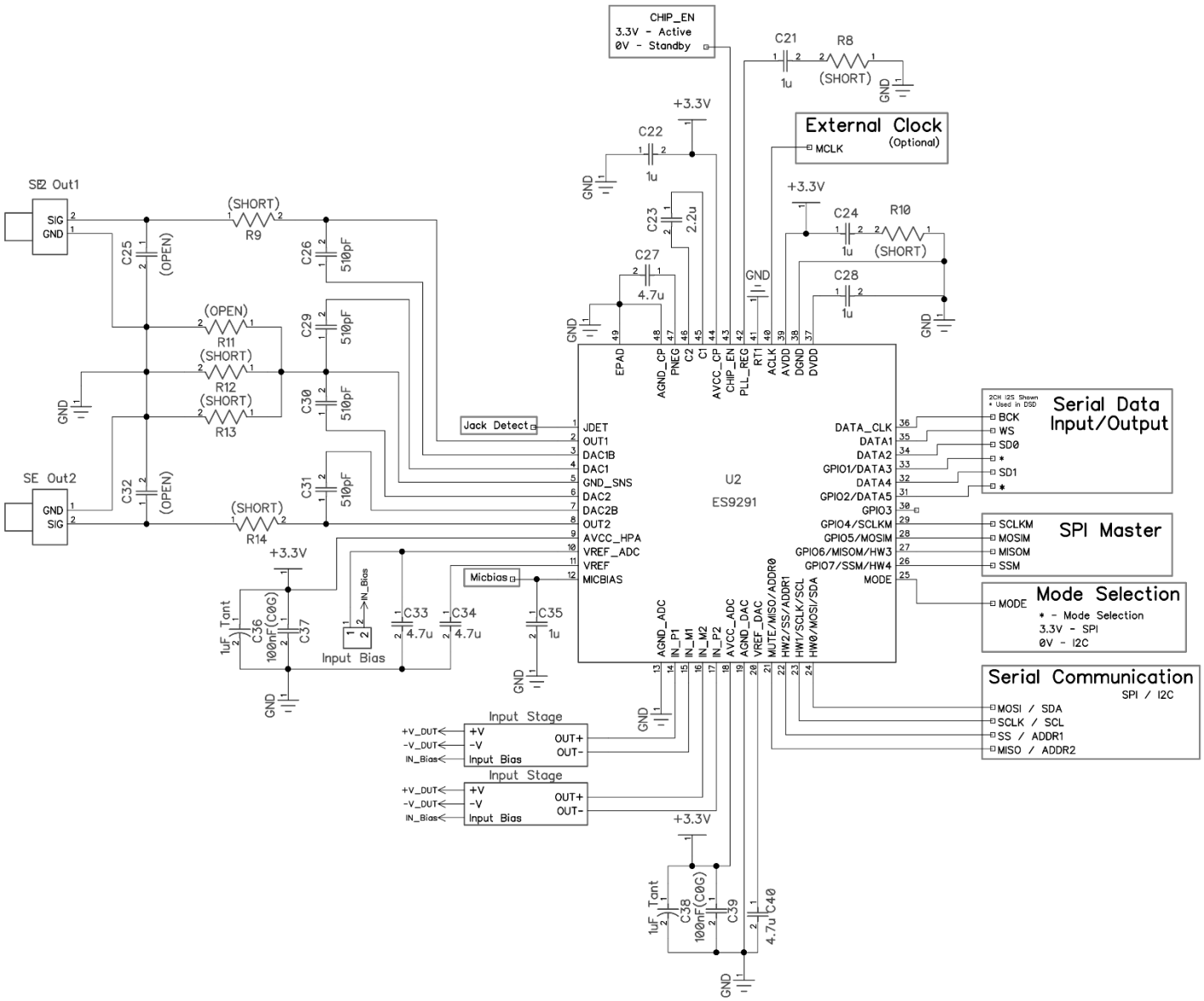


Figure 38 - ES9291 Software Mode Reference Schematic

Note: The ES9291 48QFN package has an exposed pad (Pin 49) that must be connected to ground.

Differential Input Stage

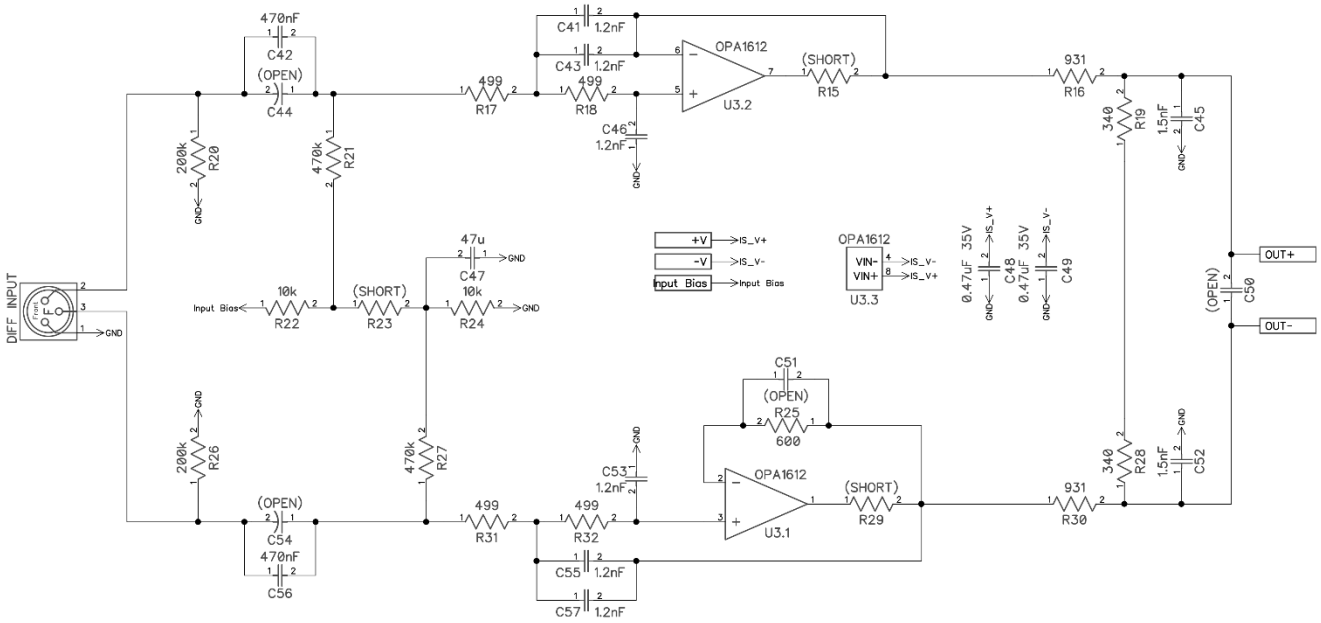


Figure 39 - Differential Input Stage Reference Schematic

Note: INPUT BIAS is sourced from VREF_ADC (Pin 10).

Single-Ended Input Stage

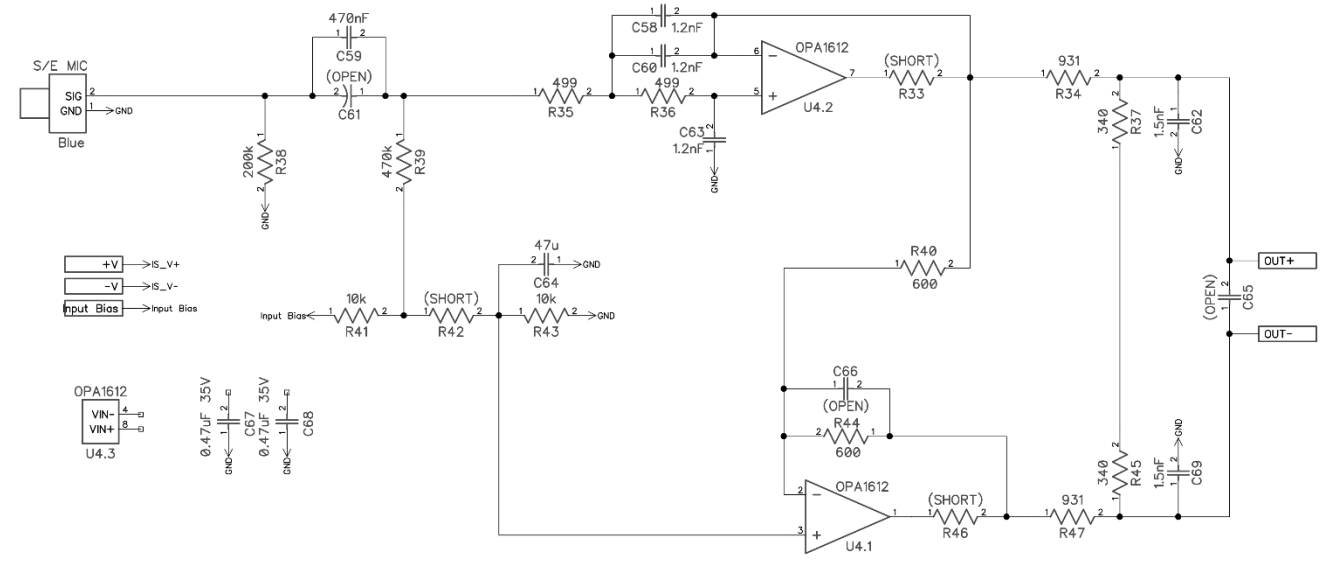


Figure 40 - Single-Ended Input Stage Reference Schematic

Note: INPUT BIAS is sourced from VREF_ADC (Pin 10).

Power Supply

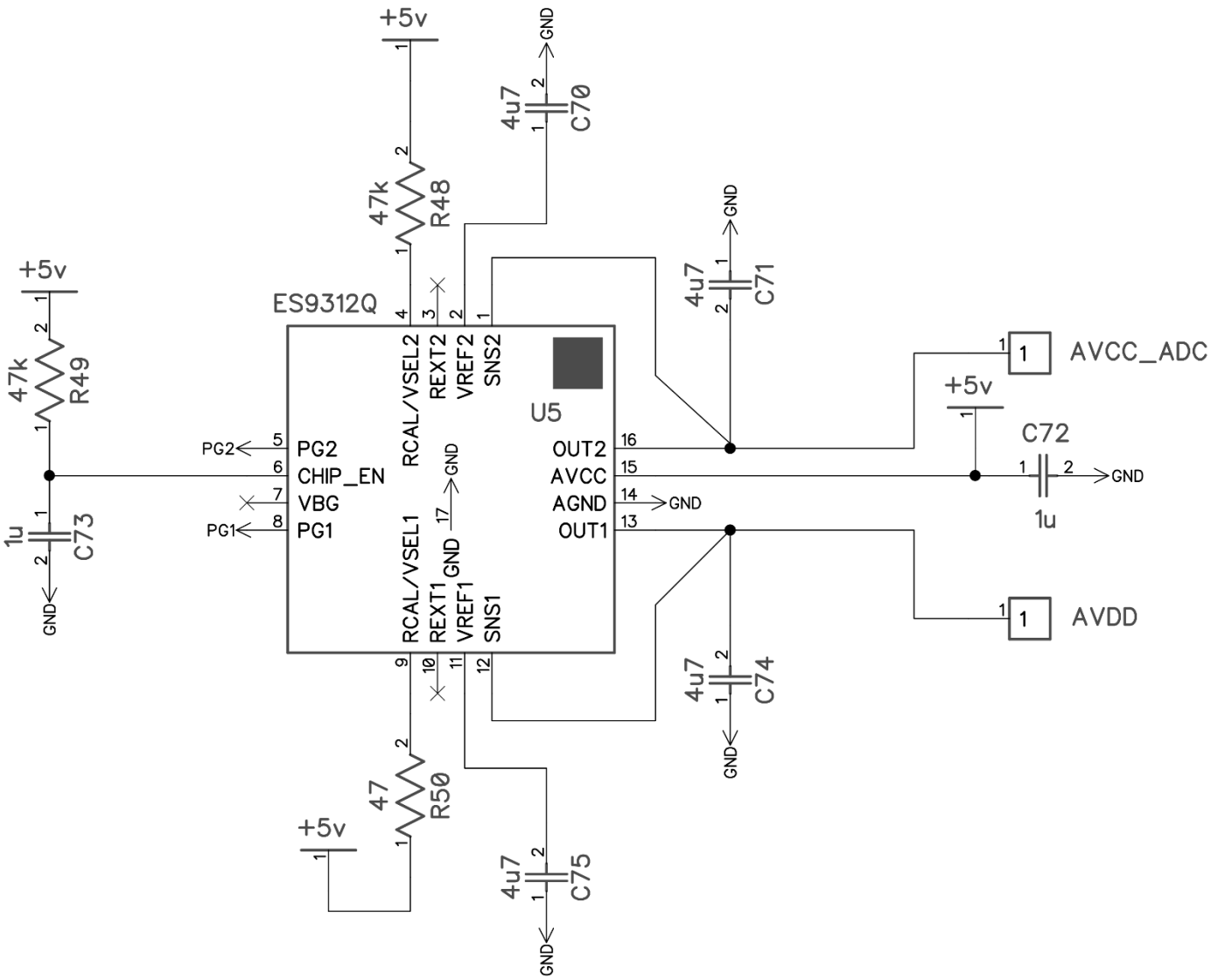


Figure 41 - Recommended Power Supply

ES9291 PCB Layout Guidelines

To maximize performance of the ES9291 ESS Technology makes the following PCB Layout recommendations:

- Use of a 4+ layer PCB with an uninterrupted ground plane immediately beneath the chip. Both analog and digital ground signal can be connected here.
- All bypass capacitors to be placed as close to the chip as possible while keeping clear ground paths between them and the chip's ground pins.
- The use of multiple vias for each supply near its bypass capacitor and chip ground pin.
- Minimize the use of vias for high-speed data and clock lines and avoid routing them near or directly underneath the analog output signals.
- The ground connections for AGND_CP and the bypass capacitors for pins PNEG and AVCC_CP should be separated from all other nearby ground connections with a small cutout on every PCB ground layer.
- Ensure the package pad is connected to ground plane on the back side of the PCB with multiple vias for heat dissipation.

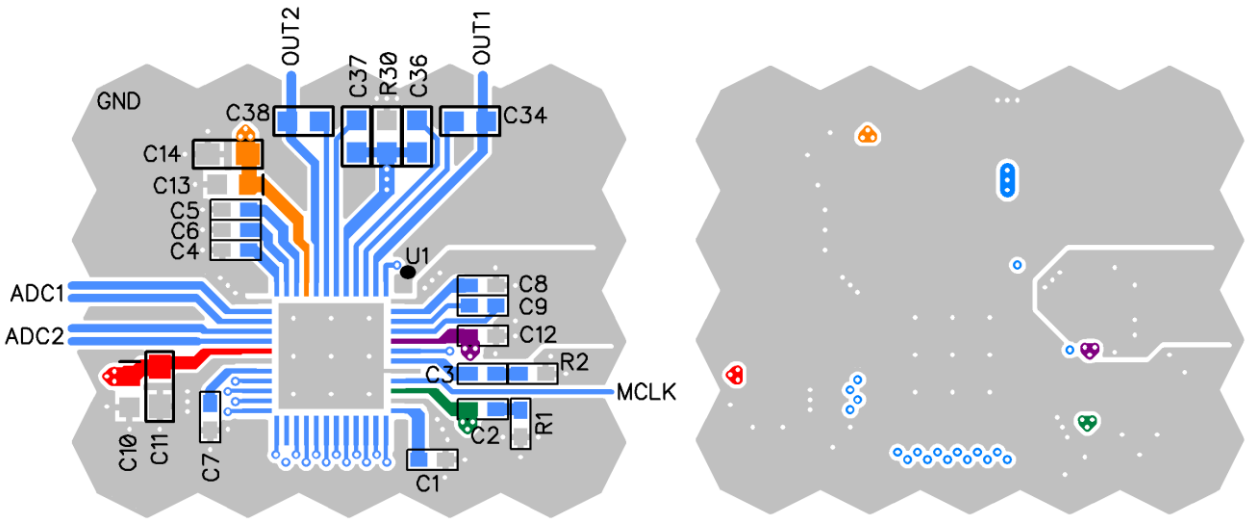
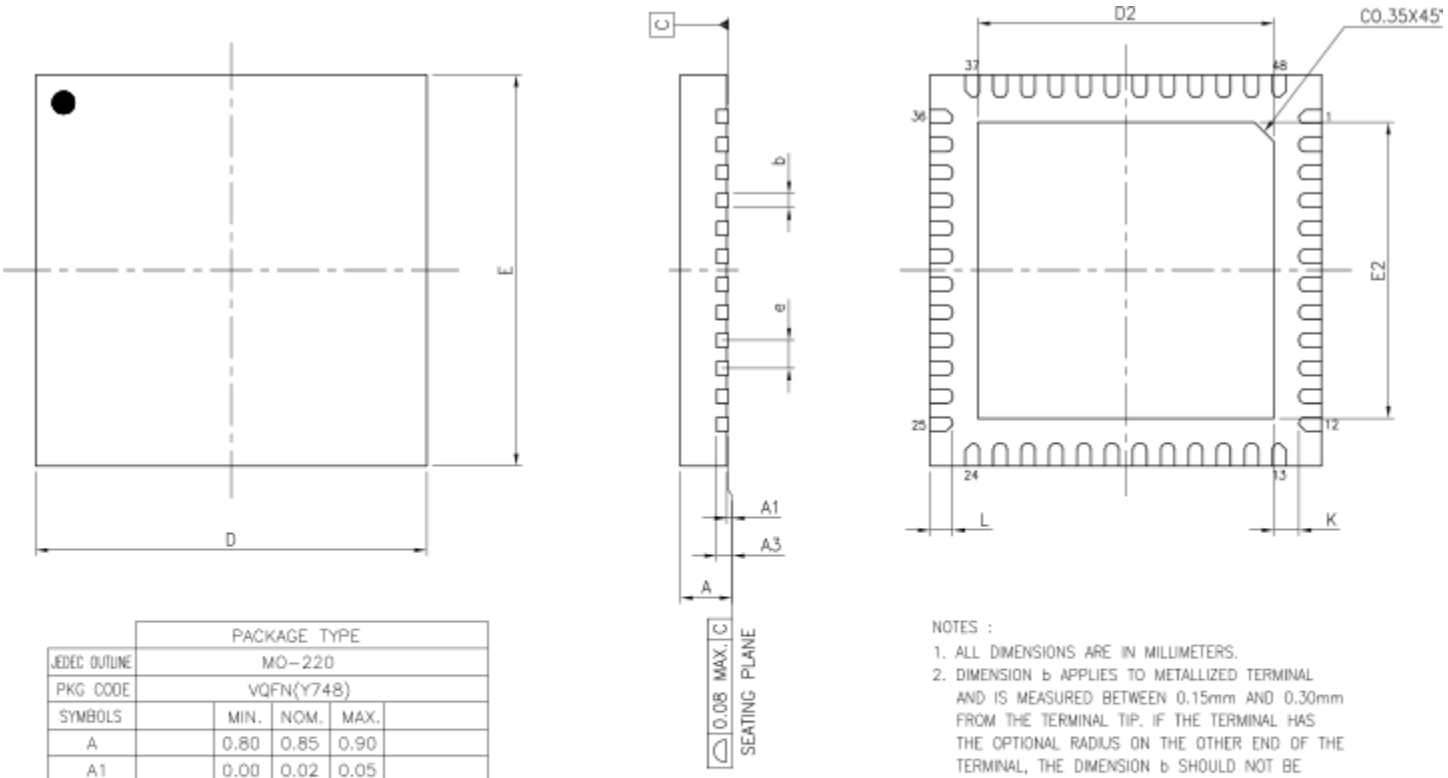


Figure 42 - ES9291 Recommended PCB Layout Guidelines

48 QFN Package Dimensions



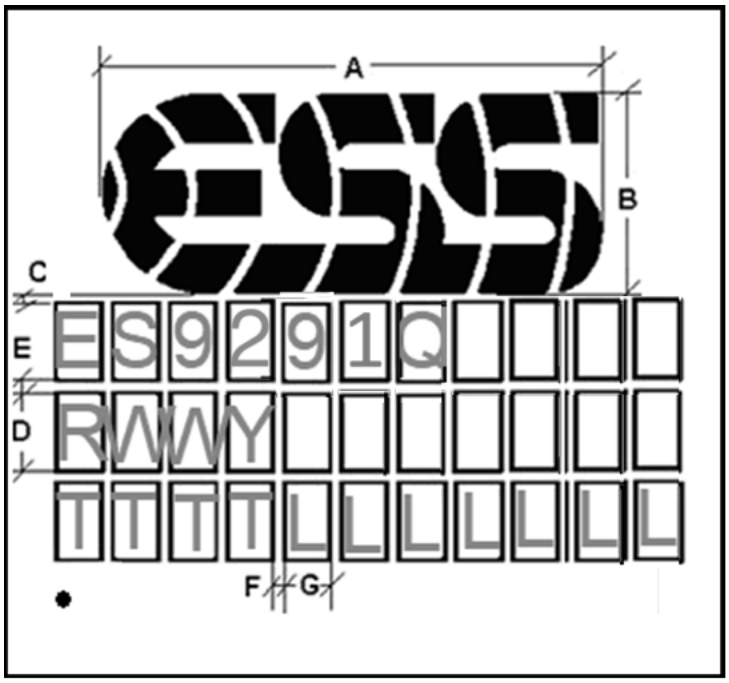
	PACKAGE TYPE			
JEDEC OUTLINE	MO-220			
PKG CODE	VQFN(Y748)			
SYMBOLS	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A3	0.203 REF.			
b	0.20	0.25	0.30	
D	7.00 BSC			
E	7.00 BSC			
e	0.50 BSC			
L	0.35	0.40	0.45	
K	0.20	–	–	

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
224X224 MIL	5.25	5.30	5.35	5.25	5.30	5.35	V	X	N/A

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 43 – ES9291 48 QFN Package Dimensions

48 QFN Top View Marking



	Dimension in mm						
Package Type	A	B	C	D	E	F	G
QFN 7mm x 7mm	5.0	2.0	0.3	0.56	0.2	0.08	0.33

T	**Tracking number**
W	Work week
Y	Last digit of year
L	Lot number
R	Silicon Revision

Marking is subject to change. This drawing is not to scale.

Figure 44 - ES9291 48 QFN Top View Markings

Reflow Process Considerations

Temperature Controlled

For lead-free soldering, the characterization and optimization of the reflow process is the most important factor to consider.

The lead-free alloy solder has a melting point of 217°C. This alloy requires a minimum reflow temperature of 235°C to ensure good wetting. The maximum reflow temperature is in the 245°C to 260°C range, depending on the package size (RPC-2-Pb-Free Process - Classification Temperatures (Tc)). This narrows the process window for lead-free soldering to 10°C to 20°C.

The increase in peak reflow temperature in combination with the narrow process window makes the development of an optimal reflow profile a critical factor for ensuring a successful lead-free assembly process. The major factors contributing to the development of an optimal thermal profile are the size and weight of the assembly, the density of the components, the mix of large and small components, and the paste chemistry being used.

Reflow profiling needs to be performed by attaching calibrated thermocouples well adhered to the device as well as other critical locations on the board to ensure that all components are heated to temperatures above the minimum reflow temperatures and that smaller components do not exceed the maximum temperature limits (Table RPC-2).

To ensure that all packages can be successfully and reliably assembled, the reflow profiles studied and recommended by ESS are based on the JEDEC/IPC standard J-STD-020 revision D.1.

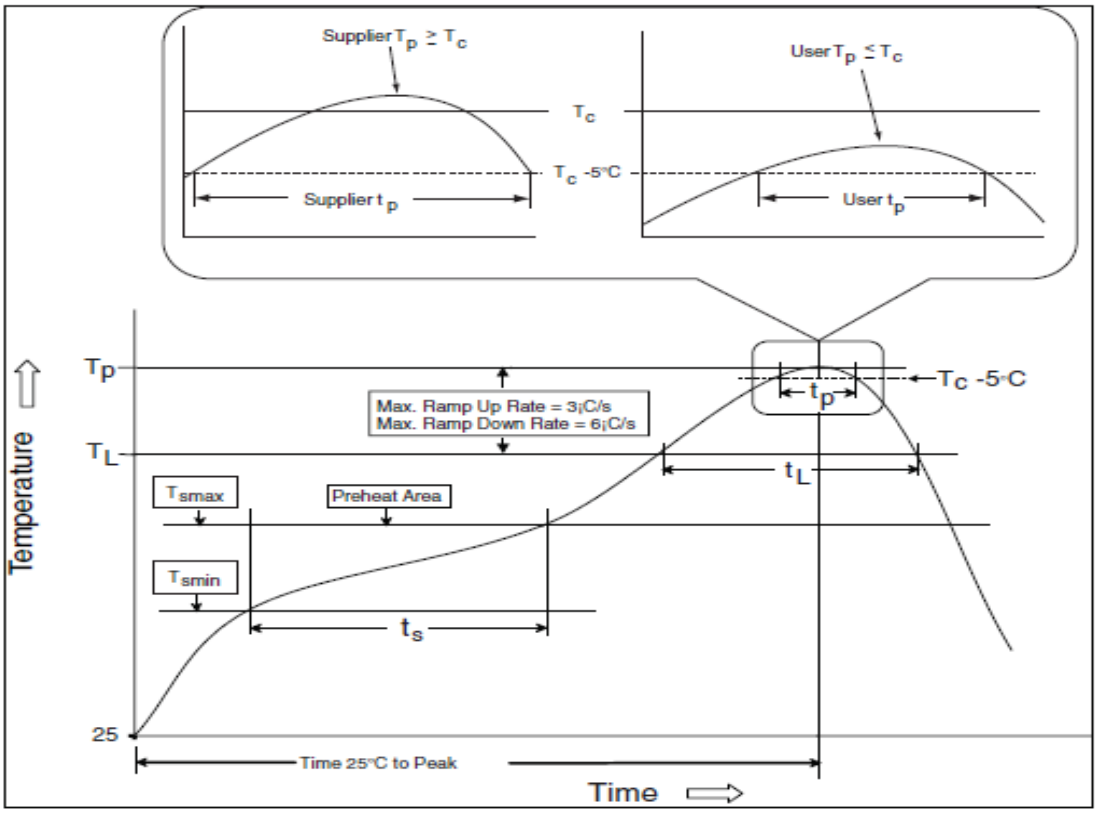


Figure 45 - IR/Convection Reflow Profile (IPC/JEDEC J-STD-020D.1)

Reflow is allowed 3 times. Caution must be taken to ensure time between re-flow runs does not exceed the allowed time by the moisture sensitivity label. If the time elapsed between the re-flows exceeds the moisture sensitivity time, bake the board according to the moisture sensitivity label instructions.

Manual

Allowed up to 2 times with maximum temperature of 350ºC no longer than 3 seconds.

RPC-1 Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (Tsmin) Temperature Max (Tsmax) Time (ts) from (Tsmin to Tsmax)	 150°C 200°C 60-120 seconds
Ramp-up rate (TL to Tp)	3°C / second maximum
Liquidous temperature (TL) Time (tL) maintained above TL	217°C 60-150 seconds
Peak package body temperature (Tp)	For users Tp must not exceed the classification temp in Table RPC-2. For suppliers Tp must equal or exceed the Classification temp in Table RPC-2.
Time (tp)* within 5°C of the specified classification temperature (Tc)	30* seconds
Ramp-down rate (Tp to TL)	6°C / second maximum
Time 25°C to peak temperature	8 minutes maximum
* Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.	

Table 46 - RPC-1 Classification Reflow Profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), Tp shall be within ±2°C of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, refer to JEP140 for recommended thermocouple use.

Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table RPC-1.

For example, if Tc is 260°C and time tp is 30 seconds, this means the following for the supplier and the user.
For a supplier: The peak temperature must be at least 260°C. The time above 255°C must be at least 30 seconds.
For a user: The peak temperature must not exceed 260°C. The time above 255°C must not exceed 30 seconds.

All components in the test load shall meet the classification profile requirements.

RPC-2 Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume mm3, <350	Volume mm3, 350 to 2000	Volume mm3, >2000
<1.6 mm	260°C	260°C	260°C
1.6 mm – 2.5 mm	260°C	250°C	245°C
>2.5 mm	250°C	245°C	245°C

Table 47 - RPC-2 Pb Free Classification Temperatures

At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (Tp) can exceed the values specified in Table RPC-2. The use of a higher Tp does not change the classification temperature (Tc).

Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Ordering Information

Part Number	Description	Package
ES9291Q	Stereo High-Performance SMART CODEC with PowerLine Driver	7x7mm 48 QFN

Table 48 - Ordering Information

Revision History

Current Version 0.2

Rev.	Date	Notes
0.2	December, 2025	Initial Production Release