

TVS Diode

Transient Voltage Suppressor Diodes

ESD200-B1-CSP0201

Low Clamping Voltage TVS Diode in a Thin 0201 Chip Scale Package

ESD200-B1-CSP0201

Data Sheet

Revision 1.0, 2013-05-21
Final

Edition 2013-05-21

**Published by
Infineon Technologies AG
81726 Munich, Germany**

**© 2013 Infineon Technologies AG
All Rights Reserved.**

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History: Revision 0.9.3, 2012-03.13

Page or Item	Subjects (major changes since previous revision)
Revision 1.0, 2013-05-21	
All	Status change to final

Trademarks of Infineon Technologies AG

AURIX™, BlueMoon™, C166™, CanPAK™, CIPOS™, CIPURSE™, COMNEON™, EconoPACK™, CoolMOS™, CoolSET™, CORECONTROL™, CROSSAVE™, DAVE™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, I²RF™, ISOFACE™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OptiMOS™, ORIGA™, PRIMARION™, PrimePACK™, PrimeSTACK™, PRO-SIL™, PROFET™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SIPMOS™, SMARTi™, SmartLEWIS™, SOLID FLASH™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™, X-GOLD™, X-PMU™, XMM™, XPOSYS™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, μVision™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-ig™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. Mifare™ of NXP. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2010-10-26

1 Low Clamping Voltage TVS Diode in a Thin 0201 Chip Scale Package

1.1 Features

- ESD / Transient protection of susceptible I/O lines to:
 - IEC61000-4-2 (ESD): ± 16 kV (air/contact discharge)
 - IEC61000-4-5 (surge): ± 3 A (8/20 μ s))
- Low clamping voltage
- Low dynamic resistance: $R_{DYN} \leq 0.2 \Omega$ typ.
- Supports applications with signal voltage between -5.5 V and 5.5 V max.
- Line capacitance: $C_L = 6.5$ pF
- Minimized overshoot due to extremely low parasitic inductance of chip scale package
- Miniature form factor (XY) = 0201 (0.58 mm x 0.28 mm)
- Thin 0.15 mm package thickness to allow direct integration into modules
- Optimized assembly: its bidirectional and symmetric I/V characteristics allow placement on the PCB with no danger of polarity orientation issues



1.2 Application Examples

- ESD Protection of highly susceptible IC/ASICs in audio, headset, human digital interfaces
- Dedicated solution to boost space saving and high performance in miniaturized modern electronics

1.3 Product Description

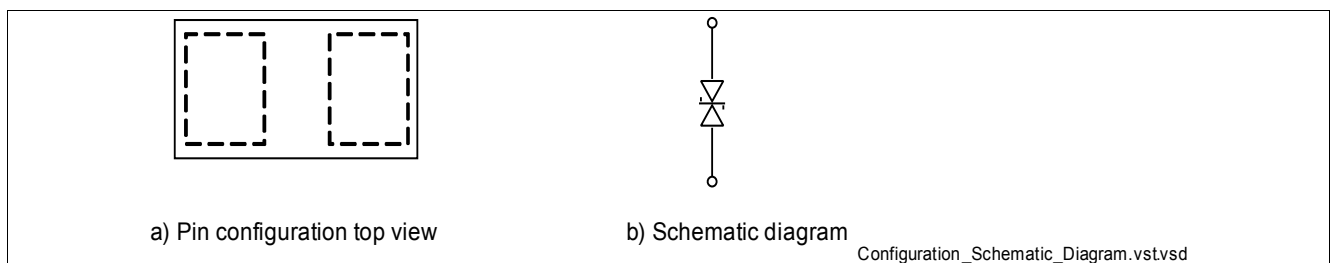


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Ordering Information

Type	Package	Configuration	Marking code
ESD200-B1-CSP0201	WLL-2-1	1 line, bi-directional	A ¹⁾

1) The device does not have any marking or date code on the device backside. The Marking code is on pad side.

2 Characteristics

2.1 Maximum Ratings

Table 2-1 Maximum Ratings at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD ¹⁾	V_{ESD}				kV
Contact discharge		-16	-	16	
Air discharge		-16	-	16	
Peak pulse current ($t_p = 8/20\text{ }\mu\text{s}$) ²⁾	I_{PP}	-3	-	3	A
Operating temperature range	T_{OP}	-40	-	125	$^\circ\text{C}$
Storage temperature	T_{stg}	-65	-	150	$^\circ\text{C}$

1) V_{ESD} according to IEC61000-4-2 ($R = 330$, $C = 150\text{ pF}$ discharge network)

2) I_{PP} according to IEC61000-4-5 ($t_p = 8/20\text{ }\mu\text{s}$)

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.2 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

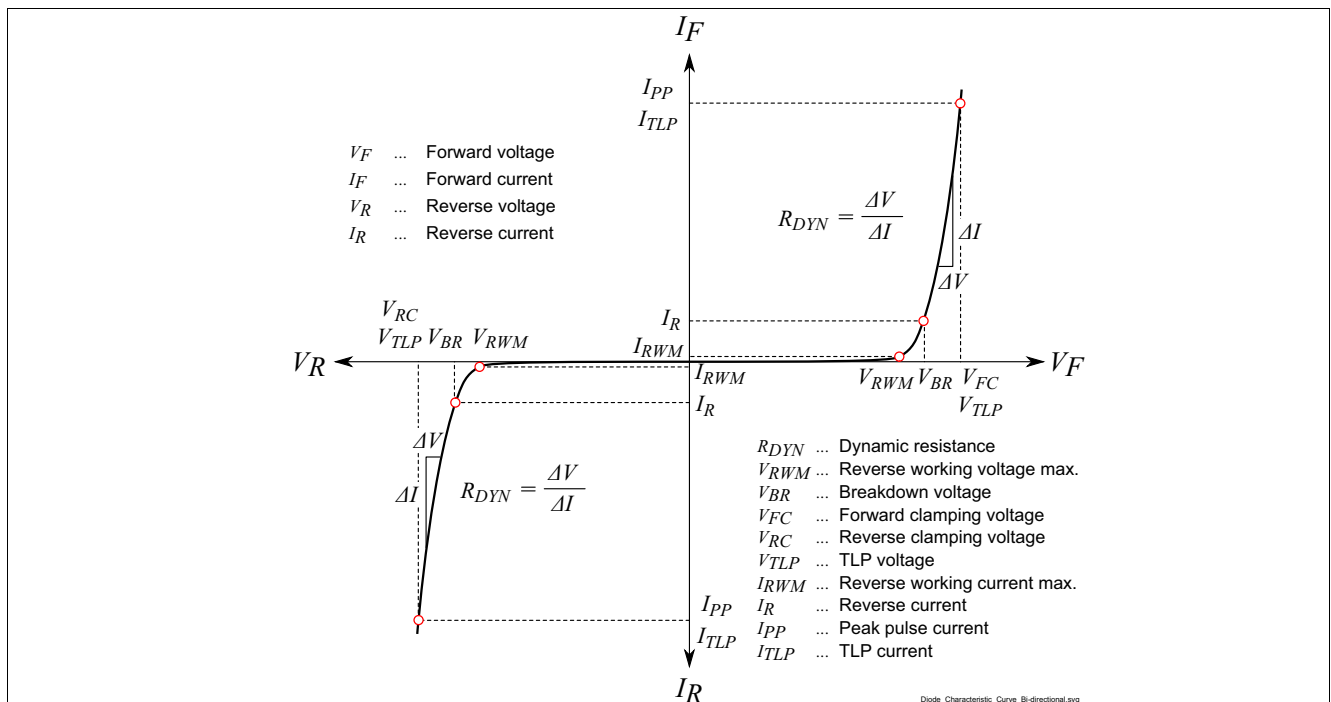


Figure 2-1 Definitions of electrical characteristics

Table 2-2 DC Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-5.5	-	5.5	V	
Breakdown voltage	V_{BR}	6	-	10	V	$I_{BR} = 1\text{ mA}$
Reverse current	I_R	-	0.1	100	nA	$V_R = 5.5\text{ V}$

Table 2-3 RF Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L		6.5		pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$

Table 2-4 ESD Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage ¹⁾	V_{CL}	-	12	-	V	$V_{ESD} = 8\text{ kV}$ contact discharge
Clamping voltage ²⁾		-	10	-		$I_{TLP} = 1\text{ A}$
		-	13	-		$I_{TLP} = 16\text{ A}$
Clamping voltage ³⁾		-	10	-	$I_{PP} = 1\text{ A}$	$I_{PP} = 3\text{ A}$
		-	12.5	-		
Dynamic resistance ²⁾	R_{DYN}	-	0.2	-	Ω	

1) V_{ESD} according to IEC61000-4-2 ($R = 330\ \Omega$, $C = 150\text{ pF}$ discharge network)

2) ANSI/ESDSTM5.5.1-Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0 = 50\ \Omega$, $t_p = 100\text{ ns}$, $t_r = 0.6\text{ ns}$, I_{TLP} and V_{TLP} average window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic resistance using squares fit to TLP characteristics between $I_{TLP1} = 2.5\text{ A}$ and $I_{TLP2} = 17\text{ A}$. Please refer to Application Note AN210[1]

3) I_{PP} according to IEC61000-4-5 ($t_p = 8/20\ \mu\text{s}$)

3 Typical Characteristics

Curves specified at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

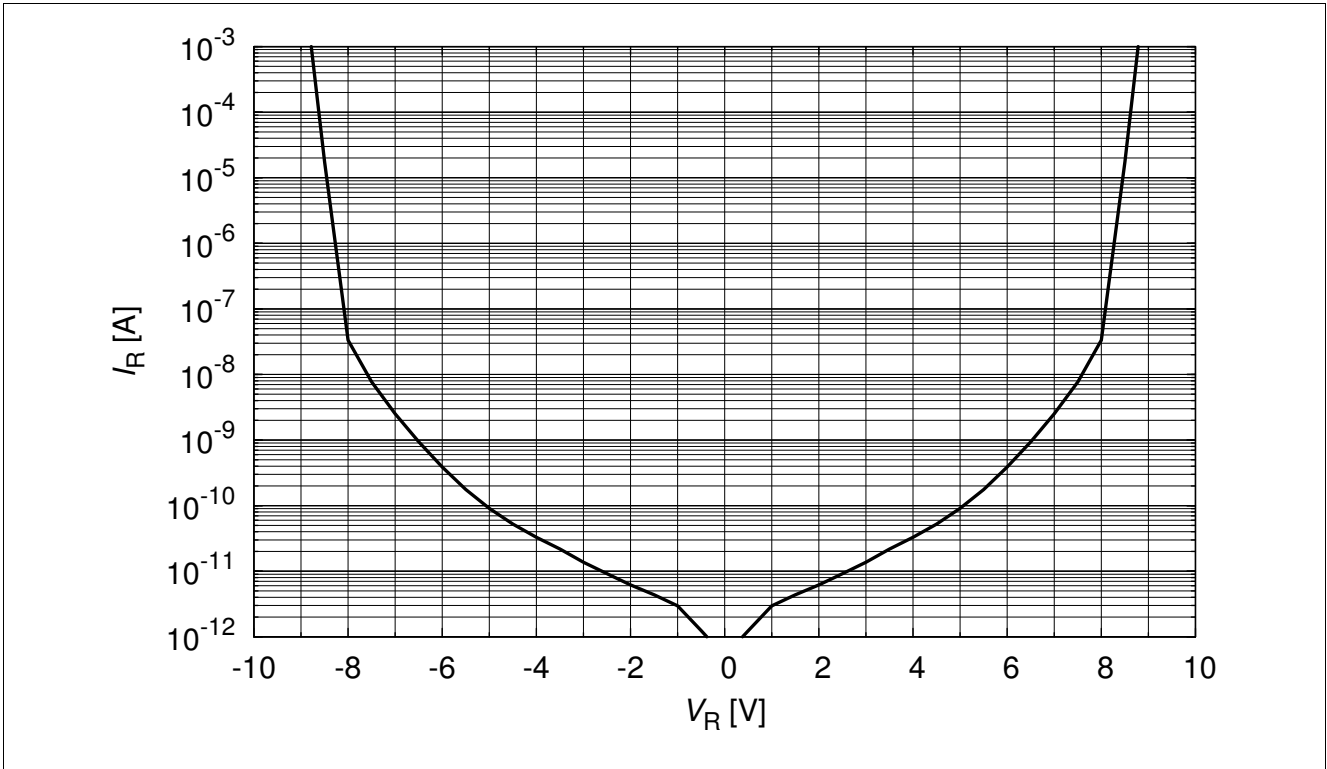


Figure 3-1 Reverse current: $I_R = f(V_R)$

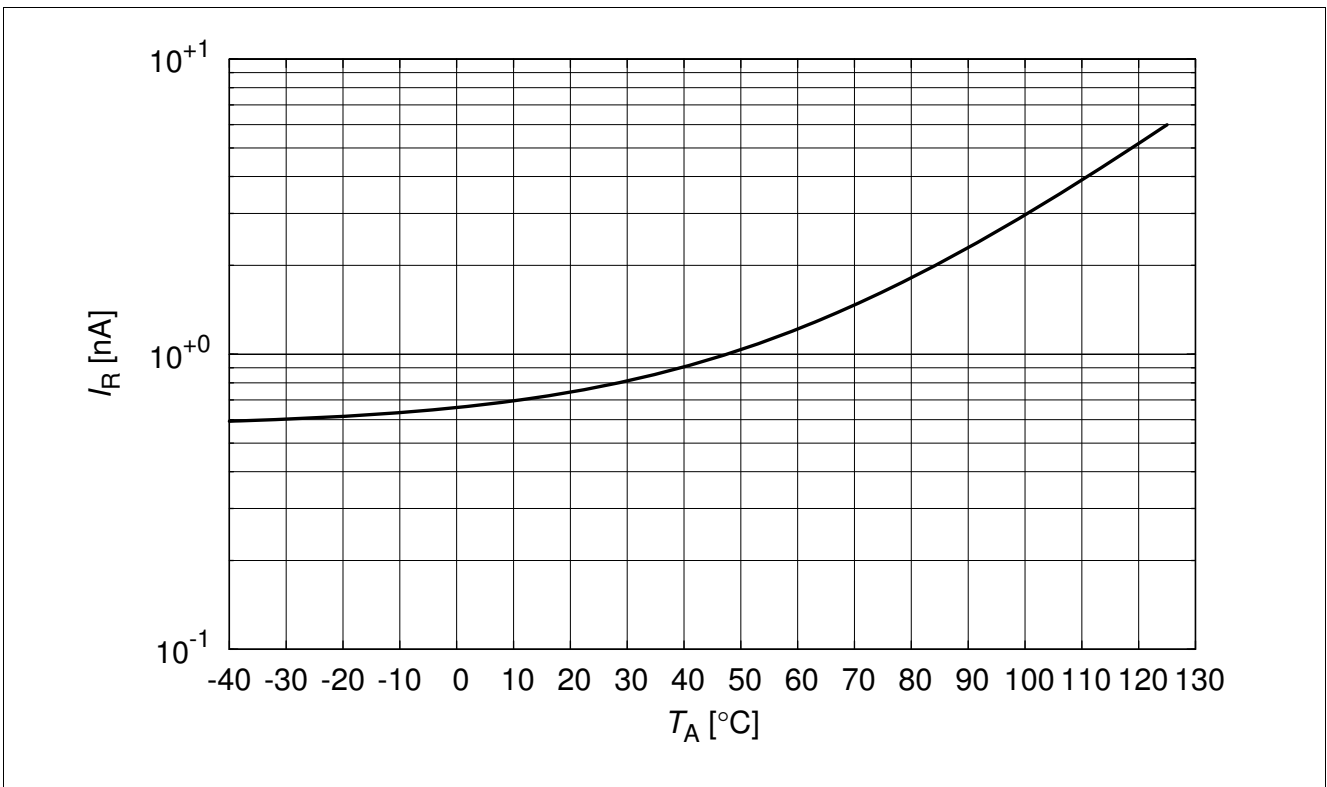


Figure 3-2 Reverse current: $I_R = f(T_A)$, $V_R = 5.5\text{ V}$

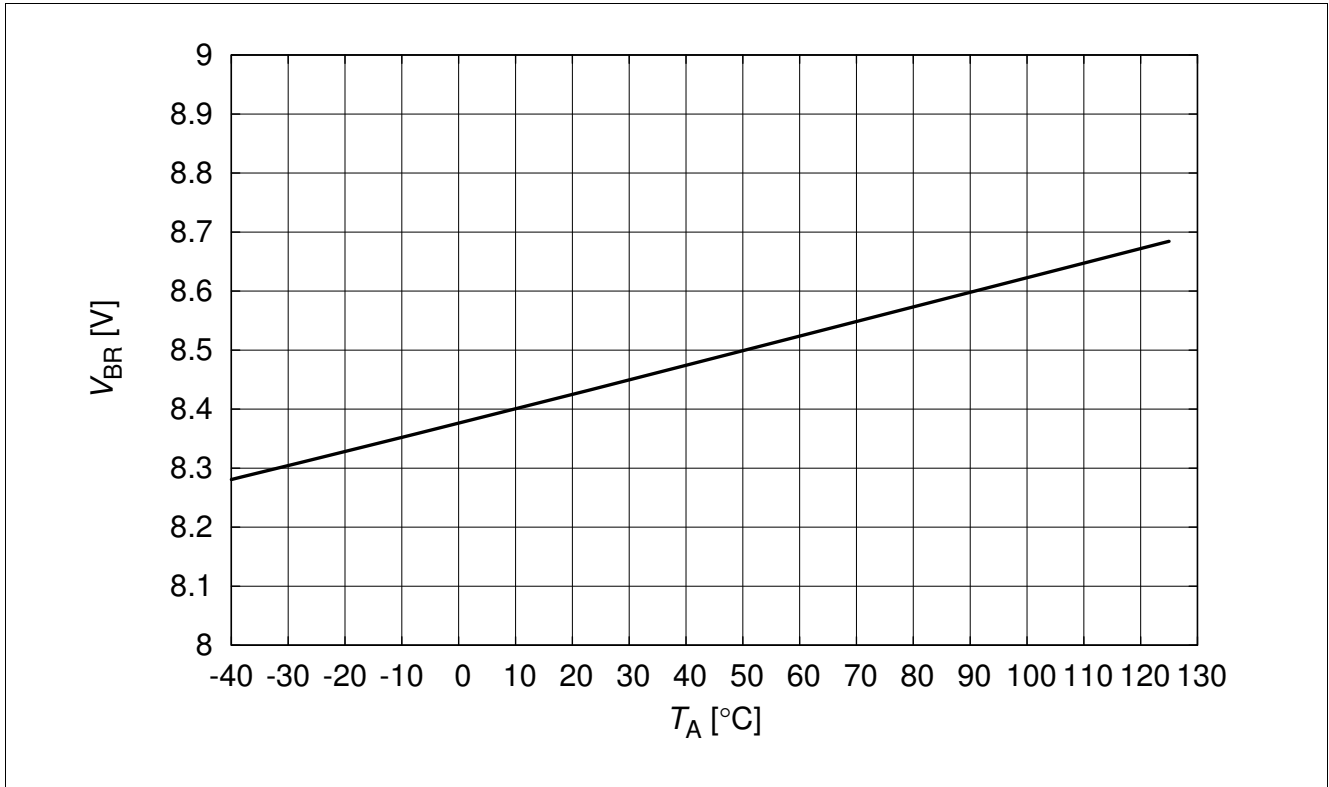


Figure 3-3 Reverse voltage: $V_{BR} = f(T_A)$, $I_R = 1 \text{ mA}$

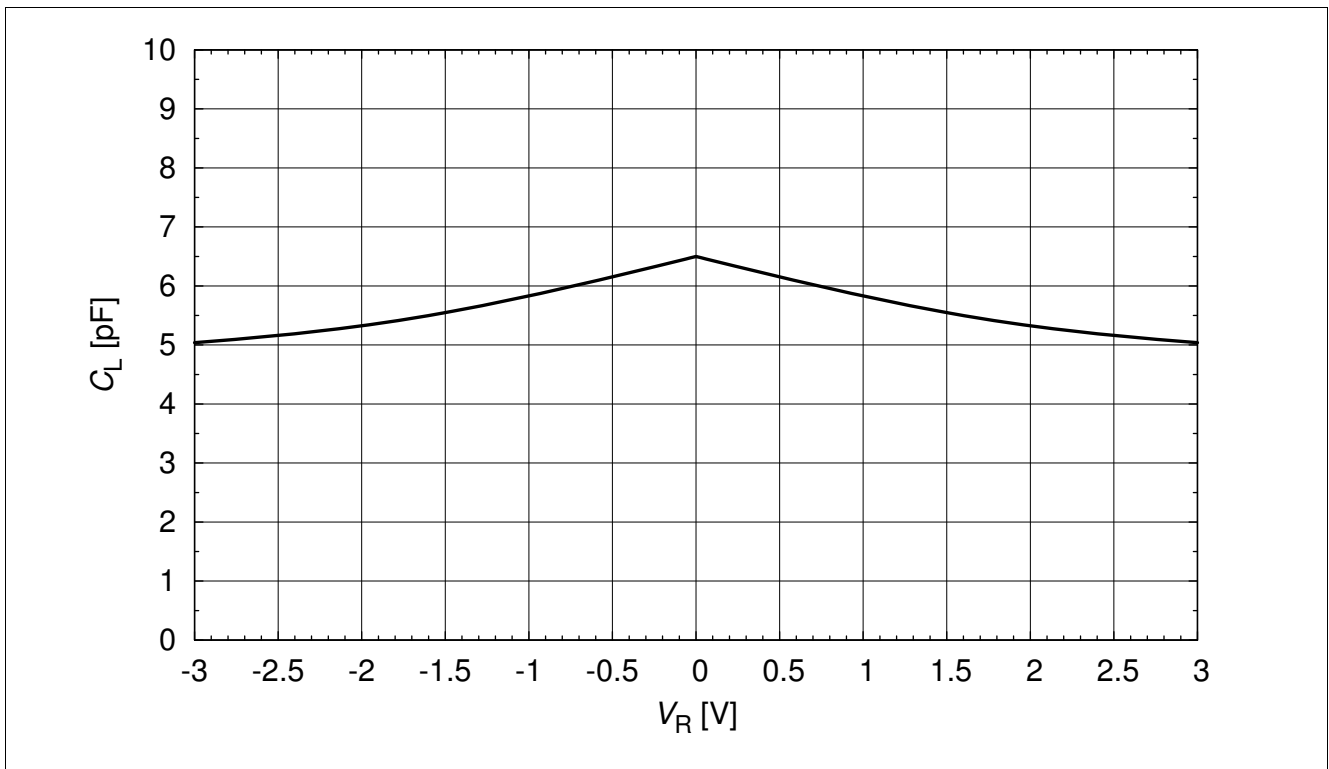


Figure 3-4 Line capacitance: $C_L = f(V_R)$, $f = 1 \text{ MHz}$

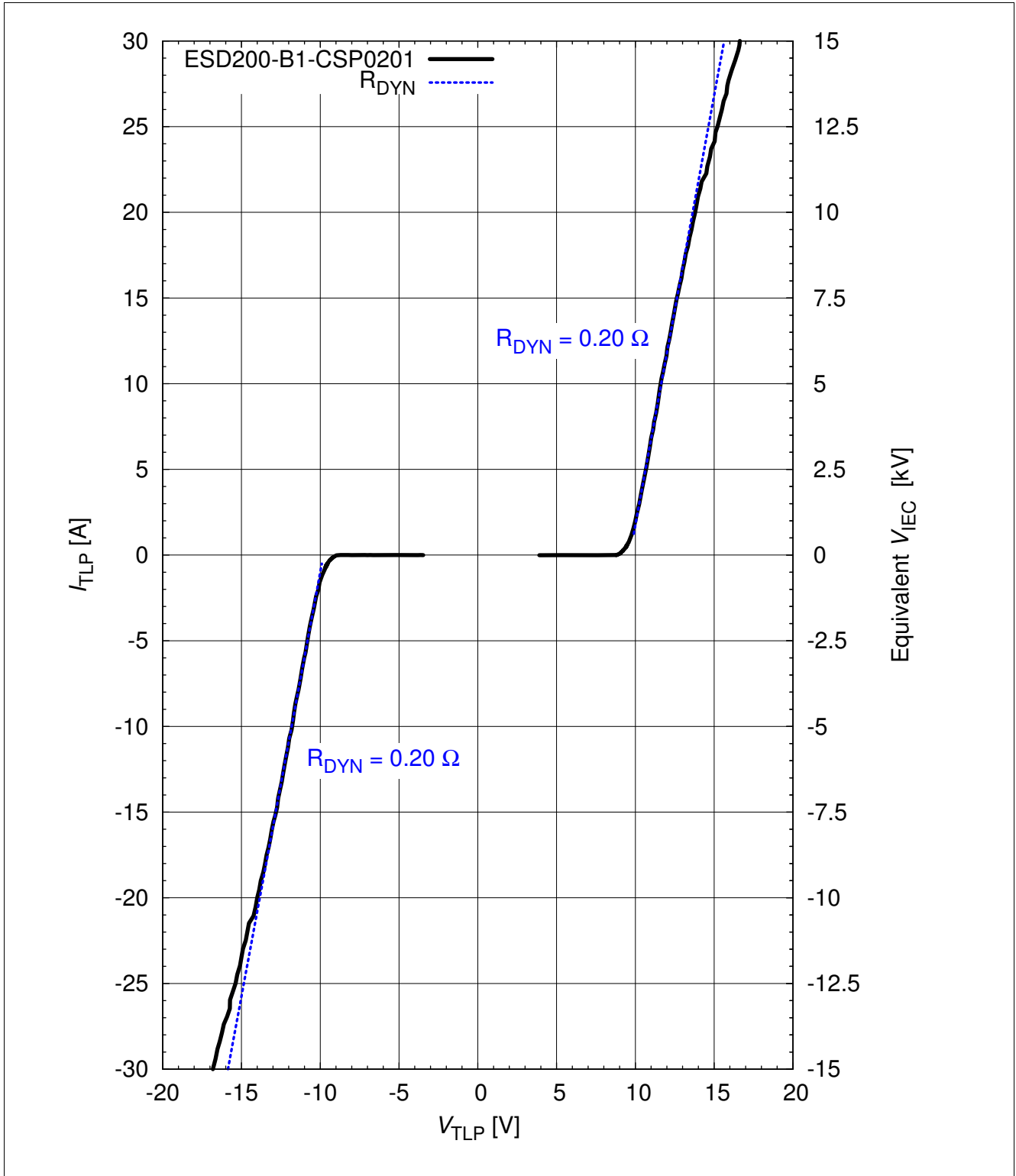


Figure 3-5 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESDSTM5.5.1-Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 0.6 \text{ ns}$, I_{TLP} and V_{TLP} average window: $t_1 = 30 \text{ ns}$ to $t_2 = 60 \text{ ns}$, extraction of dynamic resistance using squares fit to TLP characteristics between $I_{TLP1} = 2.5 \text{ A}$ and $I_{TLP2} = 17 \text{ A}$. Please refer to Application Note AN210[1]

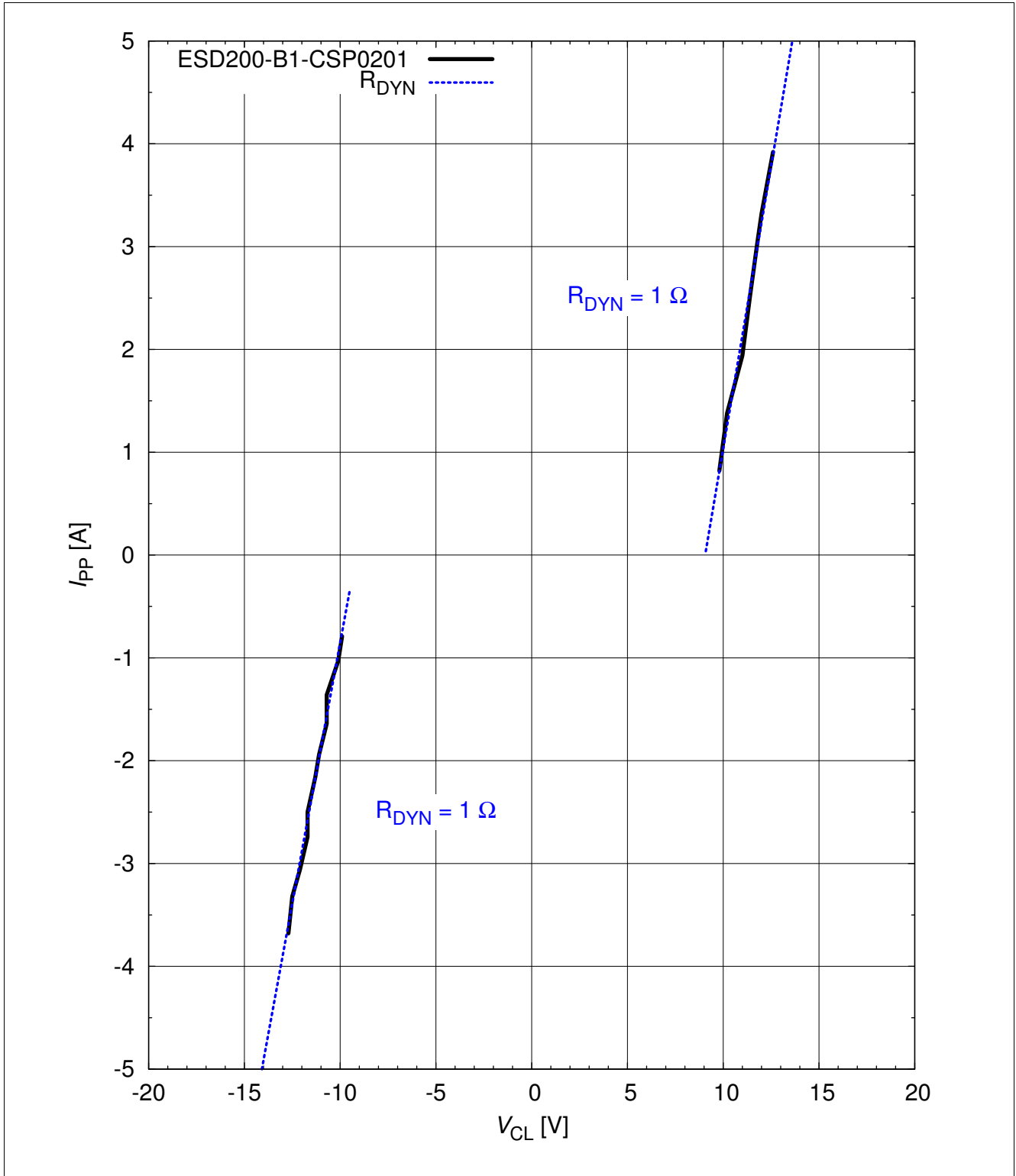


Figure 3-6 Pulse current (IEC61000-4-5) versus clamping voltage: $I_{PP} = f(V_{CL})$

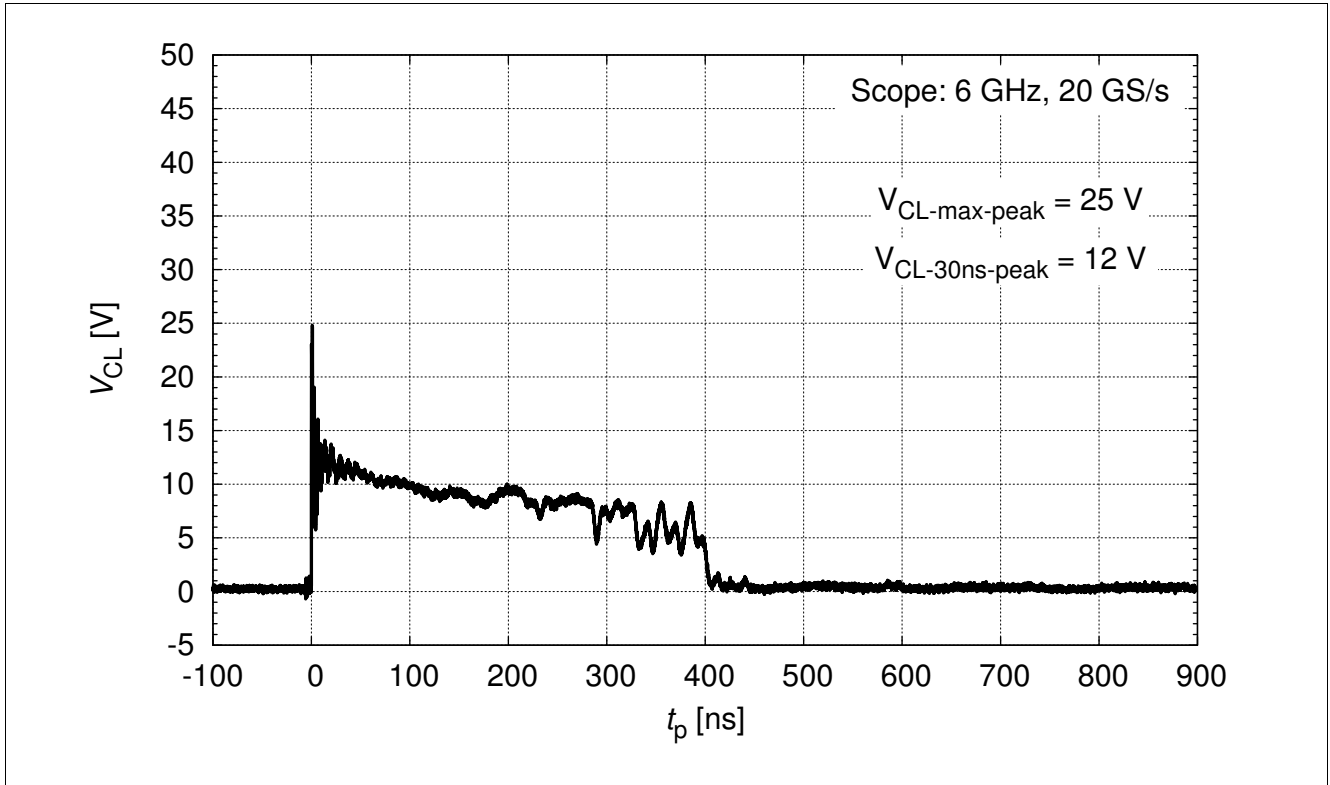


Figure 3-7 IEC61000-4-2: $V_{CL} = f(t)$, +8 kV pulse

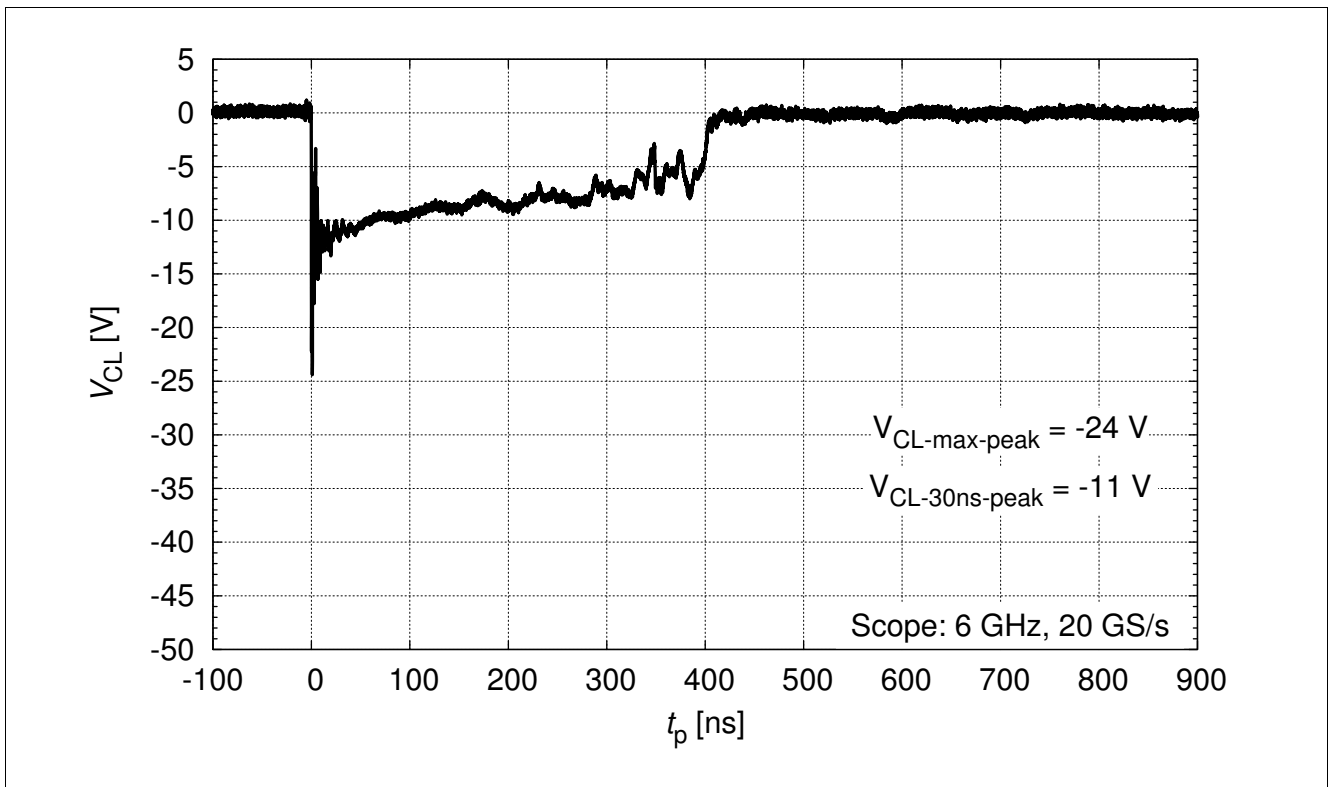


Figure 3-8 IEC61000-4-2: $V_{CL} = f(t)$, -8 kV pulse

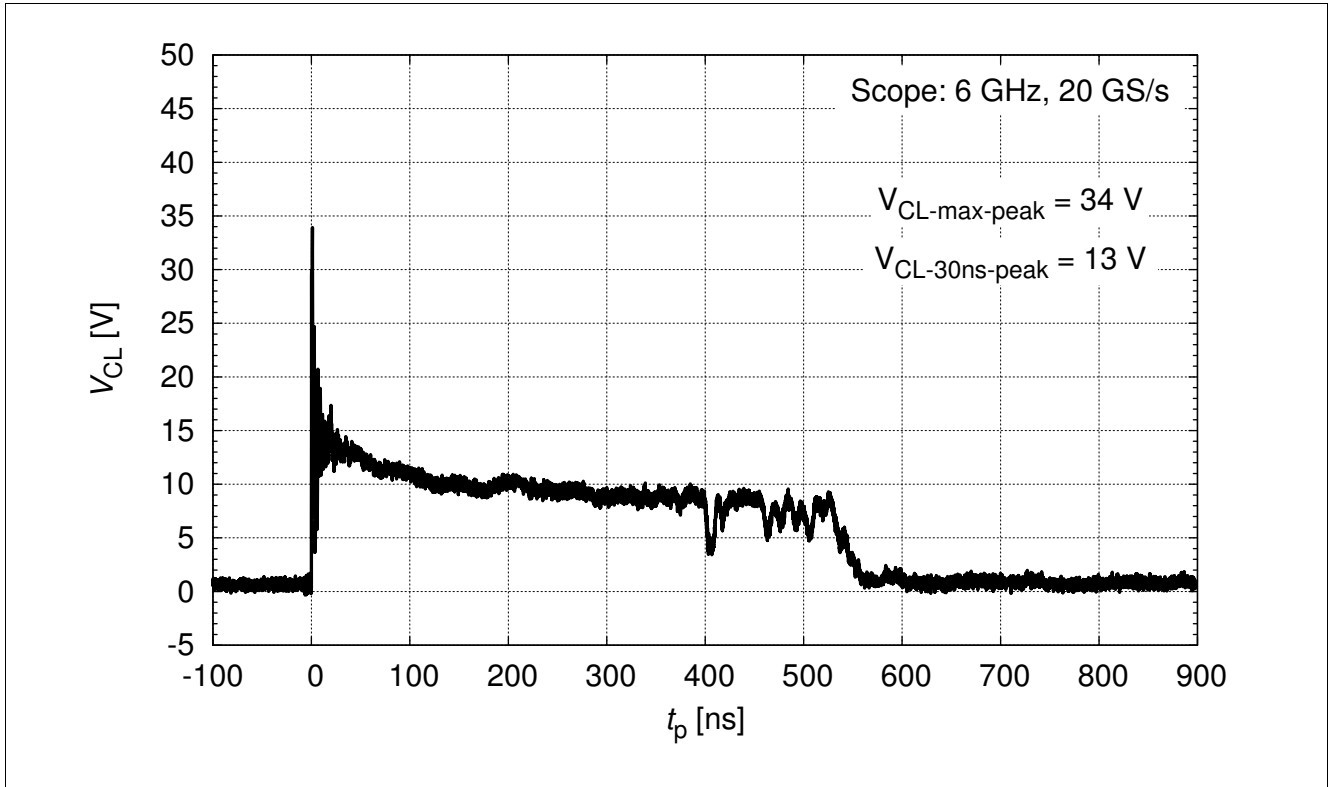


Figure 3-9 IEC61000-4-2: $V_{CL} = f(t)$, +15 kV pulse

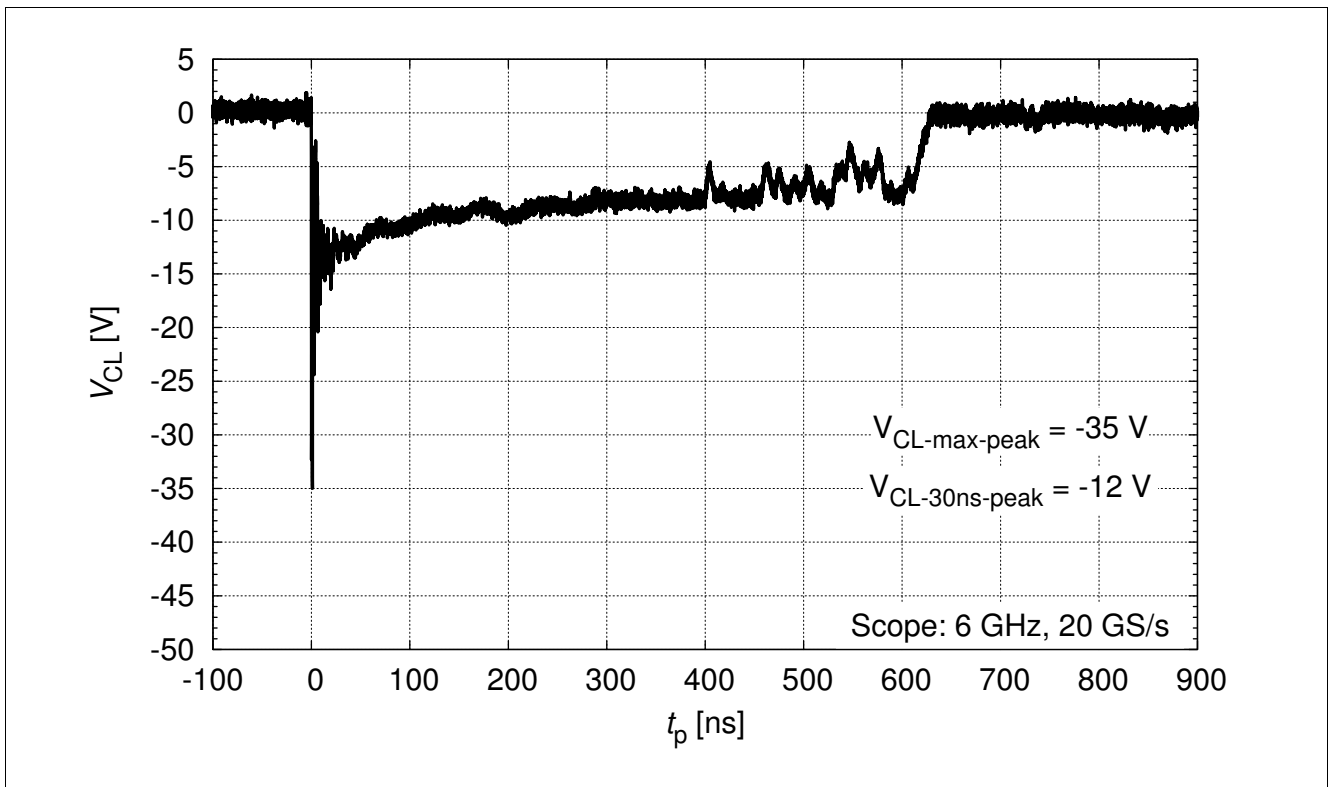


Figure 3-10 IEC61000-4-2: $V_{CL} = f(t)$, -15 kV pulse

4 Application Information

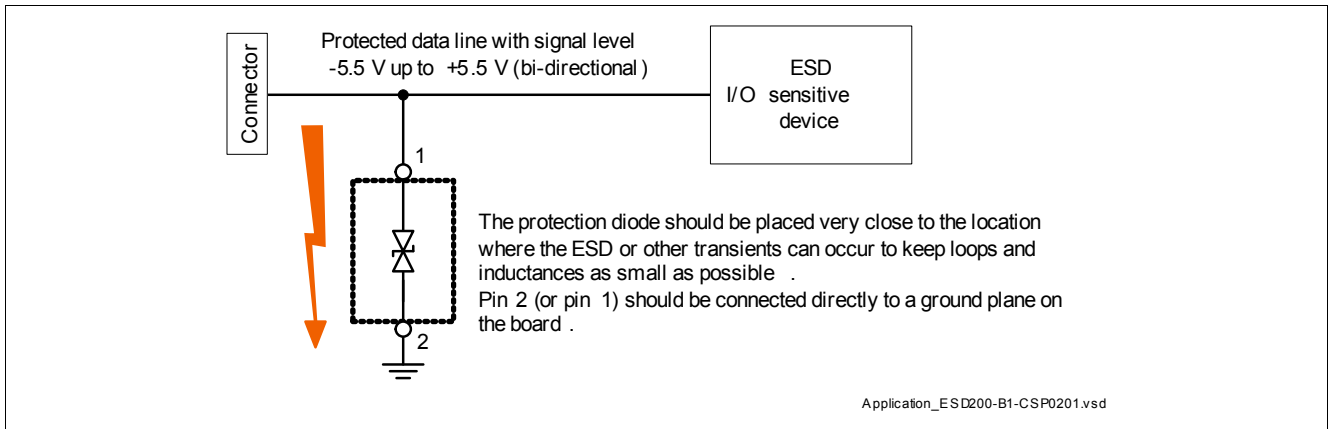


Figure 4-1 Single line, bi-directional ESD / Transient protection

5 Package

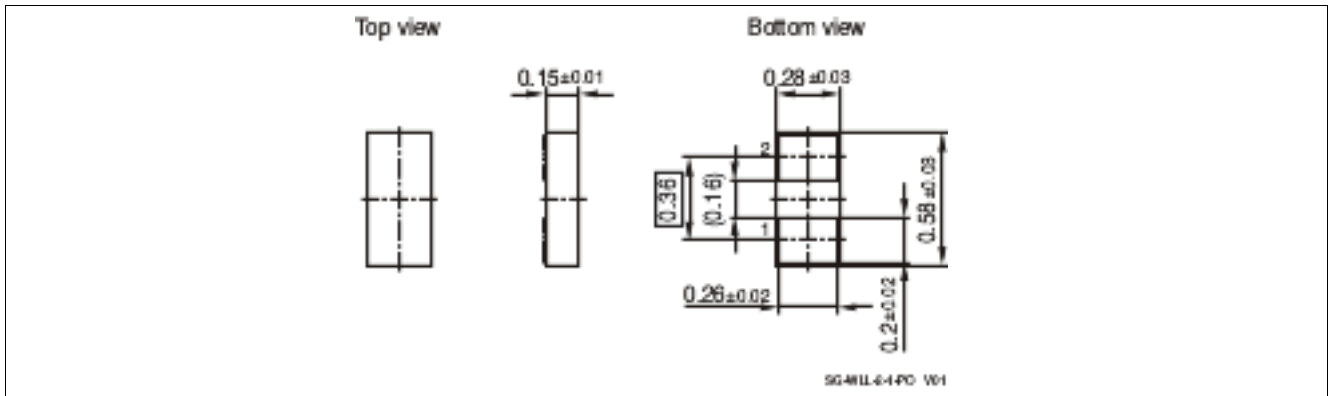


Figure 5-1 WLL-2-1 Package outline (dimension in mm)

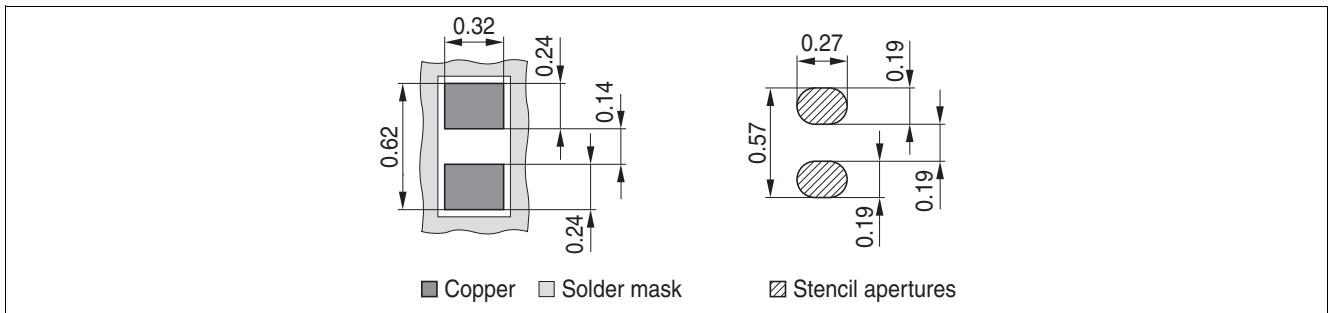


Figure 5-2 WLL-2-1 Footprint (dimension in mm)

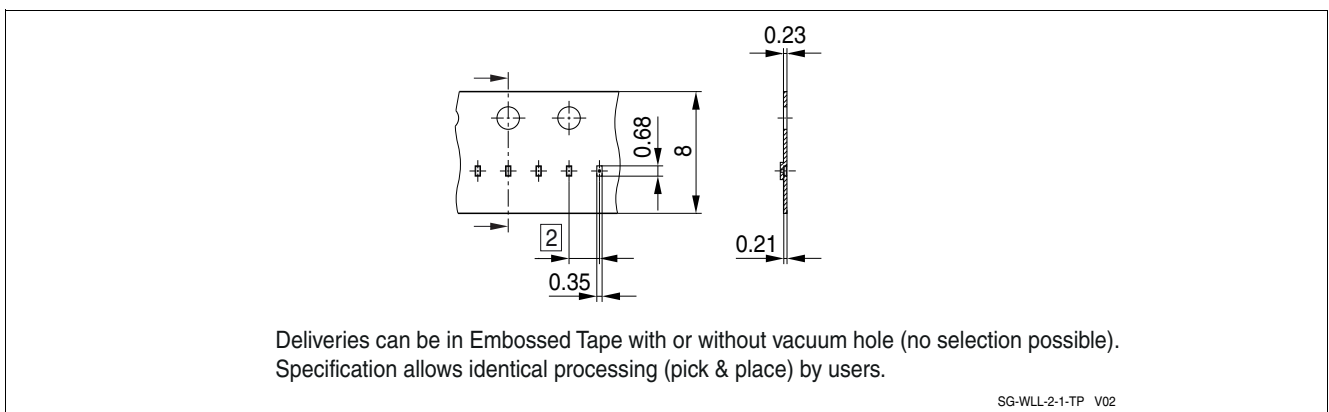


Figure 5-3 WLL-2-1 Packing (dimension in mm)

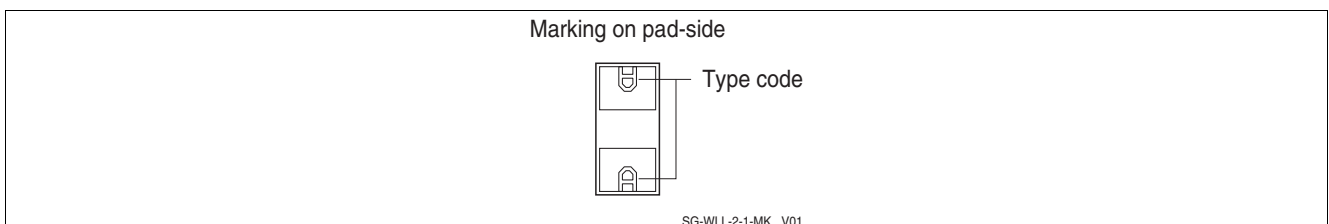


Figure 5-4 WLL-2-1 Marking (example)

References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

www.infineon.com

Published by Infineon Technologies AG