Protection Device

TVS (Transient Voltage Suppressor)

ESD307-U1-02N

Uni-directional, 10 V, 270 pF, 0603, RoHS and Halogen Free compliant

ESD307-U1-02N

Data Sheet

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Final

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Revision History: Rev. 0.9, 2014-03-13	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 2014-05-30	
All	Curves included

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Last Trademarks Update 2010-10-26

1 Product Overview

1.1 Features

- ESD / Transient / Surge protection according to:
  - **IEC61000-4-2 (ESD): ±30 kV (air / contact discharge)**
  - **IEC61000-4-4 (EFT): ±4 kV / ±80 A (5/50 ns)**
  - **IEC61000-4-5 (surge): ±34 A (8/20 µs)**
- Uni-directional working voltage up to V_{RWM} **= 10 V**
- Low capacitance: C_L **= 270 pF (typical)**
- Low clamping voltage V_{CL} **= 24 V (typical) at** I_{PP} **= 34 A**
- Low reverse current. I_R **< 1 nA (typical)**
- Small and flat-profile SMD plastic package: 1.6 mm x 0.8 mm x 0.375 mm.
- Pb-free (RoHS compliant) and halogen free package

1.2 Application Examples

- Surge protection of USB V_{BUS} lines in mobile devices

1.3 Product Description

Figure 1-1 Pin Configuration and Schematic Diagram (in mm)

Table 1-1 Ordering Information

Type	Package	Configuration	Marking code
ESD307-U1-02N	TSNP-2-2	uni-directional	7

2 Characteristics

Table 2-1 Maximum Ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values	Unit
ESD air / contact discharge[1)]	V_{ESD}	±30	kV
Peak pulse power[2)]	P_{PK}	800	W
Peak pulse current[2)]	I_{PP}	34	A
Operating temperature range	T_{OP}	-40 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

1) V_{ESD} according to IEC61000-4-2

2) Non-repetitive current pulse 8/20µs exponential decay waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

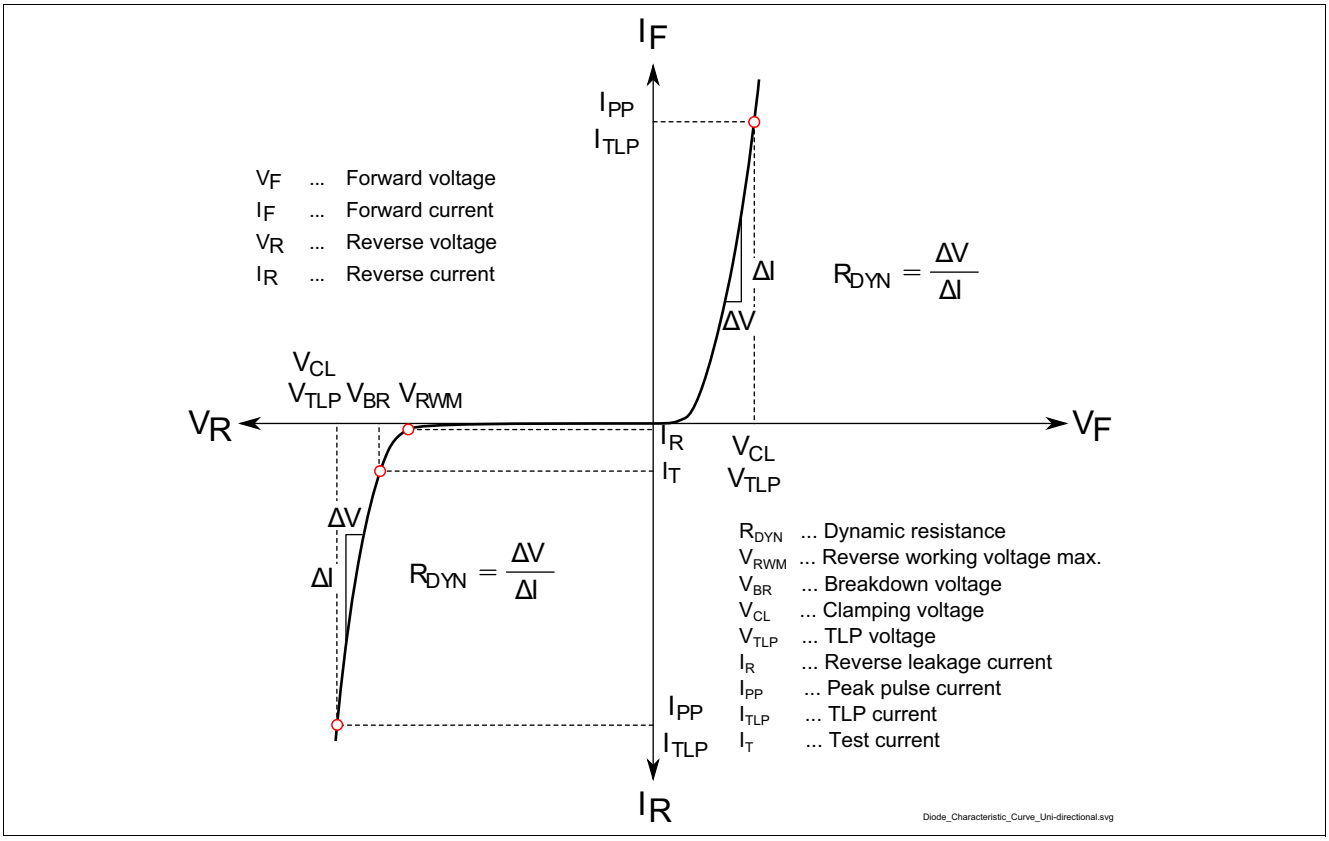

Figure 3-1 Definitions of electrical characteristics

Table 3-1 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	10	V	
Breakdown voltage	V_{BR}	11.1	12.1	–	V	I_T = 1 mA
Reverse current	I_R	–	<1	100	nA	V_R = 10V

Table 3-2 AC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	270	350	pF	V_R = 0 V, f = 1 MHz

Table 3-3 ESD and Surge Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[1)]	V_{CL}	–	17	20.5	V	I_{TLP} = 16 A, t_p = 100 ns
		–	18	22		I_{TLP} = 30 A, t_p = 100 ns
Clamping voltage[2)]		–	16	19.5		I_{PP} = 1 A, t_p = 8/20 µs
		–	24	29		I_{PP} = 34 A, t_p = 8/20 µs
Dynamic resistance[1)]	R_{DYN}	–	0.05	–	Ω	t_p = 100 ns

1) Please refer to Application Note AN210[1]. TLP parameter: Z_0 = 50 Ω , t_p = 100 ns, t_r = 600ps.

2) Non-repetitive current pulse 8/20µs exponential decay waveform according to IEC61000-4-5

4 Typical Characteristics Diagrams

Typical characteristics diagrams at T_A = 25°C, unless otherwise specified

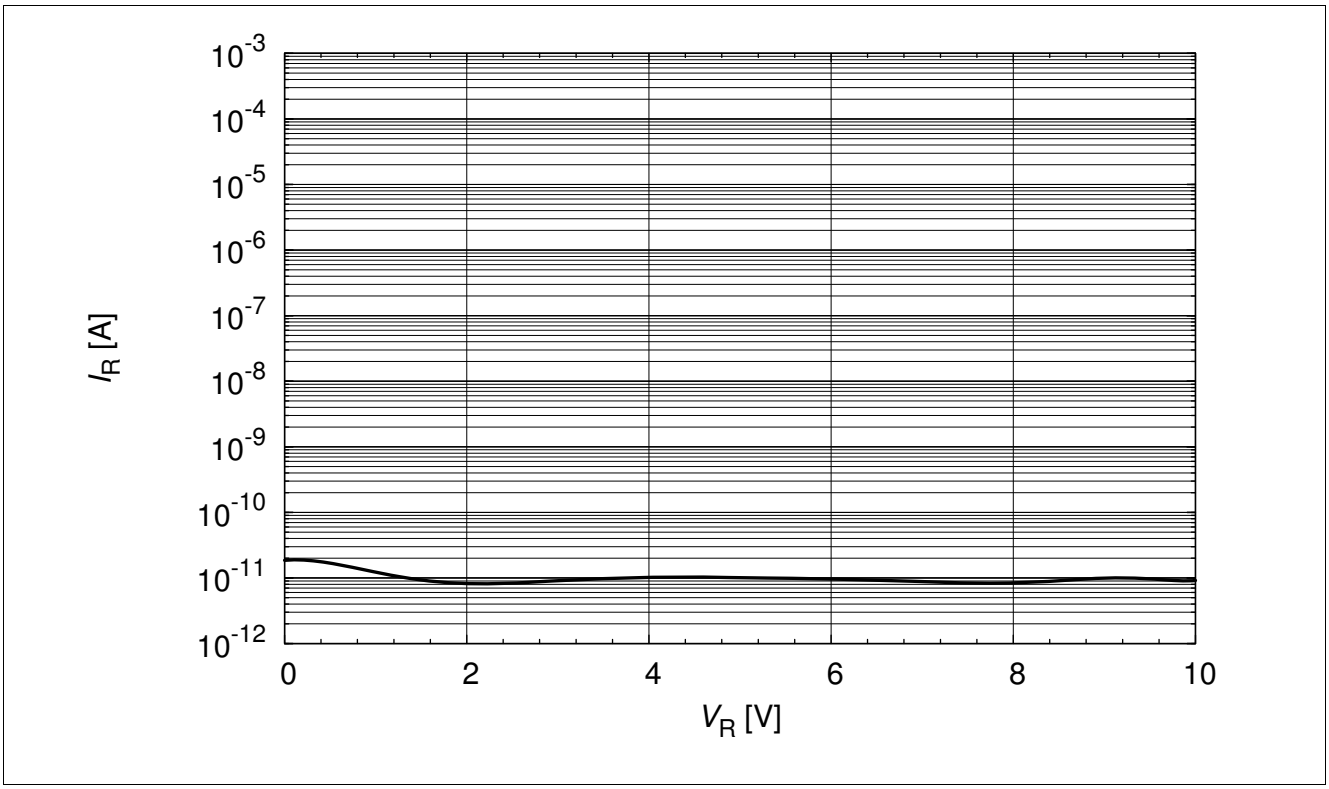

Figure 4-1 Reverse leakage current: $I_R = f(V_R)$

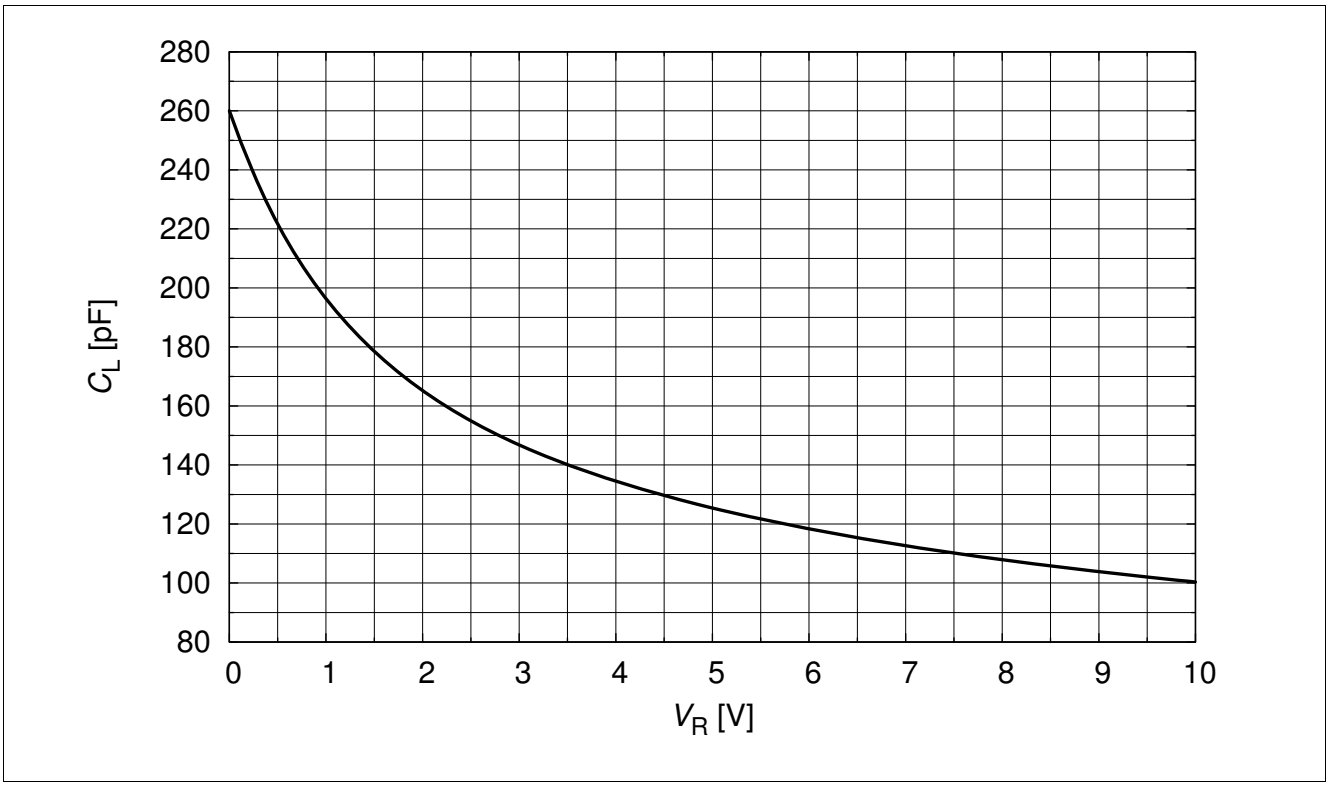

Figure 4-2 Line capacitance: $C_L = f(V_R)$

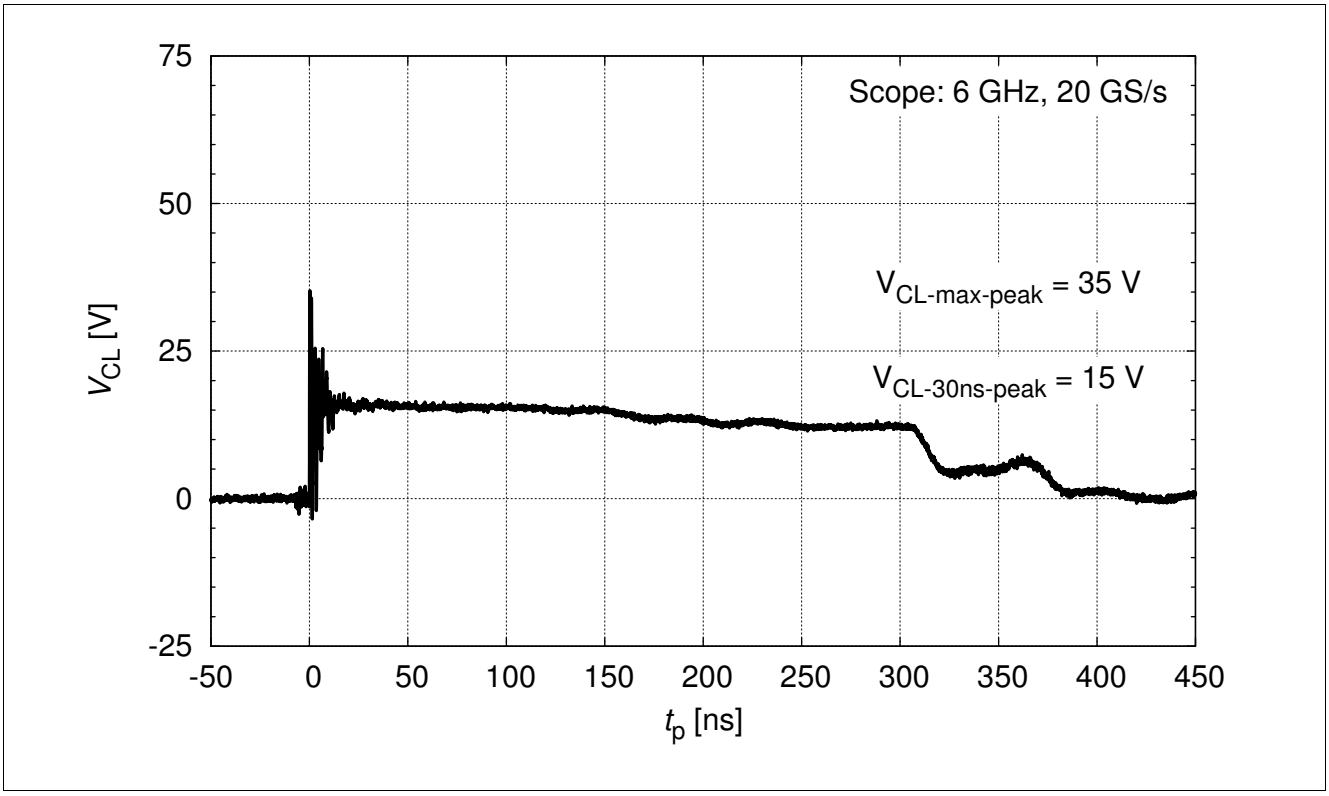

Figure 4-3 Clamping voltage (ESD): V_{CL} = *f*(*t*), 8 kV positive pulse from pin 1 to pin 2

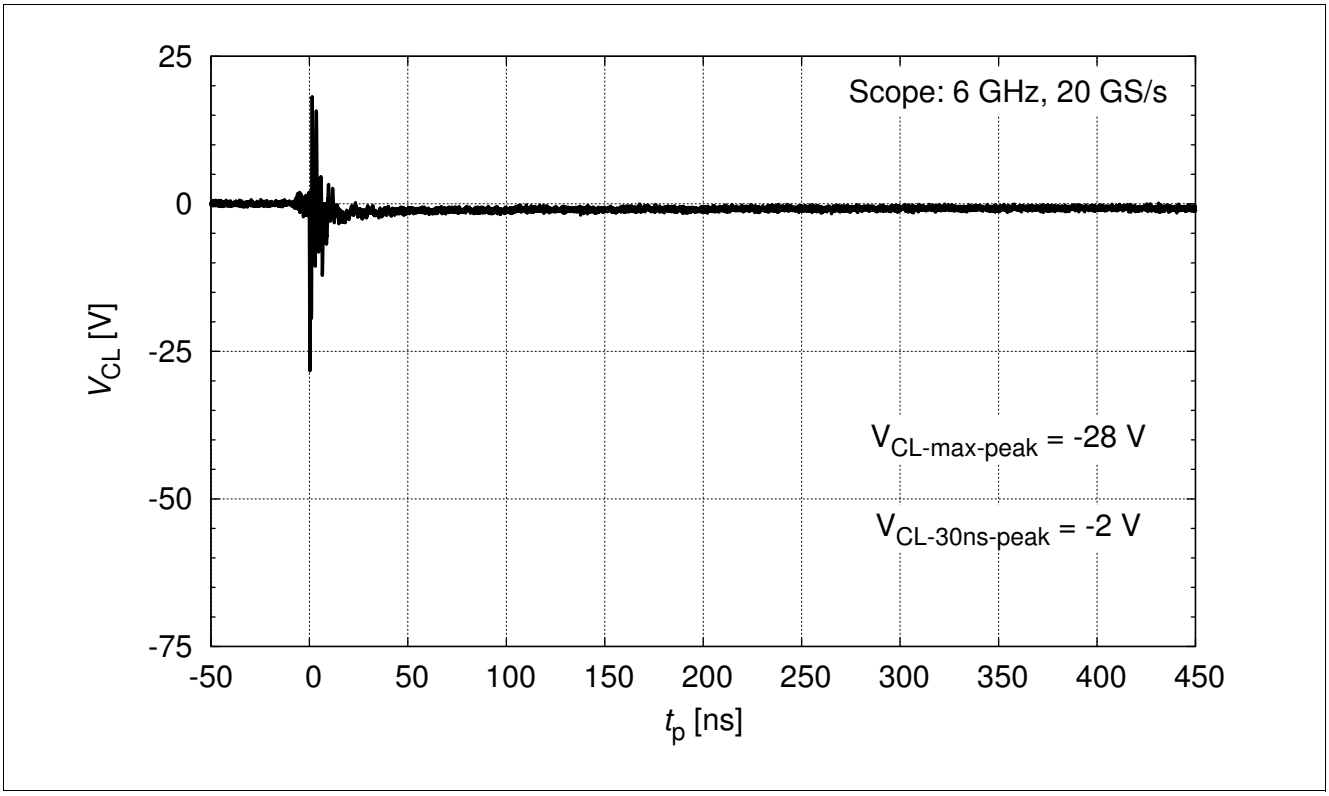

Figure 4-4 Clamping voltage (ESD) V_{CL} = *f*(*t*), 8 kV negative pulse from pin 1 to pin 2

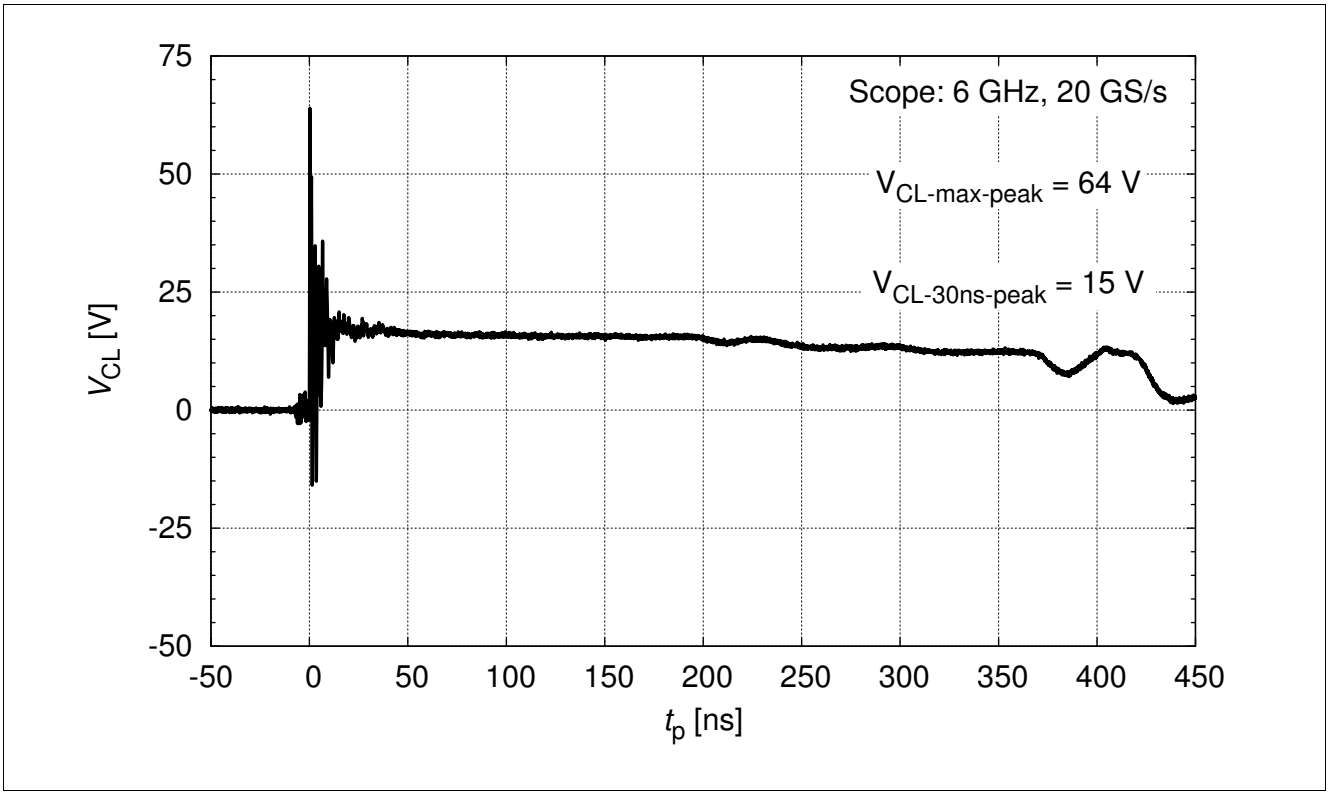

Figure 4-5 Clamping voltage (ESD) V_{CL} = *f*(*t*), 15 kV positive pulse from pin 1 to pin 2

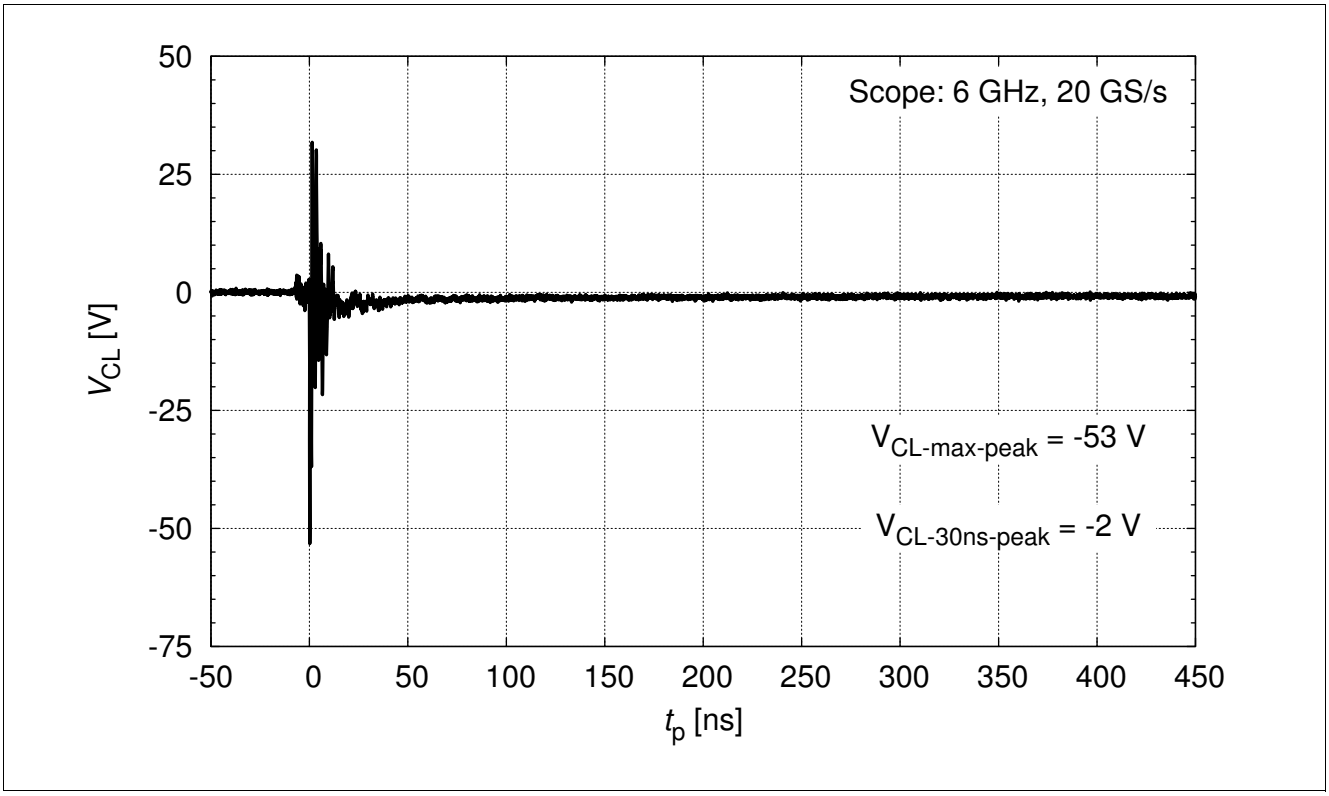

Figure 4-6 Clamping voltage (ESD) V_{CL} = *f*(*t*), 15 kV negative pulse from pin 1 to pin 2

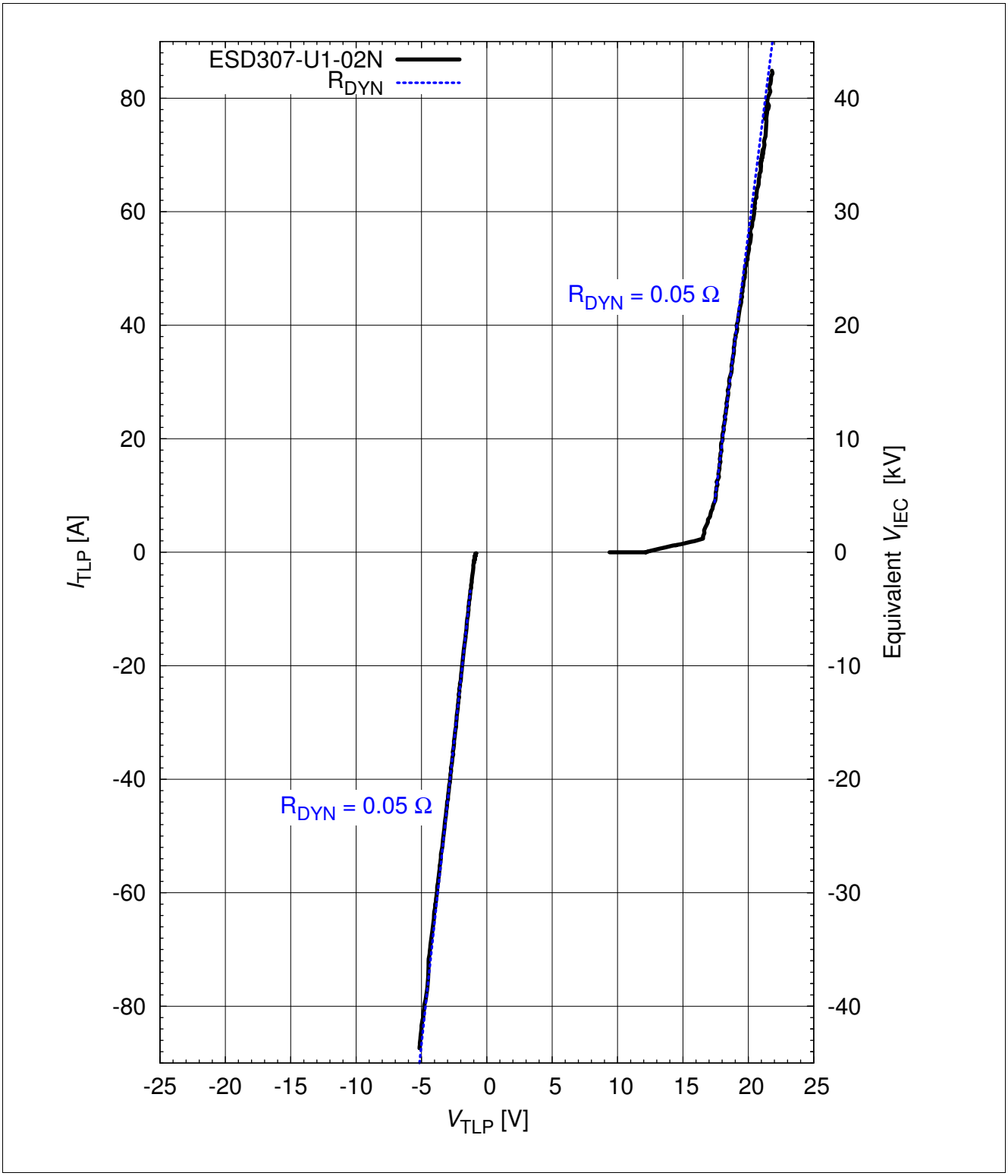

Figure 4-7 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$[1], pin 1 to pin 2

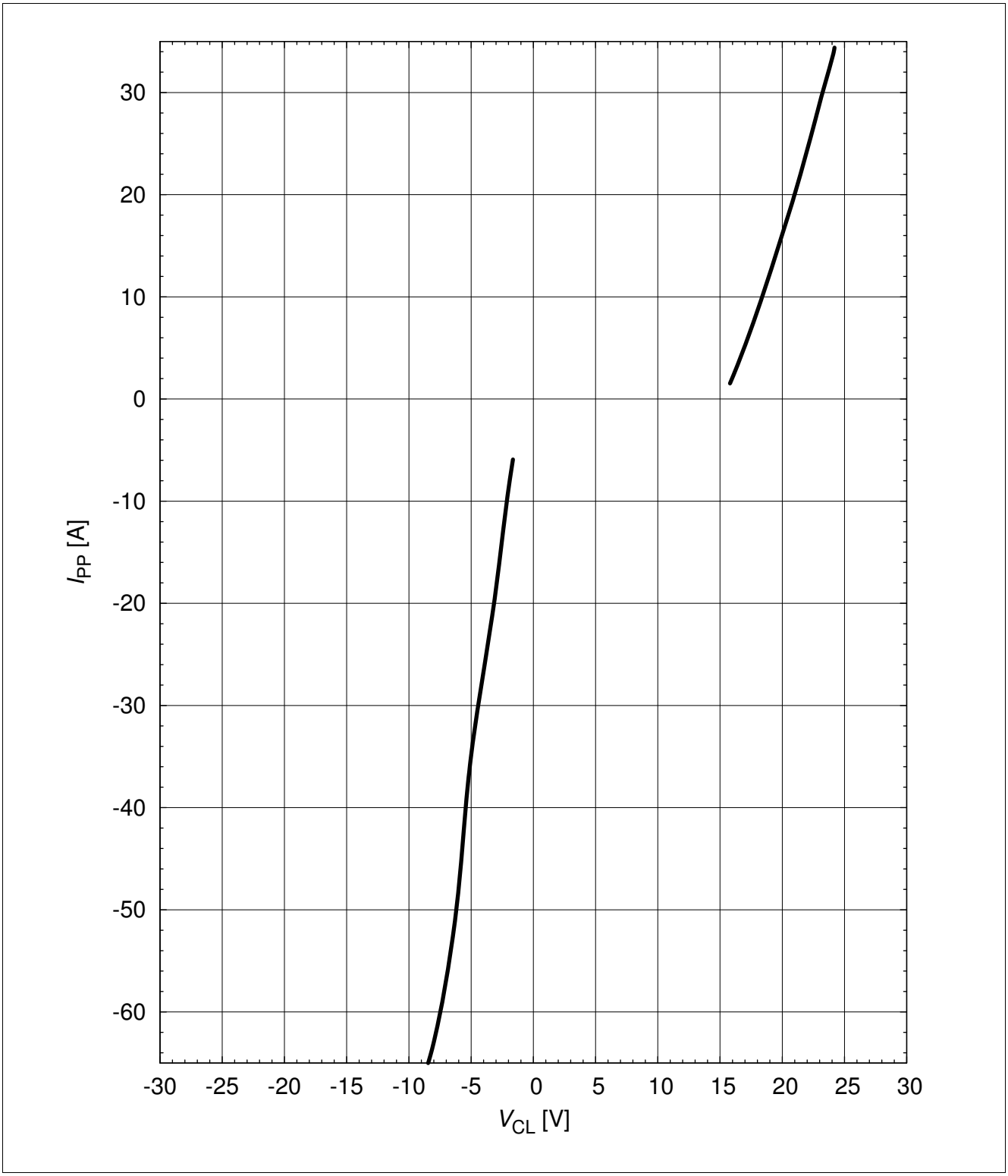

Figure 4-8 Pulse current (Surge): $I_{PP} = f(V_{CL})$[1], pin 1 to pin 2

5 Package Information

5.1 TSNP-2-2

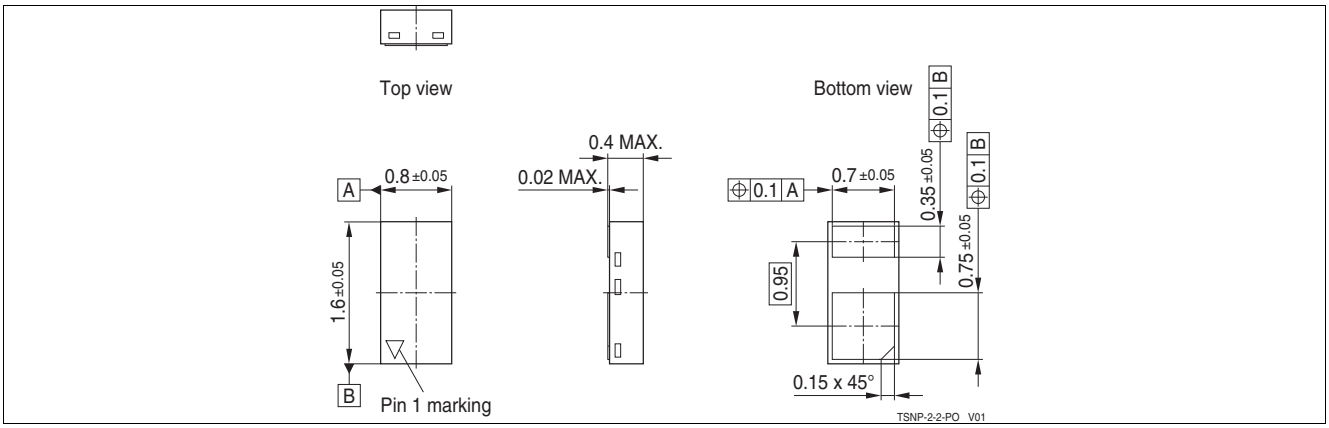

Figure 5-1 TSNP-2-2: Package overview

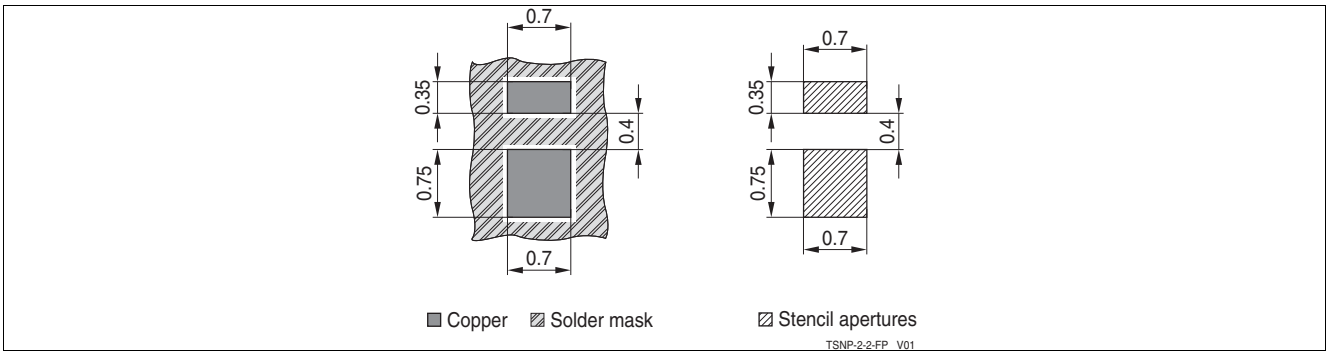

Figure 5-2 TSNP-2-2: Footprint

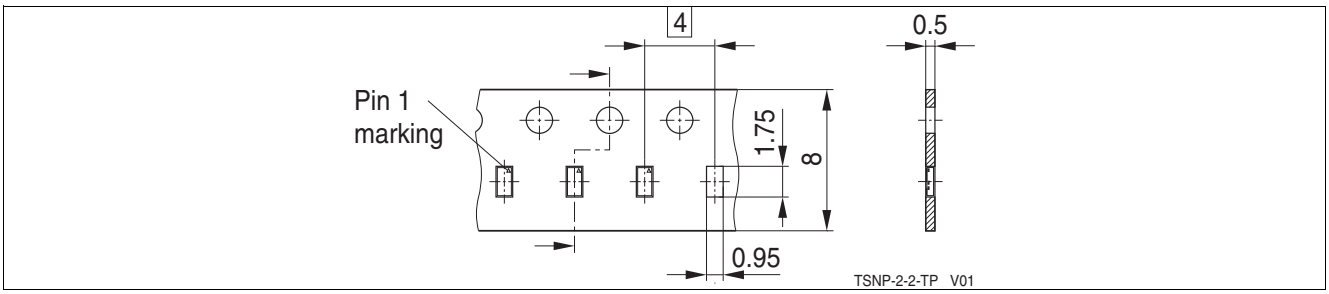

Figure 5-3 TSNP-2-2: Packing

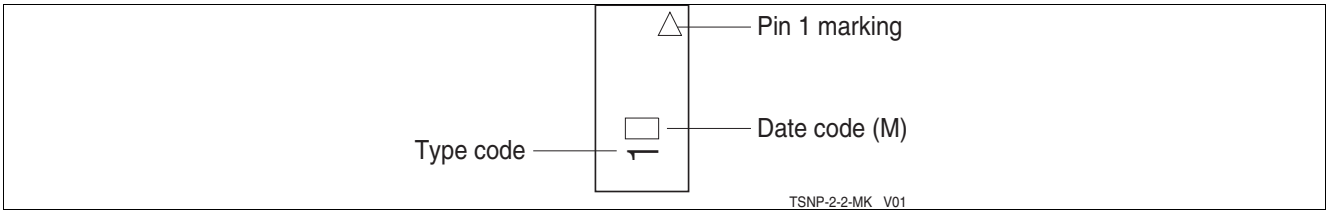

Figure 5-4 TSNP-2-2: Marking (example)

References

[1] Infineon AG - **Application Note AN210:** Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

[2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

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