ESD Protection Diodes

Micro-packaged Diodes for ESD Protection

The ESD51x1 Series is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in smartphone, smart-watch, or many other portable / wearable applications where board space comes at a premium.

Features

- Low Capacitance (5 pF Max, I/O to GND)
- Small Body Outline Dimensions
 - 01005 Size: 0.435 x 0.23 mm
 - 0201 Size: 0.6 x 0.3 mm
- Protection for the Following IEC Standards: IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25° C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	ТJ	-55 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	ΤL	260	°C
IEC 61000–4–2 Contact (ESD) IEC 61000–4–2 Air (ESD)	ESD ESD	±15 ±15	kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

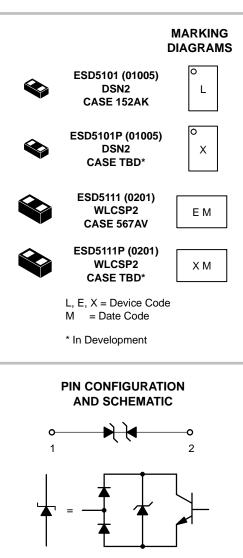
See Application Note AND8308/D for further description of survivability specs.

This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.



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ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Reverse Working Voltage	V _{RWM}	I/O Pin to GND			3.3	V
Breakdown Voltage	V _{BR}	I _T = 1 mA, I/O Pin to GND	3.68	5.0	6.5	V
Reverse Leakage Current	I _R	V _{RWM} = 3.3 V, I/O Pin to GND			0.1	μΑ
ESD5101, ESD5111 Clamping Voltage TLP (Note 1)	V _C	$I_{PP} = 8 A $ $\begin{cases} IEC 61000-4-2 \text{ Level 2 equivalent} \\ (\pm 4 \text{ kV Contact}, \pm 4 \text{ kV Air}) \end{cases}$		5.5		V
		$I_{PP} = 16 A \\ \left\{ \begin{array}{l} \text{IEC } 61000 - 4 - 2 \text{ Level } 2 \text{ equivalent} \\ (\pm 8 \text{ kV Contact}, \pm 15 \text{ kV Air}) \end{array} \right\}$		6.5		
Junction Capacitance	CJ	V _R = 0 V, f = 1 MHz			5.5	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0 = 50 \ \Omega$, $t_p = 100 \ ns$, $t_r = 4 \ ns$, averaging window; $t_1 = 30 \ ns$ to $t_2 = 60 \ ns$.

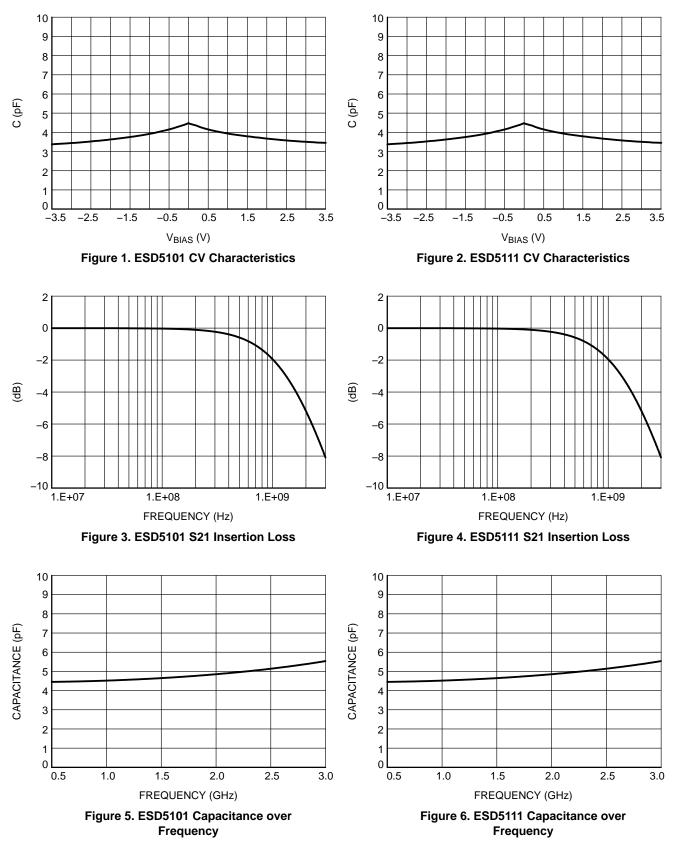
ORDERING INFORMATION

Device	Package	Shipping [†]
ESD5101FCT5G	DSN2 (Pb-Free)	10,000 / Tape & Reel
ESD5111FCT5G	WLCSP2 (Pb-Free)	10,000 / Tape & Reel
ESD5101PFCT5G**	Side wall Isolated 01005	10,000 / Tape & Reel
ESD5111PFCT5G**	Side wall Isolated 0201	10,000 / Tape & Reel

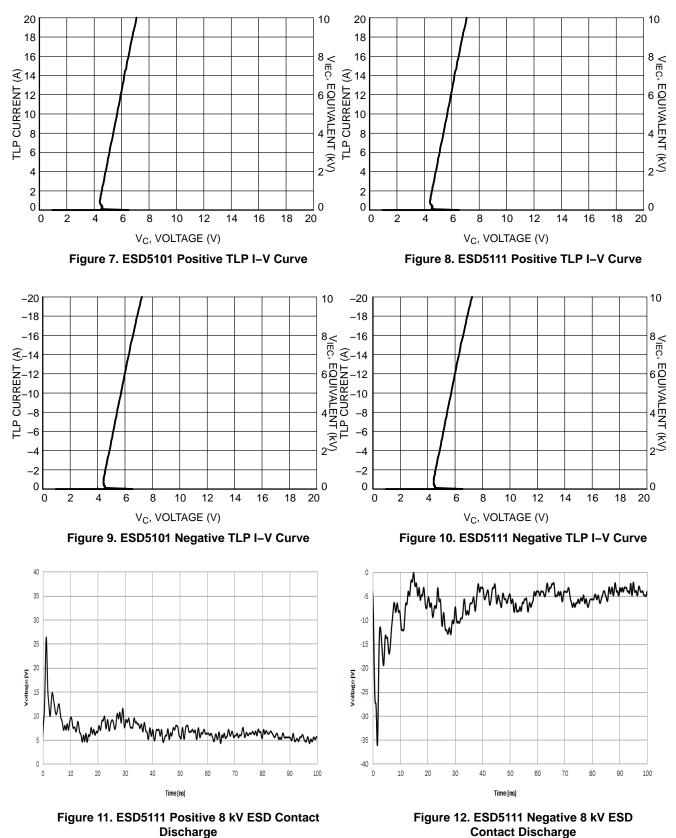
** In Development. Contact local sales rep for availability.

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



IEC 61000-4-2 Spec.

Level	Test Volt- age (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

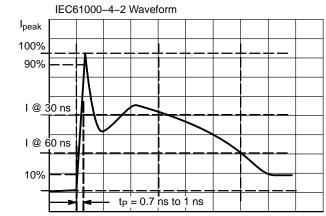


Figure 13. IEC61000-4-2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I–V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 14. TLP I–V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 15 where an 8 kV IEC 61000–4–2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I–V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

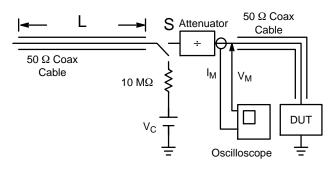


Figure 14. Simplified Schematic of a Typical TLP System

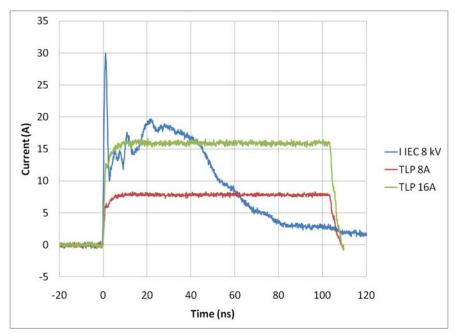
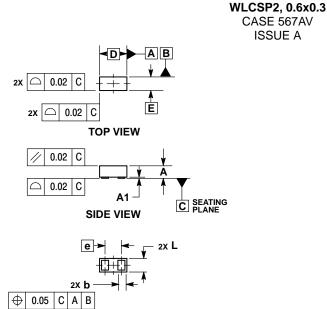


Figure 15. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

PACKAGE DIMENSIONS - ESD5111 (0201)

ISSUE A



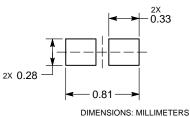
BOTTOM VIEW

NOTES: 1. DIMENSIONING AND TOLERANCING PER

ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS.



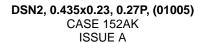
RECOMMENDED SOLDER FOOTPRINT*

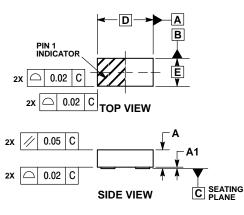


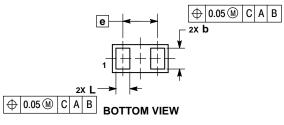
*For additional information on our Pb-Free strategy and soldering

details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS - ESD5101 (01005)







NOTES

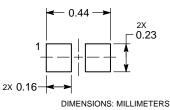
1. DIMENSIONING AND TOLERANCING PER

ASME Y14 5M 1994

2. CONTROLLING DIMENSION: MILLIMETERS.

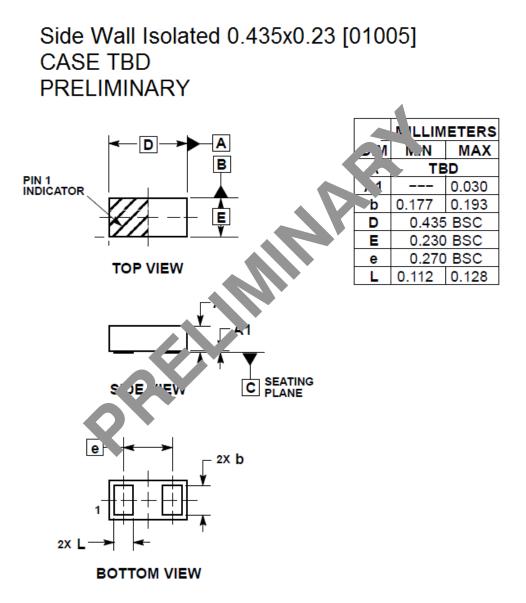
_	MILLIMETERS		
DIM	MIN	MAX	
Α	0.165	0.195	
A1		0.030	
b	0.177	0.193	
D	0.435 BSC		
E	0.230 BSC		
е	0.270 BSC		
L	0.112	0.128	

RECOMMENDED SOLDER FOOTPRINT*

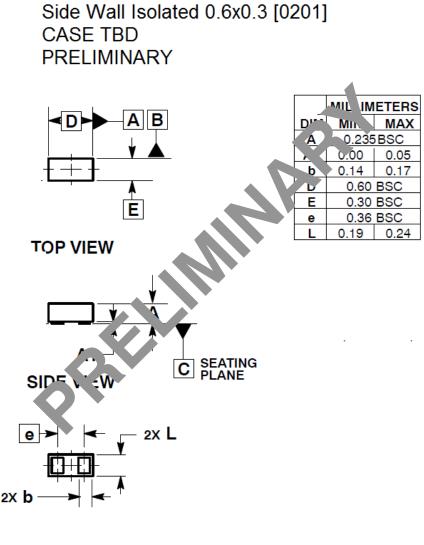


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PACKAGE DIMENSIONS – ESD5101P (01005)



PACKAGE DIMENSIONS - ESD5111P (0201)



BOTTOM VIEW

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PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

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