

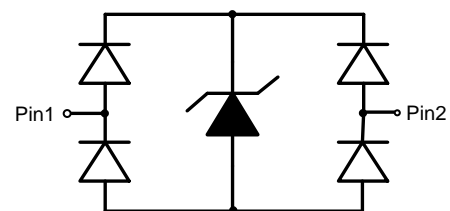
**ESD5311Z**
**1-Line, Bi-directional, Ultra-low Capacitance  
Transient Voltage Suppressor**
<http://www.sh-willsemi.com>
**Descriptions**

The ESD5311Z is an ultra-low capacitance TVS (Transient Voltage Suppressor) designed to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-stress caused by ESD (Electrostatic Discharge).

The ESD5311Z incorporates one pair of ultra-low capacitance steering diodes plus a TVS diode.

The ESD5311Z may be used to provide ESD protection up to  $\pm 20\text{kV}$  (contact discharge) according to IEC61000-4-2, and withstand peak pulse current up to 4A (8/20 $\mu\text{s}$ ) according to IEC61000-4-5.

The ESD5311Z is available in DFN0603-2L package. Standard products are Pb-free and Halogen-free.


**DFN0603-2L (Bottom View)**

**Pin configuration**
**Features**

- Stand-off voltage: 5V Max.
- Transient protection for each line according to IEC61000-4-2 (ESD):  $\pm 20\text{kV}$  (contact discharge)  
IEC61000-4-4 (EFT): 40A (5/50ns)  
IEC61000-4-5 (surge): 4 A (8/20 $\mu\text{s}$ )
- Ultra-low capacitance:  $C_J = 0.25\text{pF}$  typ.
- Ultra-low leakage current:  $I_R < 1\text{nA}$  typ.
- Low clamping voltage:  $V_{CL} = 21\text{V}$  typ. @  $I_{PP} = 16\text{A}$  (TLP)
- Small package



D = Device code  
\* = Month code

**Marking (Top View)**
**Applications**

- USB 2.0 and USB 3.0
- HDMI 1.3 and HDMI 1.4
- SATA and eSATA
- DVI
- IEEE 1394
- PCI Express
- Portable Electronics
- Notebooks

**Order information**

Device	Package	Shipping
ESD5311Z-2/TR	DFN0603-2L	10000/Tape&Reel

**Absolute maximum ratings**

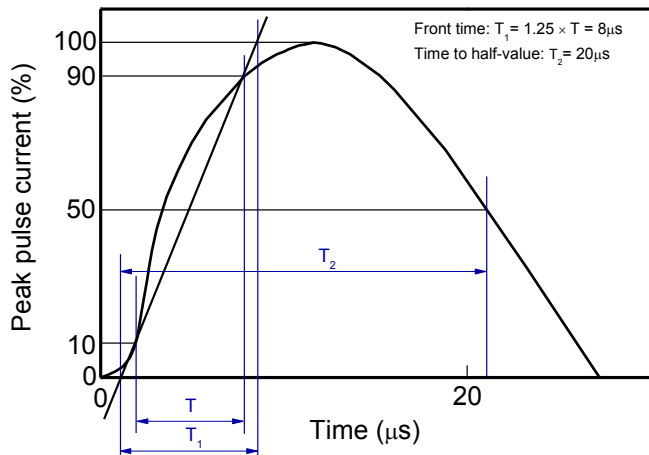
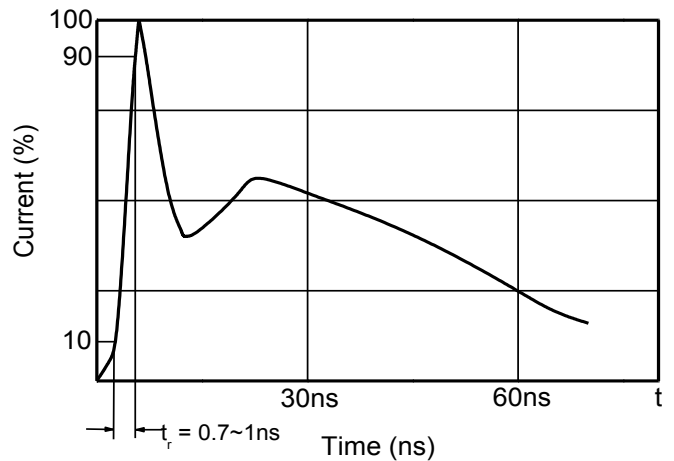
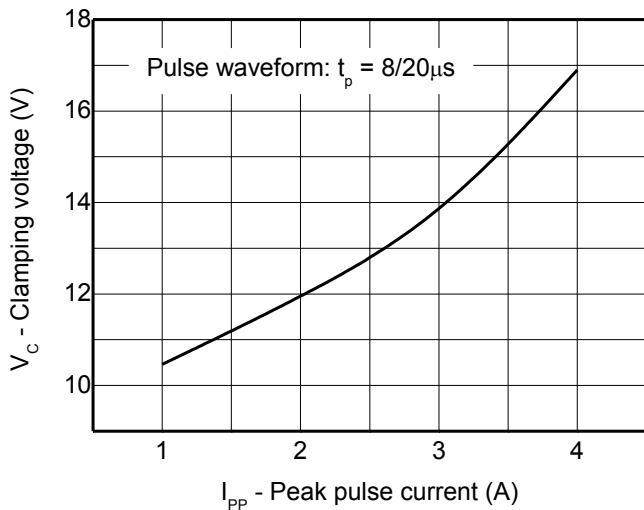
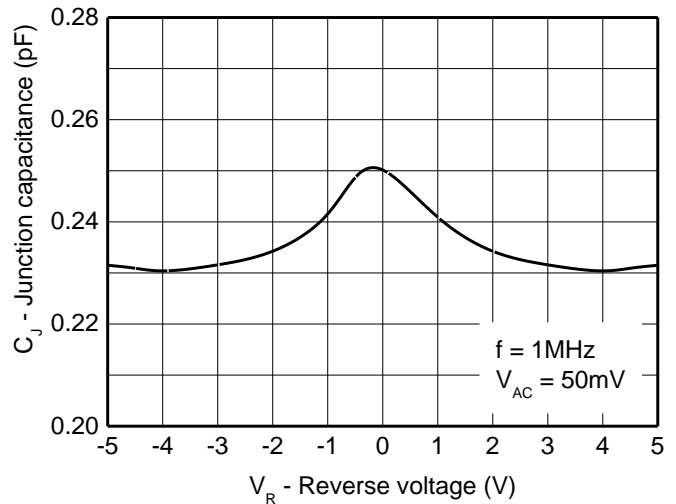
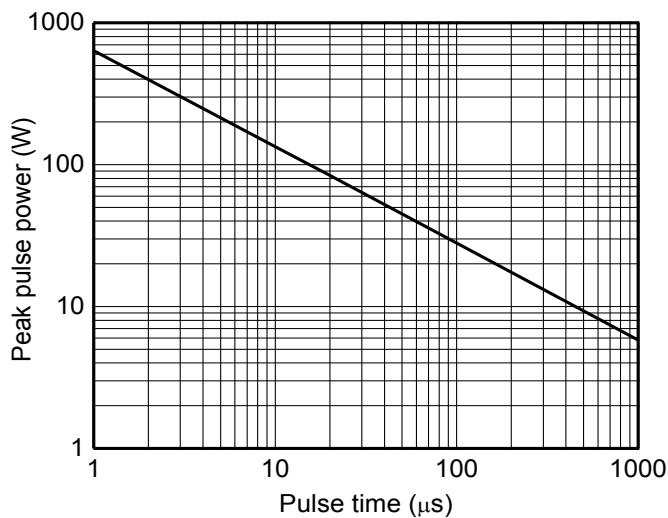
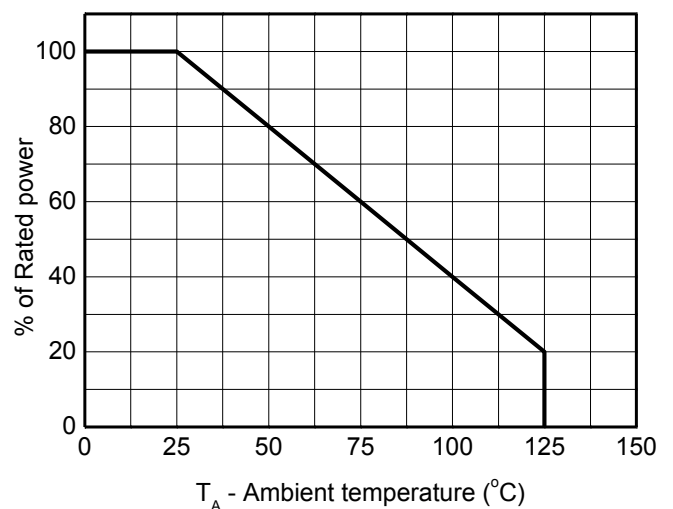
Parameter	Symbol	Rating	Unit
Peak pulse power ( $t_p = 8/20\mu s$ )	$P_{pk}$	84	W
Peak pulse current ( $t_p = 8/20\mu s$ )	$I_{PP}$	4	A
ESD according to IEC61000-4-2 air discharge	$V_{ESD}$	$\pm 20$	kV
ESD according to IEC61000-4-2 contact discharge		$\pm 20$	
Junction temperature	$T_J$	125	$^{\circ}C$
Operating temperature	$T_{OP}$	-40~85	$^{\circ}C$
Lead temperature	$T_L$	260	$^{\circ}C$
Storage temperature	$T_{STG}$	-55~150	$^{\circ}C$

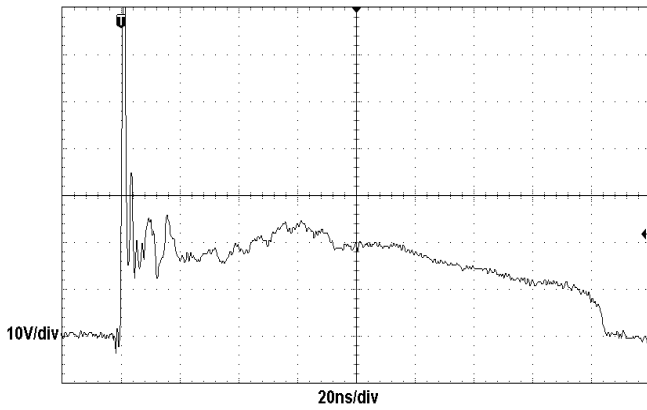
**Electrical characteristics ( $T_A=25^{\circ}C$ , unless otherwise noted)**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse maximum working voltage	$V_{RWM}$				5.0	V
Reverse leakage current	$I_R$	$V_{RWM} = 5V$		<1	100	nA
Reverse breakdown voltage	$V_{BR}$	$I_T = 1mA$	7.5	9.0	10.0	V
Clamping voltage <sup>1)</sup>	$V_{CL}$	$I_{PP} = 16A, t_p = 100ns$		21		V
Dynamic resistance <sup>1)</sup>	$R_{DYN}$			0.7		$\Omega$
Clamping voltage <sup>2)</sup>	$V_{CL}$	$V_{ESD} = 8kV$		21		V
Clamping voltage <sup>3)</sup>	$V_{CL}$	$I_{PP} = 1A, t_p = 8/20\mu s$			14	V
		$I_{PP} = 4A, t_p = 8/20\mu s$			21	V
Junction capacitance	$C_J$	$V_R = 0V, f = 1MHz$		0.25	0.4	pF

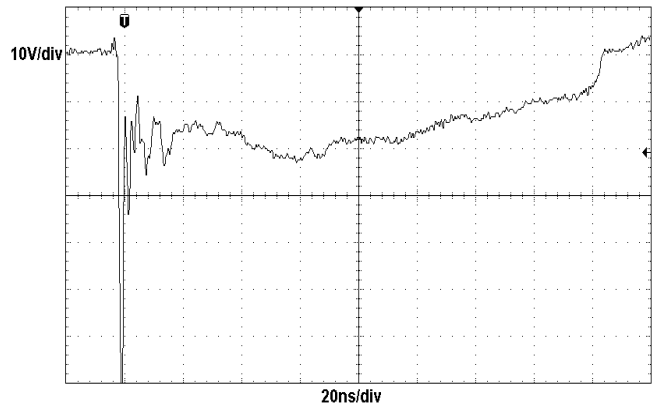
Notes:

- 1) TLP parameter:  $Z_0 = 50\Omega, t_p = 100ns, t_r = 2ns$ , averaging window from 60ns to 80ns.  $R_{DYN}$  is calculated from 4A to 16A.
- 2) Contact discharge mode, according to IEC61000-4-2.
- 3) Non-repetitive current pulse, according to IEC61000-4-5.

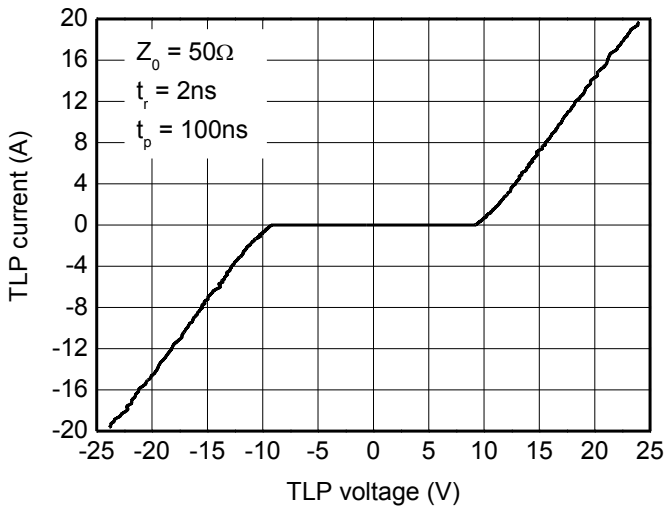
**Typical characteristics ( $T_A=25^\circ\text{C}$ , unless otherwise noted)**

**8/20 $\mu\text{s}$  waveform per IEC61000-4-5**

**Contact discharge current waveform per IEC61000-4-2**

**Clamping voltage vs. Peak pulse current**

**Capacitance vs. Reverse voltage**

**Non-repetitive peak pulse power vs. Pulse time**

**Power derating vs. Ambient temperature**



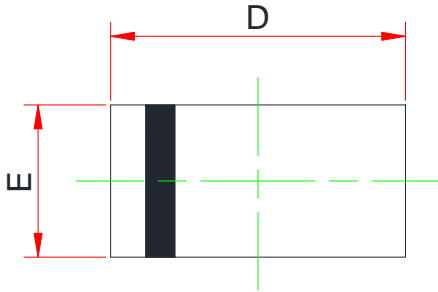
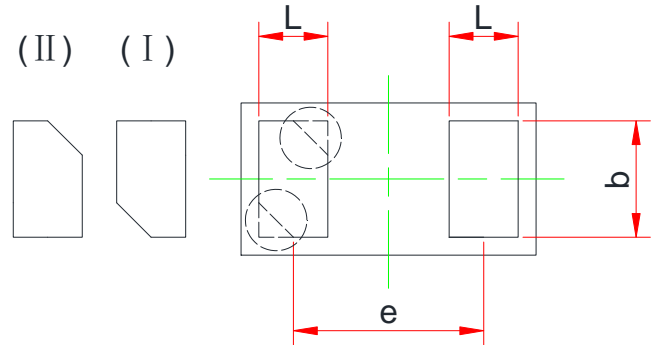
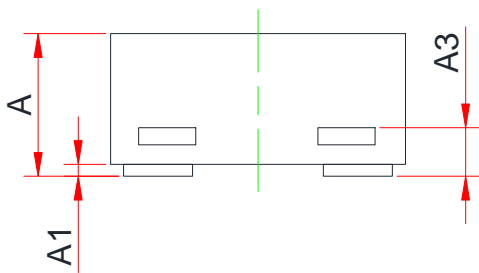
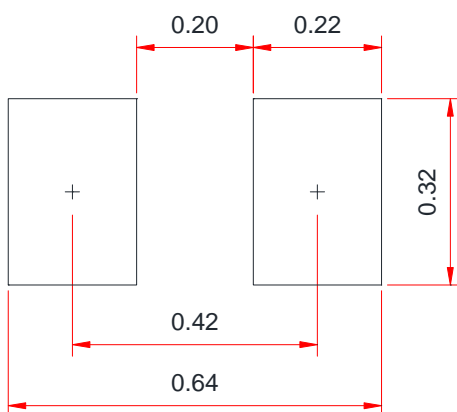
**ESD clamping**  
 (+8kV contact discharge per IEC61000-4-2)



**ESD clamping**  
 (-8kV contact discharge per IEC61000-4-2)



**TLP Measurement**

**Package outline dimensions**
**DFN0603-2L**

**Top View**

**Bottom View**

**Side View**
**Recommend land pattern (Unit: mm)**


Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.230	-	0.340
A1	0.000	-	0.050
A3	0.102 REF.		
D	0.550	0.600	0.670
E	0.250	0.300	0.370
b	0.215	-	0.295
e	0.400 BSC		
L	0.115	-	0.195

**Notes:**

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

## Reversion history

制 修 订 记 录			
文件版本	制修日期	修订页次	变更内容
Rev 1.0	2014/07/27	1-5	初版发布。
Rev 1.1	2014/10/09	5	VBR@1mA 下限由 8V 改为 7.5V。 修改电容曲线图，更改 ESD 波形图
Rev 1.2	2014/11/17	5	修改 ESD 波形图、拼写错误。
Rev 1.3	2016/6/24	1, 6	修改封装图与实物匹配。