

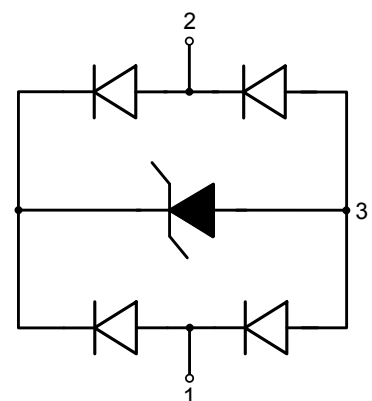
ESD5342N
**2-Lines, Uni-directional, Low Capacitance
Transient Voltage Suppressor**
<http://www.sh-willsemi.com>
Descriptions

The ESD5342N is a low capacitance TVS (Transient Voltage Suppressor) designed to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-stress caused by ESD (Electrostatic Discharge).

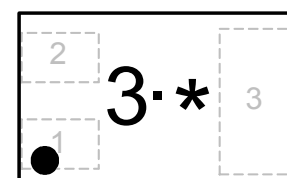
The ESD5342N incorporates two pairs of low capacitance steering diodes plus a TVS diode.

The ESD5342N may be used to provide ESD protection up to $\pm 20\text{kV}$ (contact discharge) according to IEC61000-4-2, and withstand peak pulse current up to 4A (8/20 μs) according to IEC61000-4-5.

The ESD5342N is available in DFN1006-3L package. Standard products are Pb-free and Halogen-free.


DFN1006-3L (Bottom View)

Circuit diagram
Features

- Stand-off voltage: 5V max.
- Transient protection for each line according to IEC61000-4-2 (ESD): $\pm 20\text{kV}$ (contact discharge)
IEC61000-4-4 (EFT): 40A (5/50ns)
IEC61000-4-5 (surge): 4A (8/20 μs)
- Low capacitance: $C_J = 1.0\text{pF}$ typ.
- Ultra-low leakage current: $I_R < 1\text{nA}$ typ.
- Low clamping voltage: $V_{CL} = 17.5\text{V}$ @ $I_{PP} = 16\text{A}$ (TLP)
- Solid-state silicon technology



3 = Device code

* = Month code (A~Z)

Marking (Top View)

Applications

- USB Interface
- HDMI Interface
- DVI
- Portable Electronics
- Notebooks

Order information

Device	Package	Shipping
ESD5342N-3/TR	DFN1006-3L	10000/Tape&Reel

Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Peak pulse power ($t_p = 8/20\mu s$)	P_{pk}	60	W
Peak pulse current ($t_p = 8/20\mu s$)	I_{PP}	4	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 20	kV
ESD according to IEC61000-4-2 contact discharge		± 20	
Junction temperature	T_J	125	$^{\circ}C$
Operating temperature	T_{OP}	-40~85	$^{\circ}C$
Lead temperature	T_L	260	$^{\circ}C$
Storage temperature	T_{STG}	-55~150	$^{\circ}C$

Electrical characteristics ($T_A = 25^{\circ}C$, unless otherwise noted)

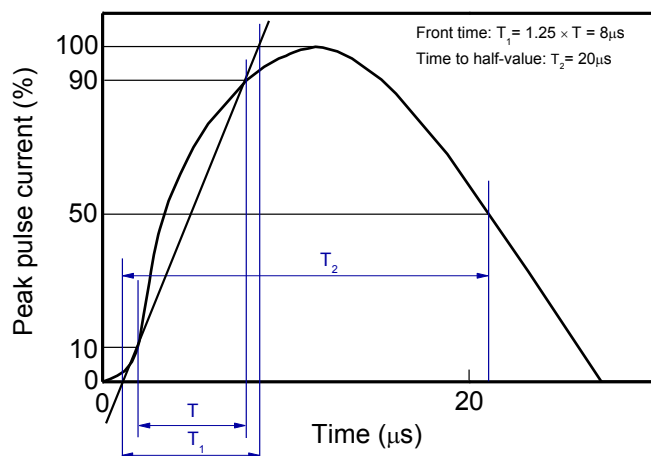
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse maximum working voltage	V_{RWM}				5.0	V
Reverse leakage current	I_R	$V_{RWM} = 5V$		<1	100	nA
Reverse breakdown voltage	V_{BR}	$I_T = 1mA$	7.0	8.0	9.0	V
Forward voltage	V_F	$I_T = 10mA$	0.6	0.9	1.2	V
Clamping voltage ¹⁾	V_{CL}	$I_{PP} = 16A, t_p = 100ns$		17.5		V
Dynamic resistance ¹⁾	R_{DYN}			0.55		Ω
Clamping voltage ²⁾	V_{CL}	$I_{PP} = 1A, t_p = 8/20\mu s$			11	V
		$I_{PP} = 4A, t_p = 8/20\mu s$			15	V
Junction capacitance	C_J	$V_R = 0V, f = 1MHz$ Pin1 or 2 to Pin3		1.0	1.4	pF
		$V_R = 0V, f = 1MHz$ Between Pin1 and Pin2		0.5	0.7	pF

Notes:

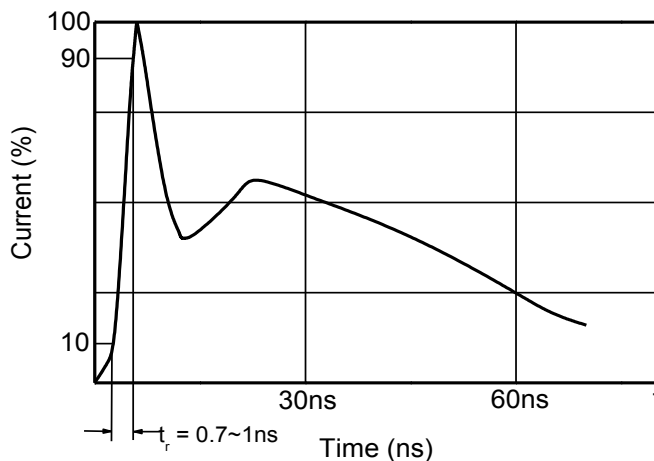
1) TLP parameter: $Z_0 = 50\Omega$, $t_p = 100ns$, $t_r = 2ns$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.

2) Non-repetitive current pulse, according to IEC61000-4-5.

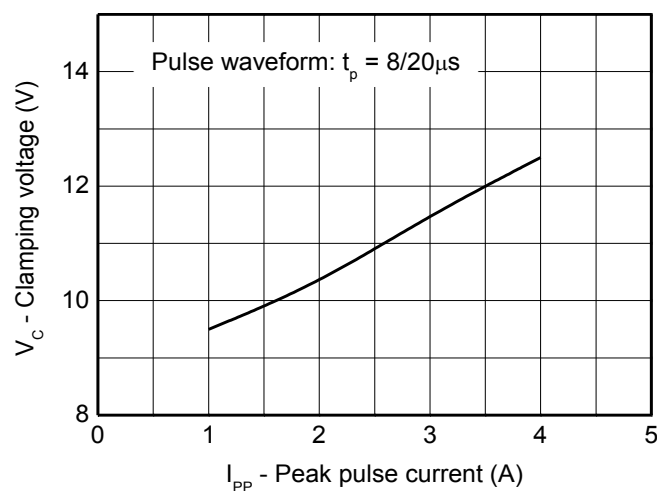
Typical characteristics ($T_A = 25^\circ\text{C}$, unless otherwise noted)



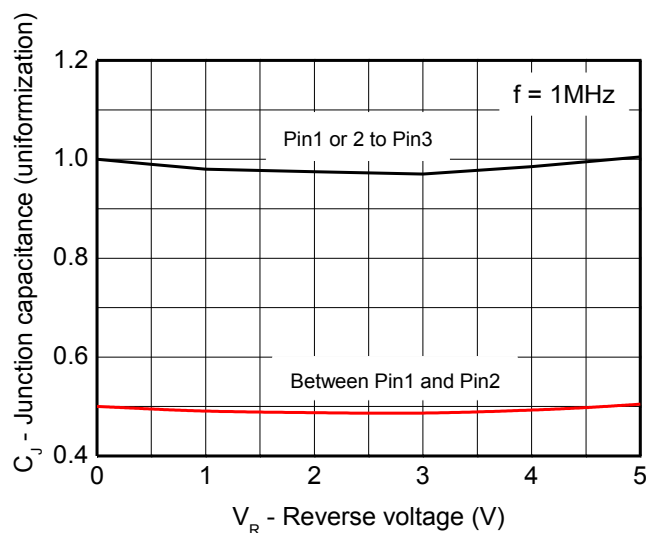
8/20 μs waveform per IEC61000-4-5



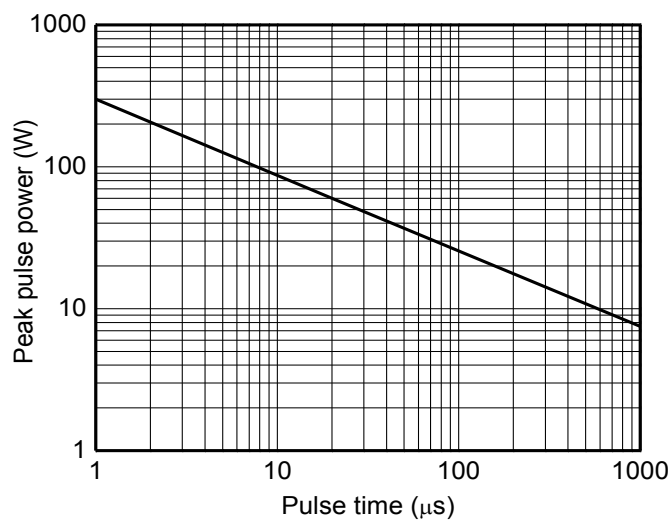
Contact discharge current waveform per IEC61000-4-2



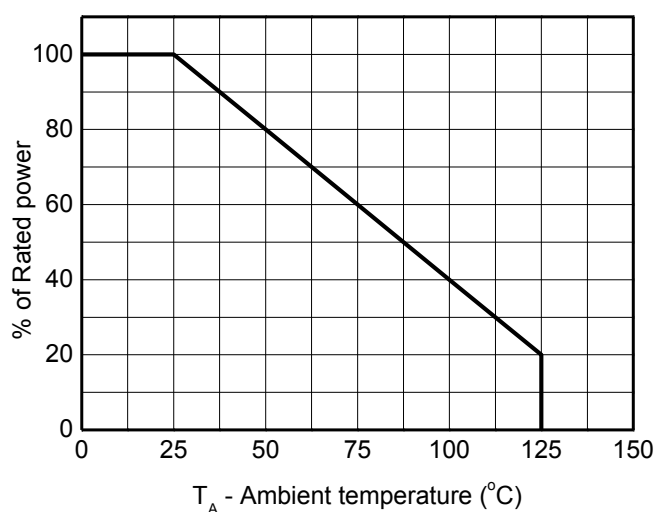
Clamping voltage vs. Peak pulse current



Capacitance vs. Reverse voltage

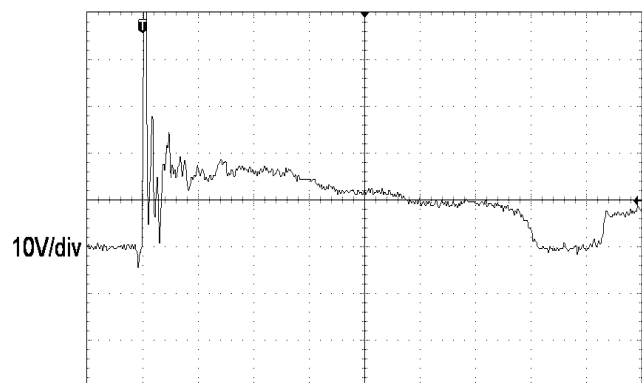


Non-repetitive peak pulse power vs. Pulse time



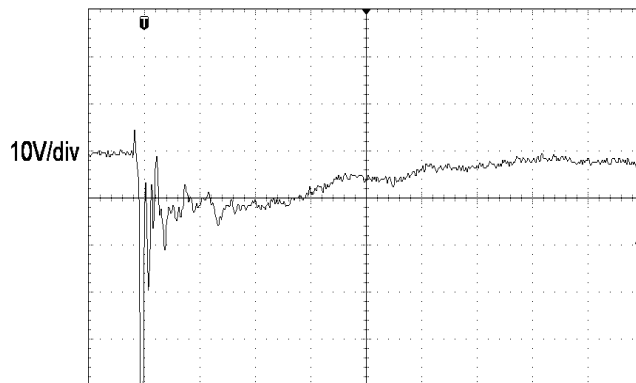
Power derating vs. Ambient temperature

Typical characteristics ($T_A = 25^\circ\text{C}$, unless otherwise noted)



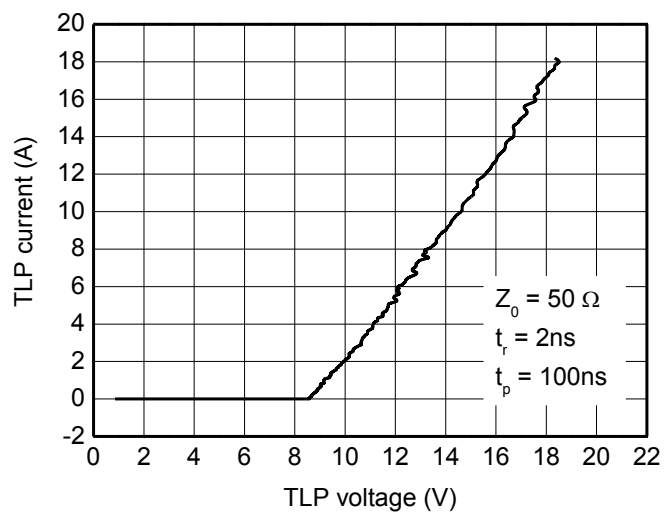
ESD clamping

(+8kV contact discharge per IEC61000-4-2)



ESD clamping

(-8kV contact discharge per IEC61000-4-2)



TLP Measurement

Application Information

The ESD5342N is designed to protect two high speed lines against ESD. Fig1 is shown the connection and Fig2 is shown PCB Layout guide for USB interface ESD protection

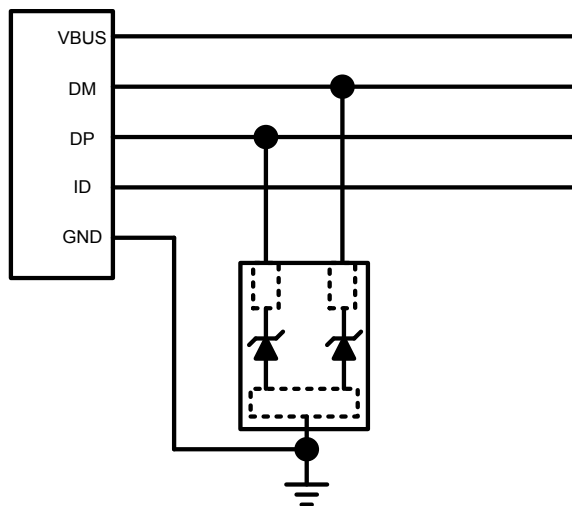


Fig1

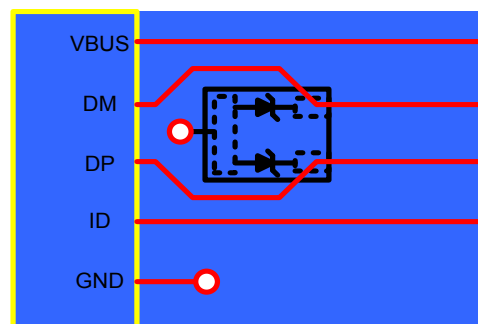
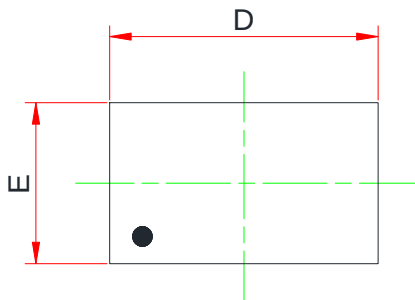


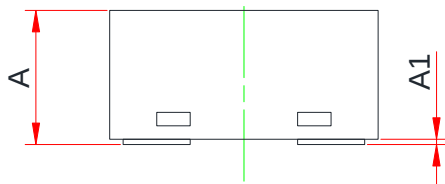
Fig2

Package outline dimensions

DFN1006-3L

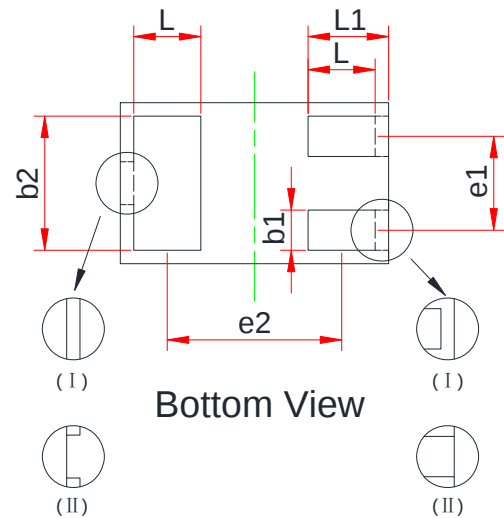
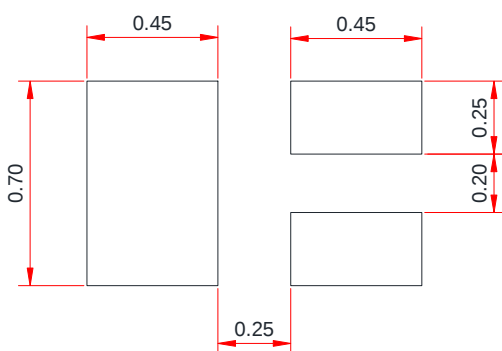


Top View



Side View

Recommend PCB Layout (Unit: mm)



Bottom View

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.36	-	0.50
A1	0.00	-	0.05
D	0.95	1.00	1.05
E	0.55	0.60	0.65
b1	0.10	0.15	0.20
b2	0.40	0.50	0.60
e1	0.35 BSC		
e2	0.65	-	0.675
L	0.20	0.25	0.30
L1	0.20	0.30	0.40

Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.