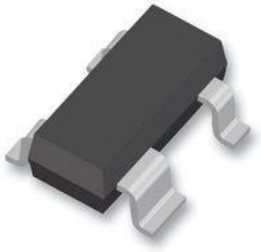
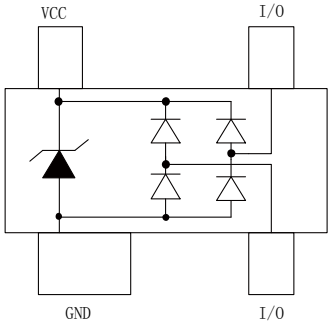
ESD5423B

2-Lines, Uni-directional, Low Capacitance Transient Voltage Suppressor

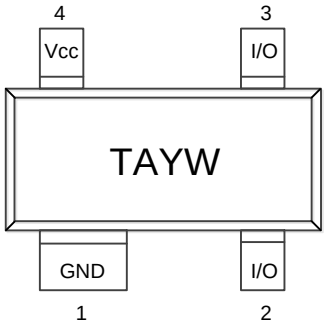
http//:www.sh-willsemi.com



SOT-143



Circuit diagram



TA = Device code
YW = Date code

Marking & Pin configuration (Top View)

Descriptions

The ESD5423B is a low capacitance TVS (Transient Voltage Suppressor) array designed to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-stress caused by ESD (Electrostatic Discharge).

The ESD5423B incorporates two pairs of low capacitance steering diodes plus a TVS diode.

The ESD5423B may be used to provide ESD protection up to ±30kV (contact discharge) according to IEC61000-4-2, and withstand peak pulse current up to 25A (8/20μs) according to IEC61000-4-5.

The ESD5423B is available in SOT-143 package. Standard products are Pb-free and Halogen-free.

Features

- Reverse stand-off voltage: 5V max.
- Transient protection for each line according to
  IEC61000-4-2 (ESD): ±30kV (contact discharge)
  IEC61000-4-5 (surge): 25A (8/20μs)
- Low capacitance: $C_{I/O-GND}$ = 3pF typ.
- Ultra-low leakage current: I_R =20nA typ.
- Low clamping voltage: V_{CL} = 11.2V @ I_{PP} = 16A (TLP)
- Solid-state silicon technology

Applications

- USB 2.0
- Video Graphics Cards
- DVI
- IEEE 1394
- Monitors and Flat Panel Displays
- 10/100 Ethernet
- Notebooks

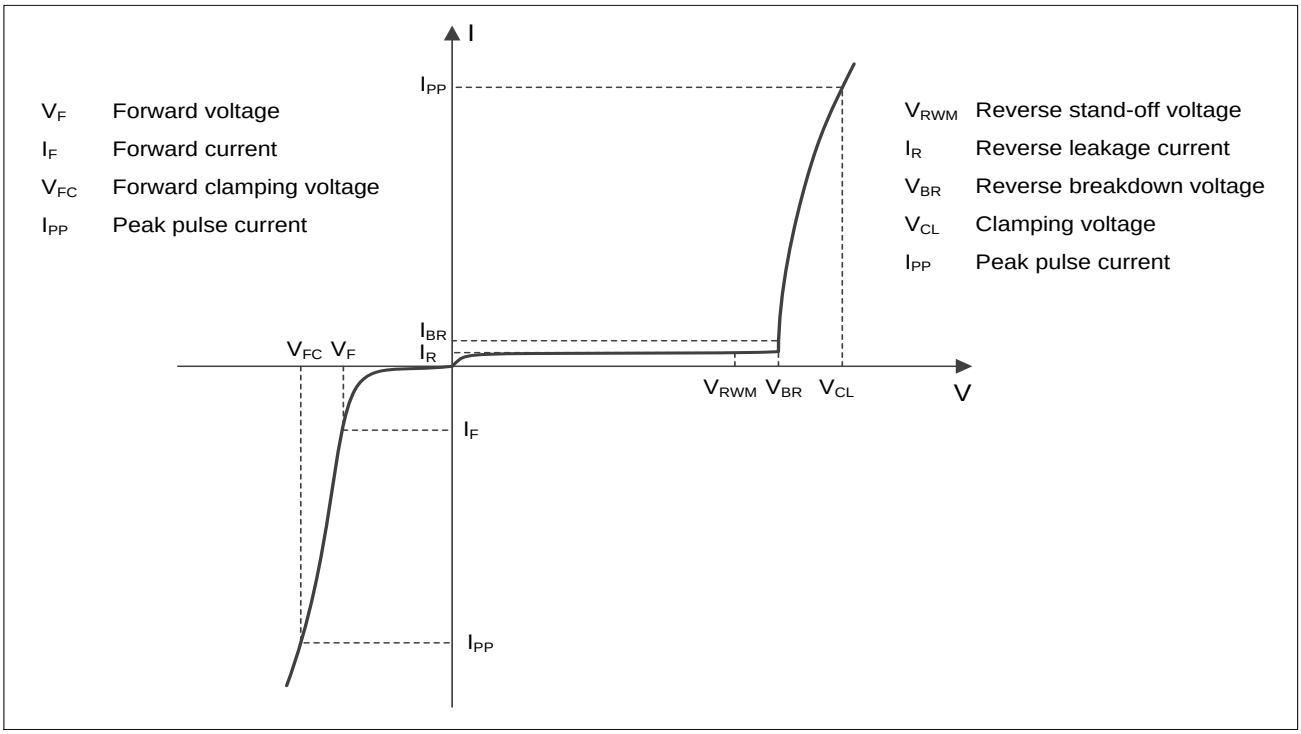
Order information

Device	Package	Shipping
ESD5423B-4/TR	SOT-143	3000/Tape&Reel

Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Peak pulse power (t_p = 8/20μs)	P_{pk}	350	W
Peak pulse current (t_p = 8/20μs)	I_{PP}	25	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	±30	kV
ESD according to IEC61000-4-2 contact discharge		±30	
Junction temperature	T_J	125	°C
Operation temperature	T_{OP}	-40-85	°C
Lead temperature	T_L	260	°C
Storage temperature	T_{STG}	-55~150	°C

Electrical characteristics (T_A = 25°C, unless otherwise noted)



Definitions of electrical characteristics

Electrical characteristics (T_A = 25°C, unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse stand-off voltage	V_{RWM}				5.0	V
Reverse leakage current	I_R	V_{RWM} = 5V			1	uA
Reverse breakdown voltage	V_{BR}	I_{BR} = 1mA	7.0	8.5	9.5	V
Forward voltage	V_F	I_F = 10mA	0.6	0.9	1.2	V
Clamping voltage *1)*	V_{CL}	I_{PP} = 16A, t_p = 100ns		11.2		V
Dynamic resistance *1)*	R_{DYN}	t_p = 100ns		0.11		Ω
Clamping voltage *2)*	V_{CL}	V_{ESD} = 8kV		12		V
Clamping voltage *3)*	V_{CL}	I_{PP} = 1A, t_p = 8/20μs		9.5		V
		I_{PP} = 25A, t_p = 8/20μs		14		V
Dynamic resistance *3)*	R_{DYN}	t_p = 8/20μs		0.19		Ω
Junction capacitance	$C_{I/O - GND}$	V_R = 0V, f = 1MHz, Vcc = floated, Any I/O to GND		3.0	5.0	pF
	$C_{I/O – I/O}$	V_R = 0V, f = 1MHz, Any I/O to I/O		1.5	2.5	pF

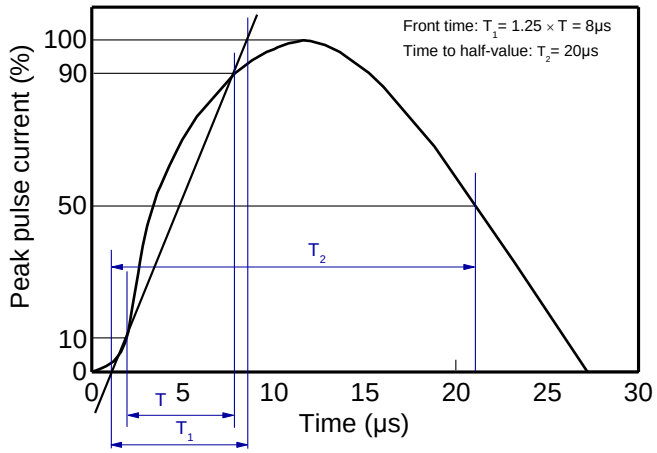
Notes:

1) TLP parameter: Z_0 = 50Ω, t_p = 100ns, t_r = 2ns, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.

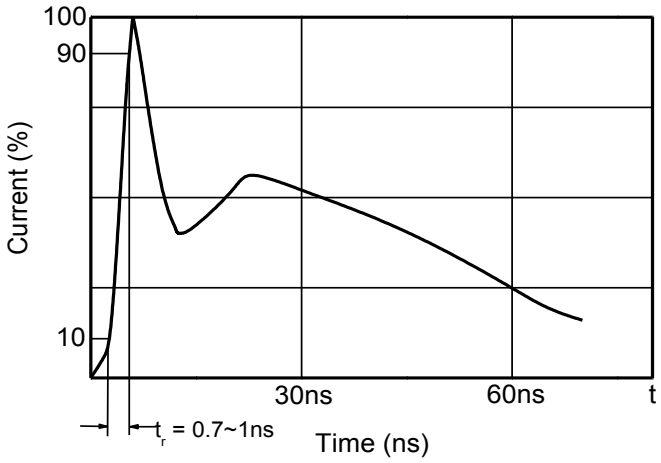
2) Contact discharge mode, according to IEC61000-4-2.

3) Non-repetitive current pulse, according to IEC61000-4-5. R_{DYN} is calculated from 5A to 20A.

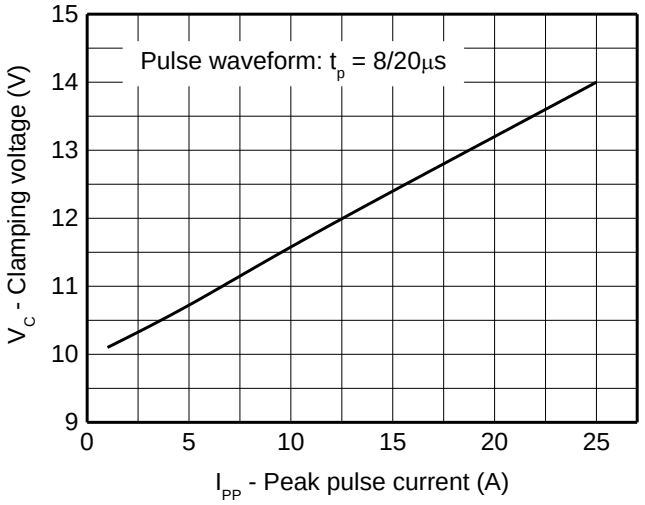
Typical characteristics (T_A = 25°C, unless otherwise noted)



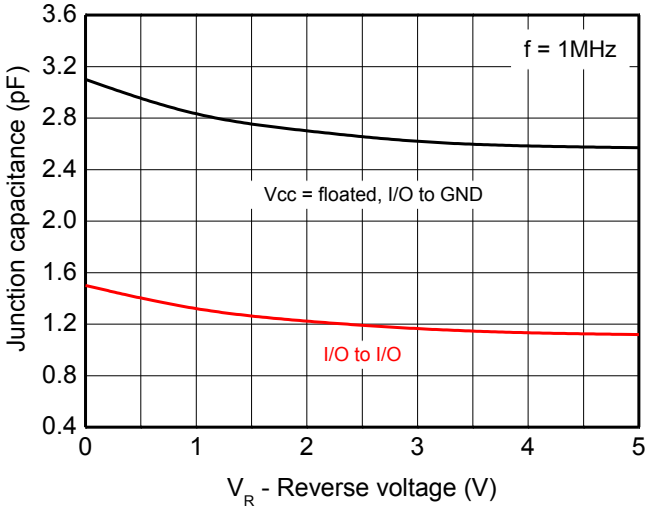
8/20μs waveform per IEC61000-4-5



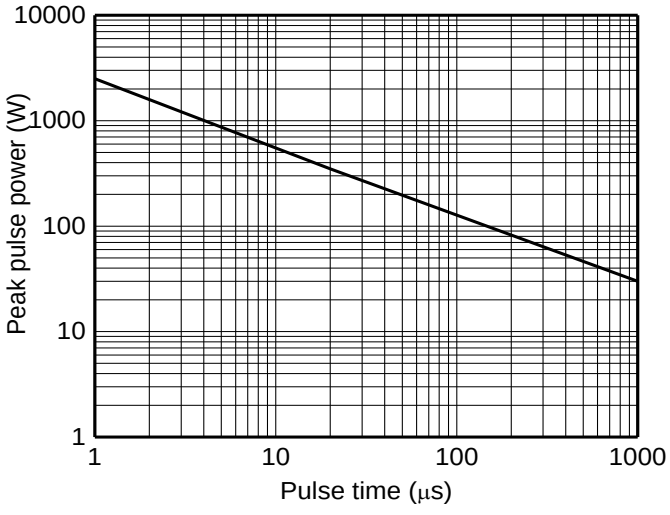
Contact discharge current waveform per IEC61000-4-2



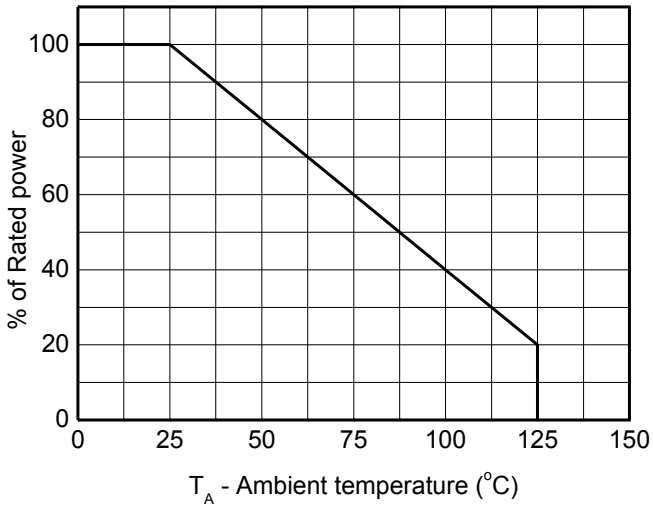
Clamping voltage vs. Peak pulse current



Capacitance vs. Reverse voltage

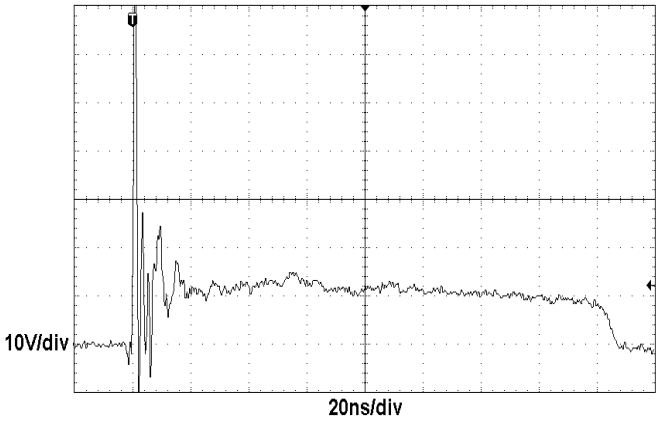


Non-repetitive peak pulse power vs. Pulse time

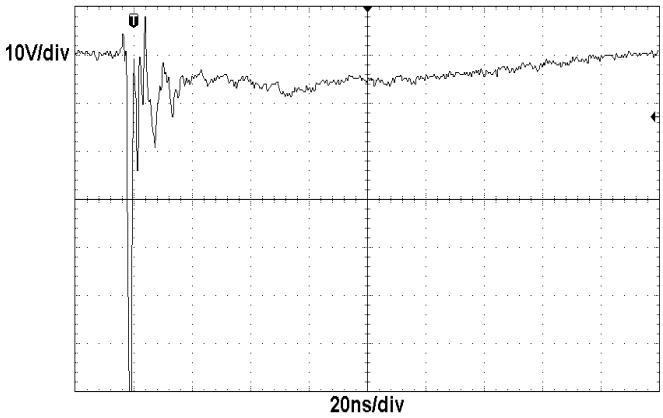


Power derating vs. Ambient temperature

Typical characteristics (T_A = 25°C, unless otherwise noted)



ESD clamping
(+8kV contact discharge per IEC61000-4-2)



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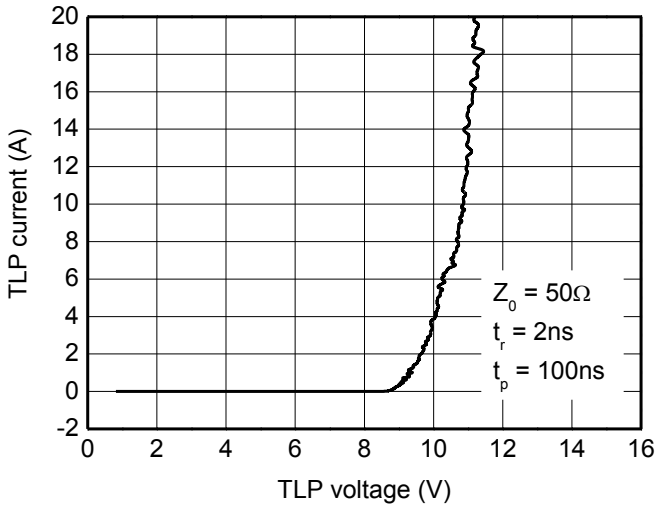
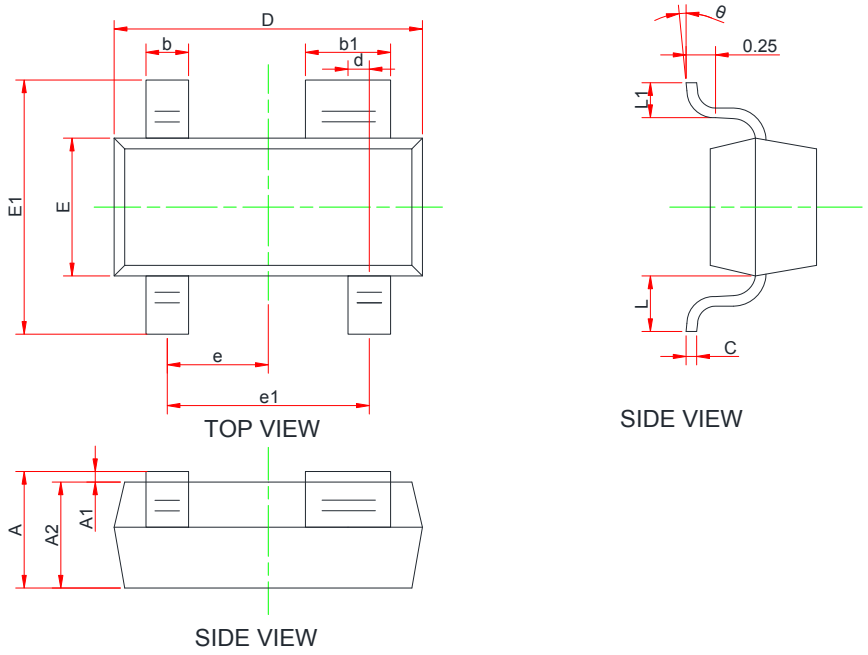
(-8kV contact discharge per IEC61000-4-2)



TLP Measurement

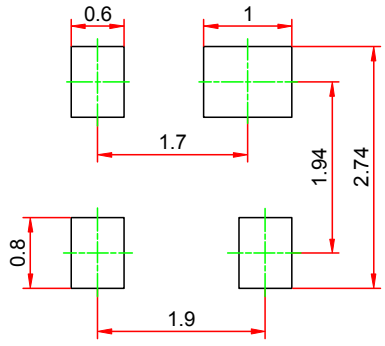
PACKAGE OUTLINE DIMENSIONS

SOT-143



Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.90	-	1.15
A1	0.00	0.05	0.10
A2	0.90	-	1.05
b	0.30	0.40	0.50
b1	0.75	-	0.90
c	0.08	-	0.15
D	2.80	2.90	3.00
d	0.20 Typ.		
E	1.20	1.30	1.40
E1	2.25	2.40	2.55
e	0.95 Typ.		
e1	1.80	1.90	2.00
L	0.55 Ref.		
L1	0.30	0.40	0.50
θ	0 °	-	8 °

Recommend PCB Layout (Unit: mm)

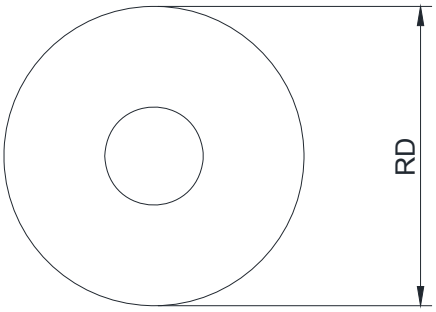


Notes:

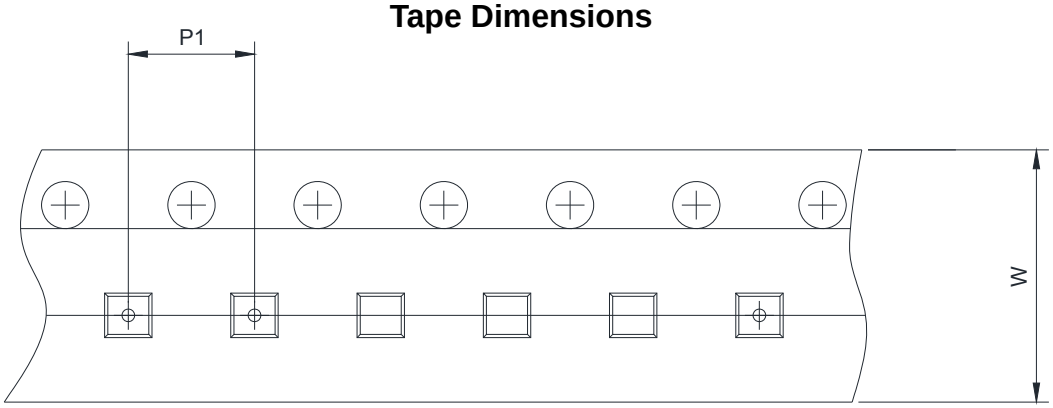
This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

TAPE AND REEL INFORMATION

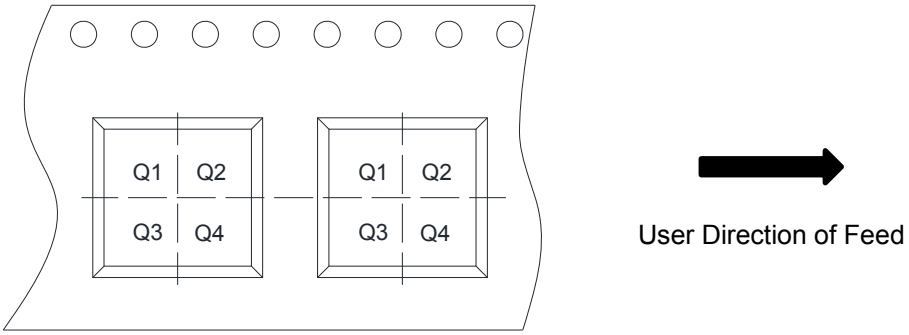
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☐ Q1	☐ Q2	☑ Q3	☐ Q4