

ESD5465E

4-Lines, Uni-directional, Low Capacitance Transient Voltage Suppressors

Descriptions

The ESD5465E is a low capacitance TVS (Transient Voltage Suppressor) array designed to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-stress caused by ESD (Electrostatic Discharge).

The ESD5465E incorporates four pairs of low capacitance steering diodes plus a TVS diode.

The ESD5465E may be used to provide ESD protection up to $\pm 30\text{kV}$ (contact discharge) according to IEC61000-4-2, and withstand peak pulse current up to 40A (5/50ns) according to IEC61000-4-4, 15A (8/20 μs) according to IEC61000-4-5.

The ESD5465E is available in SOT23-6L package. Standard products are Pb-free and Halogen-free.

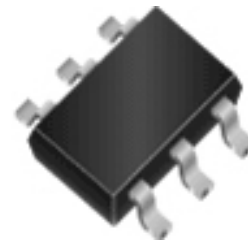
Features

- Reverse stand-off voltage: 5V max.
- Transient protection for each line according to
IEC61000-4-2 (ESD): $\pm 30\text{kV}$ (contact discharge)
IEC61000-4-4 (EFT): 40A (5/50ns, Any I/O to GND)
IEC61000-4-5 (surge): 15A (8/20 μs , Any I/O to GND)
50A (8/20 μs , VDD to GND)
- Low capacitance: $C_{\text{I/O-GND}} = 1.8\text{pF typ.}$
- Ultra-low leakage current: $I_{\text{R}} < 10\text{nA typ.}$
- Low clamping voltage: $V_{\text{CL}} = 13\text{V @ } I_{\text{PP}} = 16\text{A (TLP)}$
- Solid-state silicon technology

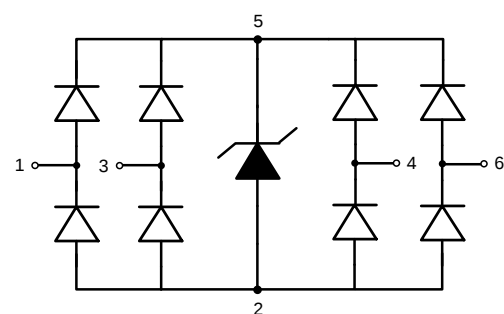
Applications

- USB 2.0
- Video Graphics Cards
- DVI
- IEEE 1394
- Monitors and Flat Panel Displays
- 10/100 Ethernet
- Notebooks

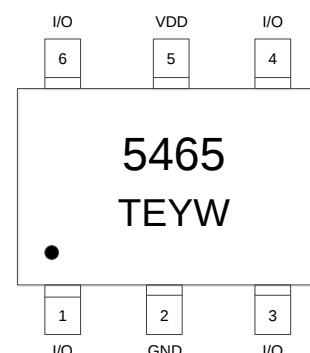
<http://www.sh-willsemi.com>



SOT23-6L



Circuit diagram



5465 = Device code
TE = Special code
YW = Date code

Marking & Pin configuration (Top View)

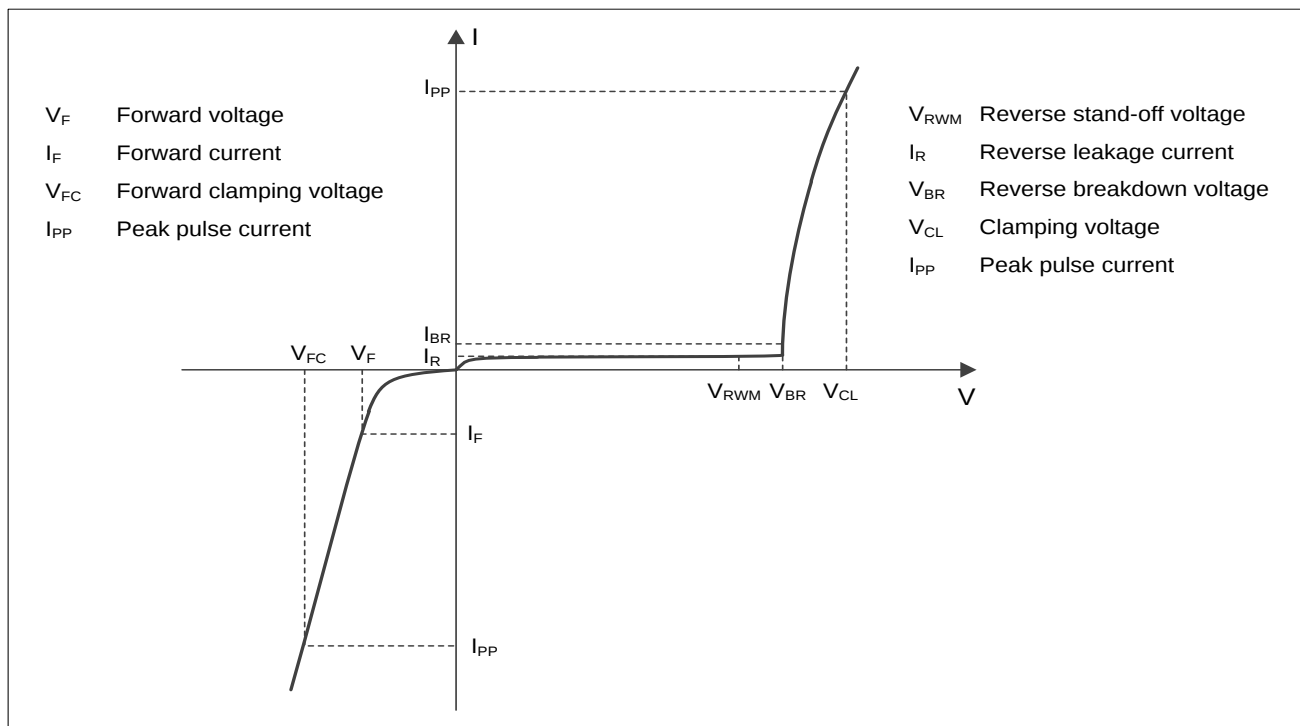
Order information

Device	Package	Shipping
ESD5465E-6/TR	SOT23-6L	3000/Tape&Reel

Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Any IO Pin			
Peak pulse power ($t_p = 8/20\mu s$)	P_{pk}	240	W
Peak pulse current ($t_p = 8/20\mu s$)	I_{pp}	15	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 30	kV
ESD according to IEC61000-4-2 contact discharge		± 30	
Junction temperature	T_J	125	$^{\circ}C$
Operation temperature	T_{OP}	-40 to 85	$^{\circ}C$
Storage temperature	T_{STG}	-55 to 150	$^{\circ}C$
Lead temperature	T_L	260	$^{\circ}C$
VDD Pin			
Peak pulse power ($t_p = 8/20\mu s$)	P_{pk}	900	W
Peak pulse current ($t_p = 8/20\mu s$)	I_{pp}	50	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 30	kV
ESD according to IEC61000-4-2 contact discharge		± 30	
Junction temperature	T_J	125	$^{\circ}C$
Operation temperature	T_{OP}	-40 to 85	$^{\circ}C$
Storage temperature	T_{STG}	-55 to 150	$^{\circ}C$
Lead temperature	T_L	260	$^{\circ}C$

Electrical characteristics ($T_A = 25^{\circ}C$, unless otherwise noted)



Definitions of electrical characteristics

Electrical characteristics ($T_A = 25^\circ\text{C}$, unless otherwise noted)

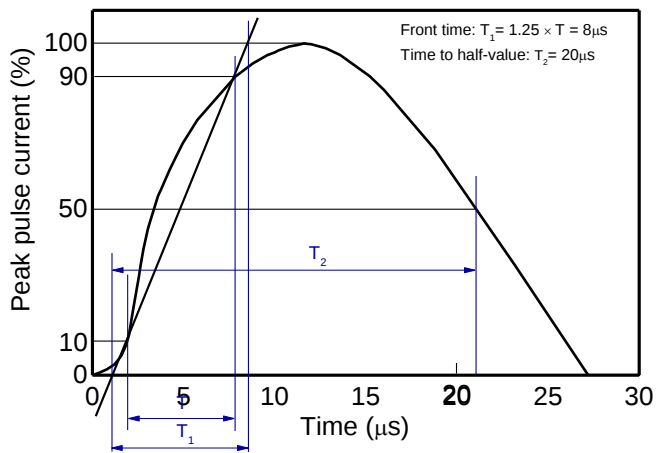
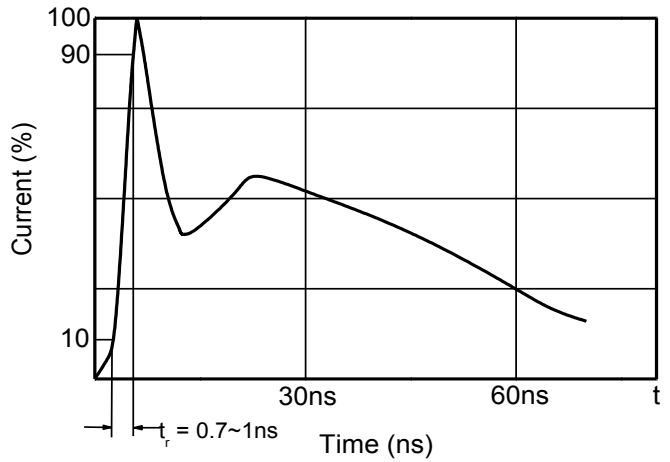
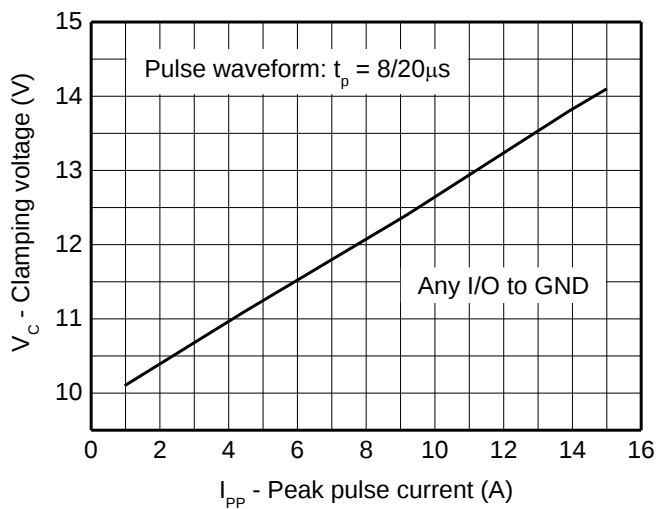
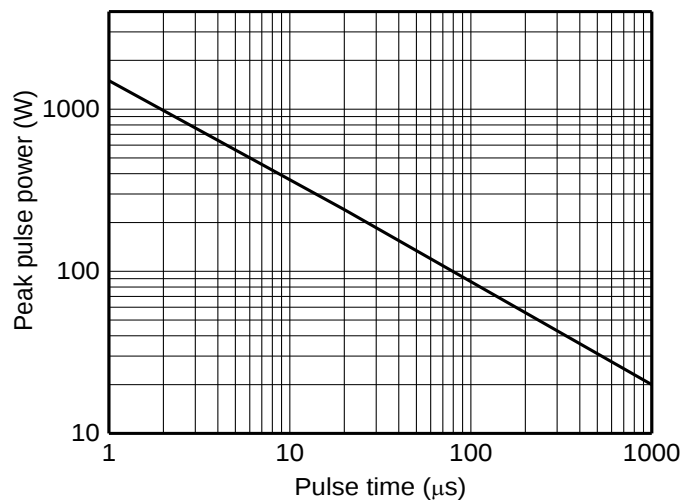
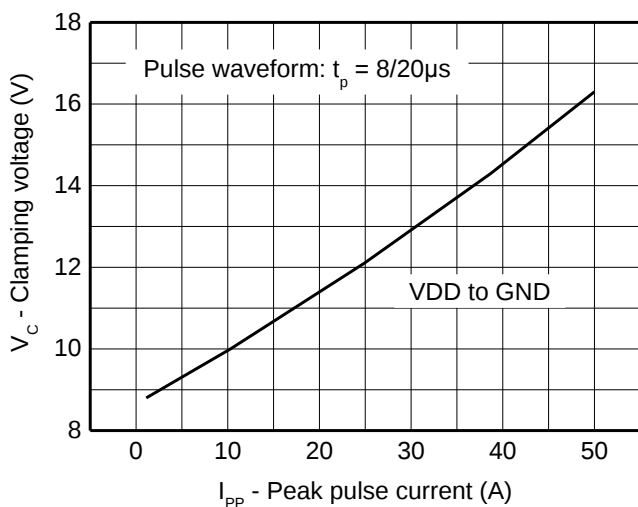
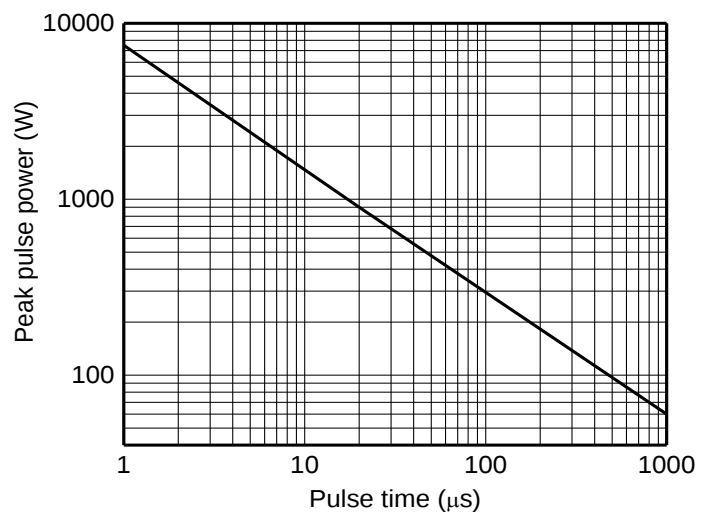
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Any IO Pin						
Reverse stand-off voltage	V_{RWM}				5.0	V
Reverse leakage current	I_R	$V_{RWM} = 5V$		<10	100	nA
Reverse breakdown voltage	V_{BR}	$I_{BR} = 1\text{mA}$	7.0	8.5	10.0	V
Forward voltage	V_F	$I_F = 10\text{mA}$	0.6	0.9	1.2	V
Clamping voltage ¹⁾	V_{CL}	$I_{PP} = 16\text{A}$, $t_p = 100\text{ns}$		13		V
Dynamic resistance ¹⁾	R_{DYN}	$t_p = 100\text{ns}$		0.2		Ω
Clamping voltage ²⁾	V_{CL}	$V_{ESD} = 8\text{kV}$		14		V
Clamping voltage ³⁾	V_{CL}	$I_{PP} = 1\text{A}$, $t_p = 8/20\mu\text{s}$			12	V
		$I_{PP} = 15\text{A}$, $t_p = 8/20\mu\text{s}$			16	V
Junction capacitance	$C_{I/O - GND}$	$V_R = 0V$, $f = 1\text{MHz}$, $V_{DD} = \text{floated}$, any I/O to GND		1.8	3.0	pF
	$C_{I/O - I/O}$	$V_R = 0V$, $f = 1\text{MHz}$, any I/O to I/O		0.9	1.8	pF
VDD Pin						
Reverse stand-off voltage	V_{RWM}				5	V
Reverse leakage current	I_R	$V_{RWM} = 5V$		<10	100	nA
Reverse breakdown voltage	V_{BR}	$I_{BR} = 1\text{mA}$	6.5	8.0	9.5	V
Forward voltage	V_F	$I_F = 10\text{mA}$	0.5	0.8	1.1	V
Clamping voltage ³⁾	V_{CL}	$I_{PP} = 1\text{A}$, $t_p = 8/20\mu\text{s}$			10	V
		$I_{PP} = 50\text{A}$, $t_p = 8/20\mu\text{s}$			18	V
Junction capacitance	C_J	$V_R = 0V$, $f = 1\text{MHz}$, V_{DD} to GND		300	450	pF

Notes:

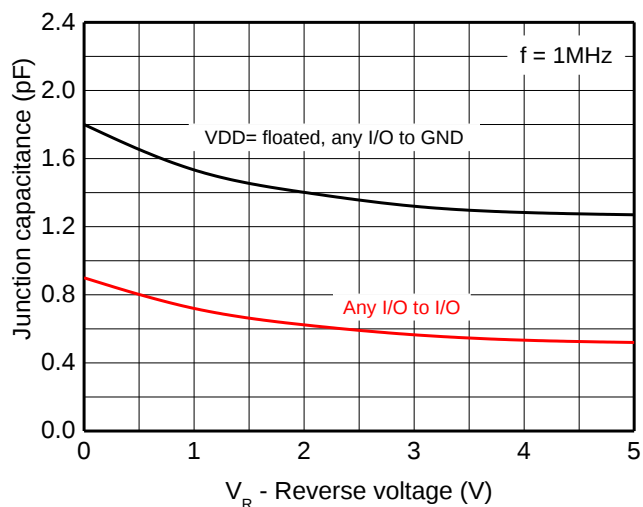
1) TLP parameter: $Z_0 = 50\Omega$, $t_p = 100\text{ns}$, $t_r = 2\text{ns}$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.

2) Contact discharge mode, according to IEC61000-4-2.

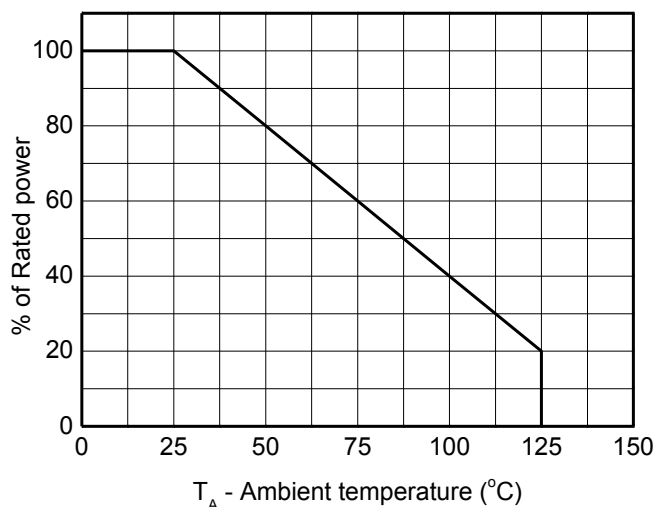
3) Non-repetitive current pulse, according to IEC61000-4-5.

Typical characteristics ($T_A = 25^\circ\text{C}$, unless otherwise noted)

8/20 μs waveform per IEC61000-4-5

Contact discharge current waveform per IEC61000-4-2

**Clamping voltage vs. Peak pulse current
(Any IO Pin)**

**Non-repetitive peak pulse power vs. Pulse time
(Any IO Pin)**

**Clamping voltage vs. Peak pulse current
(VDD Pin)**

**Non-repetitive peak pulse power vs. Pulse time
(VDD Pin)**

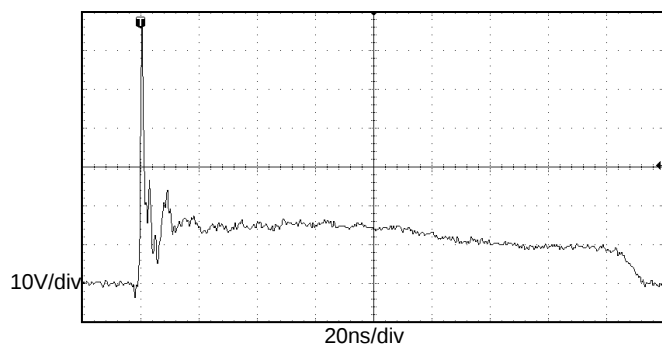
Typical characteristics ($T_A = 25^\circ\text{C}$, unless otherwise noted)



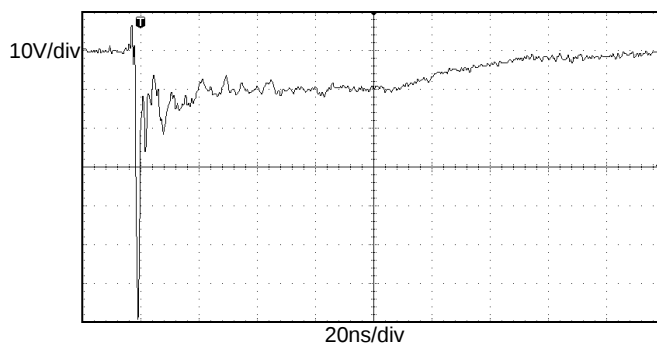
Capacitance vs. Reverse voltage
(Any IO Pin)



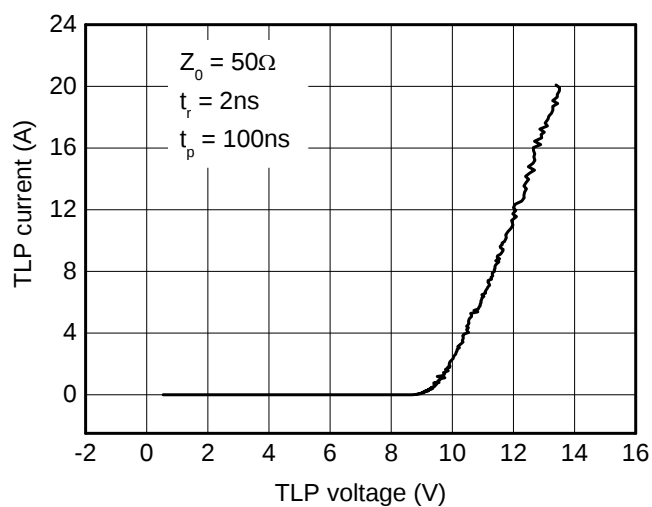
Power derating vs. Ambient temperature



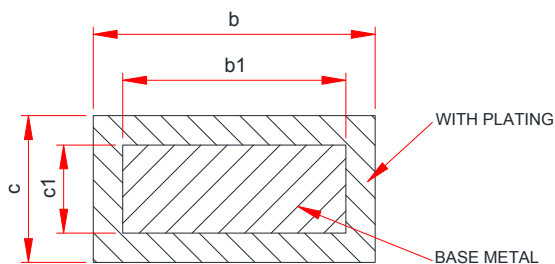
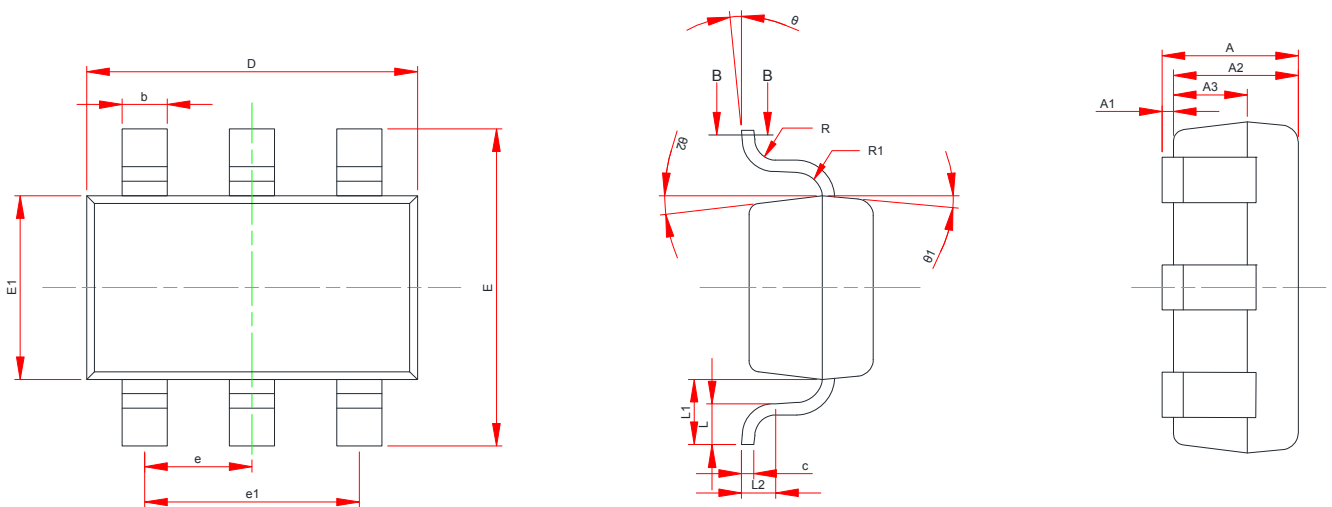
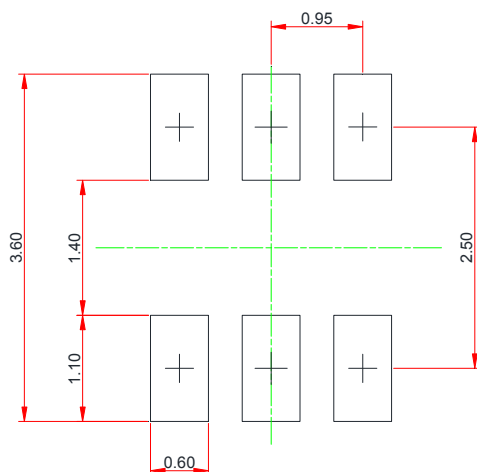
ESD clamping
(+8kV contact discharge per IEC61000-4-2)
(Any IO Pin)



ESD clamping
(-8kV contact discharge per IEC61000-4-2)
(Any IO Pin)



TLP Measurement
(Any IO Pin)

Package outline dimensions
SOT23-6L

SECTION B-B
Recommended land pattern (Unit: mm)

Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

Symbol	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	--	--	1.250
A1	0.000	--	0.150
A2	1.000	1.100	1.200
A3	0.600	0.650	0.700
b	0.360	--	0.500
b1	0.360	0.380	0.450
c	0.140	--	0.200
c1	0.140	0.150	0.160
D	2.826	2.926	3.026
E	2.600	2.800	3.000
E1	1.526	1.626	1.726
e	0.900	0.950	1.000
e1	1.800	1.900	2.000
L	0.350	0.450	0.600
L1	0.590REF		
L2	0.250BSC		
R	0.100	--	--
R1	0.100	--	0.200
θ	0°	--	8°
θ1	3°	5°	7°
θ2	6°	--	14°