ESD Protection Diode

Low Capacitance ESD Protection Diode for High Speed Data Line

ESD7361, SZESD7361

The ESD7361 Series ESD protection diodes are designed to protect high speed data lines from ESD. Ultra−low capacitance make this device an ideal solution for protecting voltage sensitive high speed data lines.

Features

- Low Capacitance (0.55 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
  - IEC61000−4−2 (ESD): Level 4 ±15 kV Contact
  - IEC61000−4−4 (EFT): 40 A −5/50 ns
  - IEC61000−4−5 (Lightning): 1 A (8/20 μs)
- ISO 10605 (ESD) 330 pF/2 kΩ ±15 kV Contact
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

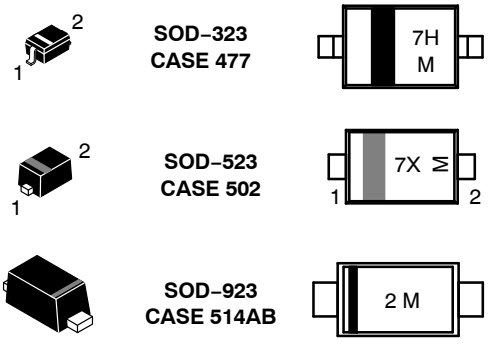
- Wireless Charger
- Near Field Communications

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD) ISO 10605 330 pF/2 kΩ Contact (ESD)	ESD ESD ESD	±15 ±15 ±15	kV kV kV

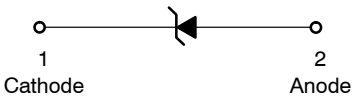
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAMS



X, XX = Specific Device Code
M = Date Code

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

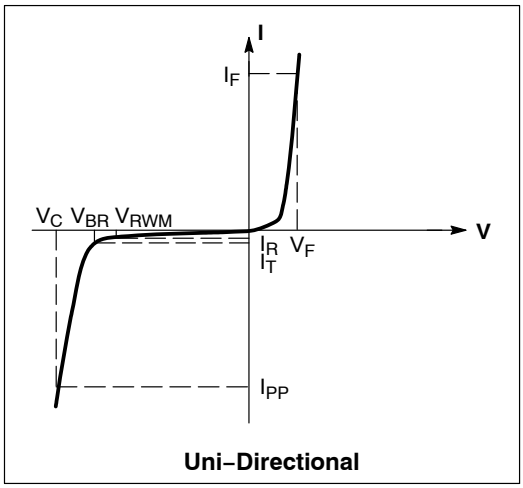
See detailed ordering and shipping information on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni−Directional

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}			5	16	V
Breakdown Voltage	V_{BR}	I_T = 1 mA; pin 1 to pin 2	16.5			V
Reverse Leakage Current	I_R	V_{RWM} = 5.0 V V_{RWM} = 15 V		<1 20	1000 1000	nA nA
Clamping Voltage (Note 2)	V_C	I_{PP} = 8 A		31		V
Clamping Voltage (Note 2)	V_C	I_{PP} = 16 A		34		V
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz V_R = 0 V, f < 1 GHz			0.55 0.55	pF
Dynamic Resistance	R_{DYN}	TLP Pulse		0.735		Ω
Insertion Loss		f = 1 MHz f = 5 GHz		0.01 2		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For test procedure see Figures 9 and 10 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

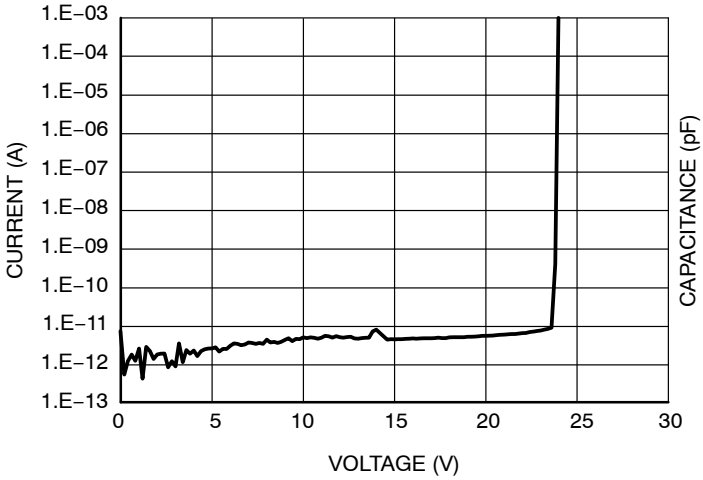


Figure 1. Typical IV Characteristics

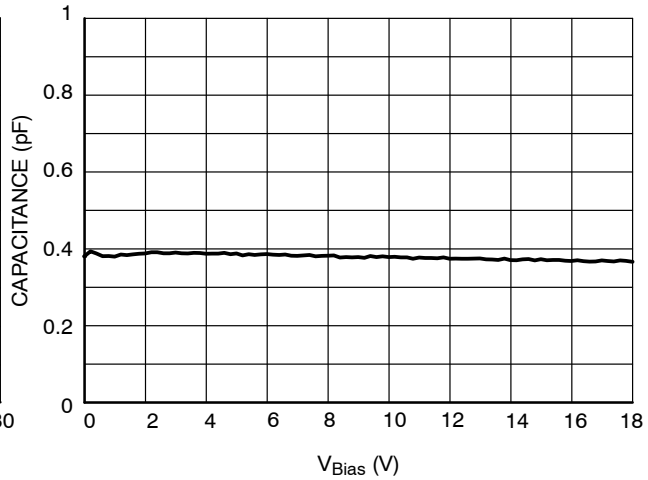


Figure 2. Typical CV Characteristics

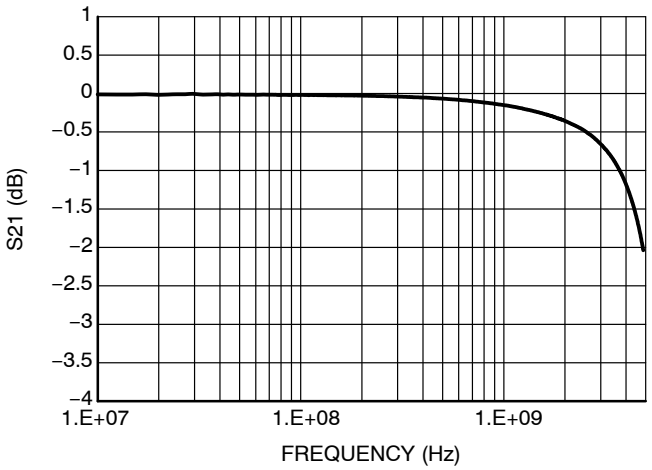


Figure 3. Typical Insertion Loss
ESD7361HT1G (SOD323)

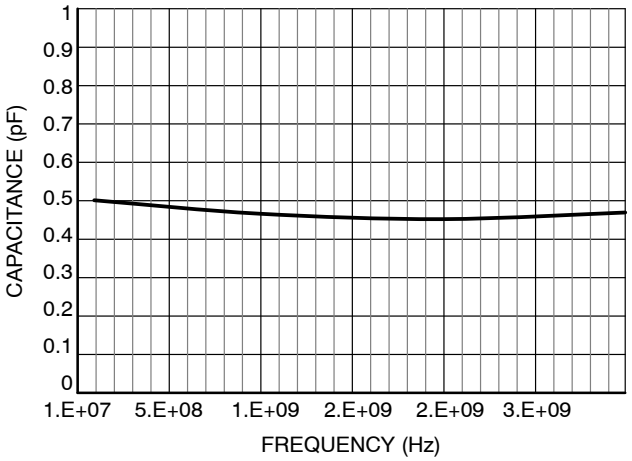


Figure 4. Typical Capacitance Over Frequency
ESD7361HT1G (SOD323)

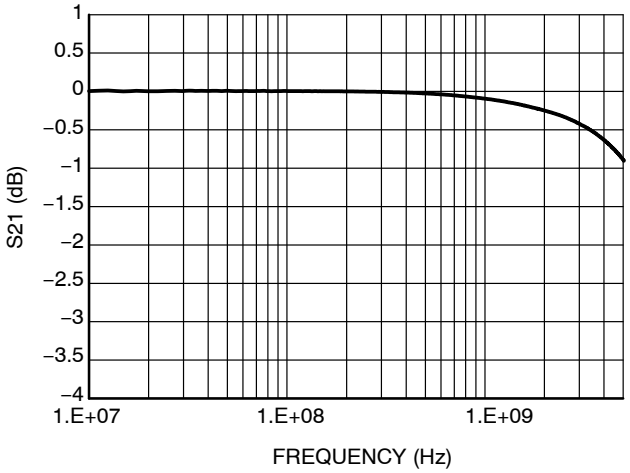


Figure 5. Typical Insertion Loss
ESD7361XV2T1G (SOD523)

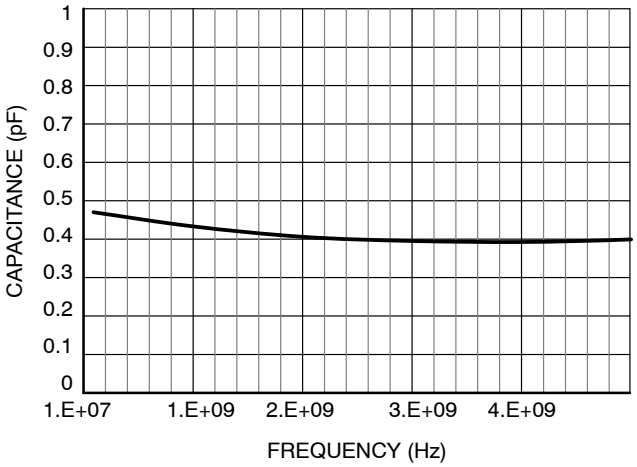


Figure 6. Typical Capacitance Over Frequency
ESD7361XV2T1G (SOD523)

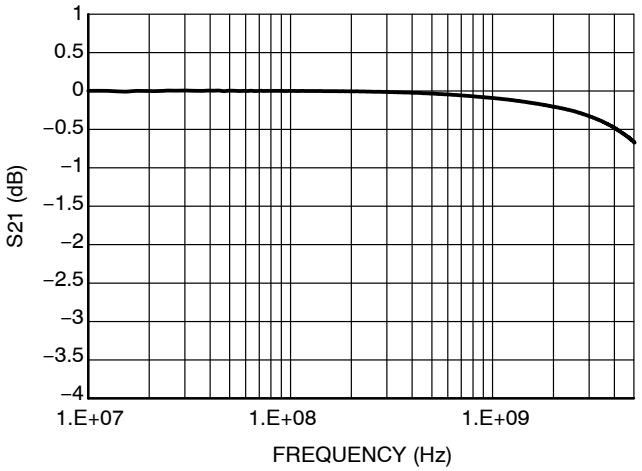


Figure 7. Typical Insertion Loss
ESD7361P2T5G (SOD923)

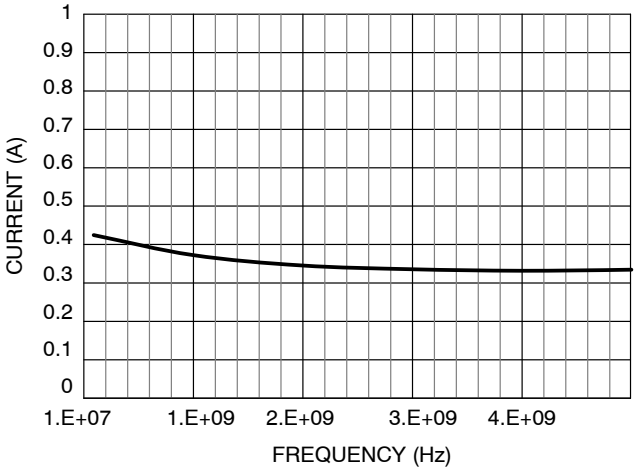


Figure 8. Typical Capacitance Over Frequency
ESD7361P2T5G (SOD923)

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

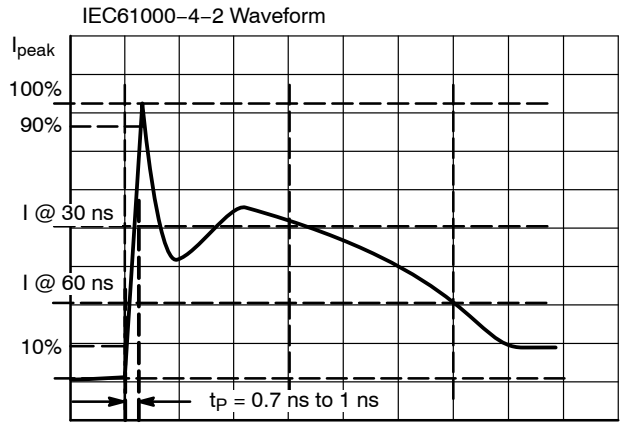


Figure 9. IEC61000−4−2 Spec

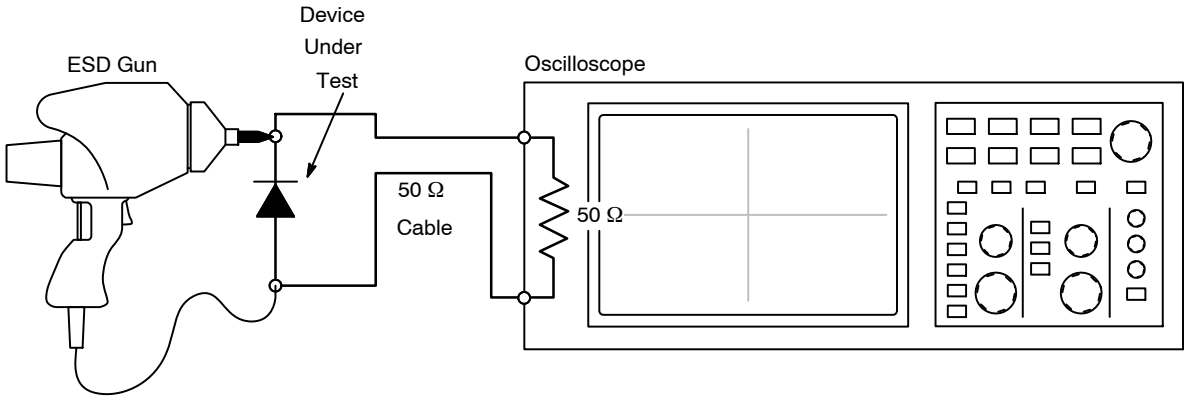


Figure 10. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

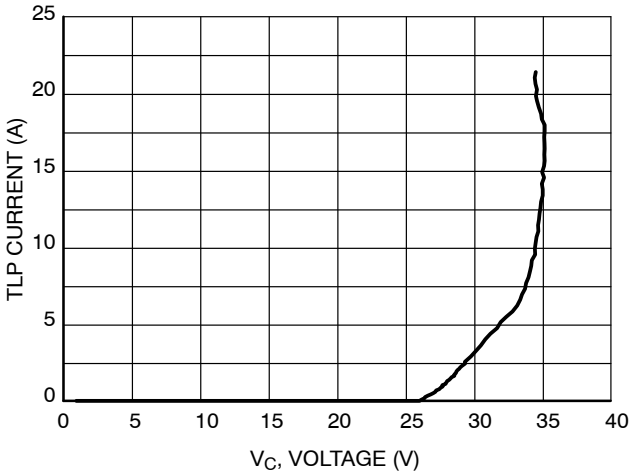


Figure 11. Positive TLP I–V Curve

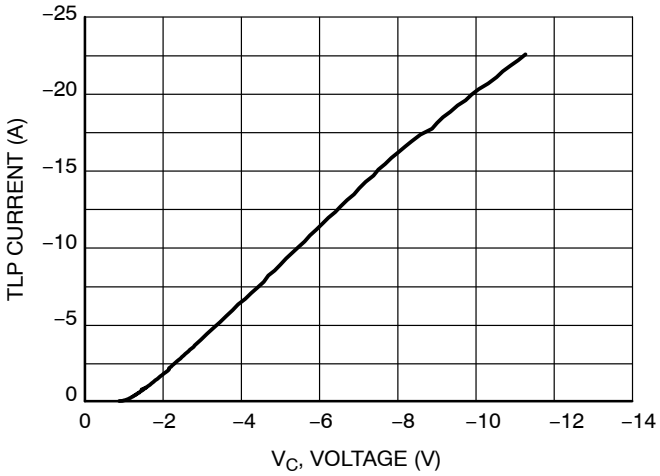


Figure 12. Negative TLP I–V Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns. V_{IEC} is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000−4−2 waveform at t = 30 ns with 2 A/kV. See TLP description below for more information.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 13. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 14 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

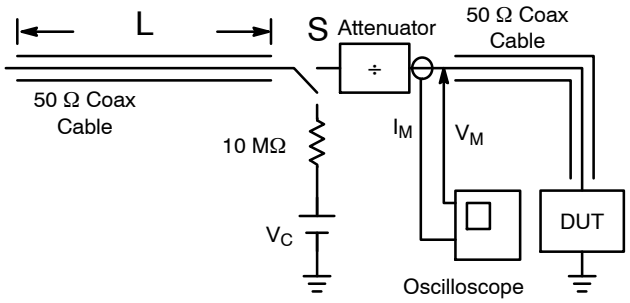


Figure 13. Simplified Schematic of a Typical TLP System

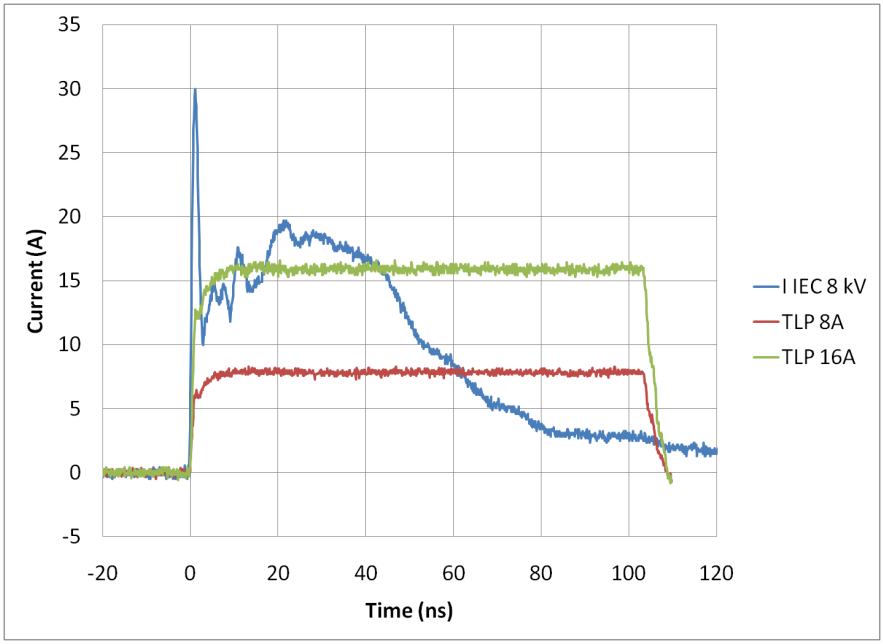


Figure 14. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

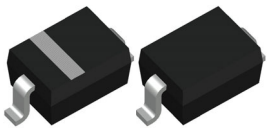
ORDERING INFORMATION

Device	Package	Shipping†
ESD7361HT1G	SOD−323 (Pb−Free)	3000 / Tape & Reel
SZESD7361HT1G*		
ESD7361XV2T1G	SOD−523 (Pb−Free)	3000 / Tape & Reel
SZESD7361XV2T1G*		
ESD7361XV2T5G		8000 / Tape & Reel
SZESD7361XV2T5G*		
ESD7361P2T5G	SOD−923 (Pb−Free)	8000 / Tape & Reel
SZESD7361P2T5G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

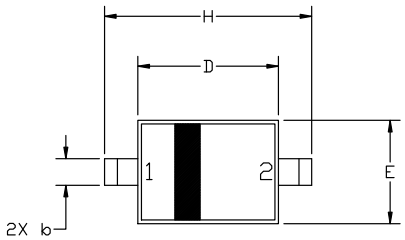
*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

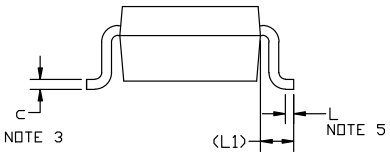


SOD−323 1.70x1.25x0.85
CASE 477
ISSUE J

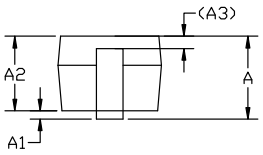
DATE 15 FEB 2024



TOP VIEW



SIDE VIEW

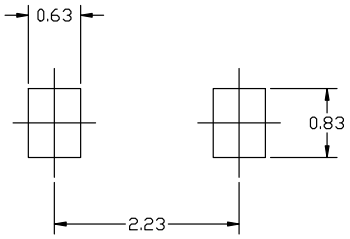


END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS SPECIFIED PER L/F DRAWING WITH SOLDER PLATING.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DIMENSION L IS MEASURE FROM END OF RADIUS.

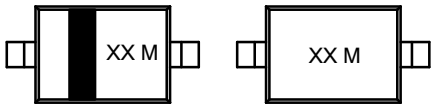
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.05	0.10
A2	0.75	0.85	0.95
A3	0.15 (REF)		
b	0.25	0.32	0.4
c	0.09	0.12	0.18
D	1.60	1.70	1.80
E	1.15	1.25	1.35
H	1.50	1.60	1.70
L	0.08	---	---
L1	0.40 (REF)		



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



STYLE 1 STYLE 2

XX = Specific Device Code
M = Date Code

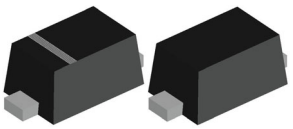
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

STYLE 2:
NO POLARITY

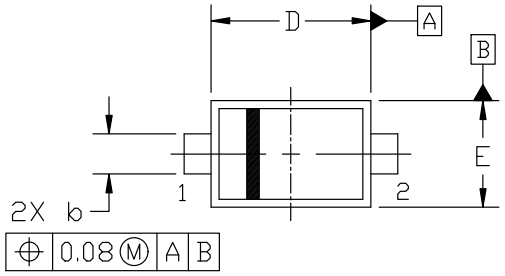
DOCUMENT NUMBER:	98ASB17533C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	SOD−323 1.70x1.25x0.85	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

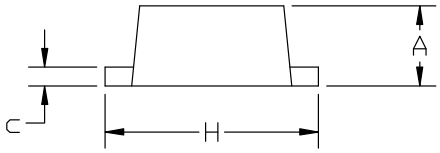


SOD−523 1.20x0.80x0.60
CASE 502
ISSUE F

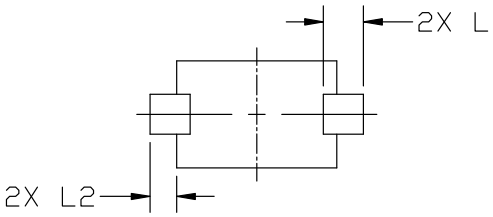
DATE 08 FEB 2024



TOP VIEW



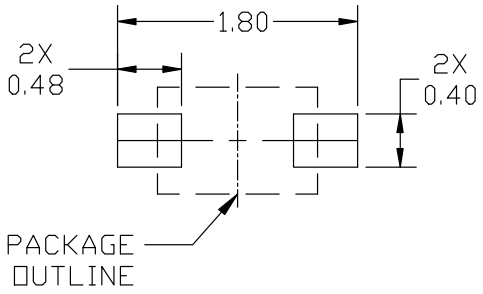
SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH, MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.50	0.60	0.70
b	0.25	0.30	0.35
c	0.07	0.14	0.20
D	1.10	1.20	1.30
E	0.70	0.80	0.90
H	1.50	1.60	1.70
L	0.30 REF		
L2	0.15	0.20	0.25



RECOMMENDED MOUNTING FOOTPRINT

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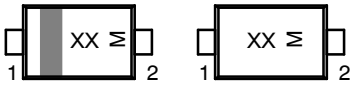
GENERIC MARKING DIAGRAM*



STYLE 1 STYLE 2

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M = Date Code

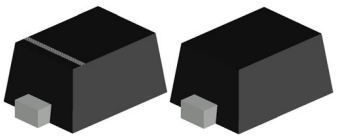
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

STYLE 2:
NO POLARITY

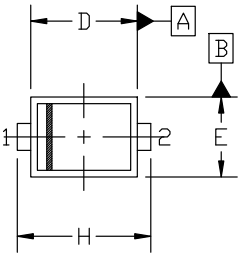
DOCUMENT NUMBER:	**98AON11524D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOD−523 1.20x0.80x0.60**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

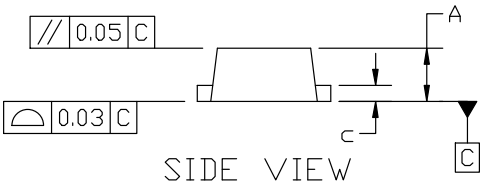


SOD−923 0.80x0.60x0.37
CASE 514AB
ISSUE E

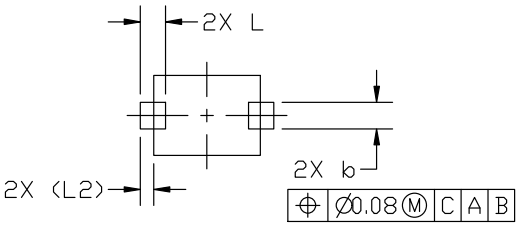
DATE 08 FEB 2024



TOP VIEW



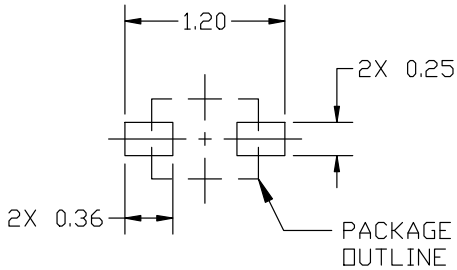
SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. DIMENSION L WILL NOT EXCEED 0.30mm.

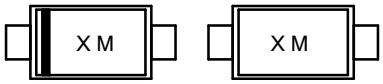
MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
b	0.15	0.20	0.25
c	0.07	0.12	0.17
D	0.75	0.80	0.85
E	0.55	0.60	0.65
H	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



STYLE 1 STYLE 2

X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

STYLE 2:
NO POLARITY

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DESCRIPTION:	**SOD−923 0.80x0.60x0.37**		**PAGE 1 OF 1**

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