ESD7471, SZESD7471

Ultra-Low Capacitance ESD Protection

Micro−Packaged Diodes for ESD Protection

The ESD7471 is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, high breakdown voltage, high linearity, low leakage, and fast response time make these parts ideal for ESD protection on designs where board space is at a premium. It has industry leading capacitance linearity over voltage making it ideal for RF applications. This capacitance linearity combined with the extremely small package and low insertion loss makes this part well suited for use in antenna line applications for wireless handsets and terminals.

Features

- Industry Leading Capacitance Linearity Over Voltage
- Ultra−Low Capacitance: 0.35 pF Max
- Stand−off Voltage: 5.3 V
- Low Leakage: < 1 nA
- Low Dynamic Resistance: < 1 Ω
- IEC61000−4−2 Level 4 ESD Protection
- 1000 ESD IEC61000−4−2 Strikes ±8 kV Contact / Air Discharged
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- RF Signal ESD Protection
- RF Switching, PA, and Antenna ESD Protection
- Near Field Communications
- USB 2.0, USB 3.0

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
IEC 61000−4−2 Contact (ESD) (Note 1) IEC 61000−4−2 Air (ESD) (Note 1)	ESD ESD	±20 ±20	KV kV
IEC 61000−4−5 (ESD) (Note 2)	ESD	2.2	A
Total Power Dissipation (Note 3) @ T_A = 25°C Thermal Resistance, Junction−to−Ambient	P_D $R_{\theta JA}$	300 400	mW °C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. At least 10 discharges at T_A = 25°C, per IEC61000−4−2 waveform.
2. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−5 waveform.
3. Mounted with recommended minimum pad size, DC board FR−4

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

XDFN2
CASE 711AM

D = Specific Device Code
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
ESD7471N2T5G	XDFN2 (Pb−Free)	8000 / Tape & Reel
SZESD7471N2T5G	XDFN2 (Pb−Free)	8000 / Tape & Reel

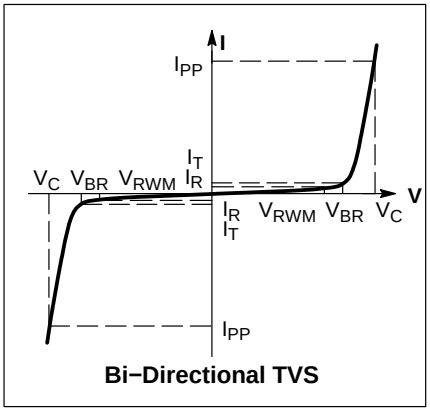
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional TVS

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}				5.3	V
Breakdown Voltage	V_{BR}	I_T = 1 mA (Note 4)	7.0			V
Reverse Leakage Current	I_R	V_{RWM} = 5.3 V		< 1	50	nA
Clamping Voltage	V_C	I_{PP} = 1 A (Note 5)		13	15	V
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz V_R = 0 V, f = 1 GHz		0.24 0.24	0.35 0.35	pF
Dynamic Resistance	R_{DYN}	TLP Pulse		0.8		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
5. Non−repetitive current pulse at 25°C, per IEC61000−4−5 waveform.

TYPICAL CHARACTERISTICS

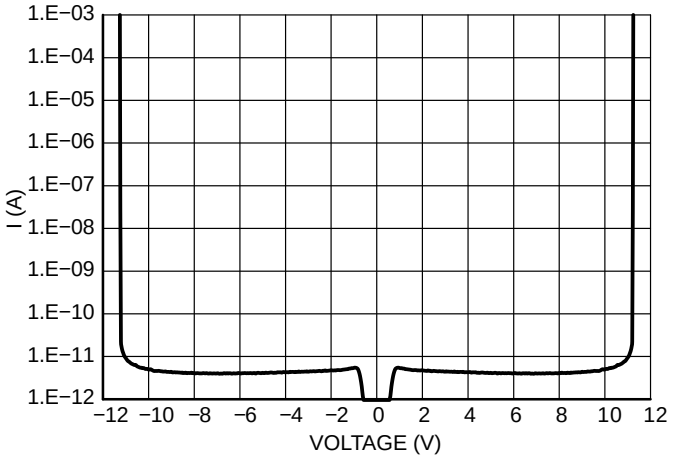


Figure 1. IV Characteristics

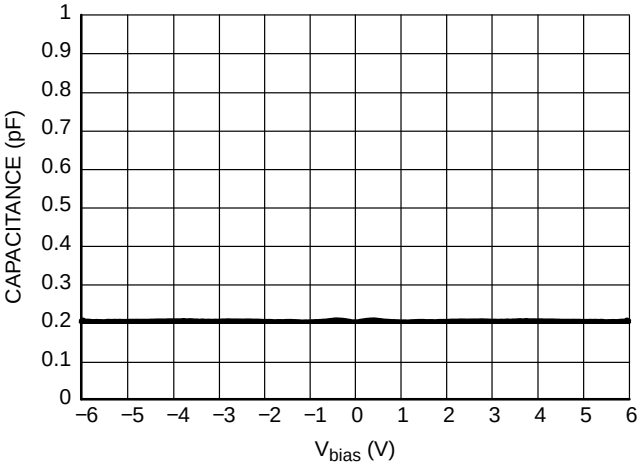


Figure 2. CV Characteristics

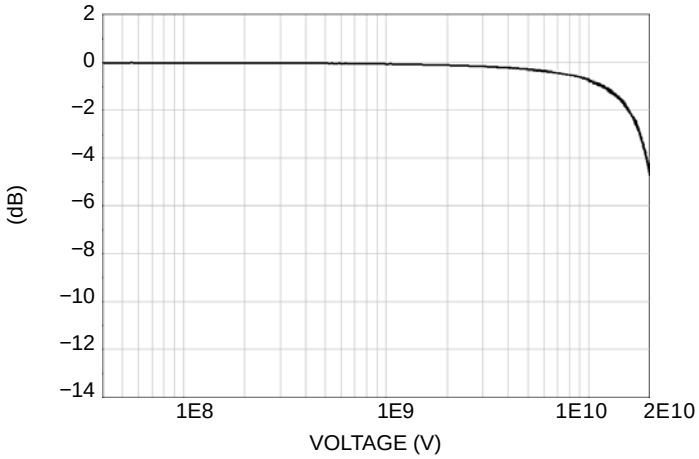


Figure 3. RF Insertion Loss

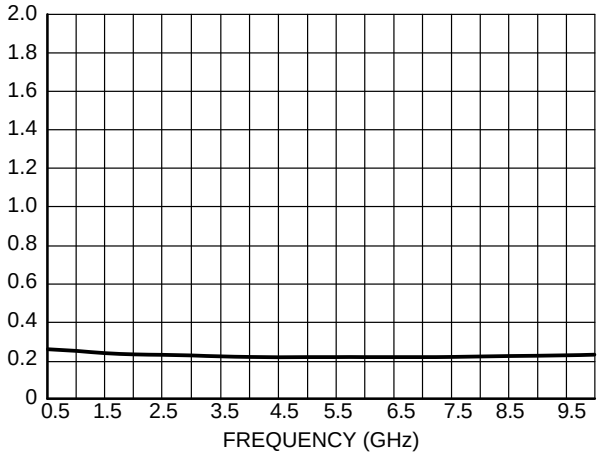


Figure 4. Capacitance over Frequency

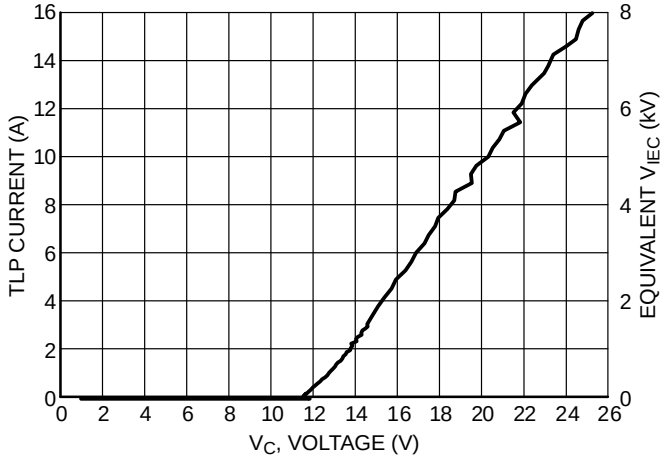


Figure 5. Positive TLP I−V Curve

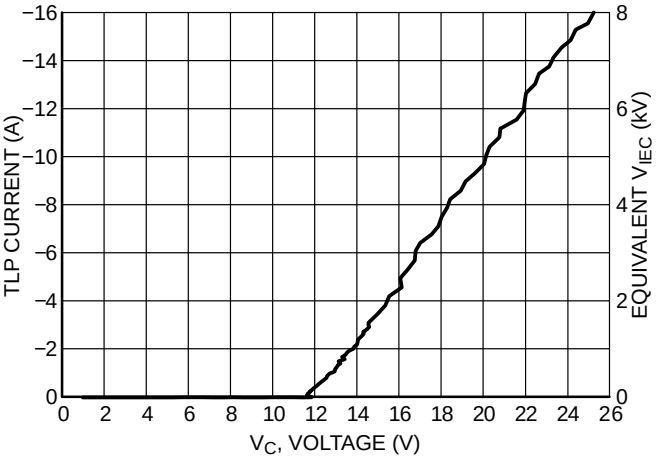
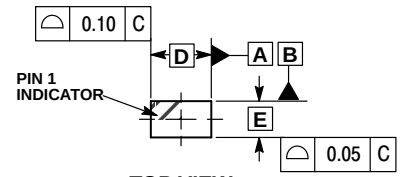


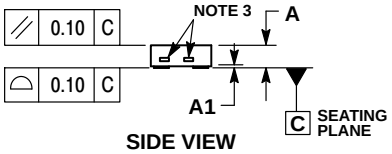
Figure 6. Negative TLP I−V Curve

PACKAGE DIMENSIONS

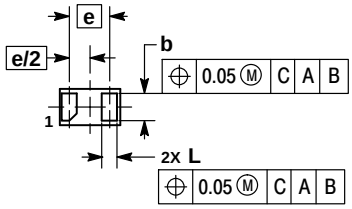
XDFN2 1.0x0.6, 0.65P (SOD−882)
CASE 711AM
ISSUE O



TOP VIEW



SIDE VIEW

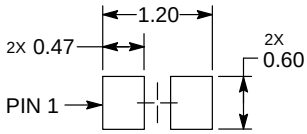


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

	MILLIMETERS	
DIM	MIN	MAX
A	0.34	0.44
A1	−−−	0.05
b	0.43	0.53
D	1.00 BSC	
E	0.60 BSC	
e	0.65 BSC	
L	0.20	0.30

RECOMMENDED SOLDER FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
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ESD7471/D