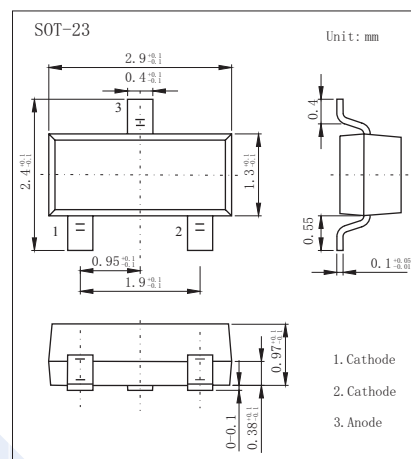
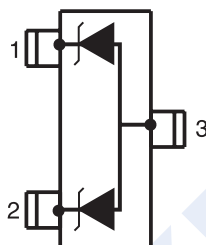


ESD Protection Diodes

ESDAxxL

■ Features

- 2 Unidirectional Transil Functions.
- Low Leakage Current: $I_{Rmax} < 20\mu A$ at V_{BR} .
- 300 W Peak Pulse Power(8/20 μs)
- High integration.
- Suitable for high density boards.

■ Absolute Maximum Ratings ($T_a = 25^\circ C$)

Parameter	Symbol	Value	Unit	
Electrostatic discharge	V _{PP}	MIL STD 883C-Method 3015-6	25	kV
		IEC61000-4-2 air discharge	16	
		IEC61000-4-2 contact discharge	9	
Peak pulse power (8/20 μs)	P _{PP}	300	W	
Junction Temperature	T _j	150	°C	
Storage Temperature range	T _{stg}	-55 to +150		
Maximum lead temperature for soldering during 10s	T _L	260		
Operating temperature range	T _{OP}	-40 to +125		

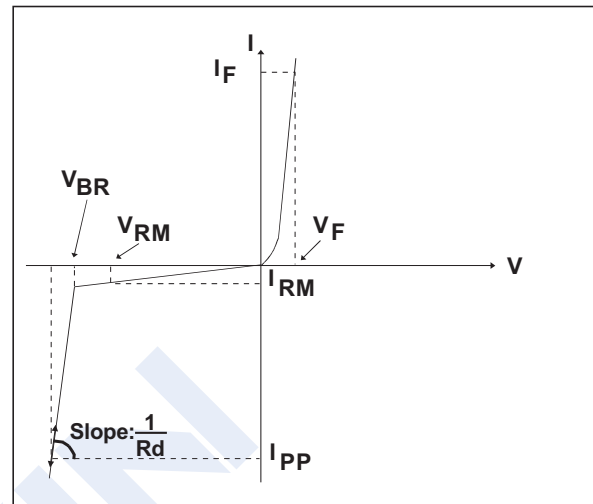
Note 1. Evolution of functional parameters is given by curves.

ESD Protection Diodes

ESDAxxL

■ Electrical Characteristics (Ta = 25°C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
C	Capacitance
R_d	Dynamic resistance
V_F	Forward voltage drop



Types	V_{BR} @		I_R	I_{RM} @ V_{RM}		R_d typ. note 1	αT max. note 2	C typ. 0V bias	V_F @ I_F	
	min.	max.		max.					max.	
	V	V	mA	μA	V	m Ω	$10^{-4}/^{\circ}C$	pF	V	mA
ESDA5V3L	5.3	5.9	1	2	3	280	5	220	1.25	200
ESDA6V1L	6.1	7.2	1	20	5.25	350	6	140	1.25	200
ESDA14V2L	14.2	15.8	1	5	12	650	10	90	1.25	200
ESDA25L	25	30	1	1	24	1000	10	50	1.2	10

note 1 : Square pulse $I_{pp} = 15A$, $t_p = 2.5\mu s$.

note 2 : $\Delta V_{BR} = \alpha T^* (T_{amb} - 25^{\circ}C) * V_{BR} (25^{\circ}C)$

■ Marking

Type	Marking
ESDA5V3L	EL53
ESDA6V1L	EL61
ESDA14V2L	EL15
ESDA25L	EL25

ESD Protection Diodes

ESDAxxL

CALCULATION OF THE CLAMPING VOLTAGE

USE OF THE DYNAMIC RESISTANCE

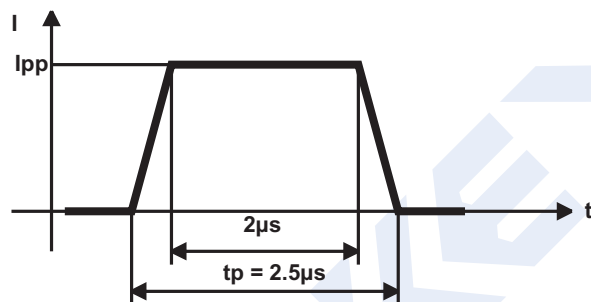
The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage V_{CL} . This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

$$V_{CL} = V_{BR} + R_d I_{PP}$$

Where I_{PP} is the peak current through the ESDA cell.

DYNAMIC RESISTANCE MEASUREMENT

The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical 8/20 μ s and 10/1000 μ s surges.



2.5 μ s duration measurement wave.

ESD Protection Diodes

ESDAxxL

■ Typical Characteristics

Fig. 1: Peak power dissipation versus initial junction temperature.

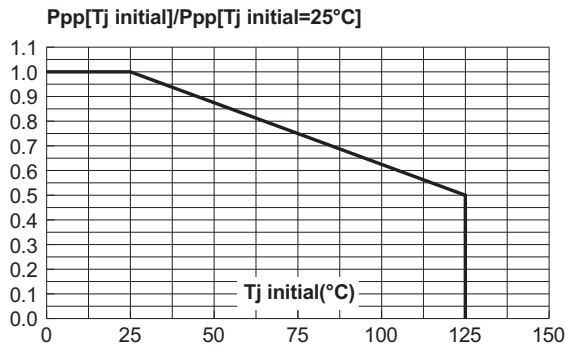


Fig. 3: Clamping voltage versus peak pulse current (Tj initial = 25 °C). Rectangular waveform tp = 2.5 μs.

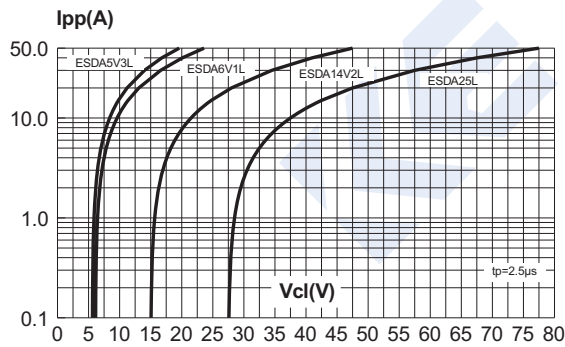


Fig. 5: Relative variation of leakage current versus junction temperature (typical values).

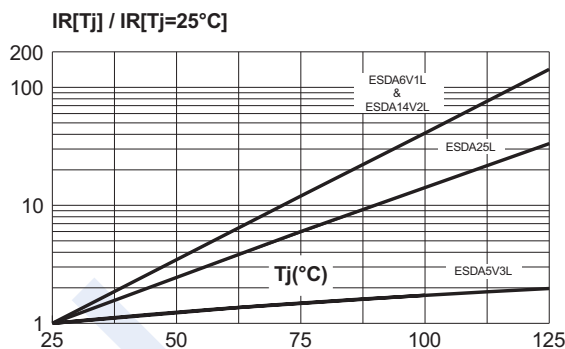


Fig. 2: Peak pulse power versus exponential pulse duration (Tj initial = 25 °C).

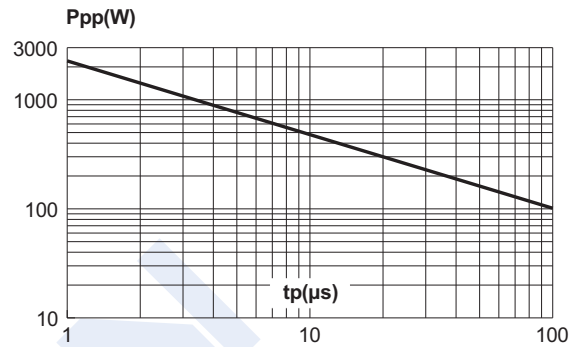


Fig. 4: Capacitance versus reverse applied voltage (typical values).

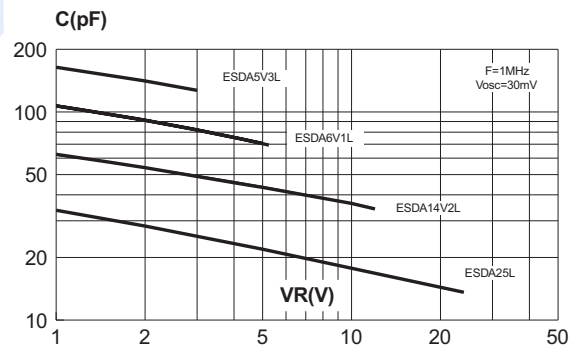
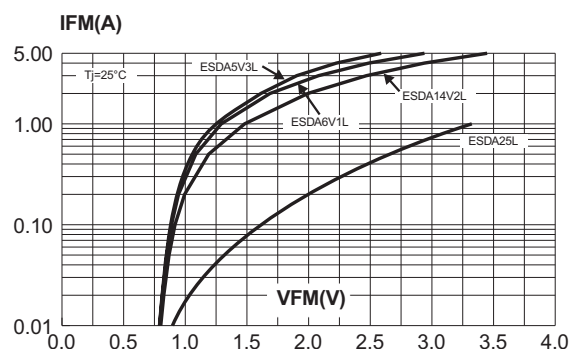


Fig. 6: Peak forward voltage drop versus peak forward current (typical values).



ESD Protection Diodes

ESDAxxL

1. ESD protection by the ESDAxxL

Electrostatic discharge (ESD) is a major cause of failure in electronic systems.

Transient Voltage Suppressors (TVS) are an ideal choice for ESD protection. They are capable of clamping the incoming transient to a low enough level such that damage to the protected semiconductor is prevented.

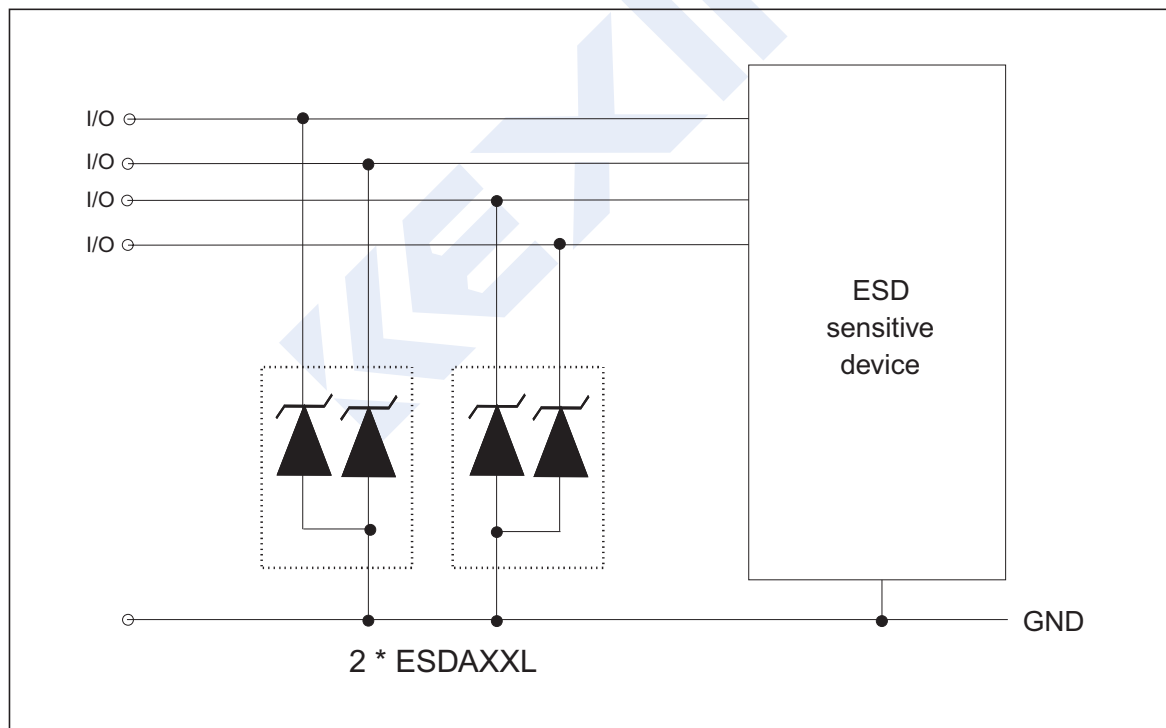
Surface mount TVS arrays offer the best choice for minimal lead inductance.

They serve as parallel protection elements, connected between the signal line to ground. As

the transient rises above the operating voltage of the device, the TVS array becomes a low impedance path diverting the transient current to ground.

The ESDAxxL array is the ideal board level protection of ESD sensitive semiconductor components.

The tiny SOT23 package allows design flexibility in the design of high density boards where the space saving is at a premium. This enables to shorten the routing and contributes to hardening against ESD.



2. Circuit Board Layout

Circuit board layout is a critical design step in the suppression of ESD induced transients. The following guidelines are recommended :

- The ESDAxxL should be placed as close as possible to the input terminals or connectors.
- The path length between the ESD suppressor and the protected line should be minimized
- All conductive loops, including power and ground loops should be minimized
- The ESD transient return path to ground should be kept as short as possible.
- Ground planes should be used whenever possible.