

ESDA6V8BLF

**2-Line, Bi-directional, Low-Capacitance,
Transient Voltage Suppressors**

<http://www.sh-willsemi.com>

Descriptions

The ESDA6V8BLF is a Bi-directional transient voltage suppressors (TVS) which provide a very high level protection for sensitive electronic components that may be subjected to electrostatic discharge (ESD). It is designed to replace multilayer varistors (MLV) in consumer equipment applications such as mobile phone, notebook, PAD, STB, LCD TV etc.

The ESDA6V8BLF is based on solid-state silicon technology and offer unique electrical characteristics like lower clamping voltage and no device degrading compared to MLV.

The ESDA6V8BLF is past ESD transient voltage up to $\pm 8\text{KV}$ (contact) according to IEC61000-4-2 and will withstand peak current up to 3A for 8/20 μs pulse to meet the IEC61000-4-5.

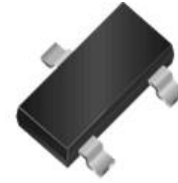
The ESDA6V8BLF is available in SOT-23-3L package. Standard products are Pb-free and Halogen-free.

Features

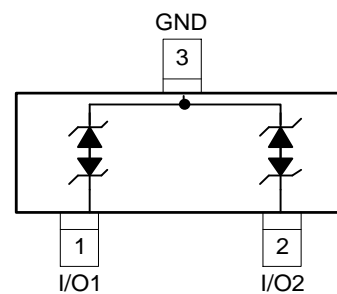
- Working voltage: $\pm 5.0\text{V}$ Max
- Transient protection for each line according to IEC61000-4-2 (ESD): $\pm 8\text{kV}$ (contact discharge)
 $\pm 15\text{kV}$ (air discharge)
- IEC61000-4-4 (EFT): 40A (5/50ns)
- IEC61000-4-5 (surge): 3A (8/20 μs)
- Low Capacitance: $C_J = 5.0\text{pF}$ typ.
- Low leakage current
- Small package

Applications

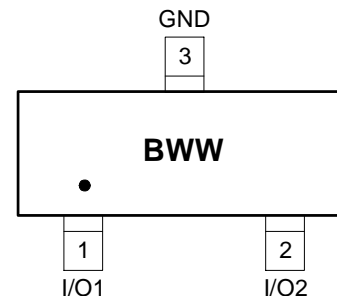
- Cell phone
- Notebook
- STB
- Digital camera
- Other electronics equipment



SOT-23



Circuit Diagram



SOT-23

B = Device code

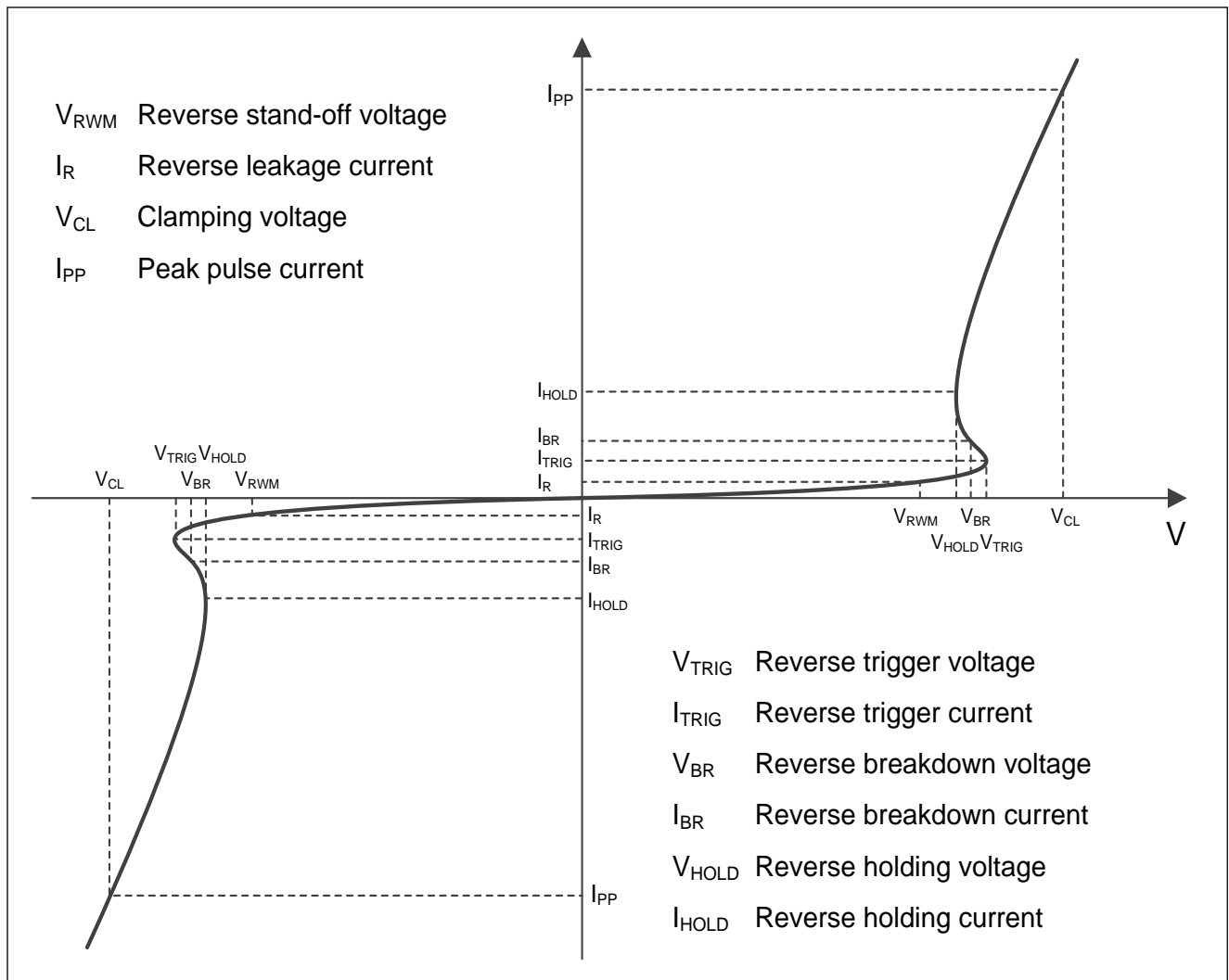
WW = Date code

Marking & Pin configuration
Order information

Device	Package	Shipping
ESDA6V8BLF-3/TR	SOT-23	3000/Tape&Reel

Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Peak pulse power (tp=8/20μs)	Ppk	33	W
Peak pulse current (tp=8/20μs)	Ipp	3	A
ESD voltage IEC61000-4-2 air	V _{ESD}	±15	kV
ESD voltage IEC61000-4-2 contact		±8	
Junction temperature	T _J	125	°C
Operating temperature	T _{OP}	-40~85	°C
Lead temperature	T _L	260	°C
Storage temperature	T _{STG}	-55~150	°C

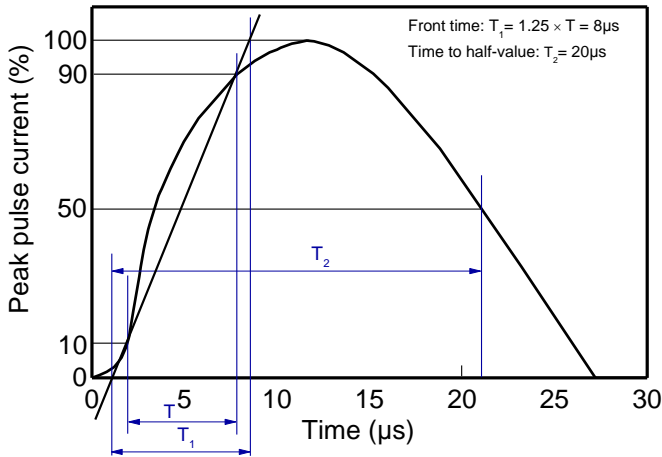
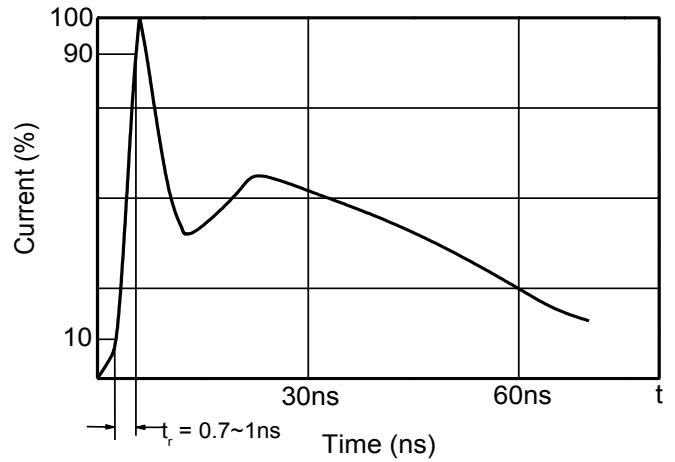
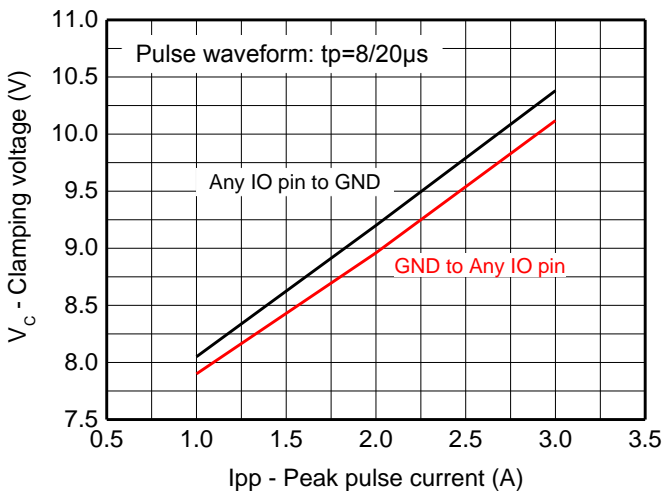
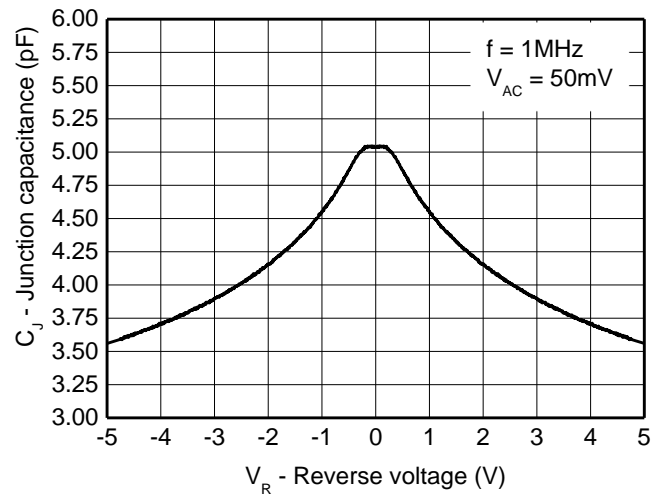
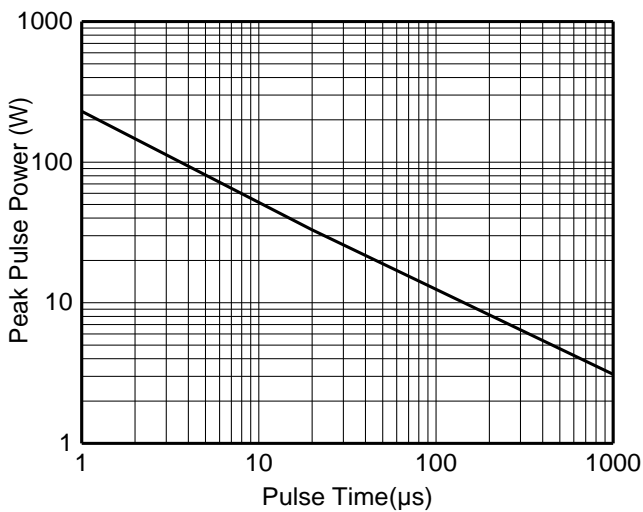
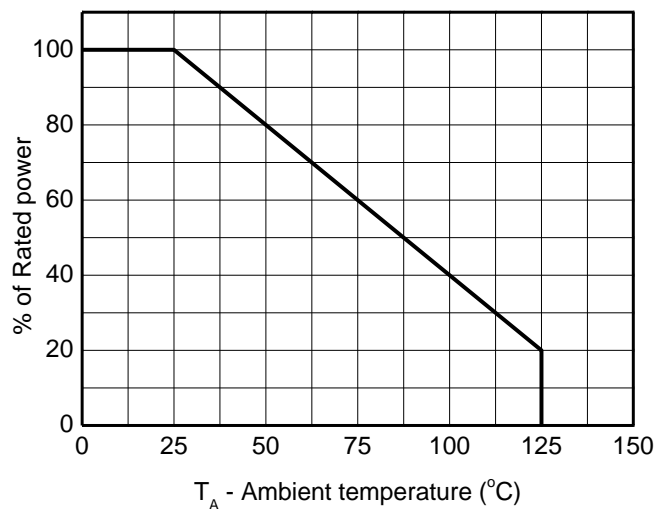
Electrical characteristics (T_A=25°C, unless otherwise noted)


Electronics characteristics (Ta=25 °C, unless otherwise noted)

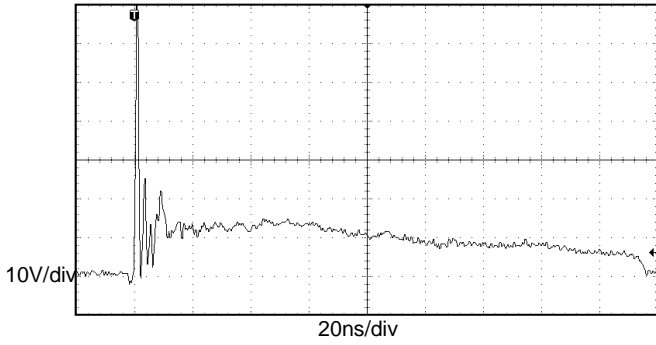
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse maximum working voltage	V_{RWM}				±5.0	V
Reverse leakage current	I_R	$V_{RWM}=5V$			1.0	μA
Reveres breakdown voltage	V_{BR}	$I_T=1mA$	6.2		8.2	V
Clamping voltage ¹⁾	V_{CL}	$I_{PP} = 16A, t_p = 100ns$		13		V
Dynamic resistance ¹⁾	R_{DYN}			0.4		Ω
Clamping voltage ²⁾	V_{CL}	$V_{ESD} = 8kV$		13		V
Clamping voltage ³⁾	V_C	$I_{pp}=1A t_p=8/20\mu s$			8.5	V
		$I_{pp}=3 A t_p=8/20\mu s$			11	V
Junction capacitance	C_J	$f=1MHz, V_R=0V$ Any I/O pin to GND		5.0	10	pF
		$f=1MHz, V_R=0V$ Between I/O pins		2.5	5	pF

Notes:

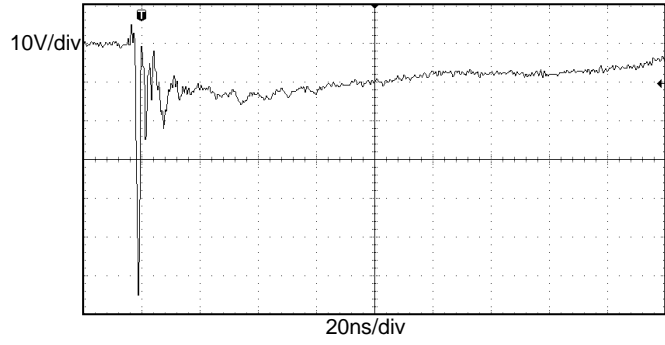
- 1) TLP parameter: $Z_0 = 50\Omega, t_p = 100ns, t_r = 2ns$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.
- 2) Contact discharge mode, according to IEC61000-4-2.
- 3) Non-repetitive current pulse, according to IEC61000-4-5.

Typical characteristics (Ta=25°C, unless otherwise noted)

8/20μs waveform per IEC61000-4-5

Contact discharge current waveform per IEC61000-4-2

Clamping voltage vs. Peak pulse current

Capacitance vs. Reverse voltage

Non-Repetitive Peak Pulse Power vs. Pulse time

Power derating vs. Ambient Temperature

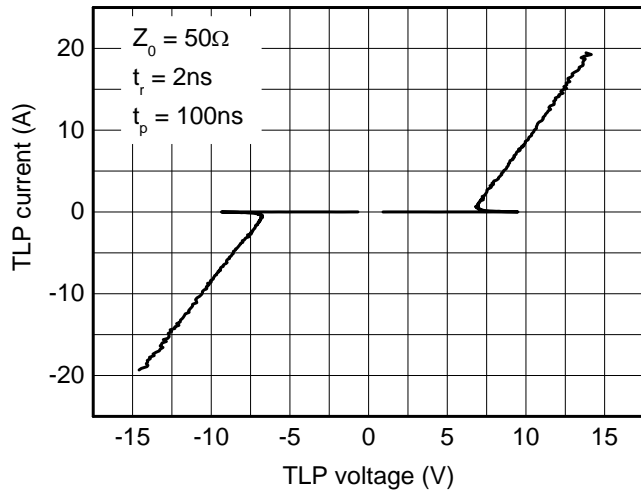
Typical characteristics ($T_A = 25^\circ\text{C}$, unless otherwise noted)



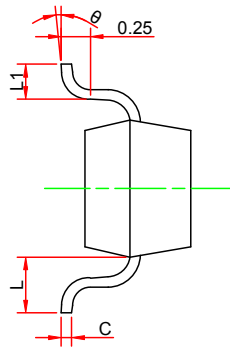
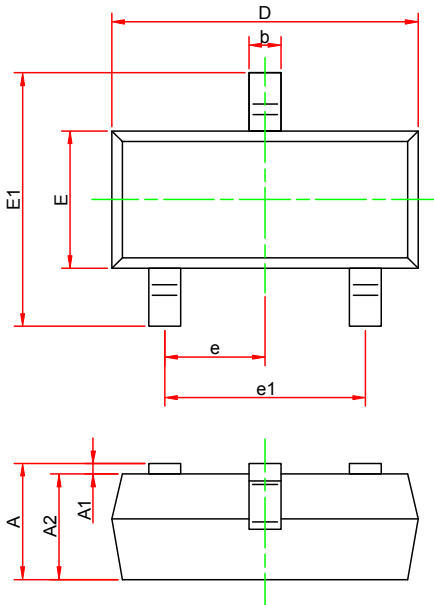
ESD clamping
 (+8kV contact discharge per IEC61000-4-2)



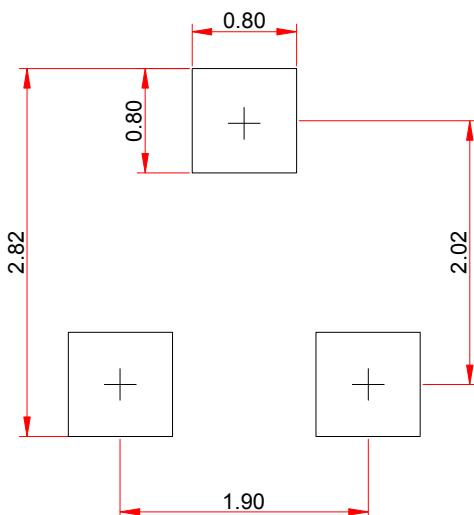
ESD clamping
 (-8kV contact discharge per IEC61000-4-2)



TLP Measurement

Package outline dimensions
SOT-23


Symbol	Dimensions in millimeter		
	Min.	Typ.	Max.
A	0.900	-	1.150
A1	0.000	-	0.100
A2	0.900	-	1.050
b	0.300	-	0.500
c	0.080	-	0.150
D	2.800	-	3.000
E	1.200	-	1.400
E1	2.250	-	2.550
e	0.950TYP		
e1	1.800		2.000
L	0.500REF		
L1	0.300	-	0.500
θ	0°	-	8°

Recommend land pattern (Unit: mm)

Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.