



ESDALC6V1-1U2

Single-line low capacitance Transil™ for ESD protection

Features

- Breakdown voltage $V_{BR} = 6.1 \text{ V min.}$
- Unidirectional device
- Multiple ESD strike sustainability
- Very low diode capacitance: 12 pF typ. at 0 V
- Low leakage current
- 0201 SMD package size compatible
- Ultra small PCB area: 0.18 mm²
- RoHS compliant

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards
- MSL1

Complies with the following standards:

- IEC 61000-4-2 level 4

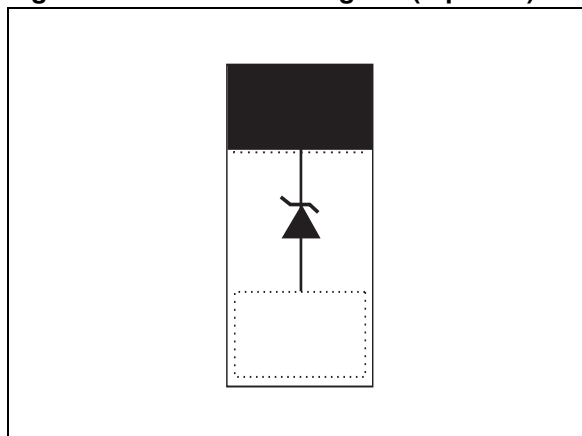
Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Portable multimedia players and accessories
- Notebooks
- Digital cameras and camcorders
- Communication systems
- Cellular phone handsets and accessories



Figure 1. Functional diagram (top view)



Description

The ESDALC6V1-1U2 is a unidirectional single line TVS diode designed to protect the data lines or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter	Value	Unit
V_{PP}	Peak pulse voltage: IEC 61000-4-2 contact discharge	± 8	kV
P_{PP}	Peak pulse power dissipation (8/20 μs) ⁽¹⁾	$T_{j\text{ initial}} = T_{amb}$ 20	W
I_{PP}	Peak pulse current (8/20 μs)	2	A
T_j	Junction temperature	125	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	- 55 to +150	$^{\circ}\text{C}$
T_L	Maximum lead temperature for soldering during 10 s	260	$^{\circ}\text{C}$
T_{op}	Operating junction temperature range	-40 to +125	$^{\circ}\text{C}$

1. For a surge greater than the maximum values, the diode will fail in short-circuit

Table 2. Electrical characteristics (definitions)

Symbol	Parameter
V_{RM}	Stand-of voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current @ V_{RM}
I_{PP}	Peak pulse current
αT	Voltage - temperature coefficient

Table 3. Electrical characteristics (values, $T_{amb} = 25\text{ °C}$)

Symbol	Test Condition	Min	Typ	Max	Unit
V_{BR}	$I_R = 1\text{ mA}$	6.1		8.0	V
I_{RM}	$V_{RM} = 3\text{ V}$			100	nA
R_d	Square pulse, $I_{PP} = 1\text{ A}$, $t_p = 2.5\text{ }\mu\text{s}$		1.3		Ω
αT	$\Delta V_{BR} = \alpha T (T_{amb} - 25\text{ }^{\circ}\text{C}) \times V_{BR} (25\text{ }^{\circ}\text{C})$			4.5	$10^{-4}/^{\circ}\text{C}$
C_{line}	$V_R = 0\text{ V}$, $F_{osc} = 1\text{ MHz}$, $V_{osc} = 30\text{ mV}$		12.0		pF

Figure 2. Relative variation of peak pulse power versus initial junction temperature

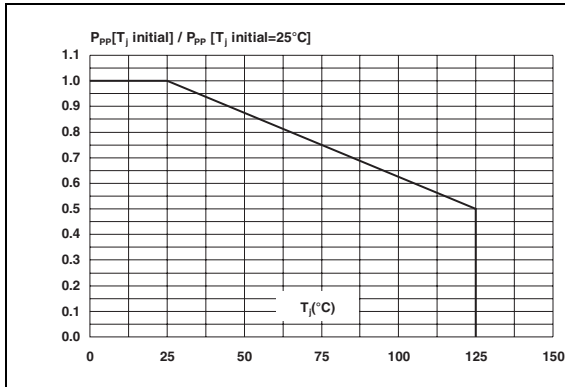


Figure 3. Peak pulse power versus exponential pulse duration

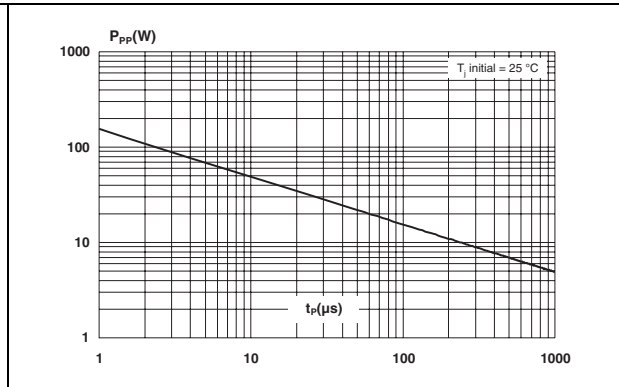


Figure 4. Clamping voltage versus peak pulse current (square pulse, typical values)

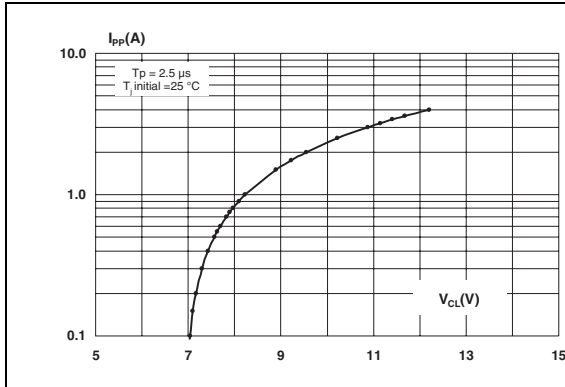


Figure 5. Junction capacitance versus reverse applied voltage (typical values)

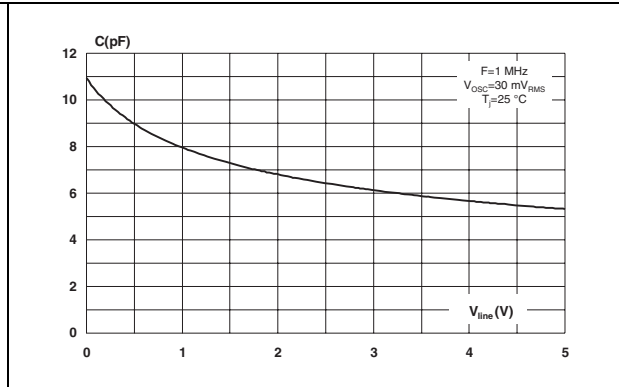


Figure 6. Relative variation of leakage current versus junction temperature (typical values)

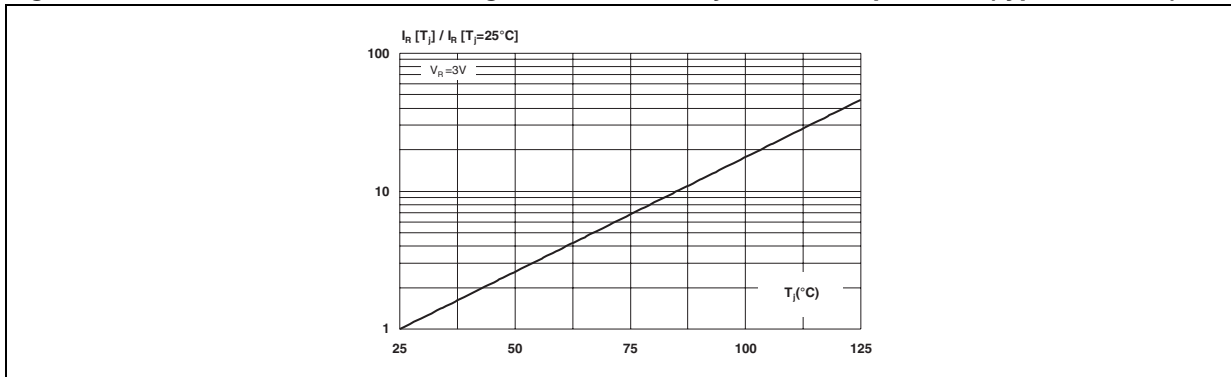


Figure 7. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

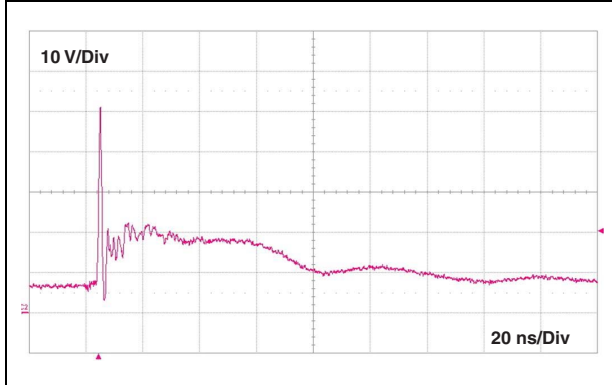


Figure 8. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

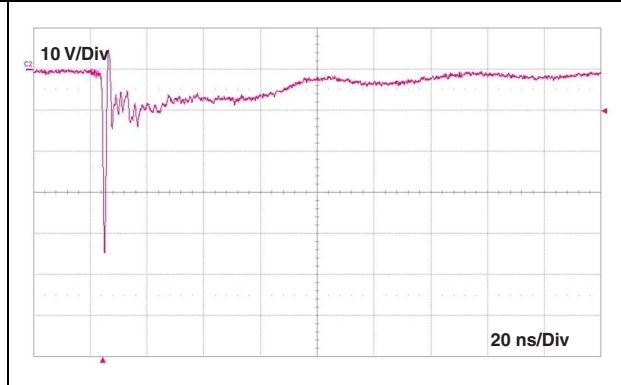
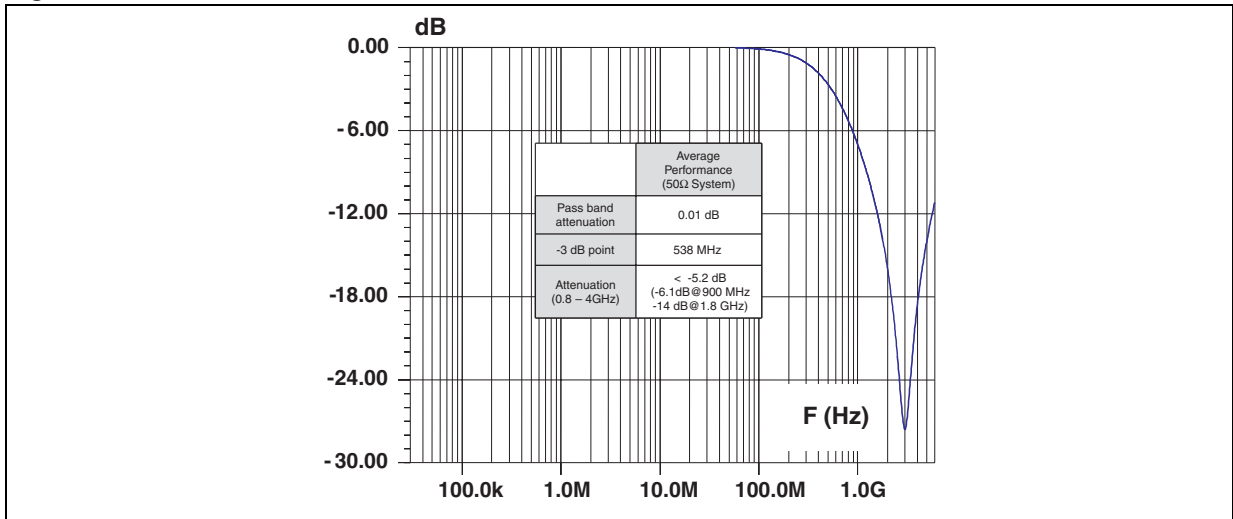
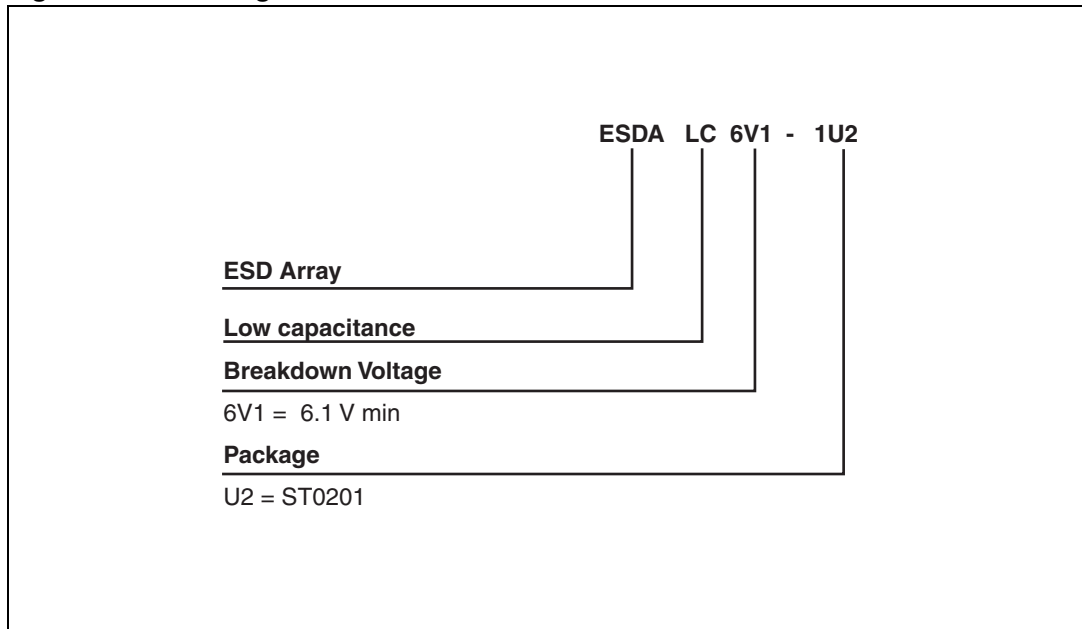


Figure 9. S21 attenuation measurement results



2 Ordering information scheme

Figure 10. Ordering information scheme



3 Package information

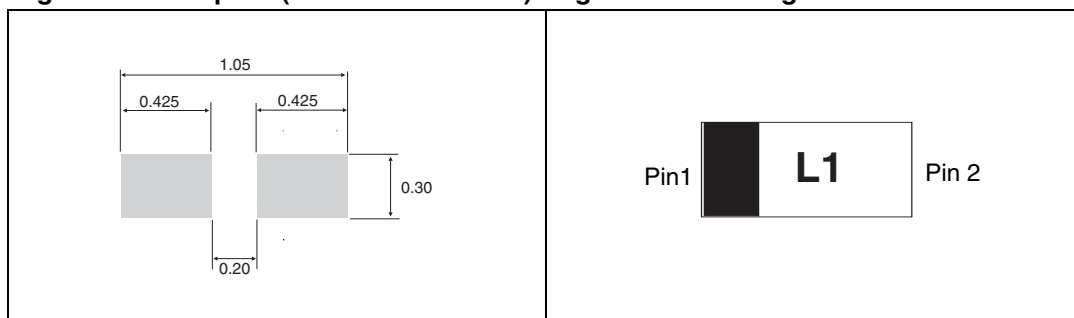
- Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Table 4. ST0201 dimensions

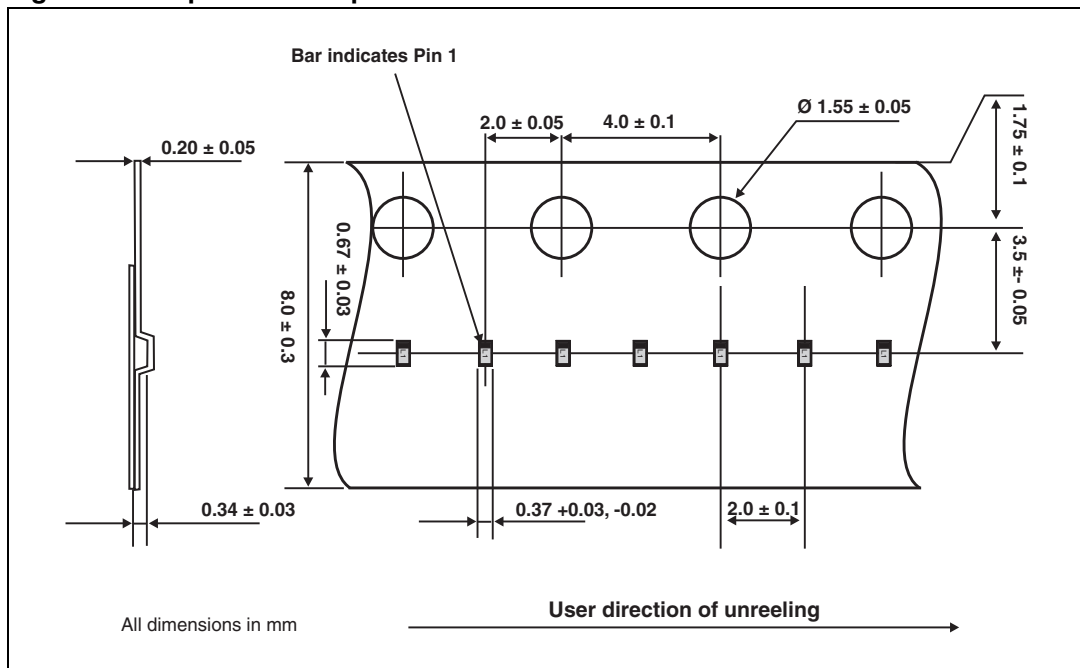
Ref	Dimensions					
	Millimetres			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.23	0.28	0.33	0.009	0.011	0.013
b1	0.13	0.18	0.23	0.005	0.007	0.009
b2	0.14	0.19	0.24	0.006	0.007	0.009
D	0.55	0.60	0.65	0.022	0.024	0.026
E	0.25	0.30	0.35	0.010	0.012	0.014
e		0.35			0.014	
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012

Figure 11. Footprint (dimensions in mm) Figure 12. Marking



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

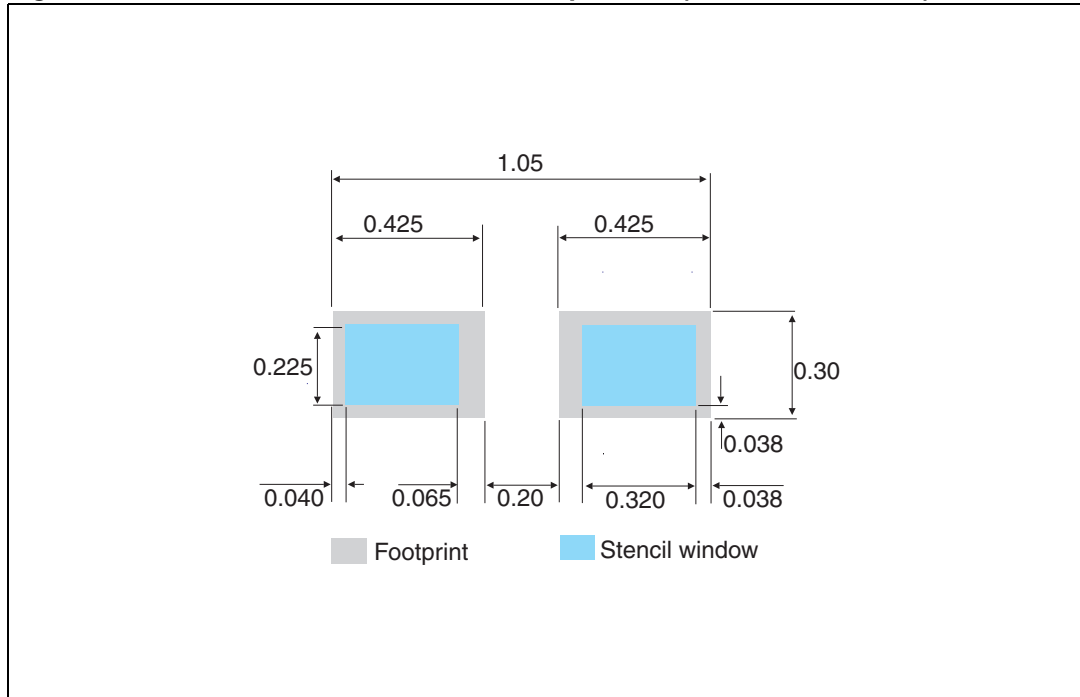
Figure 13. Tape and reel specifications



4 Recommendation on PCB assembly

4.1 Stencil opening design

Figure 14. Recommended stencil windows position (dimensions in mm)



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 μm .

4.3 Placement

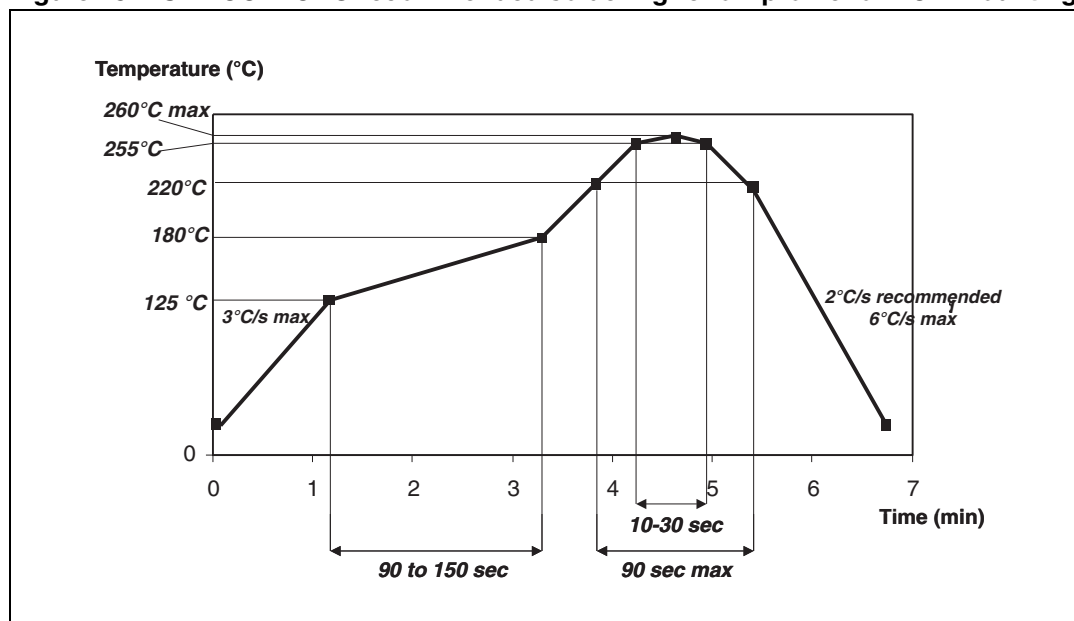
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 15. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 5. Ordering information

Order code	Marking	Weight	Base qty	Delivery mode
ESDALC6V1-1U2	L1 ⁽¹⁾	0.124 mg	5000	Tape and reel

1. The marking can be rotated by 90° to differentiate assembly location

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
07-Oct-2008	1	Initial release

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