ESDALC6V1-5P6

ESD protection for high speed interface

Features

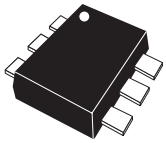
- Diode array topology
- Low capacitance (12 pF typical)
- Lead-free package

Benefits

- Low capacitance uni-directional ESD protection.
- Low PCB space consuming, 2.5 mm^2 max. footprint
- Low leakage current
- High reliability offered by monolithic integration

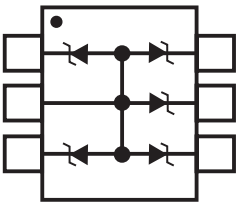
Complies with the following standards

- IEC 61000-4-2 level 4:
  - 8 kV (contact discharge)
  - 15 kV (air discharge)
- MIL STD 883G-Method 3015-7: class3B
  - Human body model



SOT666

Figure 1. ESDALC6V1-5P6 functional diagram



Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

Description

The ESDALC6V1-5P6 is a monolithic array designed to protect up to 5 lines against ESD transients.

The device is ideal for high speed interface applications where both reduced printed circuit board space and power absorption capability are required.

1 Characteristics

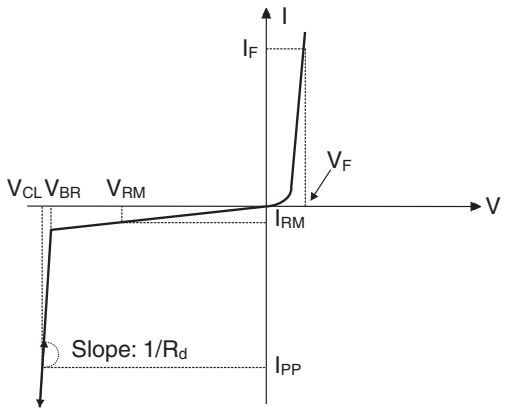
Table 1. Absolute ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP} (1)	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	± 8 ± 15	kV
P_{PP} (1)	Peak pulse power dissipation (8/20 µs)	T_j initial = T_{amb}	30	W
I_{PP}	Peak pulse current (8/20 µs)		2.5	A
T_j	Junction temperature		125	°C
T_{stg}	Storage temperature range		-55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C
T_{OP}	Operating temperature range		- 40 + 125	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
V_F	Forward voltage drop
C	Capacitance
R_d	Dynamic resistance



Parameter	Test condition		Min	Typ	Max	Unit
V_{RRM}	Reverse stand-off voltage				5	V
V_{BR}	I_R = 1 mA		6.1		7.2	V
I_{RM}	V_{RM} = 3 V				70	nA
V_{CL}	Non repetitive peak pulse voltage (8/20 µs)	I_{PP} = 1 A			10	V
		I_{PP} = 2.5 A			14	
V_F	I_F = 10 mA				1	V
R_d				2	3	Ω
αT (1)	I_R = 1 mA				5	10^{-4}/°C
C	V_R = 0 V DC, F = 1 MHz, V_{osc} = 30 mV rms			12	15	pF

1. $\Delta V_{BR} = \alpha T \times (T_{amb} - 25\ °C) \times V_{BR}\ (25\ °C)$

Figure 2. Relative variation of peak pulse power versus initial junction temperature

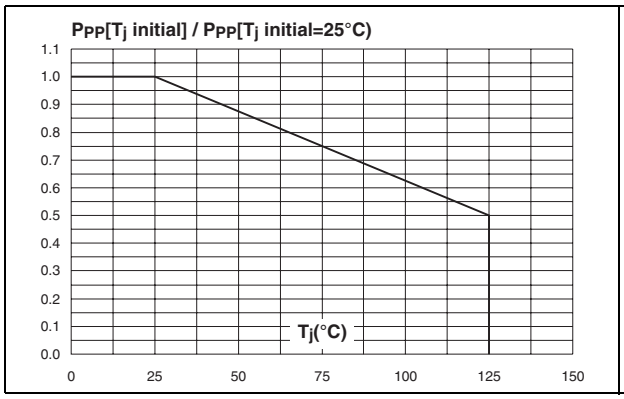


Figure 3. Peak pulse power versus exponential pulse duration (T_j initial = 25 °C)

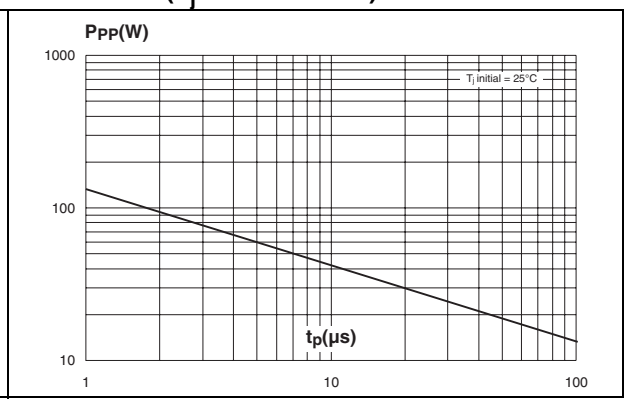


Figure 4. Clamping voltage versus peak pulse current (typical values)

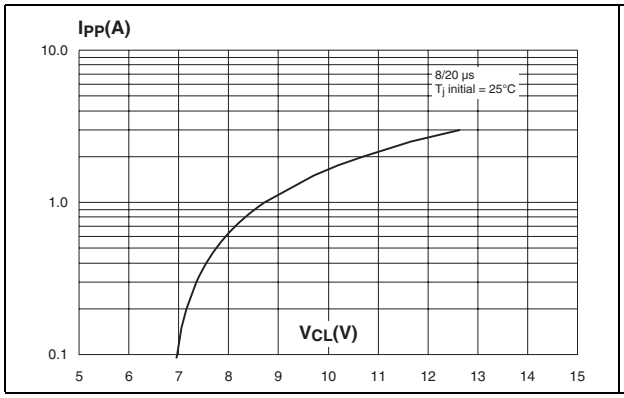


Figure 5. Relative variation of leakage current versus junction temperature (typical values)

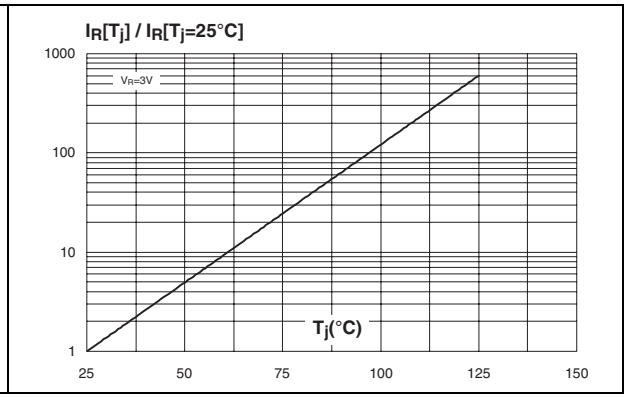


Figure 6. Breakdown voltage versus initial junction temperature

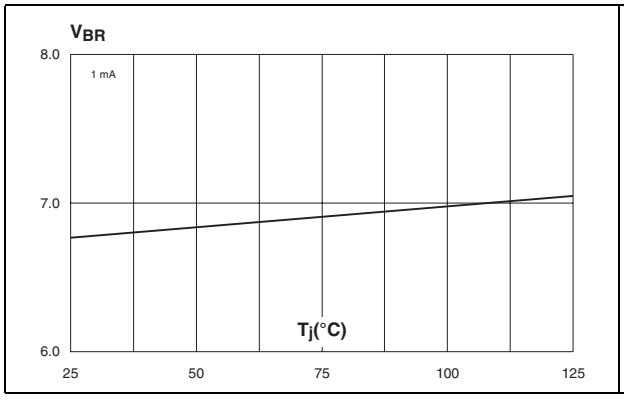


Figure 7. Junction capacitance versus reverse voltage applied (typical values)

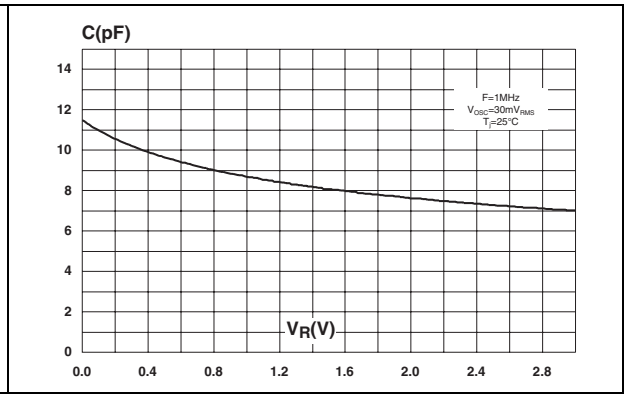


Figure 8. ESD response to IEC 61000-4-2 (air discharge +15 kV surge)

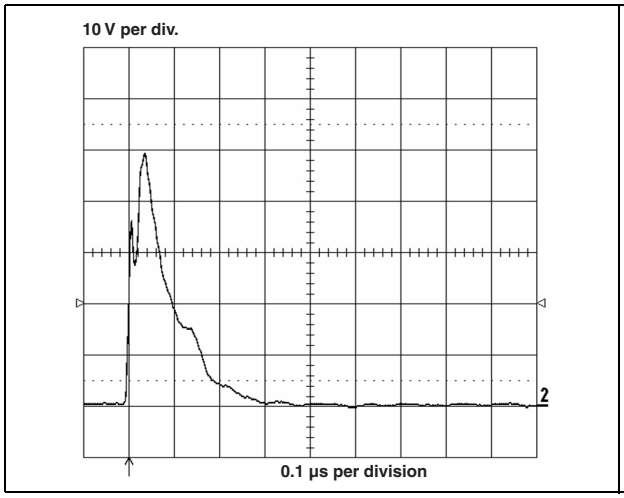


Figure 9. ESD response to IEC 61000-4-2 (air discharge -15 kV surge)

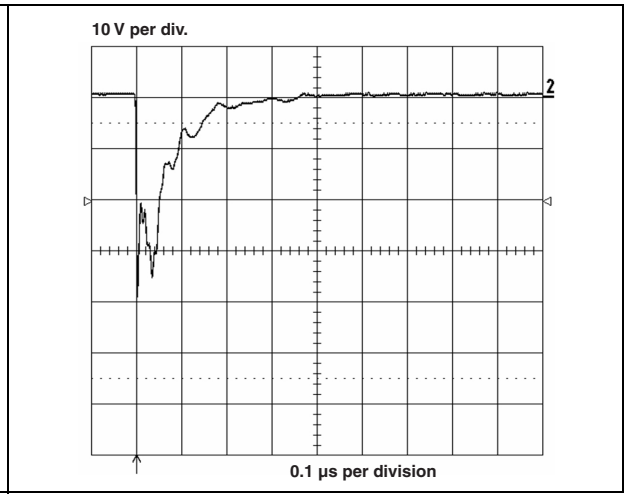


Figure 10. Frequency response curves - all lines together

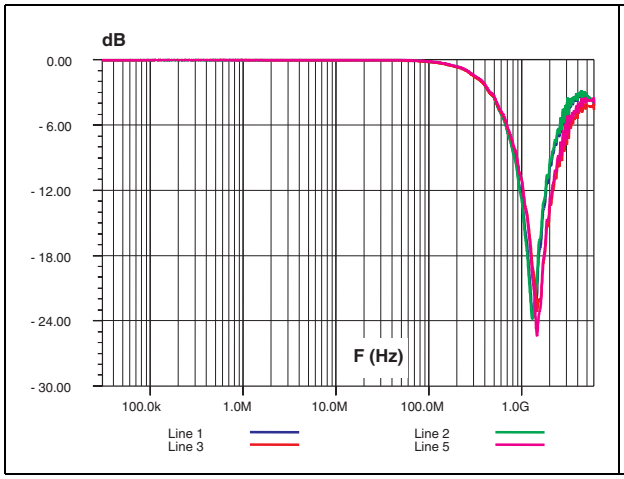
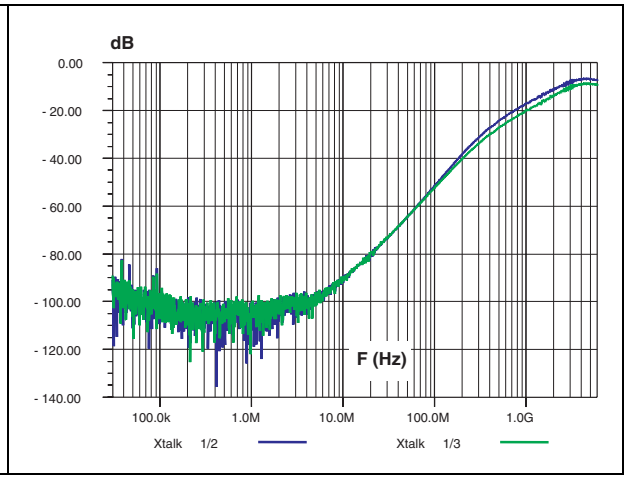
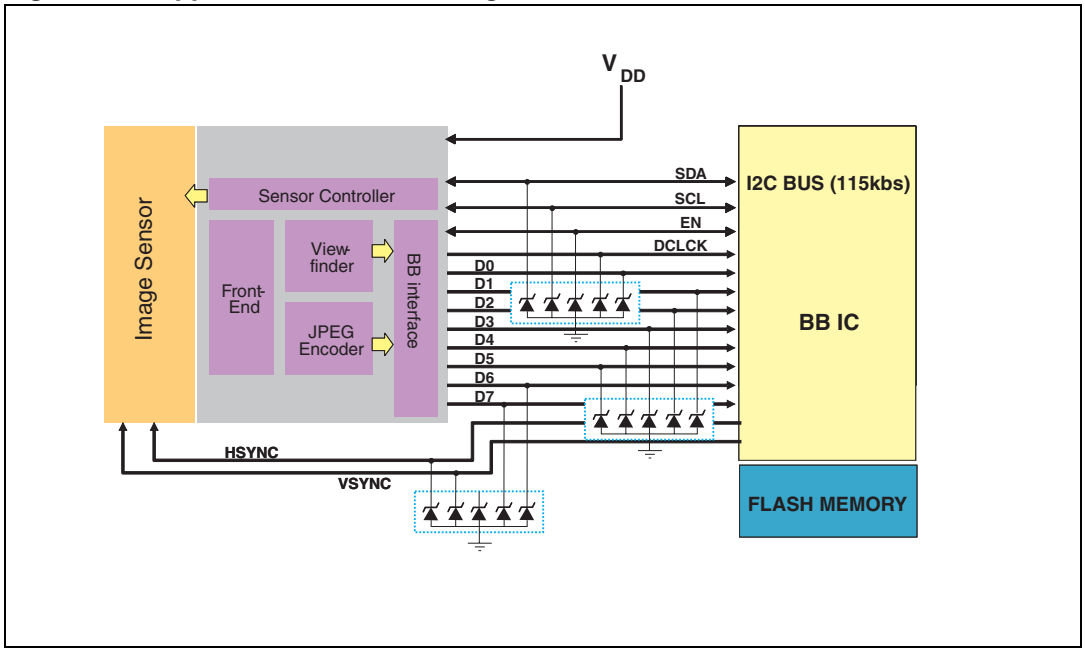


Figure 11. Crosstalk response curves - 1/2 and 1/3



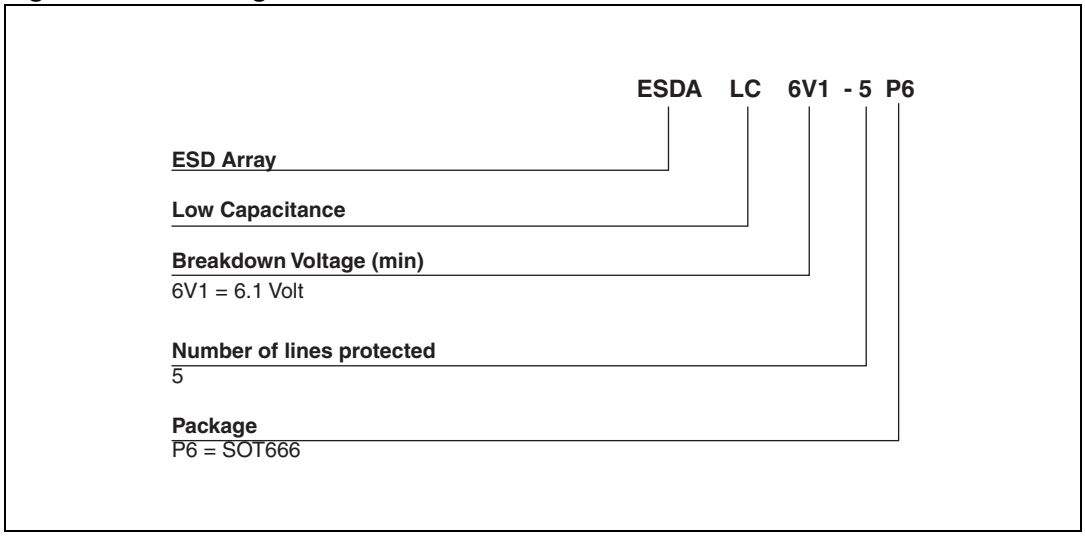
2 Application information

Figure 12. Application schematic diagram



3 Ordering information scheme

Figure 13. Ordering information scheme

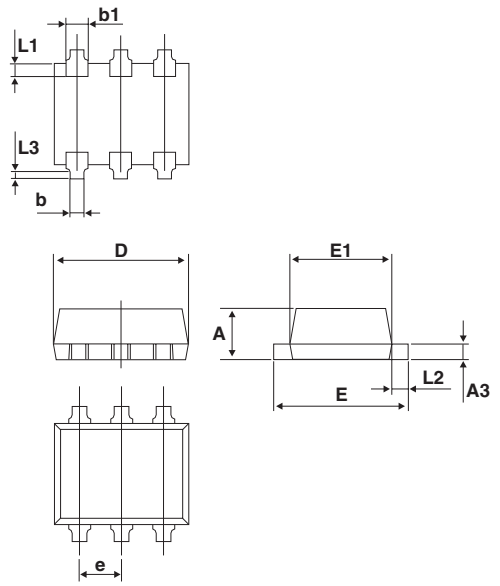


4 Package information

- Epoxy meets UL 94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 3. SOT666 dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45		0.60	0.018		0.024
A3	0.08		0.18	0.003		0.007
b	0.17		0.34	0.007		0.013
b1	0.19	0.27	0.34	0.007	0.011	0.013
D	1.50		1.70	0.059		0.067
E	1.50		1.70	0.059		0.067
E1	1.10		1.30	0.043		0.051
e		0.50			0.020	
L1		0.19			0.007	
L2	0.10		0.30	0.004		0.012
L3		0.10			0.004	

Figure 14. SOT666 footprint (dimensions in mm)

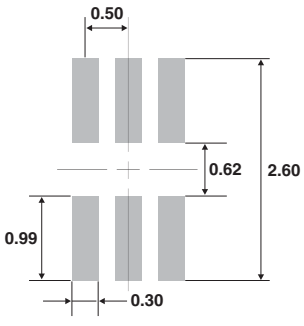
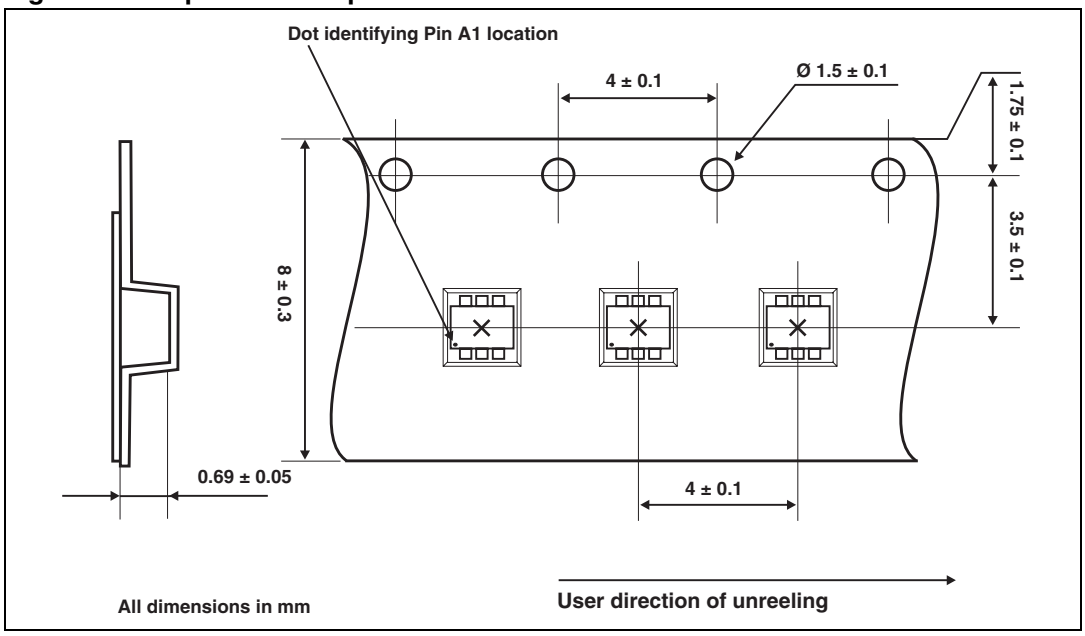


Figure 15. Tape and reel specifications



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDALC6V1-5P6	J(1)	SOT666	2.9 mg	3000	Tape and reel

1. The marking can be rotated by 90° to diferentiate assembly location

6 Revision history

Table 5. Document revision history

Date	Revision	Description of changes
29-May-2007	1	First issue.
30-Jul-2007	2	Upgrade V_{CL} from 8 V to 10 V and from 9.5 V to 14 V.
15-Nov-2007	3	Reformatted to current standards. Marking changed to J in *Table 4*. Notes on marking rotation added to *Table 4* and *Figure 15*.

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