

ESDALC6V1F2

Quad low capacitance Transil[™] array for ESD protection

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- www.DatahGommunication systems and cellular phones
 - Video equipment

This device is particularly adapted to the protection of symmetrical signals

Features

- 4 unidirectional Transil functions.
- Breakdown voltage V_{BR} = 6.1 V min.
 - Low diode capacitance (12 pF @ 0 V)
 - Low leakage current (< 500 nA @ 3 V)
 - very small PCB area (1.25 mm²)
- Lead free package

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards

Description

July 2007

The ESDALC6V1F2 is a monolithic array designed to protect up to 4 lines againast ESD transients. The device is ideal for applications where both reduced line capacitance and board space saving are required.



Figure 1. Functional diagram

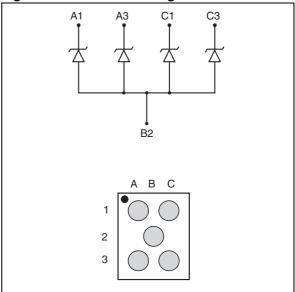


Table 1.Order code

Part number	Marking		
ESDALC6V1F2	ED		

Complies with the following standards:

IEC 61000-4-2	15 kV (air discharge)
	8 kV (contact discharge)
MIL STD 883E -	Method 3015-7: class 3
	25 kV (Human body model)

TM: Transil is a trademark of STMicroelectronics

Rev 2

1 Characteristics

Table 2.	Absolute maximum ratings (T _{amb})= 25° (0

	Symbol	Parameter			Value	Unit
	V _{PP}	ESD discharge	IEC 61000-4-2 air discha IEC 61000-4-2 contact di	•	± 15 ± 8	kV
	P _{PP}	Peak pulse power dis	Peak pulse power dissipation (8/20 μ s). ⁽¹⁾ $T_{j \text{ initial}} = T_{amb}$		25	W
	Тj	Junction temperature		125	°C	
	T _{stg}	Storage temperature	storage temperature		- 55 to +150	°C
	Τ _L	Maximum lead temp	faximum lead temperature for soldering during 10 s at 5 mm for case			°C
ita:	Top Sheet41.com	Operating temperature range - 40 to + 12			- 40 to + 125	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit

Table 3.Thermal resistance

Synbol	Parameter	Value	Unit
R _{th(j-a)}	Junction to ambient on printed circuit on recommended pad layout	150	°C/W

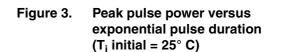
Table 4.Electrical characteristics

Symbol		Paramet	er		' ↑ ,							
V _{RM}	Stand-of vo	oltage					IF					
V _{BR}	Breakdowr	n voltage										
V _{CL}	Clamping	/oltage						VF				
I _{RM}	Leakage c	urrent @ V _F				<u>:≮</u> ≀						
I _{PP}	Peak pulse	current										
αΤ	Voltage ter	nperature co	pefficient			Slope = 1	Rd					
V _F	Forward vo	oltage drop				Ţ	IPP					
Tupo	I _{RM} @	₽ V _{RM}			v _i		@ I _R		R _D	αΤ	С	
Туре	µA max	V			nax	mA	Тур	10-4/°C max	pFtyp @	⊉0 V		
ESDALC6V1F2	0.5	3	6.1	7	7.2	1	1	5	12			



100

Figure 2. Peak power dissipation versus initial junction temperature



P_{PP}(W)

1000

100

10

1

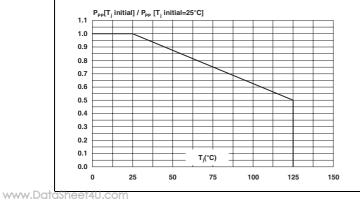


Figure 4. Clamping voltage versus peak pulse current (T_j initial = 25° C), rectangular waveform t_p = 2.5 µs).

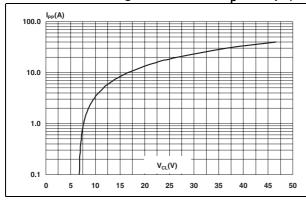


Figure 6. Relative variation of the leakage current versus junction temperature (typical values)

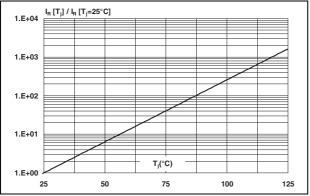
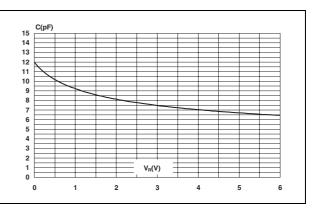


Figure 5. Capacitance versus reverse applied voltage (typical values)

t_P(µs)

10

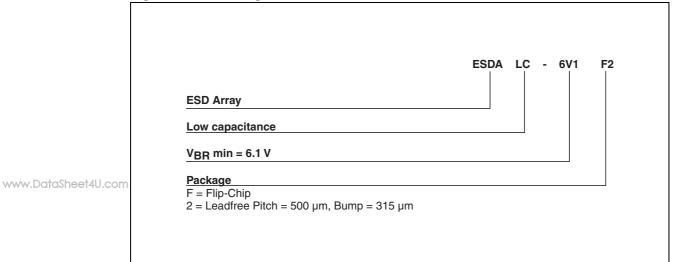




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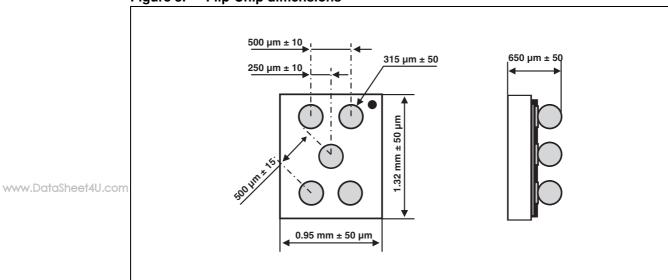
2 Ordering information scheme

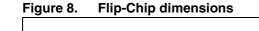
Figure 7. Ordering information scheme

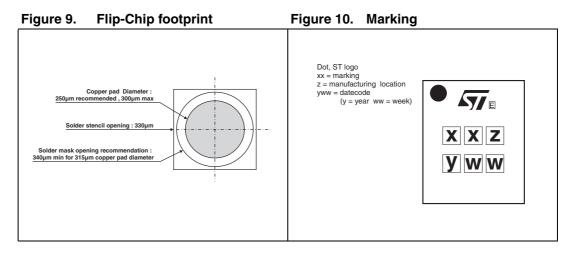




3 **Package information**







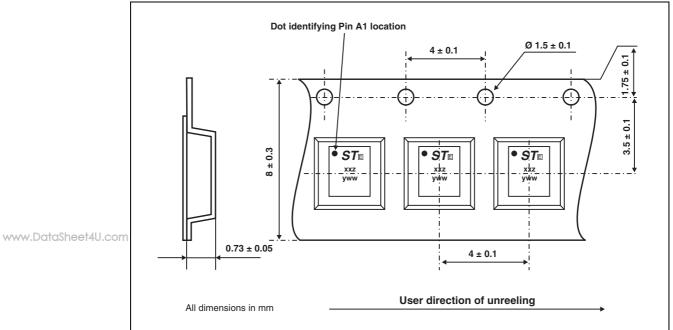


Figure 11. Flip-Chip tape and reel specifications

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

Table 5.	Ordering information	
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Part number	Marking	Package	Weight	Base qty	Delivery mode
ESDALC6V1F2	ED	Flip-Chip	2.1 mg	5000	Tape and reel

5 Revision history

Date	Revision	Changes		
07-Aug-2006	1	Initial release.		
11-Jul-2007	2	Updated marking from EDT to ED.		

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