ESD Protection Diode
Micro−Packaged Diodes for ESD Protection

ESDL1012

X4DFN2
CASE 718AA

MARKING DIAGRAM

3 = Device Code
M = Date Code

The ESDL1012 is designed to protect voltage sensitive components that require low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, the part is well suited for use in high speed data line applications.

Features

- Low Capacitance
- Low Clamping Voltage
- Small Body Outline Dimensions: 0.445 mm x 0.24 mm
- Low Body Height: 0.18 mm
- Stand−off Voltage: 1.0 V
- IEC61000−4−2 Level 4 ESD Protection
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- USB 3.x, USB 4.0
- PCIe 3x, 4.0
- Thunderbolt 3.0

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
IEC 61000−4−2 (ESD)	Contact Air		±15 ±15	kV
Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

ORDERING INFORMATION

Device	Package	Shipping†
ESDL1012MX4T5G	X4DFN2 (Pb−Free)	10000 / Tape & Reel

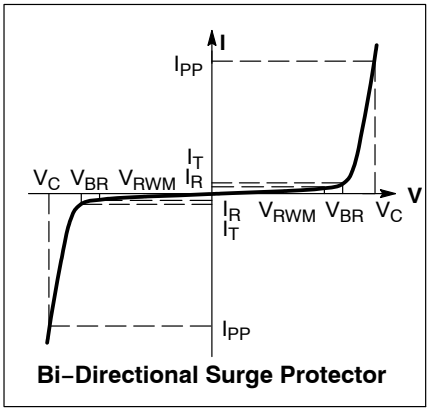
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional Surge Protector

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			1.0	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	1.4	1.6	2.1	V
Reverse Leakage Current	I_R	V_{RWM} = 1.0 V		25	500	nA
Clamping Voltage (Note 1)	V_C	IEC61000−4−2, ±8 kV Contact		Figures 1 and 2		V
Clamping Voltage 200 ns TLP	V_C	I_{PP} = 4 A } IEC61000−4−2 Level 1 Equivalent (±2 kV Contact, ±4 kV Air)		3.5	4.1	V
		I_{PP} = 8 A } IEC61000−4−2 Level 2 Equivalent (±4 kV Contact, ±8 kV Air)		4.7	5.6	
Reverse Peak Pulse Current per Figure 11	I_{PP}	per IEC61000−4−5 (1.2/50 μs), R_{eq} = 12 Ω	3.5	4.7		A
Clamping Voltage 1.2/50 μs Waveform per Figure 11	V_C	I_{PP} = 2.1 A, IEC61000−4−5 (1.2/50 μs), R_{eq} = 12 Ω		3.0	3.4	V
Clamping Voltage 1.2/50 μs Waveform per Figure 11	V_C	I_{PP} = 3.5 A, IEC61000−4−5 (1.2/50 μs), R_{eq} = 12 Ω		3.6	4.1	V
Dynamic Resistance (TLP)	R_{DYN}	I/O Pin to GND (4 A to 8 A, 200 ns TLP)		0.3		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz		0.17	0.23	pF
Insertion Loss	I_L	f = 10 GHz f = 13 GHz f = 15 GHz		0.22 0.225 0.23	0.33 0.36 0.37	dB
Return Loss	R_L	f = 10 GHz f = 13 GHz f = 15 GHz	14 12 11	19 17 16		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For test procedure see application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 200 ns, t_r = 1 ns, averaging window; t_1 = 170 ns to t_2 = 190 ns.

TYPICAL CHARACTERISTICS

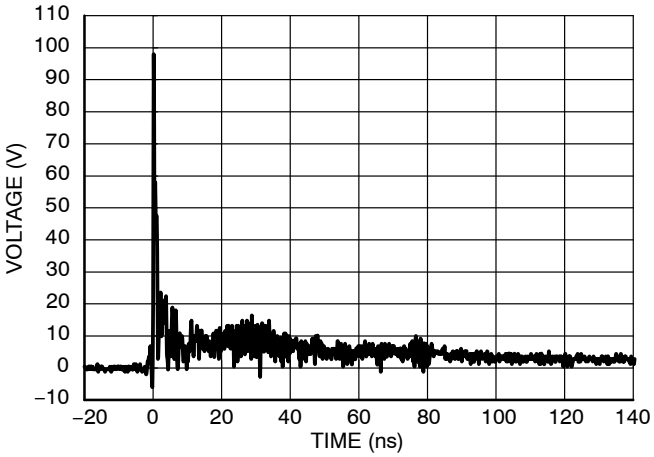


Figure 1. ESD Clamping Voltage Positive 8 kV Contact per IEC61000−4−2

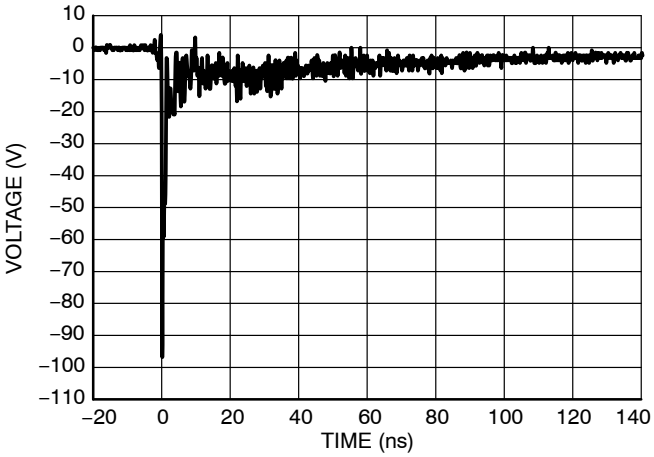


Figure 2. ESD Clamping Voltage Negative 8 kV Contact per IEC61000−4−2

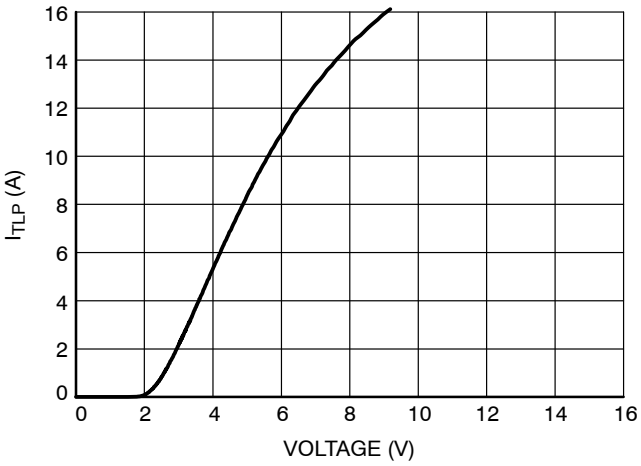


Figure 3. Positive 200 ns TLP IV Curve

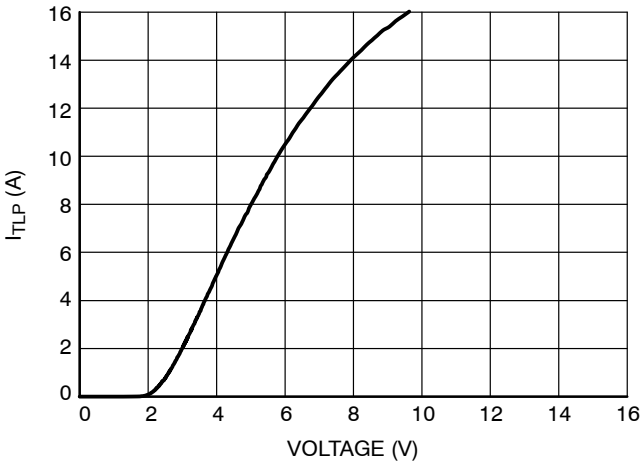


Figure 4. Negative 200 ns TLP IV Curve

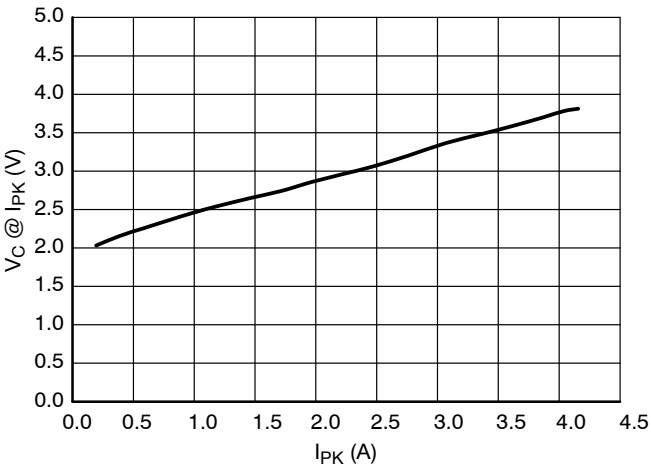


Figure 5. Positive Clamping Voltage vs. Peak Pulse Current per IEC61000−4−5 (t_p = 1.2/50 μs, R_{eq} = 12 Ω)

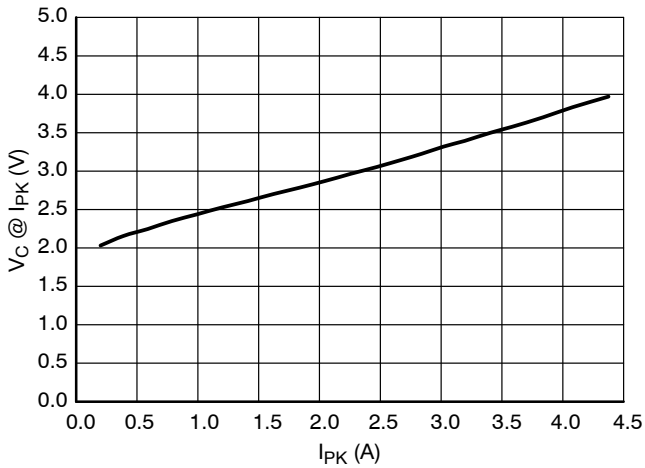


Figure 6. Negative Clamping Voltage vs. Peak Pulse Current per IEC61000−4−5 (t_p = 1.2/50 μs, R_{eq} = 12 Ω)

TYPICAL CHARACTERISTICS

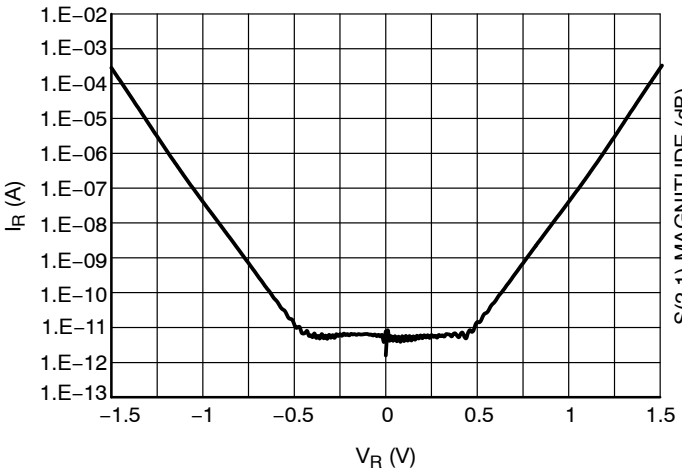


Figure 7. Reverse Leakage Current

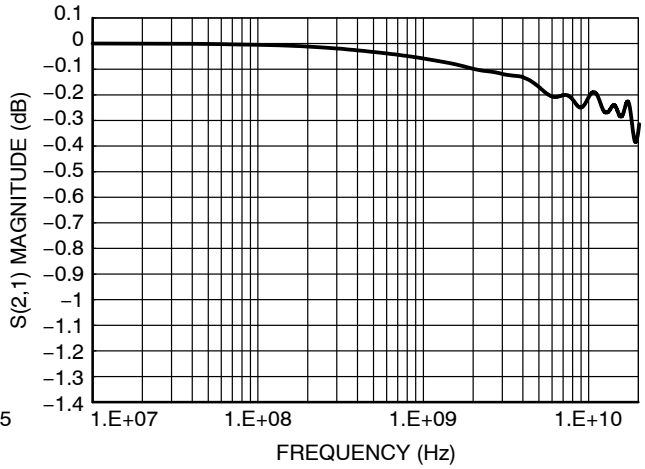


Figure 8. Insertion Loss

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

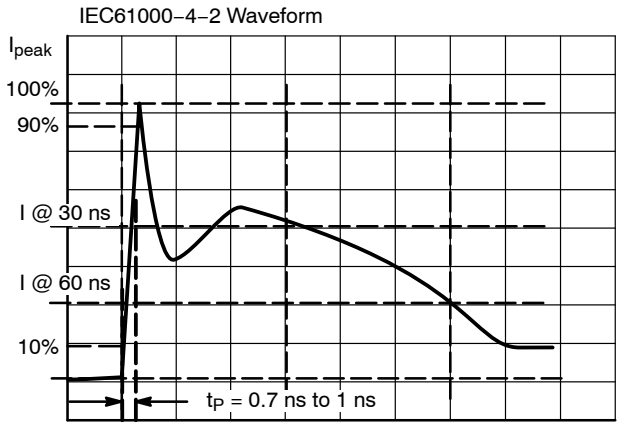


Figure 9. IEC61000−4−2 Spec

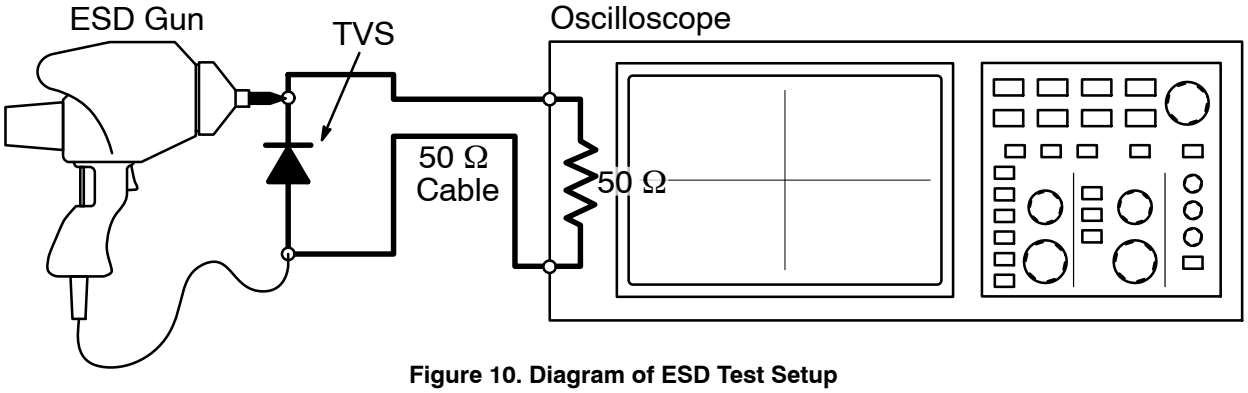


Figure 10. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

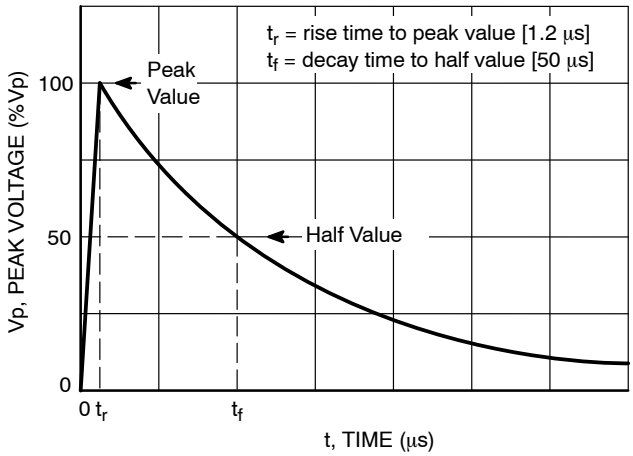
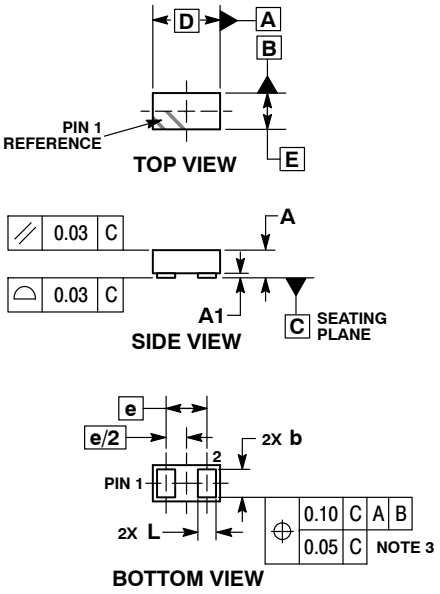


Figure 11. IEC61000−4−5 1.2/50 μs Pulse Waveform

X4DFN2, 0.445x0.24, 0.27P
CASE 718AA
ISSUE A

SCALE 10:1

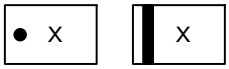
DATE 21 MAR 2017



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.15	0.18	0.21
A1	---	---	0.03
b	0.170	0.185	0.200
D	0.415	0.445	0.475
E	0.210	0.240	0.270
e	0.270 BSC		
L	0.105	0.120	0.135

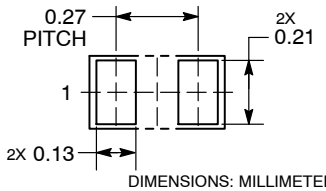
GENERIC MARKING DIAGRAMS*



X = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

See Application Note AND8398/D for more mounting details

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**X4DFN2, 0.445X0.24, 0.27P**		**PAGE 1 OF 1**

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