ESW5210/5211

27MHz FSK Receiver

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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Contents

Specification Revision History

Version	Revision Description	Date
1.0	Initial Release Edition	2000/06/05

1 Introduction

The ESW5210/5211 single-chip solution is an integrated circuit intended for use as a low cost FSK receiver to establish a frequency-agile RF link. The device is designed to provide a 10-channel receiver and intended for digital (FSK) modulated applications in the wireless Mouse and Keyboard. The chip operates at 2.7V minimum and is expressly designed for low power consumption. It offers synthesizer with a typical channel spacing of approximately 30KHz to allow narrow-band applications.

2 Feature Description

- On-Chip Phase-Locked Loop (PLL)
- Include oscillation circuit with external X-TAL (4.0MHz).
- Standby mode for power saving.
- 2.7 to 5.5V power supply range

3 Application

- Wireless Mouse
- Wireless Keyboard
- Wireless Communication Products

4 Block Diagram

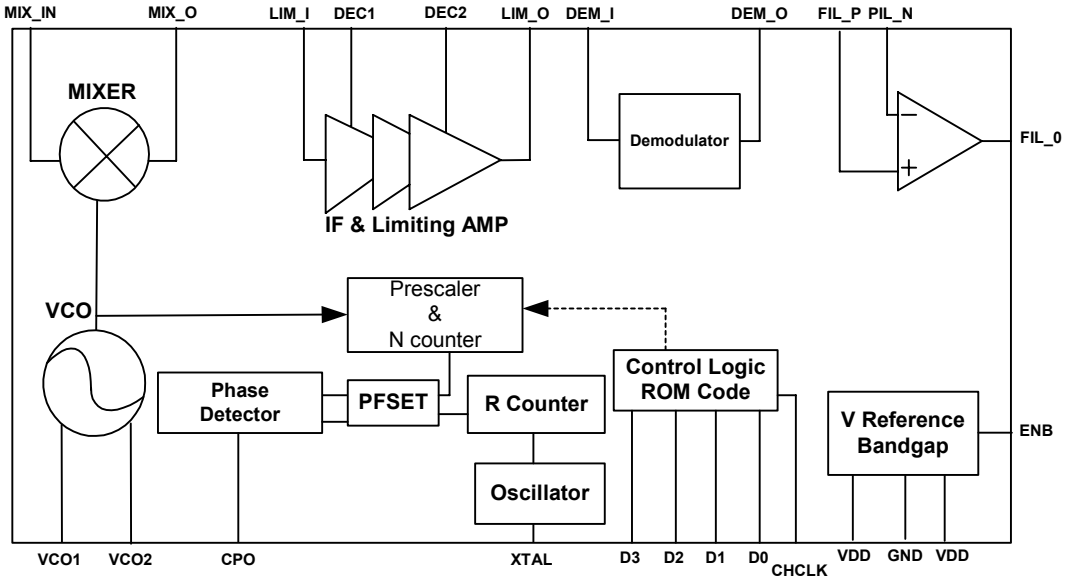


Figure 4-1 ESW5210/5211 Block Diagram

5 Pin Configuration

5.1 Pin Assignment

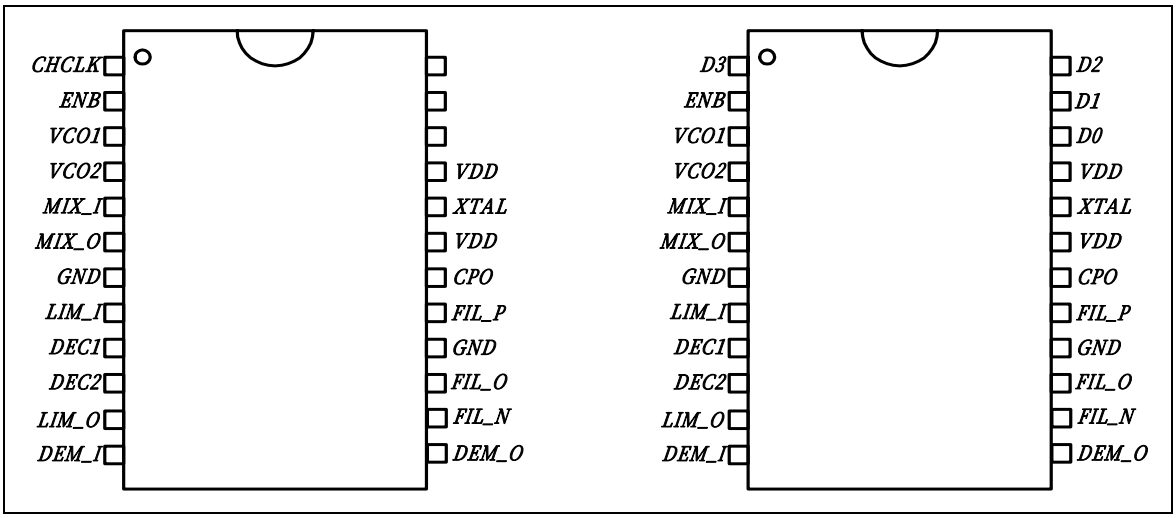


Figure 5-1 ESW5210/5211 SOP-24L (300mil) Package

5.2 Pin Descriptions

Pin No		Pin Name	Description
ESW5210	ESW5211		
19, 21	19, 21	VDD	Positive power. A 0.1 μF de-coupling capacitor should be connected as close as possible from this pin to ground
7,16	7,16	GND	This pin should be a low inductance, direct connection to ground.
2	2	ENB	Active Low, enable input
20	20	XTAL	Crystal (4MHz) Connection Input
5	5	MIX_I	RF signal input for mixer
6	6	MIX_O	Mixer signal output
8	8	LIM_I	Inter Frequency Amplifier input
11	11	LIM_O	Limiting amplifier output
12	12	DEM_I	Demodulator input
13	13	DEM_O	Demodulator output
14	14	FIL_N	Filter amplifier negative input
15	15	FIL_O	Filter amplifier output
17	17	FIL_P	Filter amplifier positive input
9	9	DEC1	IF decoupling. External 0.1μFcapacitor connected to ground
10	10	DEC2	IF decoupling. External 0.1μFcapacitor connected to ground
3	3	VCO1	For external LC tank
4	4	VCO2	For external LC tank
18	18	CPO	Phase detector output, connected to external low pass filter
1	–	CHCLK	Clock input for channel selection
–	1	D3	The channel selected pin
Reserved	22	D0	The channel selected pin
Reserved	23	D1	The channel selected pin
Reserved	24	D2	The channel selected pin.

6 Function Description

The ESW5210/5211 single-chip solution is a CMOS technology integrated circuit intended for low cost FSK receiver application and to establish a frequency-agile RF link. The device is capable of providing 10-channel receiver.

6.1 Mixer and Limiter

The mixer-oscillator (VCO) combination converts the input frequency (e.g., 27MHz) down to 455KHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. After suitable bandpass filtering (ceramic or LC), the signal goes to the input of limiter amplifier at Pin 8. The output of the limiter at Pin 11 drives a multiplier to detect the FM. This is accomplished both internally (direct access), and externally through a quadrature coil or discriminator. The other side of the limiter stages is decoupled at Pins 9 and 10. The limiter IF amplifier typically has about 75dB of gain. Decoupling capacitors should be placed close to the decoupling Pins 9 and 10 to ensure low noise and stable operation.

A simple inverter OP amp is provided with an output at Pin 15 providing DC bias to be input at Pin 14, and positive input at Pin 17 for reference voltage set. The filter can be made with external impedance elements to discriminate between frequencies.

6.2 VCO

The circuit employed an LC-tank structure to achieve low-phase noise characteristic where “L” is an off-chip high-Q inductor, and “C” is provided by a varactor with different tuning ranges.

6.3 PLL

The PLL includes 64/65 prescaler, charge pump, PFD, N-A swallow counters, and R-counter for the multi-channel applications. The channels are selected for ESW5211 via mechanical switches of parallel BCD input. For ESW5210, the channels can be easily set by an input pin CHCLK which directly selects the ROM table addresses.

6.4 Channel Selections

6.4.1 ESW5210

The channel is set by rising edge of clock at Pin 1 (CHCLK) of MCU. The initial or default channel at power on (internal power on reset) is set at Channel 10.

6.4.2 ESW5211

The input provides BCD code for selecting one of ten channels to be locked in both transmit and receive loop. When address data other than 1 – 10 are input, the decoding logic defaults to channel 10. The frequency assignments with D0 – D3 are shown in the table below. The D0 – D3 inputs have internal pull up devices.

■ **VCO Frequency and Divider Ratio**

Oscillator Frequency 4.0MHz, Ref. Divider 800

Channel	VCO Frequency	RXO Frequency	Rx Divider (5.0KHz Ref)	Input			
				D3	D2	D1	D0
1	26.530 MHz	26.985MHz	5306	0	0	0	1
2	26.560 MHz	27.015 MHz	5312	0	0	1	0
3	26.590 MHz	27.045 MHz	5318	0	0	1	1
4	26.620 MHz	27.075MHz	5324	0	1	0	0
5	26.650 MHz	27.105 MHz	5330	0	1	0	1
6	26.680 MHz	27.135 MHz	5336	0	1	1	0
7	26.710 MHz	27.165 MHz	5342	0	1	1	1
8	26.740 MHz	27.195 MHz	5348	1	0	0	0
9	26.770 MHz	27.225MHz	5354	1	0	0	1
10	26.800 MHz	27.255MHz	5360	1	0	1	0
-	26.800 MHz	27.255MHz	5360	1	0	1	1
-	26.800 MHz	27.255MHz	5360	1	1	0	0
-	26.800 MHz	27.255MHz	5360	1	1	0	1
-	26.800 MHz	27.255MHz	5360	1	1	1	0

NOTE: ***1:*** *open;* ***0:*** *ground*

6.4.3 Channel Clock Timing

■ **Timing Diagram**

Channel DATA by $F_{DIVIDER}$ Clock

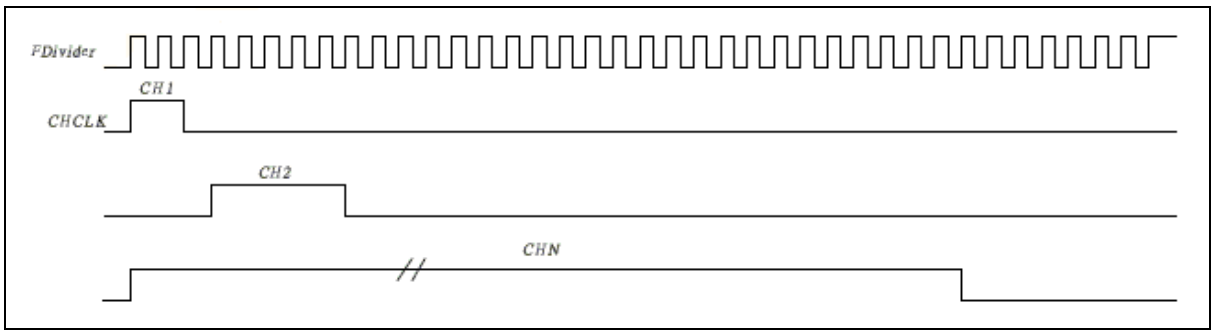


Figure 6-1 ESW5210/ ESW5211 Timing Diagram

■ **Channel Clock Timing**

The channel clock tolerance of the CHCLK signal should be within ± 150μS.

Channel	CHCLK
1	600μS
2	1.2mS
3	1.8mS
4	2.4mS
5	3.0mS

Channel	CHCLK
6	3.6mS
7	4.2mS
8	4.8mS
9	5.4mS
10	6.0mS

NOTE

■ *Only Channel 10 applies to ESW5210*

■ *Channels 1 ~ 10 applies to ESW5211*

7 Absolute Operation Maximum Ratings

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.3 to 6	V
Input Voltage	V_{in}	−0.5 to V_{DD}+0.5	V
Operating Temperature Range	Ta	0 to 70	°C

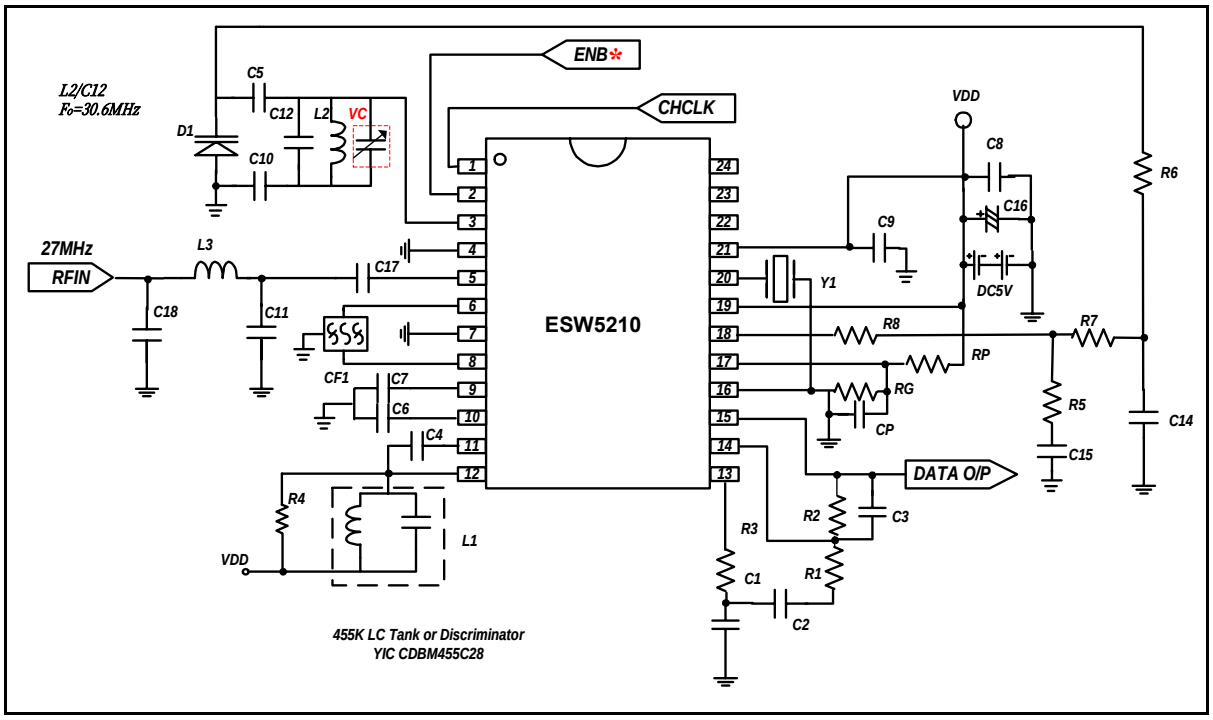
8 DC/AC Electrical Characteristic

(VDD=3.0V VSS=0V)

Parameter	Min.	Typical	Max.	Unit
Overall				
Operating Voltage	2.7		5.5	V
Current Consumption: Operating Mode Power Down Mode		 6	 10	 mA μA
Mixer				
Mixer input signal frequency		27		MHz
Mixer input impedance		2.65K-j5.7K		
Conversion gain		28		dB
Noise figure		14.8		dB
IIP3		−28		dBm
Lo Leakage to Mixer input	-40			dBm
IF Section				
Limiter Amp Voltage Gain		75		dB
S/N Ratio @60dBμV		40		dB
Sensitivity @12dB SINAD	-90			dBm
Filter Amplifier				
Voltage Gain		80		dB
PLL Section				
PLL Operating Frequency		27		MHz
OSC Operating Frequency		4		MHz
VCO phase noise: 100KHz offset 1MHz offset		 −90 −110		dBc/Hz
VCO Sensitivity		0.8		MHz/V
Output rise time			200	ns
Output fall time			200	ns
CHCLK				
Input rise time			10	μs
Input fall time			10	μs
BCD Input				
Pull up resistance	300			KΩ

9 Application Circuit

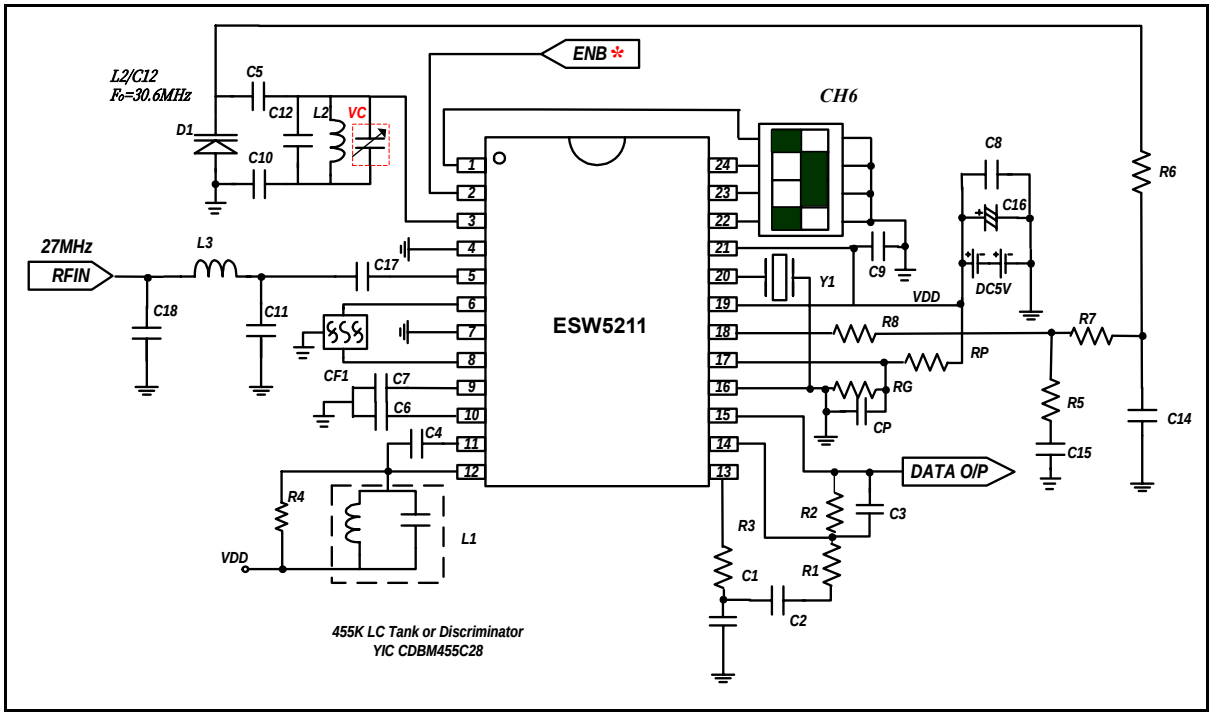
9.1 ESW5210



* **ENB:** *"Low" for Operating Mode / "High" for Idle Mode*

Figure 9-1 ESW5210 Application Circuit

9.1 ESW5211



* **ENB:** *"Low" for Operating Mode / "High" for Idle Mode*

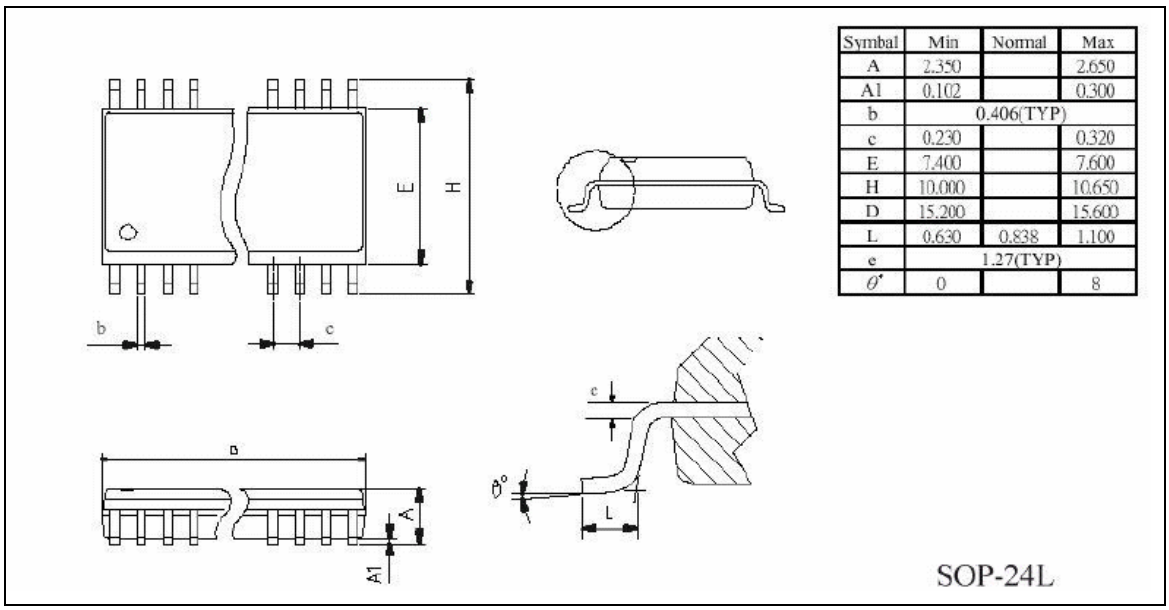
Figure 9-2 ESW5211 Application Circuit

10 Components List

Item	Part Type	Designators	Manufacturer	Remarks
1	C.F Resistor 2K2Ω	R8.	Walsin or equalvalent	
2	C.F Resistor 100Ω	R1.	Walsin or equalvalent	
3	C.F Resistor 22KΩ	R7.	Walsin or equalvalent	
4	C.F Resistor39KΩ	R3.	Walsin or equalvalent	
5	C.F Resistor 47KΩ	R5.	Walsin or equalvalent	
6	C.F Resistor 100KΩ	R6, R9, R10.	Walsin or equalvalent	
7	C.F Resis tor 10MΩ	R2.	Walsin or equalvalent	
8	Ceramic Capacitor 30P NPO	C10.	Walsin or equalvalent	
9	Ceramic Capacitor 33P NPO	C11.	Walsin or equalvalent	
10	Ceramic Capacitor 150P NPO	C5.	Walsin or equalvalent	
11	Ceramic Capacitor 220P NPO	C18.	Walsin or equalvalent	
12	Ceramic Capacitor 1n X7R	C17.	Walsin or equalvalent	
13	Ceramic Capacitor 820P X7R	C1.	Walsin or equalvalent	
14	Ceramic Capacitor 10n X7R	C2.	Walsin or equalvalent	
15	Ceramic Capacitor 4n7 X7R	C14.	Walsin or equalvalent	
16	Ceramic Capacitor 100n X7R	C6,C7, C8, C9.	Walsin or equalvalent	
17	Ceramic Capacitor 100n X7R	C15.	Walsin or equalvalent	
18	Electrolytic Capacitor 100u 6.3V	C16.	Walsin or equalvalent	
19	Varactor 1SV270	D1.	Toshiba	1SV229
20	Variable Inductor 820nH	L2.	Sumida or equalvalent	With 33P
21	Inductor 1uH-JWI	L3	Jantek or equalvalent	Q>30
22	Crystal 4M30P1 49US	Y1.	YIC or equalvalent	
23	Dip Switch 4P	SW1.		For ESW5211
24	Ceramic Filter 455KHz	CF1	YIC or Murata	LT455DW BW±15KHz
25	Discriminator 455KHz	L1.	YIC	CDBM455C28
26	C.F Resistor 5K1Ω	R4.		L2 with YIC-C28
27	Ceramic Capacitor 50P NPO	C4.		L2 with YIC-C28
28	ESW5210/211	U1	Elan	
29	Variable Capacitor 20P	VC		

11 Packaging Reference

- Dimension: mm



Symbal	Min	Normal	Max
A	2.350		2.650
A1	0.102		0.300
b	0.406(TYP)		
c	0.230		0.320
E	7.400		7.600
H	10.000		10.650
D	15.200		15.600
L	0.630	0.838	1.100
e	1.27(TYP)		
θ°	0		8

Figure 11-1 ESW5210/5211 SOP Packaging Dimensions

12 Receiver Demo Board Introduction

12.1 Top View

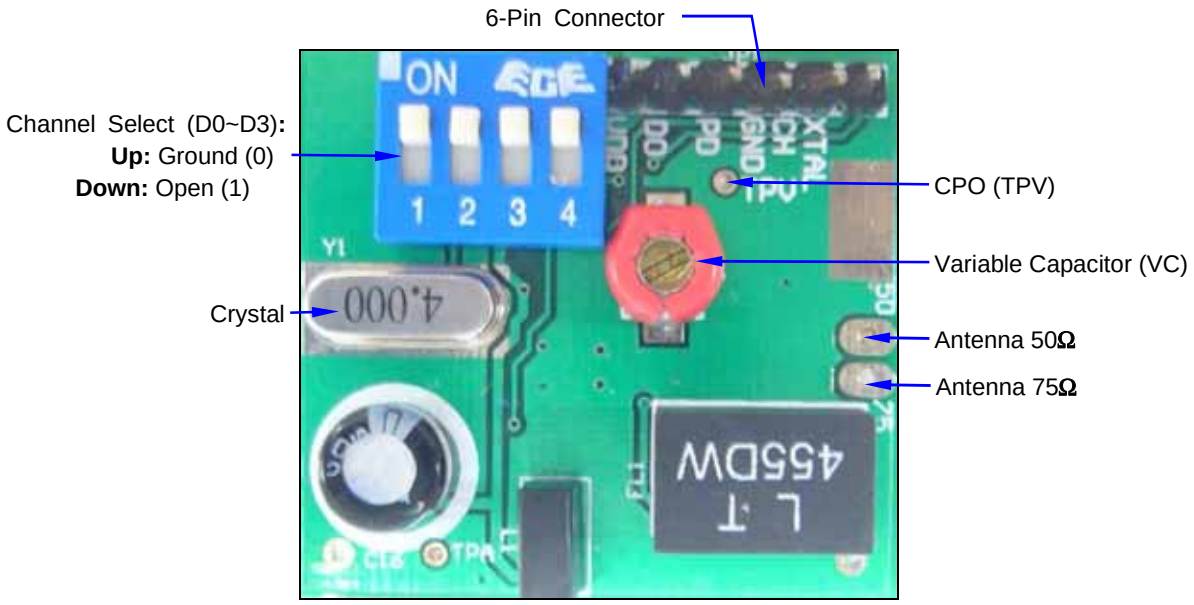


Figure 12-1 ESW5210/5211 RX Board (Top View)

NOTE

1. ***CPO:*** *When Channel-10 is selected, adjust VC until the TPV is at 2 Voltage.*
2. ***ENB:*** *Should be Active Low in order to enable input.*

12.2 Bottom View

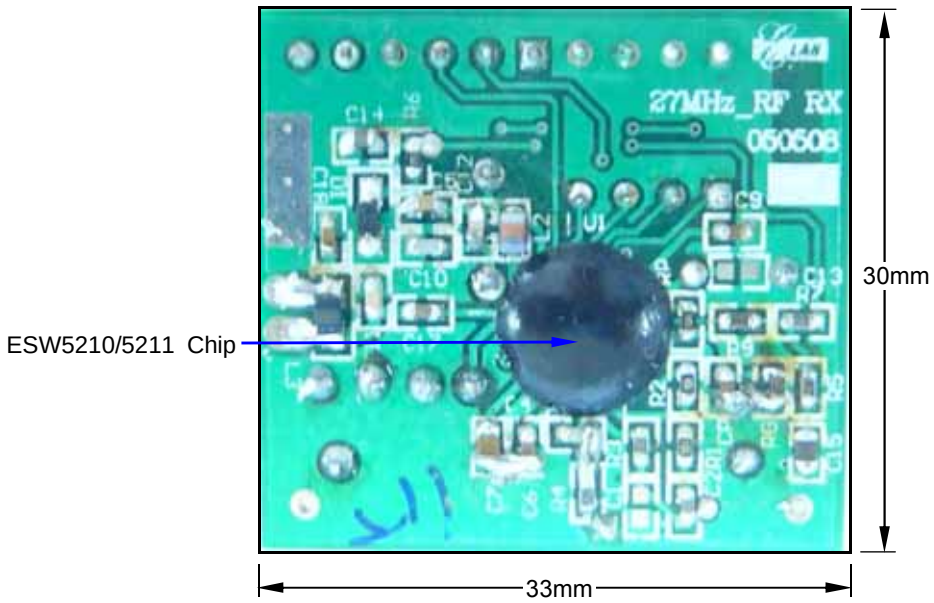


Figure 12-2 ESW5210/5211 RX Board (Bottom View)