尔 泰 科 技
ET TECHNOLOGY

PRODUCT SPECIFICATION
FOR LCD MODULE

MODULE NO. : ET-G240160B
REVERSION : V1
TYPE : COB

Customer Approval:

PREPARED BY		DATE	
CHECKED BY		DATE	
APPROVED BY		DATE	

DOCUMENT REVISION HISTORY

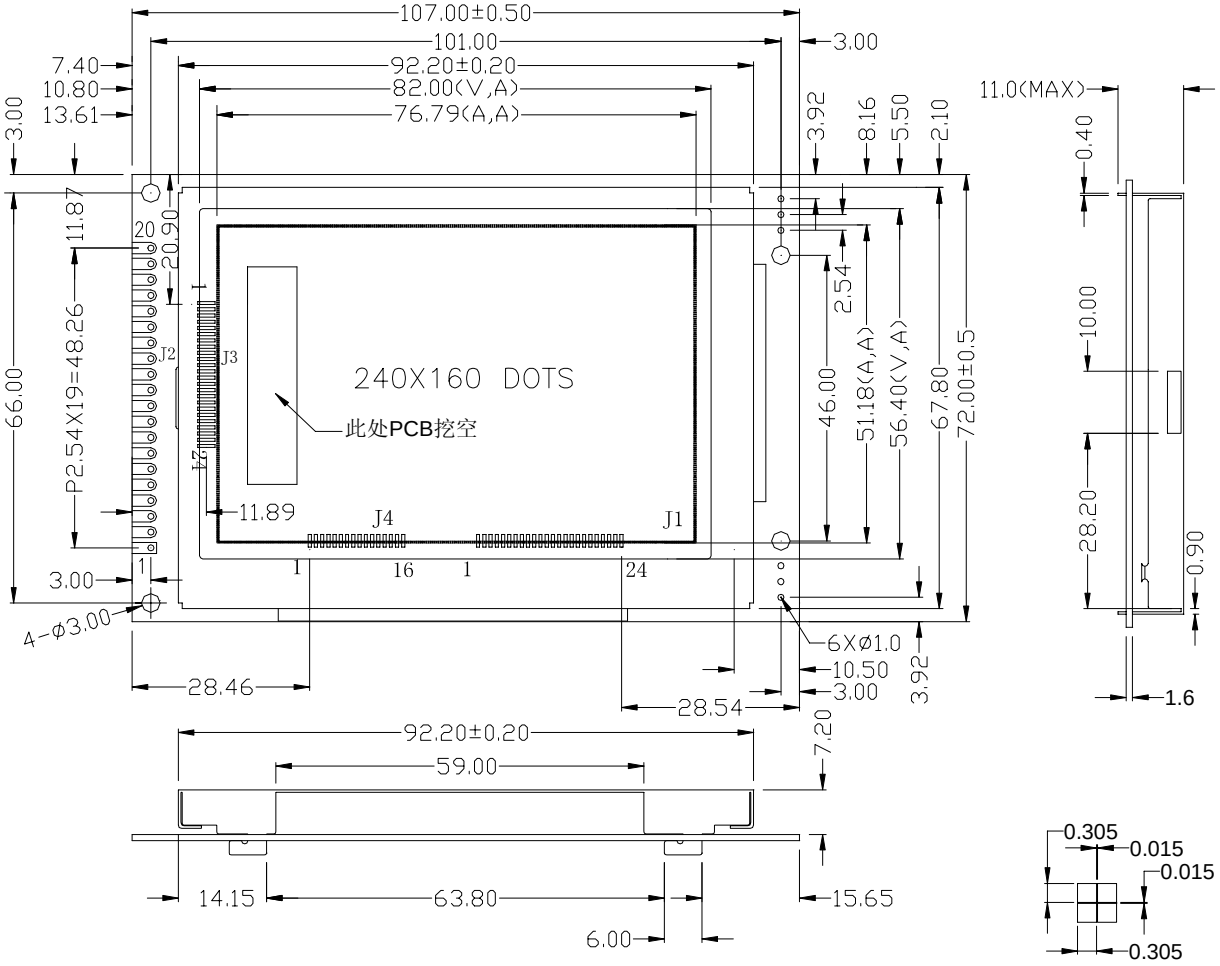
VERSION	DATE	DESCRIPTION	CHANGED BY
V1	JAN. 28. 2011	First issue	OU

1. General Specifications

Item	Standard Value	Unit
Number of dots	240(W)X160(H)	dots
Display Pattern	■Dot-Graphic ☐Character ☐Digits ☐with ICON ☐_____	
Module Dimension	107(W) X 72.0(H) X 11.0(T)	mm
Viewing Area	82.0 (W) X 56.4(H)	mm
Active Area	76.79(W) x 51.18(H)	mm
DOT Size	0.305(W) x 0.305(H)	mm
DOT Pitch	0.32(W) x 0.32(H)	mm
LCD Type	☐ TN,Positive ☐ TN, Negative ☐ HTN, Positive ☐ HTN, Negative ☐ STN, Yellow-Green ☐ STN, Gray ☐ STN, Blue ☐ FSTN, Positive ☐ FSTN, Negative ☐ Color STN ☐ FM LCD	
Polarizer Type	☐Transmissive ☐Reflective ☐Transflective ☐Anti-Glare	
View Direction	☐ 6H ☐ 12H ☐_____	
Operation Voltage	☐3.0(3.3) ☐5.0 ☐_____	V
DC-DC Converter	☐Build-in ☐External	
LCD Controller IC	■Build-in (RA8806) ☐ not Build-in	
LCD Driver IC	NT7086PQ	
LCD Driving Method	1/240duty, 1/17bias	
Interface Type	☐6800 ☐ 8080 ☐ I2C ☐ Serial ☐ SPI	
Backlight Type	☐ LED ☐ CCFL ☐ EL ☐no Backlight ☐____	
Backlight Color	☐Yellow-Green ☐ White ☐ Amber ☐ Blue ☐ Red ☐_____	
EL/CCFL Driver type	☐ Build-in ☐External	
Touch Panel IC	☐ Build-in ☐ not Build-in	
Touch Panel	☐ Build-in ☐ not Build-in	
Operation Temperature(oC)	-20~70 (T_{OPL} – T_{OPH})	deg..
Storage Temperature (oC)	-30~80 (T_{STL} -- T_{STH})	deg..

Note: Label "■ " means the option selected.

2. External Dimensions



3. Pin Description

3.1 J1(SMD24 , Pitch=1.0mm)

Pin.No	Symbol	Lever	Description
1	VSS	P	GND.
2	VDD	P	Power supply for logic and LCD.
3	V0	P	Operating voltage for LCD.
4	A0	I	Data type select
5	/WR	I	Write signal
6	/RD	I	Read signal
7-14	DB0-DB7	I/O	Data bus.
15	/CS	I	Chip select
16	/RST	I	Reset signal(Low effective).
17	VEE	P	Voltage output to LCD
18	LEDA	P	Backlight anode (+5V).
19	NC	/	No connection

20	NC	/	No connection
21	NC	/	No connection
22	NC	/	No connection
23	INT	O	RA8806 Interrupt.
24	NC	/	No connection

3.2 J2(DIP20 , Pitch=2.54mm)

Pin.No	Symbol	Lever	Description
1	VSS	P	GND.
2	VDD	P	Power supply for logic and LCD.
3	V0	P	Operating voltage for LCD.
4	/WR	I	Write signal
5	/RD	I	Read signal
6	/CS	I	Chip select
7	A0	I	Data type select
8	/RST	I	Reset signal(Low effective).
9-16	DB0-DB7	I/O	Data bus.
17	LEDA	P	Backlight anode (+5V).
18	VEE	P	Voltage output to LCD
19	LEDA	P	Backlight anode (+5V).
20	LEDK	P	Backlight anode (0V).

3.3 J3(DIP20 , Pitch=2.54mm)

Pin.No	Symbol	Lever	Description
1	FLM(Frame)	P	Input / output for chip select or data of the shift register
2	V1(V2)	P	Power supply for LCD driver
3	V4(V5)	P	Power supply for LCD driver
4	VDD	I	Power supply for logic and LCD
5	V0	I	Power supply for LCD driver
6	CL1(Load)	I	Latch pulse input/shift clock input for the shift register
7	CL2(Cp)	I	Display data shift clock input for segment mode
8	M(Df)	I	AC-converting signal input for LCD driver waveform
9	/D-OFF	I/O	Control input for deselect output level
10-13	D0-D3	I/O	Display data input for segment mode
14	VSS	P	GND
15	V2(V3)	P	Power supply for LCD driver
16	V3(V4)	P	Power supply for LCD driver.

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage(Logic)	VDD - VSS	--	- 0.3	6.5	V
Supply Voltage (LCD Drive)	VLCD - VSS	--	0	35.0	V
Input Voltage	VI	--	-0.3	VDD + 0.3	V

4.2 DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Voltage(1)	V_{DDP} / V_{DDH}	4.5	5.0	5.5	V	V_{DDP} = V_{DDH} (Refer to Figure 6-31)
Operating Voltage(2)	V_{DDP} / V_{DD}	2.4	3.3	3.6	V	V_{DDP} = V_{DD} V_{DDH} Open (Refer to Figure 6-30)
Oscillator frequency	F_{OSC}	4	8	12	MHz	V_{DD} = 5V
External clock frequency	F_{CLK}	4	8	12	MHz	V_{DD} = 5V
DC to DC Output Voltage	V_{DD}	2.8V	3.0	3.3	V	Add external 1uF Capacitor
Input						
Input High Voltage	V_{IH}	0.8xV_{DD}	--	V_{DD}	V	See Note 1, 3
Input Low Voltage	V_{IL}	Gnd	--	0.2xV_{DD}	V	See Note 1, 3
Output						
Output High Voltage	V_{OH}	V_{DD}-0.4	--	V_{DD}	V	See Note 2, 3
Output Low Voltage	V_{OL}	Gnd	--	V_{DD}+0.4	V	See Note 2, 3
Schmitt-trigger						
Output High Voltage	V_{OH}	0.5xV_{DD}	0.7xV_{DD}	0.8xV_{DD}	V	See Note 4
Output Low Voltage	V_{OL}	0.2xV_{DD}	0.3xV_{DD}	0.5xV_{DD}	V	See Note 4
Input Leakage Current 1	I_{IH}	--	--	+1	μA	
Input Leakage Current 2	I_{IL}	--	--	-1	μA	
Operation Current	I_{OPR}	1	5	10	mA	
Standby Mode Current	I_{SB}	--	1.5	1.8	mA	Case1
(Normal Mode Current)			1.8	2.1	mA	Case2
Display Off Current	$I_{DISPLAY}$	--	120	140	μA	Case1
			140	160	μA	Case2
Sleep Mode	I_{SLP}	--	0.5	1	μA	Case1
		--	20	25	μA	Case2

Notes:

1. ZCS1, CS2, ZWR, ZRD, RS, MI, DW, DB, KIN[7:0], TESTMD and TESTI are inputs. KIN[7:0] built-in pull up resistors. The TESTMD and TESTI built-in pull down resistors.
2. INT, BUSY, CLK_OUT, PWM_OUT, KOUT[7:0], LP, FR, YD, ZDOFF, XCK and LD[7:0] are outputs.
3. DATA[7:0] are Bi-direction.
4. The ZRST are Schmitt-trigger with pull-up input. The pulse width on ZRST must be at least 1024*tc. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.

Case1: V_{DDP} = V_{DD} = A_{VDD} = 3.3V, V_{DDH} = NC, LCD Driver VDD = 5V, CLK = 4MHz, CLK_OUT: Off, Segment=160, Common=160, FRM = 78Hz, T_A=25℃.

Case2: V_{DDP} = V_{DDH} = 5V, V_{DD} = A_{VDD} = 3V, LCD Driver VDD = 3.3V, CLK = 4MHz, CLK_OUT: Off, Segment=160, Common=160, FRM = 78Hz, T_A=25℃.

4.3 8080 family interface timing

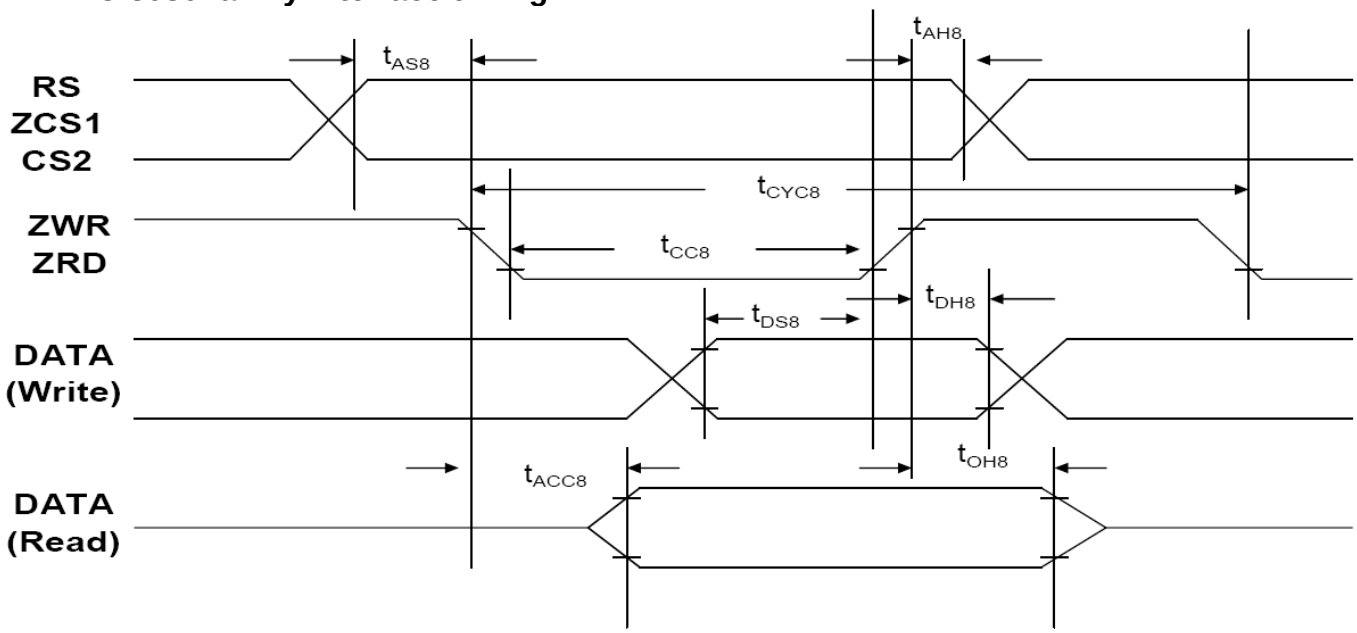


Figure 4-1: 8080 Family Interface Timing

Symbol	Description	Rating		Unit	Condition
		Min.	Max.		
t_{CYC8}	Cycle time	2*tc	--	ns	tc = one system clock period
t_{CC8}	Strobe Pulse width	50	--	ns	
t_{AS8}	Address setup time	0	--	ns	
t_{AH8}	Address hold time	20	--	ns	
t_{DS8}	Data setup time	30	--	ns	
t_{DH8}	Data hold time	20	--	ns	
t_{ACC8}	Data output access time	0	20	ns	
t_{OH8}	Data output hold time	0	10	ns	

4.4 6800 Family Interface Timing

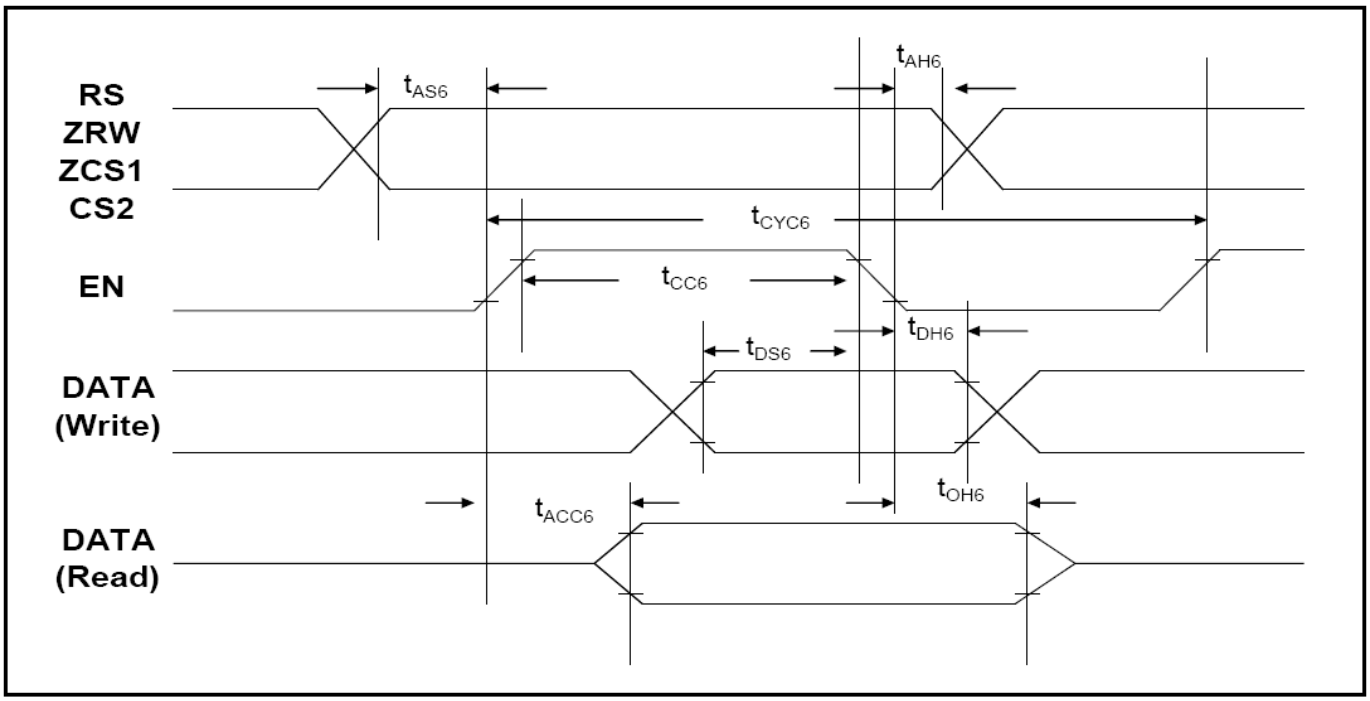


Figure 4-2: 6800 Family Interface Timing

Symbol	Description	Rating		Unit	Condition
		Min.	Max.		
t_{CYC6}	Cycle time	2*tc	--	ns	tc is one system clock period: tc = 1/CLK
t_{CC6}	Strobe Pulse width	50	--	ns	
t_{AS6}	Address setup time	0	--	ns	
t_{AH6}	Address hold time	20	--	ns	
t_{DS6}	Data setup time	30	--	ns	
t_{DH6}	Data hold time	20	--	ns	
t_{ACC6}	Data output access time	0	20	ns	
t_{OH6}	Data output hold time	0	10	ns	

5. Register List Table

REG#	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
--	STATUS	MBUSY	SBUSY	SLEEP			WAKE_STS	KS_STS	TP_STS	--
00h	WLCR	PWR	LINEAR	SRST	--	TEXT_MD	ZDOFF	GBLK	GINV	00h
01h	MISC	NO_ FLICKER	CLKO_SEL	BUSY_ LEV	INT_LEV	XCK_SEL1	XCK_SEL0	SDIR	CDIR	04h
03h	ADSR	SCR_PEND	--	--	--	BIT_INV	SCR_DIR	SCR_HV	SCR_EN	00h
0Fh	INTR	--	WAKI_EN	KEYI_EN	TPI_EN	TP_ACT	WAK_STS	KEY_STS	TP_STS	00h
10h	WCCR	CUR_INC	FULL_OFS	BIT_REV	BOLD	T90DEG	CUR_EN	CUR_BLK	---	00h
11h	CHWI	CURH3	CURH2	CURH1	CURH0	ROWH3	ROWH 2	ROWH 1	ROWH 0	00h
12h	MAMR	CUR_HV	DISPMD2	DISPMD1	DISPMD0	L_MIX1	L_MIX 0	MW_MD1	MW_MD0	11h
20h	AWRR	--	--	AWR5	AWR4	AWR3	AWR2	AWR1	AWR0	27h
21h	DWWR	--	--	DWW5	DWW 4	DWW 3	DWW 2	DWW 1	DWW 0	27h
30h	AWBR	AWB7	AWB6	AWB5	AWB4	AWB3	AWB2	AWB1	AWB0	EFh
31h	DWHR	DWH7	DWH6	DWH5	DWH4	DWH3	DWH2	DWH1	DWH0	EFh
40h	AWLR	--	--	AWL5	AWL4	AWL3	AWL2	AWL1	AWL0	00h
50h	AWTR	AWT7	AWT6	AWT5	AWT4	AWT3	AWT2	AWT1	AWT0	00h
60h	CURX	--	--	CURX5	CURX4	CURX3	CURX2	CURX1	CURX0	00h
61h	BGSG	--	--	BGSG5	BGSG4	BGSG3	BGSG2	BGSG1	BGSG0	00h
62h	EDSG	EDSG7	EDSG6	EDSG5	EDSG4	EDSG3	EDSG2	EDSG1	EDSG0	00h
70h	CURY	CURY7	CURY6	CURY5	CURY4	CURY3	CURY2	CURY1	CURY0	00h
71h	BGCM	BGCM7	BGCM6	BGCM5	BGCM4	BGCM3	BGCM2	BGCM1	BGCM0	00h
72h	EDCM	EDCM7	EDCM6	EDCM5	EDCM4	EDCM3	EDCM2	EDCM1	EDCM0	00h
80h	BTMR	BLKT7	BLKT6	BLKT5	BLKT4	BLKT3	BLKT2	BLKT1	BLKT0	00h
90h	ITCR	ITC7	ITC6	ITC5	ITC4	ITC3	ITC2	ITC1	ITC0	00h
A0h	KSCR1	KEY_EN	KEY4X8	KSAMP1	KSAMP0	LKEY_EN	KF2	KF1	KF0	00h
A1h	KSCR2	KWAK_EN	--	--	--	LKEY_T1	LKEY_T0	KEYNO1	KEYNO0	00h
A2h	KSDR0	KSD07	KSD06	KSD05	KSD04	KSD03	KSD02	KSD01	KSD00	00h
A3h	KSDR1	KSD17	KSD16	KSD15	KSD14	KSD13	KSD12	KSD11	KSD10	00h
A4h	KSDR2	KSD27	KSD26	KSD25	KSD24	KSD23	KSD22	KSD21	KSD20	00h
B0h	MWCR	MWD7	MWD6	MWD5	MWD4	MWD3	MWD2	MWD1	MWD0	--
B1h	MRCR	MRD7	MRD6	MRD5	MRD4	MRD3	MRD2	MRD1	MRD0	--
C0h	TPCR1	TP_EN	TP_SMP2	TP_SMP1	TP_SMP0	TPWAK _EN	ACLK2	ACLK1	ACLK0	00h
C1h	TPXR	TPX9	TPX8	TPX7	TPX6	TPX5	TPX4	TPX3	TPX2	00h
C2h	TPYR	TPY9	TPY8	TPY7	TPY6	TPY5	TPY4	TPY3	TPY2	00h
C3h	TPZR	TPX1	TPX0	--	--	TPY1	TPY0	--	--	00h
C4h	TPCR2	MTP_MD	--	--	--	--	--	MTP_PH1	MTP_PH2	00h
D0h	PCR	PWM_EN	PWM_DIS_ LEV	--	--	PCLK_R3	PCLK_R2	PCLK_R1	PCLK_R0	00h
D1h	PDCR	PDUTY7	PDUTY6	PDUTY5	PDUTY4	PDUTY3	PDUTY2	PDUTY1	PDUTY0	00h
E0h	PNTR	PND7	PND6	PND5	PND4	PND3	PND2	PND1	PND0	00h
F0h	FNCR	ISO8859_E N	--	--	--	MCLR	ASC	ASC_SEL1	ASC_SEL0	00h
F1h	FVHT	FH1	FH0	FV1	FV0	--	--	--	--	00h

6. Register Description

STATUS Register (RS = 1, ZWR = 1)

Bit	Description	Access
7	**Memory Write Busy Flag** 0 : Not busy. 1 : Busy, when font write or memory clear cycle is running, the busy flag = 1.	R
6	**SCAN_BUSY** 0 : Not busy. 1 : When driver scan logic is not idle(i.e. XCK is active), SCAN_BUSY = 1.	R
5	**SLEEP** 0 : Normal mode. 1 : Sleep mode.	R
4-3	**NA**	R
2	**Wakeup Status bit** (The same with REG[0Fh] Bit-2.)	R
1	**KS Status bit** (The same with REG[0Fh] Bit-1.)	R
0	**TP Status bit** (The same with REG[0Fh] Bit-0.)	R

REG [00h] Whole Chip LCD Controller Register (**WLCR**)

Bit	Description	Default	Access
7	**Power Mode** 0 : Normal Mode. All of the functions of RA8806 are available in this mode. 1 : Sleep Mode. When RA8806 is in Sleep mode, all of functions enter off mode, except the wake-up trigger block. If wake-up event occurred, RA8806 would wake-up and return to Normal mode.	0	R/W
6	**Linear Decode mode** This bit is used to define the Font ROM address mapping rule. The standard product is set to 0. And 1 for special application that when user a want to create a new Mask Code. 0 : BIG5/GB ROM mapping rule. 1 : User-defined ROM mapping rule.	0	R/W
5	**Software Reset** 0 : Normal Operation. 1 : Reset all registers except the contents of Display Data RAM (Only work at Normal mode). When this bit set to "1", the next MPU cycle for RA8806 have to wait 3 clocks at least.	0	R/W
4	**Reserved**	0	R
3	**Text Mode Selection** 0 : Graphical Mode. The written data will be treated as a bit-map pattern. 1 : Text Mode. The written data will be treated as an ASCII, BIG5 or GB code.	0	R/W

2	**Set Display On/Off Selection** The bit is used to control LCD Driver Interface signal – "DISP_OFF". 0 : DISP_OFF pin output low(Display Off). 1 : DISP_OFF pin output high(Display On).	0	R/W
1	**Blink Mode Selection** 0 : Normal Display. 1 : Blink Full Screen. The blink time is set by register BTMR.	0	R/W
0	**Inverse Mode Selection** 0 : Normal Display. 1 : Inverse Full Screen. It will cause the display inversed.	0	R/W

REG [01h] Misc. Register (**MISC**)

Bit	Description	Default	Access
7	**Eliminating Flicker** 1 : Eliminating flicker mode, scan will auto-pending when busy. 0 : Normal mode.	0	R/W
6	**Clock Output** (Pin CLK_OUT) Control 1 : The pin "CLK_OUT" indicates the SLEEP state of Status Register(0: Normal Mode, 1: Sleep Mode). 0 : The pin "CLK_OUT" is the output of Internal system clock.	0	R/W
5	**Busy Polarity (for "BUSY" pin)** 1 : Set Active High. 0 : Set Active Low.	0	R/W
4	**Interrupt Polarity (for "INT" pin)** 1 : Set Active High. 0 : Set Active Low.	0	R/W
3-2	**Driver Clock Selection** These two bits are used to select the clock frequency of XCK. 0 0 : XCK = CLK/8 0 1 : XCK = CLK/4 (Default) 1 0 : XCK = CLK/2 1 1 : XCK = CLK The "CLK" means system clock.	01	R/W
1	**SEG Scan Direction**(SDIR) 0 : SEG order is 0 ~ 319. 1 : SEG order is 319 ~ 0.	0	R/W
0	**COM Scan Direction**(CDIR) 0 : COM order 0 ~ 239. 1 : COM order 239 ~ 0.	0	R/W

REG [03h] Advance Display Setup Register (**ADSR**)

Bit	Description	Default	Access
7	**Scroll Function Pending** 1 : Scroll function pending 0 : Scroll function keep active **Note:** When SCR_HV(Bit-1) and SCR_EN(Bit-0) are changed, the function does not support.	0	R/W
6-4	**Reserved**	000	R

3	**BIT_ORDER**(Set driver data output bit order) 1 : Inverse driver output data order(Bit-7 to Bit-0, Bit-6 to Bit-1 and so on) 0 : Normal Mode	0	R/W
2	**SCR_DIR**(Scroll Direction) When SCR_HV = 0(Horizontal Scroll) 0 : Left → Right. 1 : Right → Left. When SCR_HV = 1(Vertical Scroll) 0 : Top → Bottom. 1 : Bottom → Top.	0	R/W
1	**SCR_HV**(Scroll Horizontal/Vertical) 0 : Segment Scrolling(Horizontal). 1 : Common Scrolling(Vertical).	0	R/W
0	**SCR_EN**(Scroll Enable) 1 : Scroll function enable. 0 : Scroll function disable.	0	R/W

REG [0Fh] Interrupt Setup and Status Register (**INTR**)

Bit	Description	Default	Access
7	**Reserved**	0	R
6	**Wakeup Interrupt Mask** 1 : Enable wake-up Interrupt. 0 : Disable wake-up Interrupt.	0	R/W
5	**Key-Scan Interrupt Mask** 1 : Enable Key-Scan Interrupt. 0 : Disable Key-Scan Interrupt.	0	R/W
4	**Touch Panel Interrupt Mask** 1 : Generate interrupt output if touch panel was detected. 0 : Don't generate interrupt output if touch panel was detected.	0	R/W
3	**Touch Panel Event**(Only activate in TP Manual mode) 1 : Touch panel is touched. 0 : Touch panel is not touched.	0	R
2	**Wakeup Interrupt Status bit** 1 : Interrupt that indicate wake-up event happen from Sleep mode. 0 : No wake-up interrupt happen. User must write "0" to clear the Status bit.	0	R/W
1	**Key-Scan Interrupt Status bit** 1 : Key-Scan Detects Key Input. 0 : Key-Scan doesn't Detect Key Input. User must write "0" to clear the Status bit.	0	R/W
0	**Touch Panel Detect Status bit** 1 : Touch Panel Touched. 0 : Touch Panel Untouched. User must write "0" to clear the Status bit.	0	R/W

REG [10h] Whole Chip Cursor Control Register (**WCCR**)

Bit	Description	Default	Access
7	**CUR_INC** (Auto Increase Cursor Position in Reading/Writing DDRAM Operation.) 1 : Disable. 0 : Enable(Auto Increase).	0	R/W
6	**FULL_OFS (Full-size and Half-size Character Alignment)** 1 : Enable, in Full-size and Half-size character mixed mode. Chinese always start at full-size alignment. 0 : Disable.	0	R/W
5	**Reversed Data Write mode** 0 : Store Current Data to DDRAM Directly. 1 : Store Current Data to DDRAM Inversely.(i.e. 01101101→ 10010010)	0	R/W
4	**Bold Font (Character Mode Only)** 1 : Bold Font 0 : Normal Font	0	R/W
3	**Font Rotate mode(T90DEG)** 1 : Font rotates 90 degree. (See Section 6-10-4 for detail) 0 : Normal font.	0	R/W
2	**Cursor Display** 1 : Set Cursor Display On. 0 : Set Cursor Display Off.	0	R/W
1	**Cursor Blinking** 1 : Blink Cursor. The blink time is determined by register BTMR. 0 : Normal.	0	R/W
0	**Reserved**	0	R

REG [11h] Cursor Height and Word Interval Register (**CHWI**)

Bit	Description	Default	Access
7-4	**Set Cursor Height** 0000 b → Height = 1 pixel. 0001 b → Height = 2 pixels. 0010 b → Height = 3 pixels. : : 1111 b → Height = 16 pixels. **Note:** In normal font, the cursor width fixed to one byte(8 pixels). And cursor's height is from 1~16pixels that depends on Bit[7:4]. In vertical font, the cursor height fixed to 16 pixels, and width is from 1~8 pixels that depends on Bit[6:4].	0000	R/W
3-0	**Set Line Gap** 0000 b → Gap = 1 pixel. 0001 b → Gap = 2 pixels. 0010 b → Gap = 3 pixels. : : 1111 b → Gap = 16 pixels.	0000	R/W

REG [12h] Memory Access Mode Register (**MAMR**)

Bit	Description	Default	Access
7	**Cursor Auto Shifting Direction** 0 : Cursor moves horizontally (left to right) first then vertically (top to down). 1 : Cursor moves vertically first then horizontally. **Note:** In graphic mode, the cursor moving is treated as unit of bytes in horizontal direction. At vertical direction, it's treated as unit of bit. At text mode, the bit is ignored, and the cursor moving is always in horizontal direction.	0	R/W
6-4	**Display Layer and Display Mode Selection** 0 0 0 : Gray Mode. In this mode, each pixel consists with 2 continuous bits in memory data. With the FRC methodology, 4-level-gray mode is implemented. The bit mapping is list as below. bit1 bit0 Gray 0 0 Level1 (Lightest) 0 1 Level2 1 0 Level3 1 1 Level4 (Darkest) **Note:** Gray mode doesn't support text-mode input. 0 0 1 : Show DDRAM1 data on screen. 0 1 0 : Show DRRAM2 data on screen. 0 1 1 : Show Two Layer Mode. The display rule depends on Bit-3 and Bit-2 as following. 1 0 X : NA. 1 1 0 : Extension Mode (1), the panel will show both DDRAM1 and DDRAM2 data on the screen. The RA8806 is available for 640x240 pixels panel. 1 1 1 : Extension Mode (2), the panel will show both DDRAM1 and DDRAM2 on the screen. The RA8806 is available for 320x480 pixels panel.	001	R/W
3-2	**Two Layer Mode Selection** Combine the data of DDRAM1 and DDRAM2 on the screen when Bit[6:4] is set as "011". 0 0 : DDRAM1 "OR" DDRAM2. 0 1 : DDRAM1 "XOR" DDRAM2. 1 0 : DDRAM1 "NOR" DDRAM2. 1 1 : DDRAM1 "AND" DDRAM2.	00	R/W
1-0	**MPU Read/Write Layer Selection** 0 0 : Access CGRAM.(512Byte) 0 1 : Access DDRAM1. 1 0 : Access DDRAM2. 1 1 : Access both DDRAM1 and DDRAM2 concurrently	01	R/W

REG [20h] Active Window Right Register (**AWRR**)

Bit	Description	Default	Access
7-6	**Reserved**	00	R
5-0	**Active Window Right Position → Segment-Right** **Note:** AWRR must be equal or larger then AWLR, and less or equal then the value 27h (40 in decimal).	27h	R/W

Note:

REG[20h, 30h, 40h, and 50h] are used to dominate an active window for line/row changing when writing data. Users can use these four registers to set the left/right/top/bottom boundary of active window. When data goes beyond the right boundary of it, the cursor will automatically change the next line to write data. It will move to the left boundary of new line in active window. When the data comes to the right-bottom corner, the next write will cause the cursor to move to the left-top corner.

REG [21h] Display Window Width Register (**DWWR**)

Bit	Description	Default	Access
7-6	**Reserved**	00	R
5-0	**Set Display Window Width Position → Segment-Width** **Segment-Right = (Segment Number / 8) – 1** If LCD panel resolution is 320x240, the value of the register is: (320 / 8) - 1 = 39 = 27h	27h	R/W

Note:

REG[21h, 31h] are used to set Display Window Resolution. Users can set the viewing scope of Display Data RAM. Column width (DWWR) of RA8806 can be set between 0h ~ 27h, and Row height (DWHR) can be set between 0h ~ EFh.

REG [30h] Active Window Bottom Register (**AWBR**)

Bit	Description	Default	Access
7-0	**Active Window Bottom Position → Common-Bottom** **Note:** AWBR must be equal or larger then AWTR, and less or equal then the value EFh(239 in decimal)	EFh	R/W

REG [31h] Display Window Height Register (**DWHR**)

Bit	Description	Default	Access
7-0	**Display Window Height Position → Common- Height** **Common_ Height = LCD Common Number –1** If LCD panel resolution is 320x240, the value of the register is: 240 – 1 = 239 = EFh	EFh	R/W

REG [40h] Active Window Left Register (**AWLR**)

Bit	Description	Default	Access
7-6	**Reserved**	00	R
5-0	**Active Window Left Position → Segment-Left** **Note:** AWLR must be equal or less then AWRR, and less then the value 27h(39 in decimal)	00h	R/W

REG [50h] Active Window Top Register (**AWTR**)

Bit	Description	Default	Access
7-0	**Active Window Top Position → Common-Top** **Note:** AWTR must be equal or less then AWBR, and less then the value EFh (239 in decimal)	00h	R/W

REG [60h] Cursor Position X Register (**CURX**)

Bit	Description	Default	Access
7-6	**Reserved**	00	R
5-0	**Cursor Position of Segment / RAM0 Address[4:0]** Define the cursor address of segment, a value from 0h ~ 27h(0 ~ 40 in decimal) When CGRAM write mode is selected (REG[12h] Bit[1:0] = 00b), the Bit[4:0] is the address for writing bit-map data. When create a full-size font, normally set to 0. When create an odd half-size font, normally set to 0, and set 10h for even font.	00h	R/W

REG [61h] Begin Segment Position Register of Scrolling (**BGSG**)

Bit	Description	Default	Access
7-6	**Reserved**	00	R
5-0	**Segment Start Position of Scrolling Mode** REG[61h] defines the start position (left boundary) of scroll window, it must be a value that less or equal to the REG[62h], which defines the end position(right boundary) of scroll window. Also it must be less then the value of 27h (40 in decimal), for the Display Data RAM limit.	00h	R/W

Note:

REG[61h, 62h, 71h, 72h] dominate a named scroll window for scroll function. They must be set before the scroll function is enable.

REG [62h] End Segment Position Register of Scrolling (**EDSG**)

Bit	Description	Default	Access
7-6	**Reserved**	00	R
5-0	**Segment End Position of Scrolling Mode** REG[62h] defines the end position(right boundary) of scroll window, it must be a value that larger or equal to the REG[61h], which defines the end position(left boundary) of scroll window. Also it must be less or equal then the value of 27h(40 in decimal), for the Display Data RAM limit.	00h	R/W

REG [70h] Cursor Position Y Register (**CURY**)

Bit	Description	Default	Access
7-0	**Cursor Position of Common / RAM0 Address[8:5]** Define the cursor address of common, a value from 0h ~ EFh(0 ~ 239 in decimal). When CGRAM write mode is selected (REG[12h] Bit[1:0] = 00b), the Bit[3:0] is indicate which font will be created. And Bit[7:4] are not available.	00h	R/W

REG [71h] Scrolling Action Range Begin Common Register (**BGCM**)

Bit	Description	Default	Access
7-0	**Common Start Position of Scrolling Mode** REG[71h] defines the begin position(top boundary) of scroll window, it must be a value that less or equal to the REG[72h], which defines the end position(bottom boundary) of scroll window. Also it must be less then the value of EFh (239 in decimal), for the Display Data RAM limit.	00h	R/W

REG [72h] Scrolling Action Range END Common Register (**EDCM**)

Bit	Description	Default	Access
7-0	**Common Ending Position of Scrolling Mode** REG[72h] defines the end position(bottom boundary) of scroll window, it must be a value that larger or equal to the REG[71h], which defines the end position(top boundary) of scroll window. Also it must be less or equal then the value of EFh (239 in decimal), for the Display Data RAM limit.	00h	R/W

REG [80h] Blink Time Register (**BTMR**)

Bit	Description	Default	Access
7-0	**Cursor Blink Time and Scroll Time** **Blinking Time = Bit[7:0] x (Frame width)** **Frame width = 1/Frame Rate** The Frame Rate is depends on the DWWR and DWHR and ITCR setting.	00h	R/W

Notes:

1. The Setting also determines the scroll moving speed.
2. The Frame width is the time that the controller scan whole panel, it depends on the system clock frequency, setting of display window, driver interface (4-bits/8-bits), Idle time (ITCR), and dual mode or gray scale mode, etc.

REG [90h] Idle Time Counter Register (**ITCR**)

Bit	Description	Default	Access
7-0	**Idle Time Setting, in count of system clock.** The value can determine the scan time of each COM of the LCD. **COM_PRD = (COM_SCAN + ITCR) x XCK_PRD** In which, **COM_SCAN = (SEG_NO/LD_WIDTH) x (1 + EXT_MD)** **XCK_PRD = 1 / XCK** **COM_PRD:** The finally scan period for each COM(Unit : ns). **COM_SCAN:** The really scan time for each COM. **XCK_PRD:** One cycle time of XCK. XCK is depends on the system clock(CLK) and REG[01h] Bit[3:2]. If system clock is 8MHz, REG[01h] Bit[3:2] = 10b, then XCK_PRD = 250ns. **SEG_NO:** Segment number, i.e. 240x160 panel, SEG_NO = 240. **EXT_MD:** In extension mode1 or 2(REG[12h] Bit[6:4] = 111b or 110b), the EXT_MD = 1, otherwise EXT_MD = 0. **LD_WIDTH:** Driver data width. If LCD driver data bus is 4-bits then LD_WIDTH = 4. If LCD driver data bus is 8-bits then LD_WIDTH = 8. Please refer pin "DW" description of Section 4-3.	00h	R/W

REG [A0h] Key-Scan Control Register 1 (**KSCR1**)

Bit	Description	Default	Access
7	**Key-Scan Enable Bit** 1 : Enable. 0 : Disable.	0	R/W
6	**Key-Scan Matrix Selection** 1 : 4x8 Matrix(KOUT[3:0] is used, KOUT[7:4] please keep floating) 0 : 8x8 Matrix(KOUT[7:0] is used)	0	R/W
5-4	**Key-Scan Data Sampling Times** De-bounce times of scan frequency. 0 0 : 4 0 1 : 8 1 0 : 16 1 1 : 32	00	R/W
3	**LNGKEY_EN : Long Time Key Function Enable** LNGKEY_EN = 0 → Long key function is disable. LNGKEY_EN = 1 → Long key function is enable.	0	R/W

<table>
<tr>
<td>2-0</td>
<td>KF2-0: Key-Scan frequency.
If system clock is 10MHz, then the related Key-Scan timing are as following:
<table>
<tr><th>KF2</th><th>KF1</th><th>KF0</th><th>Key-Scan Pulse Width (KOUT period)</th><th>Key-Scan Cycle (4x8)</th><th>Key-Scan Cycle (8x8)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>16µs</td><td>64µs</td><td>128µs</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>32µs</td><td>128µs</td><td>256µs</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>64µs</td><td>256µs</td><td>512µs</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>128µs</td><td>512µs</td><td>1.024ms</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>256µs</td><td>1.024ms</td><td>2.048ms</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>512µs</td><td>2.048ms</td><td>4.096ms</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1.024ms</td><td>4.096ms</td><td>8.192ms</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>2.048ms</td><td>8.192ms</td><td>16.384ms</td></tr>
</table>
</td>
<td>000</td>
<td>R/W</td>
</tr>
</table>

REG [A1h] Key-Scan Controller Register 2(**KSCR2**)

Bit	Description	Default	Access
7	**Key-Scan Wakeup Function Enable Bit** 0: Key-Scan Wakeup function is disable. 1: KEY-SCAN Wakeup function is enable.	0	R/W
6-4	**Reserved**	000	R
3-2	**Long Key Timing Adjustment** 00 : About 0.625sec(for 8MHz Clock source) 01 : About 1.25sec(for 8MHz Clock source) 10 : About 1.875 sec(for 8MHz Clock source) 11 : About 2.5 sec(for 8MHz Clock source)	00	R/W
1-0	**Numbers of Key Hit.** 00 : No key is pressed 01 : One key is pressed, read REG[A2h] for the key number. 10 : Two key is pressed, read REG[A2h ~ A3h] for the key number. 11 : Three key is pressed, read REG[A2h ~ A4h] for the key number.	00	R

REG [A2h ~ A4h] Key-Scan Data Register (**KSDR0 ~ 2**)

Bit	Description	Default	Access
7-0	**Key Strobe Data** The corresponding key number that is pressed. Please reference Section 6-5 "Key-Scan".	00h	R

REG [B0h] Memory Write Command Register (**MWCR**)

Bit	Description	Default	Access
7-0	**Memory data write command from the cursor position.** **Note:** Write memory data, user must write the MWCR command first, then write DATA cycle.	NA	R/W

REG [B1h] Memory Read Command Register (**MRCR**)

Bit	Description	Default	Access
7-0	**Memory data read command from the cursor position.** **Note:** Memory read cycle in text mode, the cursor move in same behavior like graphic mode. B1h will perform a pre-read function. So the cursor position will increase after the MRCR command is write.	NA	R/W

REG [C0h] Touch Panel Control Register 1 (**TPCR1**)

Bit	Description	Default	Access
7	**Touch Panel Enable Bit** 1 : Enable. 0 : Disable.	0	R/W
6-4	**TP Sample Time Adjusting** 000 : Wait 50μs for ADC data ready. 001 : Wait 100μs for ADC data ready. 010 : Wait 200μs for ADC data ready. 011 : Wait 400μs for ADC data ready. 100 : Wait 800μs for ADC data ready. 101 : Wait 1.6ms for ADC data ready. 110 : Wait 3.2ms for ADC data ready. 111 : Wait 6.4ms for ADC data ready. **Note:** When touch panel detects the Touch event, to avoid the signal instability, the sampled time is delayed to wait the signal stable. The TP Sample Time Adjusting and ADC Clock Convert Speed relation just refer to Section 6-4-3.	000	R/W
3	**Touch Panel Wake-up Enable:** 1 : Touch panel can wake-up the Sleep mode(At the condition that ADC is enabled). 0 : Disable the touch panel wake-up function	0	R/W
2-0	**ADC Clock Convert Speed** 0 0 0 : CLK / 4 0 0 1 : CLK / 8 0 1 0 : CLK /16 0 1 1 : CLK / 32 1 0 0 : CLK / 64 1 0 1 : CLK / 128 1 1 0 : CLK / 256 1 1 1 : CLK / 512 The “CLK” means system clock.	000	R/W

REG [C1h] Touch Panel X High Byte Data Register (**TPXR**)

Bit	Description	Default	Access
7-0	**Touch Panel X Data Bit[9:2](Segment)**	00h	R

REG [C2h] Touch Panel Y High Byte Data Register (**TPYR**)

Bit	Description	Default	Access
7-0	**Touch Panel Y Data Bit[9:2] (Common)**	00h	R

REG [C3h] Touch Panel Segment/Common Low Byte Data Register (**TPZR**)

Bit	Description	Default	Access
7-4	**Reserved**	0000	R
3-2	**Touch Panel Y Data Bit[1:0] (Common)**	00	R
1-0	**Touch Panel X Data Bit[1:0] (Segment)**	00	R

REG [C4h] Touch Panel Control Register 2 (**TPCR2**)

Bit	Description	Default	Access
7	**TP Manual Mode Enable** 1 : Using the manual mode. 0 : Auto mode.	0	R/W
6-2	**Reserved**	00h	R
1-0	**Mode selection for TP Manual Mode** 00 : IDLE mode: ADC idles. 01 : Wait for TP event, touch panel event could cause the interrupt or be read from REG[0Fh] B3. 10 : Latch X data, in the phase, X Data can be latched in REG[C1h] and REG[C3h]. 11 : Latch Y data, in the phase, Y Data can be latched in REG[C2h] and REG[C3h].	00	R/W

REG [D0h] PWM Control Register (**PCR**)

Bit	Description	Default	Access
7	**PWM enable** 1 : Enable 0 : Disable, PWM_OUT level depends on the REG[D0h] Bit-6.	0	R/W
6	**PWM Disable Level** 0 : PWM_OUT is Normal L when PWM disable or Sleep mode. 1 : PWM_OUT is Normal H when PWM disable or Sleep mode.	0	R/W
5-4	**Reserved**	00	R
3-0	**PWM Clock Source Divide Ratio** 0000 b → CLK / 1 0001 b → CLK / 2 0010 b → CLK / 4 0011 b → CLK / 8 : : 1111 b → CLK / 32768 The "CLK" means system clock. For example, CLK is 8MHz: 0000 b → PWM clock source = 8MHz, 0001 b → PWM clock source = 4MHz, : : 1111 b → PWM clock source = 244Hz.	0000	R/W

REG [D1h] PWM Duty Cycle Register (**PDCR**)

Bit	Description	Default	Access
7-0	**PWM Cycle Duty Selection Bit** 00h → 1 / 256 01h → 2 / 256 High period 02h → 3 / 256 High period : : FFh → 256 / 256 High period	00h	R/W

REG [E0h] Pattern Data Register (**PNTR**)

Bit	Description	Default	Access
7-0	**Data Written to DDRAM(Display Data RAM)** The pattern that will be filled to active window in memory clear function. When REG[F0h] Bit-3 is '1', the data in the REG[E0h] will be filled to the whole active window.	00h	R/W

REG [F0h] Font Control Register (**FNCR**)

Bit	Description	Default	Access
7	**ISO8859 Mode** 0 : Disable. The contents of ASCII block 1 ~ 4 are show as Table C-1~ Table C-4 of Appendix B. 1 : Enable. The ASCII block 1 ~ 4 indicate the ISO8859-1 ~ 4 standard and show as Table C-5 ~ Table C-8 of Appendix C.	0	R/W
6-4	**Reserved**	000	R
3	**Memory Clear Function** Write Function 0 : No Action. 1 : Memory clear function active, fill the data of FNTR to Active window. When this bit is set to "1", RA8806 will automatically read PNTR data, and fill it to Active window (Range: [AWLR, AWTR] ~ [AWRR, AWBR]), after clear completed, this bit will be cleaned to "0".	0	R/W
2	**ASCII Mode Enable** 1 : All input data will be decoded as ASCII (00h ~ FFh) 0 : In text mode (REG[00h] Bit-3), the RA8806 will check the first written byte data first. If less then 80h then it's treated as ASCII (Half-size). Or it's treated as a full-size text(GB, BIG5 or User-created font).	0	R/W
1-0	**ASCII Blocks Select** 0 0 : Map to ASCII block 1. (Table C-1 and Table C-5 of Appendix C.) 0 1 : Map to ASCII block 2. (Table C-2 and Table C-6 of Appendix C.) 1 0 : Map to ASCII block 3. (Table C-3 and Table C-7 of Appendix C.) 1 1 : Map to ASCII block 4. (Table C-4 and Table C-8 of Appendix C.)	00	R/W

REG [F1h] Font Size Control Register (**FVHT**)

Bit	Description	Default	Access
7-6	**Set Character Horizontal Size** 0 0 : One Time of normal font width. 0 1 : Two Times of normal font width. 1 0 : Three Times of normal font width. 1 1 : Four Times of normal font width.	00	R/W
5-4	**Set Character Vertical Size** 0 0 : One Time of normal font height. 0 1 : Two Times of normal font height. 1 0 : Three Times of normal font height. 1 1 : Four Times of normal font height.	00	R/W
3-0	**Reserved**	0000	R

7. Software Design Guide

```
//================================RA8806 Software 8080 drivers=================
void RA8806_Write_CMD(uchar dat)
{
//   LCM_ChkBusy();

     CS2 = 1;
     RS = 1;


     DATA_PORT = dat;
  WRITE = 0;
//   _nop_();
//   _nop_();
     WRITE = 1;
  CS2 = 0;
}
//=============================================================================
void RA8806_Write_DAT(uchar dat)
{

     CS2 = 1;
     RS = 0;

     DATA_PORT = dat;


    WRITE = 0;
//   _nop_();
//   _nop_();
    WRITE = 1;

     CS2 = 0;


}
//============================LCM drivers=====================================
void LCM_Write_REG(uchar reg, uchar cmd)
{
   RA8806_Write_CMD(reg);
```

```
   RA8806_Write_DAT(cmd);
}
//================================================================================
void Init_LCM(void)
{
    Delay_ms(50);
    RST = 0;                //reset must be delay for a short time
    Delay_ms(50);
    RST = 1;
    Delay_ms(50);

//-------------------------------------------------------------------------
       LCM_Write_REG(0x00,0x04);
       LCM_Write_REG(0x01,0x08);

       LCM_Write_REG(0x03,0x04);
       LCM_Write_REG(0x10,0x40);

       LCM_Write_REG(0x11,0x00);
       LCM_Write_REG(0x12,0x11);

//------------------------ display window width and hight Setting-----------------------------
       LCM_Write_REG(0x21,0x27);
       LCM_Write_REG(0x31,0xef);
       //LCM_Write_REG(0x21,Seg_reg);
       //LCM_Write_REG(0x31,Com_reg);
//------------------------active  window Setting-----------------------------
       LCM_Write_REG(0x20,0x27);
       LCM_Write_REG(0x30,0xef);
       //LCM_Write_REG(0x20,Seg_reg);
       //LCM_Write_REG(0x30,Com_reg);
       LCM_Write_REG(0x40,0x00);
       LCM_Write_REG(0x50,0x00);

       LCM_Write_REG(0x60,0x00);
       LCM_Write_REG(0x70,0x00);

       LCM_Write_REG(0x61,0x00);
       LCM_Write_REG(0x62,0x00);
       LCM_Write_REG(0x71,0x00);
       LCM_Write_REG(0x72,0X00);

       LCM_Write_REG(0x80,0x00);
       LCM_Write_REG(0x90,0x40);
       //LCM_Write_REG(0x90,Fre_reg);

       LCM_Write_REG(0xA0,0xD0);
       LCM_Write_REG(0xA1,0x00);

       LCM_Write_REG(0xC0,0x00);
       LCM_Write_REG(0xC4,0x00);

       LCM_Write_REG(0xD0,0x00);
       LCM_Write_REG(0xD1,0x00);

       LCM_Write_REG(0xE0,0x00);
       LCM_Write_REG(0xF0,0x00);
       LCM_Write_REG(0xF1,0x00);
}
```

8. PRECAUTIONS FOR USING LCD MODULES

Handing Precautions

(1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.

(2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.

(3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

(4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

(5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents :

- Isopropyl alcohol
- Ethyl alcohol

(6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.

- Water
- Ketone
- Aromatic solvents

(7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

(8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.

(9) Do not attempt to disassemble or process the LCD module.

(10) NC terminal should be open. Do not connect anything.

(11) If the logic circuit power is off, do not apply the input signals.

(12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

- Be sure to ground the body when handling the LCD modules.
- Tools required for assembling, such as soldering irons, must be properly grounded.
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.
- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

Storage Precautions

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.

- Terminal electrode sections.

10. USING LCD MODULES

Liquid Crystal Display Modules

LCD is composed of glass and polarizer. Pay attention to the following items when handling.

(1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.

(2) Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.).

(3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropylalcohol.

(4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.

(5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

(6) Avoid contacting oil and fats.

(7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.

(8) Do not put or attach anything on the display area to avoid leaving marks on.

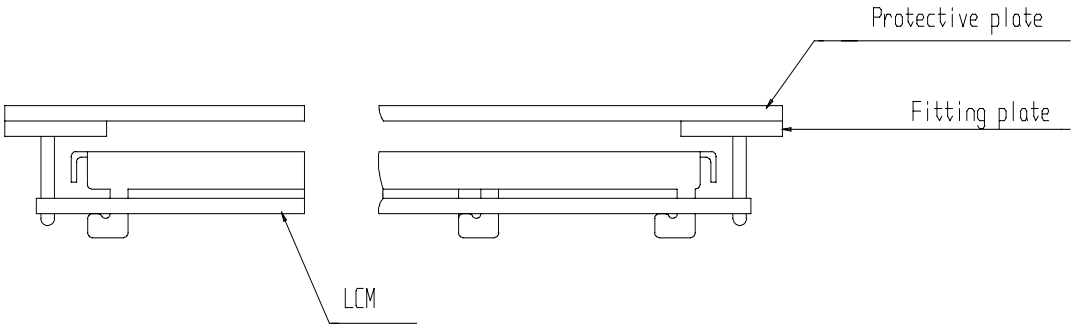
(9) Do not touch the display with bare hands. This will stain the display area and degradate insulation between terminals (some cosmetics are determinated to the polarizers).

(10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be ±0.1mm.

Precaution for Handing LCD Modules

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

(1) Do not alter, modify or change the shape of the tab on the metal frame.

(2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.

(3) Do not damage or modify the pattern writing on the printed circuit board.

(4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.

(5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.

(6) Do not drop, bend or twist LCM.

(7) In order to avoid the cracking of the FPC, you should to pay attention to the area of FPC (R50mm) where the FPC was bent .the edge of coverlay ; the area of surface of Ni-Au plating, the area of soldering land, the area of through hole.

Electro-Static Discharge Control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handing LCM.

(2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.

(3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.

(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutator of the motor.

(5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.

(6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

Precaution for soldering to the LCM

(1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.

- Soldering iron temperature : 260°C ± 10°C.
- Soldering time : 3-4 sec.
- Solder : eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage dur to flux spatters.

(2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

(3) When remove the electoluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

(4)Soldering iron is not allowed to touch the surface of FPC's cover film directly.

Precautions for Operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (VO). Adjust VO to show the best contrast.

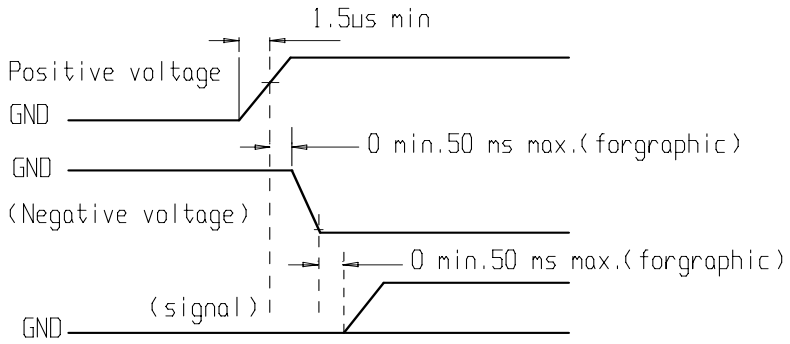
(2) Driving the LCD in the voltage above the limit shortens its life.

(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.

(4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.

(5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, it must be used under the relative condition of 40°C , 50% RH.

(6) When turning the power on, input each signal after the positive/negative voltage becomes stable.



Storage

When storing LCDs as spares for some years, the following precaution are necessary.

(1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for dessicant.

(2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.

(3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)

(4) Environmental conditions :

- Do not leave them for more than 160hrs. at 70°C.
- Should not be left for more than 48hrs. at -20°C.

Safety

(1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2) If any liquid leakes out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

Limited Warranty

Unless agreed between EAST and customer, EAST will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with EAST LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to EAST within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of EAST limited to repair and/or replacement on the terms set forth above. EAST will not be responsible for any subsequent or consequential events.

Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB's eyelet, conductors and terminals.