

PRODUCT SPECIFICATION FOR LCD MODULE

MODULE NO.: ET-G320240FV1 REVERSION: V1 TYPE: COG+COB

PREPARED BY	DATE	
CHECKED BY	DATE	
APPROVED BY	DATE	

Customer Approval:





DOCUMENT REVISION HISTORY

VERSION	DATE	DESCRIPTION	CHANGED BY
V1	11-21-2011	First issue	zhou

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1. General Specifications

Item	Standard Value	Unit
Number of dots	320 (W) x 240(H)	dots
Display Pattern	■Dot-Graphic □Character □Digits □with ICON □	
Module Dimension	100.1(W) x71. 75(H) x10.4 (T)	mm
Viewing Area	79.8 (W) x60.6 (H)	mm
Active Area	76.785 (W) x 57.585 (H)	mm
DOT Size	0.225 (W) x 0.225 (H)	mm
DOT Pitch	0.24(W) x 0.24(H)	mm
	☐ TN,Positive ☐ TN, Negative	
	☐ HTN, Positivee ☐ HTN, Negative	
LCD Turns	☐ STN, Yellow-Green ☐ STN, Gray ☐ STN, Blue	
LCD Type	■ FSTN, Positive □ FSTN, Negative	
	☐ Color STN	
	☐ FM LCD	
Polarizer Type	☐ Transmissive ☐ Reflective ■ Transflective ☐ Anti-Glare	
View Direction	□6H □12H ■ _9H	
Operation Voltage	□3.0(3.3) ■5.0 □	V
DC-DC Converter	■Build-in □External	
LCD Controller & Driver	RA8803	
LCD Driving Method	1/240duty, 1/16bias	
Interface Type	■6800 ■ 8080 □ I2C □ Serial	
	□SPI	
Backlight Type	■ LED □ CCFL □ EL □ no Backlight	
Backlight Color	□Yellow-Green ■ White □ Amber □ Blue □ Red	
EL/CCFL Driver type	☐ Build-in ☐ External	
Operation Temperature(oC)	-10~60 (TOPL ~ TOPH)	deg
Storage Temperature (oC)	-20~70 (TsтL ~ Tsтн)	deg

Note: Label "■ " means the option selected.

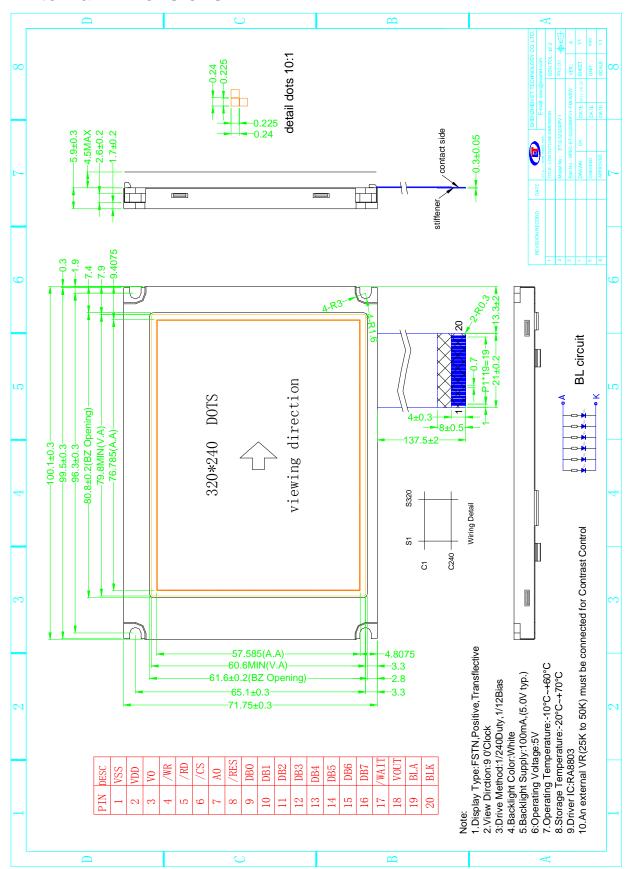
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2. External Dimensions



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3. Pin Description

Pin No.	Symbol	I/O	Description
1	VSS	P	Ground.
2	VDD	P	The digital power supply
3	V0	P	
4	/WR(R/W)	I	Write(8080 Series)/Read-Write(6800 Series).Low active.
5	/RD(EN)	I	Read Enable(8080 Series)/ Enable(6800 Series).
6	/CS	I	Chip Select, low active.
7	A0	I	Register/Memory Select
8	/RES	I	Reset Signal
9	DB0	I/O	Data Bus.
10	DB1	I/O	Data Bus.
11	DB2	I/O	Data Bus.
12	DB3	I/O	Data Bus.
13	DB4	I/O	Data Bus.
14	DB5	I/O	Data Bus.
15	DB6	I/O	Data Bus.
16	DB7	I/O	Data Bus.
17	/WAIT	О	Busy Signal
18	VOUT	P	
19	A	P	LED POWER
20	K	P	rest commands

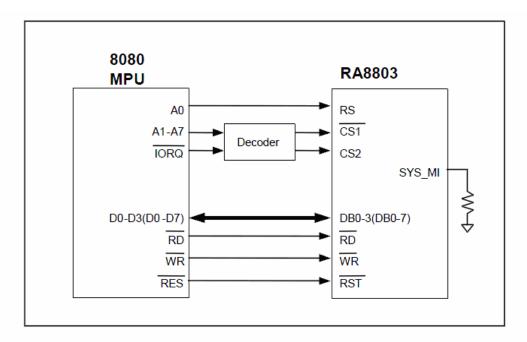
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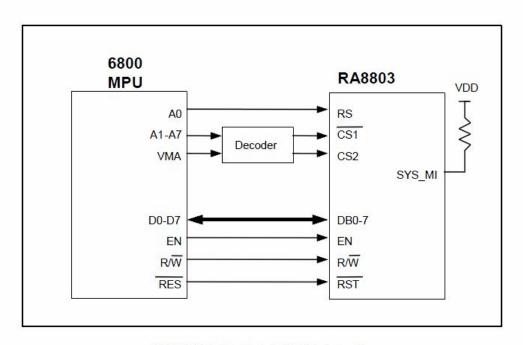
4. MPU Interface

The RA8803 support 8080 or 6800 compatible MPU interface. When the pin SYS_MI is pull low then the MPU interface is set to 8080 compatible. If SYS_MI pull high then the MPU interface is defined as 6800 compatible.

And the pin SYS_DB is used to select the 8080 MPU data bus is 4-Bit or 8-Bit. When SYS_DB pull low, then the data bus for data transition is 4-Bit. If pin SYS_DB pull high, the data transition is 8-Bit. The option of 4-Bit or 8-Bit data bus is for 8080 MPU only. Of course, if used 4-Bit interface then the 8080 MPU has to take double time to communicate with RA8803.



8080 (4/8-Bit) MPU Interface



6800 (8-Bit Only) MPU Interface

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5. Register Description 5.1 Register List Table

Reg.	Reg.	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Defaul
No	Name										t Data
00h	WLCR	R/W	PW1	PW0	SR		CG	DP	DK	DV	C9h
01h	MISC	R/W		CKN		PLR			CKB1	CKB0	F0h
02h	APSR	R/W			SP1	SP0	OAR		SRFS		10h
03h	ADSR	R/W					DADR	AUCM	AUSG	SGCM	80h
10h	WCCR	R/W	ARI	ALG	WDI	WBC	AWI	CP	CK	CSD	6Fh
11h	DWLR	R/W	CR3	CR2	CR1	CR0	DY3	DY2	DY1	DY0	22h
12h	MAMR	R/W	GIM	RM2	RM1	RM0	OP1	OP2	WM1	WM0	91h
20h	AWRR	R/W			X5	X4	Х3	X2	X1	X0	27h
21h	DWRR	R/W			A5	A4	A3	A2	A1	A0	27h
30h	AWBR	R/W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	EFh
31h	DWBR	R/W	B7	B6	B5	B4	В3	B2	B1	B0	EFh
40h	AWLR	R/W			SS5	SS4	SS3	SS2	SS1	SS0	00h
41h	DWLR	R/W			C5	C4	C3	C2	C1	C0	00h
50h	AWTR	R/W	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00h
51h	DWTR	R/W	D7	D6	D5	D4	D3	D2	D1	D0	00h
60h	CPXR	R/W			RS5	RS4	RS3	RS2	RS1	RS0	00h
61h	BGSG	R/W			DS5	DS4	DS3	DS2	DS1	DS0	00h
70h	CPYR	R/W	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	00g
71h	BGCM	R/W	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	00h
72h	EDCM	R/W	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	EFh
80h	BTMR	R/W	BT7	BT6	BT5	BT4	BT3	BT2	BT1	BT0	33h
81h	FRCA	R/W			-						00h
90h	SCCR	R/W	CK7	CK6	CK5	CK4	CK3	CK2	CK1	CK0	04h
91h	FRCB	R/W			1				-		00h
A0h	INTR	R/W	INK	INT	INX	INY	MSK	MST	MSX	MSY	00h
A1h	KSCR	R/W	KEN	KSZ	KDT1	KDT0		KF2	KF1	KF0	00h
A2h	KSDR	RO	KS7	KS6	KS5	KS4	KS3	KS2	KS1	KS0	00h
A3h	KSER	RO	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	00h
B0h	INTX	R/W			IX5	IX4	IX3	IX2	IX1	IX0	27h
B1h	INTY	R/W	IY7	IY6	IY5	IY4	IY3	IY2	IY1	IY0	EFh
C0h	TPCR	R/W	AZEN	AZOE	1	SCAN	AS3	AS2	AS1	AS0	00h
C1h	TPSR	R/W	ARDY	ADET	1	1	AF1	AF0	-		0Fh
C8h	TPXR	RO	TPX9	TPX8	TPX7	TPX6	TPX5	TPX4	TPX3	TPX2	00h
C9h	TPYR	RO	TPY9	TPY8	TPY7	TPY6	TPY5	TPY4	TPY3	TPY2	00h
CAh	TPZR	RO	TPX1	TPX0			TPY1	TPY0			00h
D0h	LCCR	R/W	DZEN			DAC4	DAC3	DAC2	DAC1	DAC0	8Fh
E0h	PNTR	R/W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	00h
F0h	FNCR	R/W	TNS	BNK	RM1	RM0	FDA	ASC	ABS1	ABS0	92h
F1h	FVHT	R/W	FH1	FH0	FV1	FV0	1	1	1	1	0Fh

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5.2 Register Description

REG [00h] Whole Chip LCD Controller Register (WLCR)

Bit	Description	Text/Graph	Default	Access
7-6	Power Mode		O.I.	D/W/
	11: Normal Mode.		3h	R/W
	0 0 : Off Mode.			
5	Software Reset:			
	1 : Reset all registers except flushing RAM		0h	R/W
	0 : Normal Operation			
4	Reserved.		0h	R/W
3	Display Mode Selection			
	1 : Character Mode.		1h	R/W
	0 : Graphical Mode.			
2	Set Display On/Off Selection			
	1 : DISP_OFF pin output high(Display On).	Text/Graph	0h	R/W
	0 : DISP_OFF pin output low(Display Off).			
1	Blink Mode Selection			
	1 : Blink Full Screen.	Text/Graph	0h	R/W
	0 : Normal Display.			
0	Inverse Mode Selection			
	1 : Normal Display	Text/Graph	1h	R/W
	0 : Inverse Full Screen.	'		

REG [01h] Misc. Register (MISC)

Bit	Description	Default	Access
7	Reserved	1h	R/W
6	Clock Output (Pin CLK_OUT) Control		
	1 : Enable	1h	R/W
	0 : Disable		
5	Reserved.	1h	R/W
4	Interrupt (INT) and Busy Polarity		
	1 : Set Active High	1h	R/W
	0 : Set Active Low		
3-2	Reserved.	0h	R/W
1-0	Clock Speed Selection		
	0 0 : 3MHz		
	0 1 : 4MHz	0h	R/W
	1 0 : 8MHz		
	1 1 : 12MHz		

REG [02h] Advance Power Setup Register (APSR)

Bit	Description	Default	Access
7-6	Reserved	0h	R/W
5-4	ROM/RAM Reading Speed 0 0 : Speed0 (30ns@Vdd=3.3V) 0 1 : Speed1 (60ns@Vdd=3.3V) 1 0 : Speed2 (90ns@Vdd=3.3V) 1 1 : Speed3 (120ns@Vdd=3.3V)	1h	R/W
3	ROM/RAM Reading Speed 0 0 : Speed0 (30ns@Vdd=3.3V) 0 1 : Speed1 (60ns@Vdd=3.3V) 1 0 : Speed2 (90ns@Vdd=3.3V) 1 1 : Speed3 (120ns@Vdd=3.3V)	0h	R/W
2	Reserved	0h	R/W
1	Scrolling Reset for Start 0 : Disable	0h	R/W

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	1 : Enable		
0	Reserved	0h	R/W

REG [03h] Advance Display Setup Register (ADSR)

Bit	Description	Default	Access
7-4	Reserved	8h	R/W
3	Set Display RAM Order (Byte) 1 : Inverse Data of Byte 0 : Normal Mode	0h	R/W
2	Common Auto Scrolling 1 : Enable 0 : Disable	0h	R/W
1	Segment Auto Scrolling 1 : Enable 0 : Disable	0h	R/W
0	Common or Segment Scrolling Selection 1 : Segment Scrolling 0 : Common Scrolling In Extension Mode(REG[12h] bit[6:4] = "110" or "111"), this bit must be high.	0h	R/W

REG [10h] Whole Chip Cursor Control Register (WCCR)

Bit	Description	Text/Graph	Default	Access
7	Auto Increase Cursor Position in Reading DDRAM Operation. 1 : Enable (Auto Increase) 0 : Disable	Text/Graph	0h	R/W
6	Chinese/English Character Alignment 1 : Enable 0 : Disable	Text	1h	R/W
5	Store Current Data to DDRAM 1 : Store Current Data to DDRAM Directly 0 : Store Current Data to DDRAM Inversely	Text/Graph	1h	R/W
4	Bold Font (Character Mode Only) 1 : Bold Font 0 : Normal Font	Text	0h	R/W
3	Auto Increase Cursor Position in Writing DDRAM Operation. 1 : Enable (Auto Increase) 0 : Disable	Text/Graph	1h	R/W
2	Cursor Display 1 : Set Cursor Display On 0 : Set Cursor Display Off	Text/Graph	1h	R/W
1	Cursor Blinking 1 : Blink Cursor. The blink time is determined by BTMR. 0 : Normal	Text/Graph	1h	R/W
0	Cursor Width 1: Cursor width is auto adjust by input data. When half size font, the width is one bit(8 Pixel). When full size font, the width is two bit(16 Pixel). 0: Cursor is fixed at one byte width(8 Pixel).	Text	1h	R/W

REG [11h] Distance of Words or Lines Register (DWLR)

	1 = 10 tall 10 0 11 0 10 0 1 10 0 10 10 0 0 0 10 0 0 10 0 0 10 0 0 0 10 0 0 0 10 0 0 0 10 0 0 0 10 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
Bit	Description	Default	Access
7-4	Set Cursor Height	2h	R/W
3-0	Set Line Distance	2h	R/W

REG [12h] Memory Access Mode Register (MAMR)

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LCD MODULE

Bit	Description	Default	Access
7	In Graphic Mode, Cursor Auto Shifting Direction		
	1 : Horizontal moving first then Vertical.	1h	R/W
	0 : Vertical moving first then Horizontal.		
6-4	Display Layer Selection		
	0 0 1 : Only Show Page1		
	0 1 0 : Only Show Page2		
	0 1 1 : Show Two Layer Mode. The display rule depends on Bit3 and Bit2 as		
	following.		
	0 0 0 : Gray Mode.	1h	R/W
	1 1 0 : Extension Mode, the panel will show both Page1 and		
	Page2. The RA8803 is available for 640x240 dots panel,		
	1 1 1 : Extension Mode, the panel will show both Page1 and		
	Page2. The RA8803 is available for 320x480 dots panel,		
3-2	Two Layer Mode Selection		
	0 0 : Page1 RAM "OR" Page2 RAM		
	0 1 : Page1 RAM "XOR" Page2 RAM	0h	R/W
	1 0 : Page1 RAM "NOR" Page2 RAM		
	1 1 : Page1 RAM "AND" Page2 RAM		
1-0	MPU Read/Write Layer Selection		
	0 0 : Access Page0 (512B SRAM) Display Data RAM.		
	0 1 : Access Page1 (9.6KB SRAM) Display Data RAM.	1h	R/W
	1 0 : Access Page2 (9.6KB SRAM) Display Data RAM.		
	1 1 : Access Page1 and Page2 Display Data RAM at the same time.		

REG [20h] Active Window Right Register (AWRR)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	Active Window Right Position Segment-Right	27h	R/W

Note: REG [20h, 30h, 40h, 50h] are used for the function of change the line and page. Users can use these four Registers to set a block as an active window. When data goes beyond the right boundary of active window (The value is set by REG [20h, 30h, 40h, 50h]), then the cursor will automatically change the line and write in data continuously. It means the cursor will move to the left boundary of active window, which is set by REG [40h]. When the data comes to the bottom line of the right side (set by REG [20h and 30h]), then the cursor will be moved to the first line of the left side automatically and continue to put in data. (set by REG [40h, 50h]).

REG [30h] Active Window Bottom Register (AWBR)

Bit	Des	cription	Default	Access
7-0	Active Window Bottom Position	Common-Bottom	EFh	R/W

REG [40h] Active Window Left Register (AWLR)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	Active Window Left Position Segment-Left	0h	R/W

REG [50h] Active Window Top Register (AWTR)

	Bit		Description	Default	Access
7	-0	Active Window Top Position	Common-Top	0h	R/W

REG [21h] Display Window Right Register (DWRR)

Bit	Description Description		Access
7-6	Reserved	0h	R/W
5-0	Set Display Window Right Position Segment-Right	27h	R/W

REG [31] Display Window Bottom Register (DWBR)

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Second Common C				
T-0	Rit	Description	Default	Acces
G [41] Display Window Left Register (DWLR)				R/W
Bit				1
T-0				
Section Sect				Acces
Bit	7-0	Display Window Left Position Segment-Left	Oh	R/W
Bit	G [51] D	isplay Window Top Register (DWTR)		
G Goh Cursor Position X Register (CPXR)			Default	Acces
Bit Description Default Access 7-6 Reserved Access 7-6 Reserved Oh R RW 5-0 Cursor Position of Segment Oh RW G [61h] Begin Segment Position Register (BGSG) Bit Description Default Access 7-6 Reserved Oh RW 5-0 Segment Start Position of Scrolling Mode Oh RW G [70h] Cursor Position Y Register (CPYR) Bit Description Default Access 7-0 Cursor Position of Common G [71h] Scrolling Action Range, Begin Common Register (BGCM) Default Access 7-0 Common Start Position of Scrolling Mode G [72h] Scrolling Action Range END Common Register (EDCM) Bit Description Default Access 7-0 Common Ending Position of Scrolling Mode G [80h] Blink Time Register (BTMR) Bit Description Default Access 7-0 Cursor Blink Time G [90h] Shift Clock Control Register (SCCR) Bit Description Default Access 7-0 Cursor Blink Time G [90h] Shift Clock Cycle ScCR (SCLK x DW) / (Seg x Com x FRM) SCLK : RA8803 System Clock (Unit: Hz) DW: Bus Width of LCD Driver(Unit: Bit) Seg: Segment Number of LCD Panel (Unit: Pixel) Com: Common Number of LCD Panel (Unit: Pixel) Ah R/W	7-0	Display Window Top Position Common-Top	0h	R/W
Bit Description Default Access 7-6 Reserved Access 7-6 Reserved Oh R RW 5-0 Cursor Position of Segment Oh RW G [61h] Begin Segment Position Register (BGSG) Bit Description Default Access 7-6 Reserved Oh RW 5-0 Segment Start Position of Scrolling Mode Oh RW G [70h] Cursor Position Y Register (CPYR) Bit Description Default Access 7-0 Cursor Position of Common G [71h] Scrolling Action Range, Begin Common Register (BGCM) Default Access 7-0 Common Start Position of Scrolling Mode G [72h] Scrolling Action Range END Common Register (EDCM) Bit Description Default Access 7-0 Common Ending Position of Scrolling Mode G [80h] Blink Time Register (BTMR) Bit Description Default Access 7-0 Cursor Blink Time G [90h] Shift Clock Control Register (SCCR) Bit Description Default Access 7-0 Cursor Blink Time G [90h] Shift Clock Cycle ScCR (SCLK x DW) / (Seg x Com x FRM) SCLK : RA8803 System Clock (Unit: Hz) DW: Bus Width of LCD Driver(Unit: Bit) Seg: Segment Number of LCD Panel (Unit: Pixel) Com: Common Number of LCD Panel (Unit: Pixel) Ah R/W	C (COb)	Cursor Position V Pogistor (CDVD)		
7-6 Reserved 0h R 5-0 Cursor Position of Segment 0h R/W 6 [61h] Begin Segment Position Register (BGSG) Default Access 8tit Description Default Access 7-6 Reserved 0h R/W 5-0 Segment Start Position of Scrolling Mode 0h R/W G [70h] Cursor Position Y Register (CPYR) Default Access 7-0 Cursor Position of Common 0h R/W G [71h] Scrolling Action Range, Begin Common Register (BGCM) Bit Default Access 7-0 Common Start Position of Scrolling Mode 0h R/W G [72h] Scrolling Action Range END Common Register (EDCM) Bit Description Default Access 7-0 Common Ending Position of Scrolling Mode EFh R/W G [80h] Blink Time Register (BTMR) Bit Description Default Access 7-0 Cursor Blink Time 33h R/W G [90h] Shift Clock Control Register (SCCR) Bit Description			Default	Acces
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7-6			Default	Λ 0000
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T-0 Cursor Position of Common				
G [71h] Scrolling Action Range, Begin Common Register (BGCM) Bit Description Default Acces 7-0 Common Start Position of Scrolling Mode Oh R/W G [72h] Scrolling Action Range END Common Register (EDCM) Bit Description Default Acces 7-0 Common Ending Position of Scrolling Mode EFh R/W G [80h] Blink Time Register (BTMR) Bit Description Default Acces 7-0 Cursor Blink Time Output Acces 7-0 Cursor Blink Time Output Acces 7-0 Shift Clock Control Register (SCCR) Bit Description Default Acces 7-0 Shift Clock Cycle SCCR = (SCLK x DW) / (Seg x Com x FRM) SCLK : RA8803 System Clock (Unit : Hz) DW : Bus Width of LCD Driver(Unit : Bit) Seg : Segment Number of LCD Panel (Unit : Pixel) Com : Common Number of LCD Panel (Unit : Pixel)			Default	Acces
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Bit Description Default Access 7-0 Common Ending Position of Scrolling Mode EFh R/W G [80h] Blink Time Register (BTMR) Bit Description Default Access 7-0 Cursor Blink Time 33h R/W G [90h] Shift Clock Control Register (SCCR) Bit Description Default Access 7-0 Shift Clock Cycle SCCR = (SCLK x DW) / (Seg x Com x FRM) SCLK : RA8803 System Clock (Unit : Hz) DW : Bus Width of LCD Driver(Unit : Bit) Seg : Segment Number of LCD Panel (Unit : Pixel) Com : Common Number of LCD Panel (Unit : Pixel)	7 0	Common ctart i conton of coloning mode	011	10,00
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G [80h] Blink Time Register (BTMR) Bit Description Default Acces 7-0 Cursor Blink Time 33h R/W G [90h] Shift Clock Control Register (SCCR) Bit Description Default Acces 7-0 Shift Clock Cycle SCCR = (SCLK x DW) / (Seg x Com x FRM) SCLK : RA8803 System Clock (Unit : Hz) DW : Bus Width of LCD Driver(Unit : Bit) Seg : Segment Number of LCD Panel (Unit : Pixel) Com : Common Number of LCD Panel (Unit : Pixel)				
Bit Description Default Access 7-0 Cursor Blink Time 33h R/W G [90h] Shift Clock Control Register (SCCR) Default Access 8it Description Default Access 7-0 Shift Clock Cycle SCCR = (SCLK x DW) / (Seg x Com x FRM) SCLK : RA8803 System Clock (Unit : Hz) An R/W DW : Bus Width of LCD Driver(Unit : Bit) 4h R/W Seg : Segment Number of LCD Panel (Unit : Pixel) Com : Common Number of LCD Panel (Unit : Pixel)	7-0	Common Ending Position of Scrolling Mode	EF11	K/VV
Bit Description Default Access 7-0 Cursor Blink Time 33h R/W G [90h] Shift Clock Control Register (SCCR) Default Access 8it Description Default Access 7-0 Shift Clock Cycle SCCR = (SCLK x DW) / (Seg x Com x FRM) SCLK : RA8803 System Clock (Unit : Hz) An R/W DW : Bus Width of LCD Driver(Unit : Bit) 4h R/W Seg : Segment Number of LCD Panel (Unit : Pixel) Com : Common Number of LCD Panel (Unit : Pixel)	:G [80h] I	Blink Time Register (BTMR)		
G [90h] Shift Clock Control Register (SCCR) Bit Description Default Access 7-0 Shift Clock Cycle SCCR = (SCLK x DW) / (Seg x Com x FRM) SCLK : RA8803 System Clock (Unit : Hz) DW : Bus Width of LCD Driver(Unit : Bit) Seg : Segment Number of LCD Panel (Unit : Pixel) Com : Common Number of LCD Panel (Unit : Pixel)			Default	Acces
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7-0 Shift Clock Cycle SCCR = (SCLK x DW) / (Seg x Com x FRM) SCLK : RA8803 System Clock (Unit : Hz) DW : Bus Width of LCD Driver(Unit : Bit) Seg : Segment Number of LCD Panel(Unit : Pixel) Com : Common Number of LCD Panel (Unit : Pixel)			Default	Acces
SCCR = (SCLK x DW) / (Seg x Com x FRM) SCLK : RA8803 System Clock (Unit : Hz) DW : Bus Width of LCD Driver(Unit : Bit) Seg : Segment Number of LCD Panel (Unit : Pixel) Com : Common Number of LCD Panel (Unit : Pixel)		· · · · · · · · · · · · · · · · · · ·	20.0011	1 13333
DW: Bus Width of LCD Driver(Unit: Bit) Seg: Segment Number of LCD Panel(Unit: Pixel) Com: Common Number of LCD Panel (Unit: Pixel)		SCCR = (SCLK x DW) / (Seg x Com x FRM)		
Seg : Segment Number of LCD Panel(Unit : Pixel) Com : Common Number of LCD Panel (Unit : Pixel)		SCLK : RA8803 System Clock (Unit : Hz)	<u> </u>	
Com : Common Number of LCD Panel (Unit : Pixel)			4h	R/W
		FRM : Frame Rate of LCD Panel (Unit : Pixel)		

REG [A0h] Interrupt Setup & Status Register (INTR)

Bit	Description	Default	Access
7	Key Scan Interrupt Flag		
	1 : Key Scan Detects Key Input	0h	R
	0 : Key Scan doesn't Detect Key Input		

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6	Touch Panel Detect 1 : Touch Panel Touched	0h	R
	0 : Touch Panel Untouched		
5	Cursor Column Status		
	1 : The Cursor Column is equal to INTX	0h	R
	0 : The Cursor Column is not equal to INTX		
4	Cursor Row Status		
	1 : The Cursor Row is equal to INTY	0h	R
	0 : The Cursor Row is not equal to INTY		
3	Key Scan Interrupt Mask		
	1 : Enable Key Scan Interrupt. Enable BUSY signal.	0h	R/W
	0 : Disable Key Scan Interrupt		
2	Touch Panel Interrupt Mask		
	1 : Generate interrupt output if touch panel was detected. Enable BUSY	0h	R/W
	signal.		
	0 : Don't generate interrupt output if touch panel was detected.		
1	Register[B0h] INTX Event Mask		
	1 : Enable INTX Interrupt. Enable BUSY signal.	0h	R/W
	0 : Disable INTX Interrupt		
0	Register[B1h] INTY Event Mask		
	1 : Enable INTY Interrupt. Enable BUSY signal.	0h	R/W
	0 : Disable INTY Interrupt		

REG [D0h] LCD Contrast Control Register (LCCR)

Bit	Description	Default	Access
7	DAC Function 1 : Disable 0 : Enable	1h	R/W
6-5	Reserved	0h	
4-0	DAC Driving Current	0Fh	R/W

REG [F0h] Font Control Register (FNCR)

Bit	Description	Text/Graph	Default	Access
7	Font ROM Transfer Circuit			
	1 : Enable		1h	R/W
	0 : Bypass			
6	When bit5~4 set as "00" ROM Mode0, this bit could be			
	used to select the upper or lower part of 256KB ROM.		0h	R/W
	1 : Select lower part of 256KB ROM			
	0 : Select upper part of 256KB ROM			
5-4	Select Font ROM Type			
	0 0 : Select GB font ROM (256KB, Mode0)		1h	R/W
	0 1 : Select BIG5 font ROM (512KB, Mode1)			
	1 0 : Support GB font ROM (512KB, Mode2)			
3	Fill PNTR Data to DDRAM	Graph		
	1 : Fill Data to DDRAM Enable		0h	R/W
	0 : No Action			
2	ASCII Code Selection	Text		
	1 : All input data will be decoded as ASCII (00~FFh)		0h	R/W
	0 : The RA8803/8822 will check the first byte data first.			
1-0	ASCII Blocks Select			
	0 0 : Map to ASCII block 0, Latin_1			5 444
	0 1 : Map to ASCII block 1, Latin_2		2h	R/W
	1 0 : Map to ASCII block 2, Latin_3			
	1 1 : Map to ASCII block 3, Latin_4			

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5.3 Registers for Display Resolution

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Segment	Common	REG[20h] AWRR	REG[30h] AWBR	REG[21h] DWRR	REG[31h] DWBR
160	80	13h	4Fh	13h	4Fh
160	128	13h	7Fh	13h	80h
160	160	13h	9Fh	13h	9Fh
240	64	1Dh	3Fh	1Dh	3Fh
240	128	1Dh	7Fh	1Dh	80h
240	160	1Dh	9Fh	1Dh	9Fh
320	240	27h	EFh	27h	EFh

6. Function Description

6.1 Command / Decoder Registers

This circuit store and implement the command from MPU Interface. The register WLCR, MISC, APSR and ADSR are used for system setting. Registers WCCR, DWLR, CPXR and CPYR are used for cursor feature. Registers AWRR, AWBR, AWLR and AWTR are used for setting the range of active window. The RA8803 set up registers – DWRR, DWBR, DWLR and DWTR to support (0,0) ~ (320,240) pixel LCD Panel.

Registers INTR, INTX and INTY provide the interrupt related functions to reduce MPU's loading. The registers KSCR, KSDR and KSER are used for Key Scan features. The others hardware such as ADC(controlled by Registers TPSR, TPXR, TPYR, TPZR) and DAC(controlled by Register LCCR) are also controlled by these circuit and related registers.

6.2 Command / Decoder Registers

The RA8803 embedded two 9.6Kbyte display RAM for two layers display. It supports the maximum resolution of LCD panel is 320Column x 240Row. RA8822 embedded two 4.8Kbyte display RAM and support 240Column x 160Row for maximum resolution. The RA8803/8822 support both text and graphics mode. The user could switch both two modes at any time.

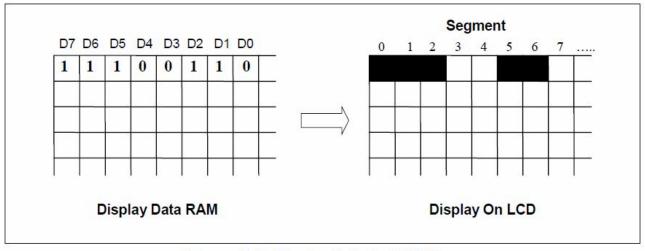


Figure 6-3: Display Data to LCD Map

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6.3 Display Timing Generator (DTGC)

The main function of DTGC is to generate Frame (FRM), Latch Pulse (LP), YD and Data Bus signals for external LCD driver IC. RA8803 could both support 4-bit and 8-bit LCD driver interface. SYS_DW is for LCD driver data bus selection. If SYS_DW pull high then 8-bit LCD driver is used.

6.4 LCD Display

RA8803 support many different resolution of LCD panel. The maximum resolution - 320x240 dots that means 20x 15 full size Chinese character(RA8803 define a Chinese character is 16x16 dots and ASCII is 8x16). Due to the smaller display RAM size. For different resolution of panel, RA8803 could change the setting of some registers like DWRR, DWLR and DWTR to modify display window size. And use registers AWRR, AWBR, AWLR and AWTR to change the active window size.

For example, if use RA8803 to support 320x240 LCD panel, then the related register setting are as following:

DWRR = (320 / 8) - 1 = 39 = 27h DWBR = 240 - 1 = 239 = EFh

DWLR = 0DWTR = 0

The active window range is less than display window. So user has to care the rule as following:

1. DWRR≥ AWRR≥ CPXR≥ AWLR≥ DWLR

LCD MODULE

2. DWBR≥ AWBR≥ CPYR≥ AWTR≥ DWTR

6.5 Font ROM and Font Size

RA8803 embedded 512KByte Font ROM, having the standard and special fonts(16x16) of BIG5, GB, and ASCII(8x16) code. It can support the display 16x16 dot for full-size fonts consisting of Chinese, 8x16 dots for half-size fonts of alphanumeric characters and symbols in the same display.

RA8803-S: Built-in 7,602 standard Simple Chinese character, 408 special character and 4 blocks ASCII character.

Besides that, it also features with bigger Font size. Users can use Register FVHT to set the Font size to 16x32, 16x48, 16x64, 32x16, 32x32, 32x48, 32x64, 48x16, 48x32, 48x48, 48x64, 64x16, 64x32, 64x48 and 64x64 for maximum.

The RA8803/8822 also provide Font ROM readable feature. The MPU could read the bitmap of each font from Font ROM for other application.

6.6 System Clock

RA8802/8803 could depend on SYS_FQ Pull High or Low to decide the clock source. Pull Low is using internal PLL and external 32KHz crystal, and Pull High is using external CLK input as clock source.

6.7 DAC

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The RA8803/8822 built-in one 5-bit fixed current type Digital-to-Analog Converter (D/A). This DAC will generate different current output through the setting of register. So users can use it to control the external booster and adjust the LCD voltage to control the brightness of LCD panel. The DAC out put "IOUT" is tri-state when DAC disable.

6.8 Power

The power architecture of RA8803 is show as Figure 6-7. The I/O power is VDDP and GNDP. The analog power for internal ADC are AVDD and AGND. The RA8803/8822 built-in a 5V to 3V DC/DC Converter. The input power of this Converter is VDD5, and VDD3 is the output. VDD3 supply the power of internal core and DAC. If the system uses 3V only, then connect the 3V power to VDDP, VDD3 and AVDD directly. Please refer t to AP note Appendix B-2.

The RA8803/8822 provide two operation modes: Normal Mode and Off Mode. Please refer to Chapter 5-2 for Register WLCR explanation. When RA8803/8822 is under Off Mode, it can accept the following three methods to Wake-up.

- 1. Directly Command REG[00h], then it will return to Normal Mode
- 2. Touch event is detected
- 3. Key Scan is detected

6.9 ASCII Block Font Selection

RA8803 built in four ASCII Font Blocks, and could be set by register ABS1 and ABS0. If users need special symbols or graphic, it could also be achieved by adjusting ROM Code. Please refer Application Note Chapter 9-21 for more detail.

6.10 Create Font

The RA8803 embedded a 512Byte SRAM for user to create new character. The user could create 16 full size(16x16) Chinese font or special symbol in this memory. Please refer to AP Note for more details.

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7. Sample Program

```
*/
/* Model
                                                              */
             : ET-G320240FV1 (320x240
                                                             */
/* Interface
             : 8 bit Parallel(8080)
  Compiler: KeilC51 Ver7.5
                                                             */
/* Written by
          : 06/Aug/2011
/* Date
/* Check by
                                                              */
/* Check date: /
                                                              */
/* Driver IC: RA8803
/* IC Spec Ver : V2.2
                                                              */
                                                              */
/* Program Ver : V1.0
                                                              */
                                                              */
           : 1. 8 bit Parallel bus drive programme.
           2. Default Crystal 12.000Mhz.
                                                              */
                                                              */
#include <absacc.h>
#include <reg51.h>
#include <intrins.h>
//#include <stdlib.h>
//#include <stdio.h>
//#include <string.h>
#include<ET-G320240.h>
#include"et.h"
#define DATA_PORT P1
#define uchar unsigned char
#define uint unsigned int
uchar h,l;
uint j,k;
sbit CS1
             = P3^0:
             = P3^7:
//sbit CS2
sbit RS
             = P3^4;
sbit
     INT
             = P3^6:
             = P3^3;
sbit
     RST
     BUSY
             = P3^5;
sbit
sbit WRITE = P3^2;
                           //when 8080 .it is /WR;6800.it is R/W
sbit READ
            = P3^1;
                           when 8080 ,it is E
//----- function prototype -----
void Delay_ms(uint ms);
void initial();
void TR_DAT(uchar dat);
void TR_CMD(uchar cmd);
```

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```
void fill(uchar dat1,uchar dat2);
void Write_REG(uchar reg, uchar cmd);
void Write_dot();
void Write_text();
void Delay ms(uint ms)
 uint n=86;
 while (ms--)
   n=86;
   while (n--);
}
             void TR_CMD(uchar cmd)
// LCM_ChkBusy();
 CS1 = 0;
 READ =1;
 RS = 0:
 DATA_PORT = cmd;
 WRITE = 0;
// _nop_();
// _nop_();
 WRITE = 1;
 CS1 = 1;
              void TR_DAT(uchar dat)
{
 CS1 = 0;
 READ = 1;
 RS = 1;
 DATA_PORT = dat;
 WRITE = 0;
// _nop_();
 _nop_();
 WRITE = 1;
 CS1 = 1;
void Write_REG(uchar reg, uchar cmd)
 TR CMD(reg);
 TR_CMD(cmd);
```

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```
void initial()
  IE = 0x00:
  CS1 = 0;
  READ = 1:
  RS = 1:
  WRITE = 1;
  RST = 1:
  RST = 0:
  Delay_ms(200);
  RST = 1;
  Delay_ms(100);
//----- (active window Setting)-----
                             // SEG RIGHT, set AWRR (X1) (240/8)-1=29 == 0x1D
  Write REG(0x20,0x27);
                             // COM BOTTOM,set AWBR (Y1) 128-1=127=7F
  Write_REG(0x30,0xEF);
  Write_REG(0x40,0x00);
                          // SEG LEFT,0 (X2)
  Write_REG(0x50,0x00);
                            // COM TOP,0 (Y2)
//----- ( display window width and hight Setting)------
                       // SEG RIGHT=(segment number/8)-1;set DWWR(X1)
  Write REG(0x21,0x27);
  Write_REG(0x31,0xEF);
                            // COM BOTTOM=com number-1;set DWHR (Y1)
  Write_REG(0x41,0x00);
                            // SEG LEFT,0 (X2
                             // COM TOP,0 (Y2)
  Write_REG(0x51,0x00);
  Write REG(0xE0.0x00):
                             // Pattern Data Registe
  Write REG(0xF0,0xA0);
                             //Font Control Register
  Delay_ms(10);
  Write_REG(0x00,0xCD);
                             // the whole chip LCD controller register
                             //Normal Mode. Character Mode.
  Write REG(0x01,0xf1);
                             /MISC //8M 0xf2
  Write REG(0x02,0x22);
                             // Advance Power Setup Register 90ns 0x02
                             // Advance Display Setup Register
  Write REG(0x03,0x80);
  Write REG(0x10,0xa8);
                             //Whole Chip Cursor Control Register
                             // Distance of Words or Lines Register
  Write REG(0x11,0x00);
  Write_REG(0x12,0x91);
                             //Memory Access Mode Register
  Write_REG(0x90,0x08);
                             //Shift Clock Control Register
  Write REG(0xA0,0x00);
                             //Interrupt Setup & Status Register
                             // Font Control Register //-----
  Write REG(0xF0,0xA0);
 Write REG(0x00,0xCD);
                             // the whole chip LCD controller register
                             //Normal Mode, Character Mode.
}
void fill(uchar dat1,uchar dat2)
{
  Write REG(0x00,0xC5):
  Write REG(0x60,0x00);
  Write_REG(0x70,0x00);
```

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```
for(j=0;j<240;j++)
     for(k=0;k<40;k++)
        if(j\%2==0)
           TR_DAT(dat1);
           TR_DAT(dat2);
     }
}
                                         mode =
void Write_dot()
  Write_REG(0x00,0xC5);
                                    // the whole chip LCD controller register
  Write_REG(0x60,0x00);
  Write_REG(0x70,0x00);
  for(j=0;j<9600;j++)
     TR_DAT(bmp[j]);
}
//=====================text mode ============================
void Write_text()
  Write_REG(0x00,0xcd);
  k = 0;
  for(h=0;h<15;h++)
     Write_REG(0x60,0x00);
     Write_REG(0x70,h*16);
     for(l=0;l<40;l++)
        TR_DAT(table[k++]);
}
void main()
{
  initial();
  while(1)
     Write_dot();
     Delay_ms(2000);
```

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Write_dot1();

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Delay_ms(2000);	
FND	

8. Precautions For Using LCD Modules adfasf

Handing Precautions

- (1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.
- (2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.
- (3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- (4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- (5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents:
 - Isopropyl alcohol
 - Ethyl alcohol
- (6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.
 - Water
 - Ketone
 - Aromatic solvents
- (7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.
- (8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.
 - (9) Do not attempt to disassemble or process the LCD module.
 - (10) NC terminal should be open. Do not connect anything.
 - (11) If the logic circuit power is off, do not apply the input signals.
- (12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
 - Be sure to ground the body when handling the LCD modules.
 - Tools required for assembling, such as soldering irons, must be properly grounded.
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.
- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

Storage Precautions

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

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To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.

LCD MODULE

- Terminal electrode sections.

Liquid Crystal Display Modules

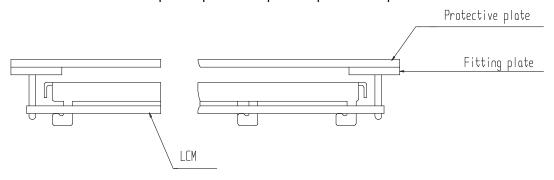
LCD is composed of glass and polarizer. Pay attention to the following items when handling.

- (1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.
- (2) Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.).
- (3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropylalcohol.
- (4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.
- (5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.
 - (6) Avoid contacting oil and fats.
- (7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.
 - (8) Do not put or attach anything on the display area to avoid leaving marks on.
- (9) Do not touch the display with bare hands. This will stain the display area and degradate insulation between terminals (some cosmetics are determinated to the polarizers).
- (10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be ± 0.1 mm.

Precaution for Handing LCD Modules

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

- (1) Do not alter, modify or change the shape of the tab on the metal frame.
- (2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
 - (3) Do not damage or modify the pattern writing on the printed circuit board.
 - (4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.
 - (5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
 - (6) Do not drop, bend or twist LCM.

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(7) In order to avoid the cracking of the FPC, you should to pay attention to the area of FPC (R50mm) where the FPC was bent .the edge of coverlay; the area of surface of Ni-Au plating, the area of soldering land, the area of through hole.

Electro-Static Discharge Control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handing LCM.

LCD MODULE

- (2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.
- (3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.
- (4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutator of the motor.
- (5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.
- (6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

Precaution for soldering to the LCM

- (1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.
 - Soldering iron temperature : 260°C ± 10°C.
 - Soldering time: 3-4 sec.
 - Solder : eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage dur to flux spatters.

- (2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.
- (3) When remove the electoluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.
 - (4) Soldering iron is not allowed to touch the surface of FPC's cover film directly.

Precautions for Operation

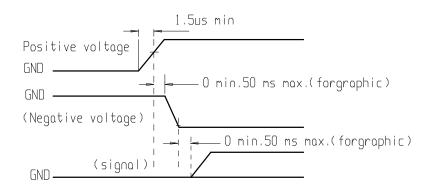
- (1) Viewing angle varies with the change of liquid crystal driving voltage (VO). Adjust VO to show the best contrast.
 - (2) Driving the LCD in the voltage above the limit shortens its life.
- (3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.
- (4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.
- (5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, it must be used under the relative condition of 40° C, 50% RH.
 - (6) When turning the power on, input each signal after the positive/negative voltage becomes stable.

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LCD MODULE



Storage

When storing LCDs as spares for some years, the following precaution are necessary.

- (1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for dessicant.
- (2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.
- (3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)
 - (4) Environmental conditions:
 - Do not leave them for more than 160hrs. at 70°C.
 - Should not be left for more than 48hrs, at -20°C.

Safety

- (1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- (2) If any liquid leakes out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

Limited Warranty

Unless agreed between EAST and customer, EAST will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with EAST LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to EAST within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of EAST limited to repair and/or replacement on the terms set forth above. EAST will not be responsible for any subsequent or consequential events.

Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are:

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be re moved completely without damaging the PCB's eyelet, conductors and terminals.

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