ETIC
an Avago Technologies company

ANALOG SIGNAL PROCESSOR
with BALANCE TRIM
and VARIABLE GAIN

ET2010

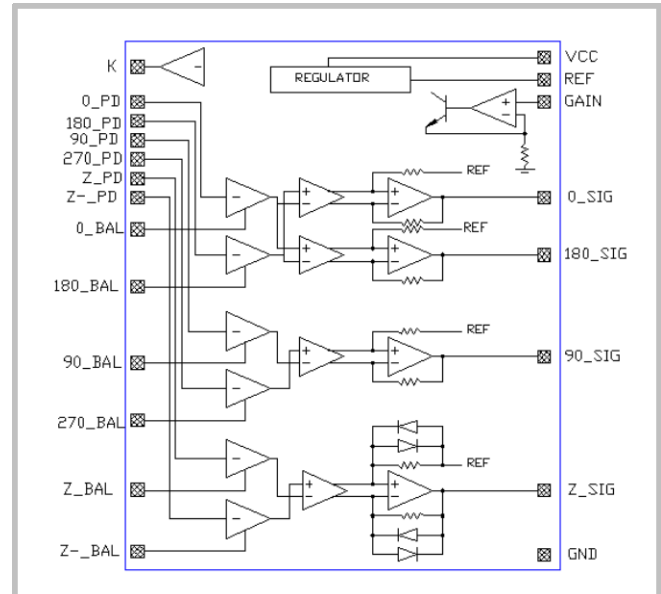## FEATURES

- Single supply operation
- Handles Sine/Cosine inputs from DC to 125KHz
- Photodiode input photocurrent range from 100nA
- Adjustable gain
- DC offset adjustable at each output
- Interfaces directly with ET2015, ET2024, or ET2110 Interpolation devices
- ESD protection to 2kV

BLOCK DIAGRAM

DESCRIPTION

The ET2010 ASP is a monolithic bipolar ASIC designed to transform nanoamp-level differential photocurrents into 1Vpp sinewaves that are suitable for interpolation. A gain adjustment is provided that affects all channels in concert. Separate balance adjustments are provided for each output, for centering the waveforms on the reference voltage. In applications where the photocurrents are generated in phased-array photodiodes, the balance adjustments are generally not needed. In these cases, the BAL pins should be connected to GND. In most encoder designs, the LED optical output level changes with supply voltage, temperature, and age. This causes corresponding changes in the photocurrent signal levels. The ASP rejects these variations in the input signals, resulting in output levels that are stable over time, temperature, and supply voltage. In practice, the maximum usable gain setting may be limited by noise considerations. The comparators in Interpolation ASIC's have a minimal amount of hysteresis, and care must be taken that the noise is well below the hysteresis value. If necessary, the noise can be reduced by lowering the photodiode capacitance or by rolling off the ASP outputs with RC filters.

ABSOLUTE MAXIMUM SPECIFICATIONS

Parameter	Symbol	Min.	Max.	Units	Comments
Operating Temperature Range	T_A	-40	120	°C	
Storage Temperature Range	T_S	-55	150		
Supply Voltage Range	V_{CC}	4.5	5.5	V	

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC}=5V, T_A = 25°C, I_{OFFSET} = 1.5uADC, and I_{IN} = 750nA$_{(P-P)}$ @ 100KHz. All BAL pins are tied to GND for testing.

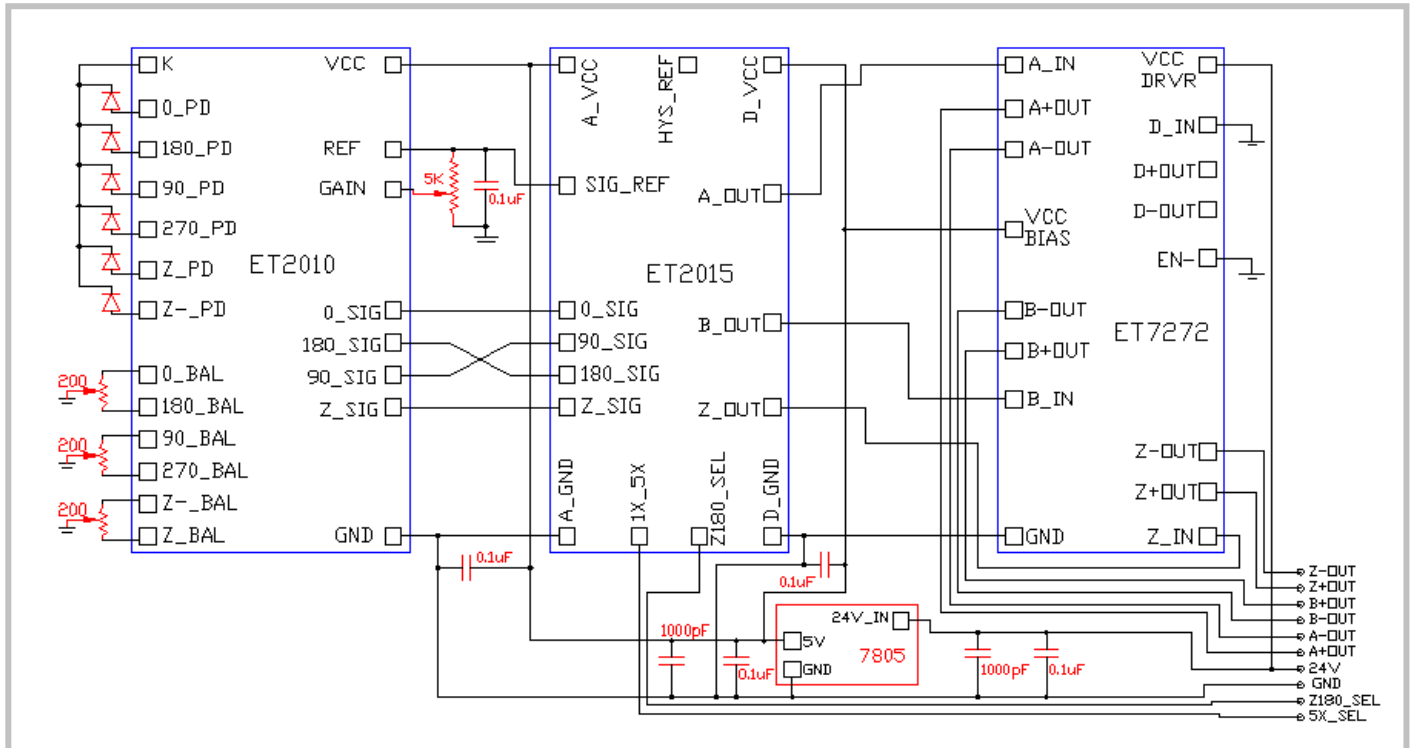| Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply Current	I_{CC}	--	10.7	16	mA	VCC=5.5V
REF Voltage	V_{REF}	2.5	2.65	2.8	V	
K (photodiode cathode bias)	V_K	1.2	1.26	1.4	V	
0_SIG, 90_SIG, 180_SIG, & Z_SIG output voltage, peak to peak	V_{P-P}	--	810	--	mV	GAIN=1.25V and default input conditions
0_SIG, 90_SIG, 180_SIG, & Z_SIG output voltage, DC offset	V_{OFFSET}	--	2.65	--	V	GAIN=1.25V and default input conditions

PIN FUNCTION TABLE

PIN #	PIN NAME	FUNCTION
1,2,3,4	0_PD,180_PD, 90_PD, 270_PD	Inputs for the photodiode signals from the data channels
5,6	Z+_PD, Z-_PD	Inputs for the photodiode signals from the index channel
7,8,9,10	0 BAL,180 BAL, 90 BAL, 270 BAL	Adjust pins for data signal balancing via resistor to ground
11,12	Z+ BAL, Z- BAL	Adjust pins for index signal balancing via resistor to ground
13,14	N.C.	
15	GND	Return for supply voltage
16	Z_SIG	Index channel amplified sinewave output, level shifted
17,18,19	90_SIG, 180_SIG, 0_SIG	Data channel amplified sinewave output, level shifted
20	REF	Output of internal reference voltage (to feed forward as comparator threshold set point)
21	GAIN	Input for voltage controlled amplifiers, 0-2.5V
22	VCC	Supply voltage input, 5V
23	N.C.	
24	K	Output of internal bias voltage for cathode of photodiodes

Application

For applications that use photodiode sensing, and are intended for interpolation of these signals, ETIC offers the ET2010 Analog Signal Processor. With photodiodes representing differential optical channels on its inputs, the device provides four channels of amplified sinewave outputs compatible with the downstream interpolation circuitry. Balance adjustment is provided to correct for amplitude differences between inputs. Sufficient gain (voltage adjustable) is provided so that amp input signals produce output sinewaves in excess of the 400mVpp required at the input of an interpolation device such as the ET2015 or ET2024. Additionally, the ET2010 provides a level shifting of these signal and provides the DC offset of 2.5V (VCC/2) used to bias the SIG_REF pin of these interpolation devices. Please see the **Application Circuit** for interconnection of the signal processor, an interpolation device, and a four channel ET7272B differential output line driver.

Application Circuit

East Texas Integrated Circuits, 275 W. Campbell Rd. Suite 310, Richardson, TX 75080 ph.(972)234-5656 fax (972)234-5657
E-mail to Sales@etic-avago.com or visit our website, www.etic-avago.com .

Ordering Information:

PART NUMBER	DESCRIPTION	Packaging	MINIMUM ORDER
ET2010 TSSOP	24L TSSOP (See drawing)	50 per tube	50
ET2010 T&R SCAN	TSSOP on Tape & Reel with 100% lead inspection	Reel size & qty per customer PO	500

ET2010-TSSOP
Package Drawing for 24L TSSOP

```
        1
0_PD   [====]┌─────────┐[====]  K
180_PD [====]│  ○      │[====]  N.C.
90_PD  [====]│         │[====]  VCC
270_PD [====]│         │[====]  GAIN
Z+_PD  [====]│         │[====]  REF
Z-_PD  [====]│         │[====]  0 SIG
0 BAL  [====]│         │[====]  180 SIG
180 BAL[====]│         │[====]  90 SIG
90 BAL [====]│         │[====]  Z SIG
270 BAL[====]│         │[====]  GND
Z+ BAL [====]│         │[====]  N.C.
Z- BAL [====]└─────────┘[====]  N.C.
```