10-pin, 24-Bit, 192kHz Stereo D/A Converter

General Description

The ET4344 family members are complete, stereo digital-to-analog output systems including interpolation,multi-bit D/A conversion and output analog filtering in a 10-pin package. The ET4344/5/6/8 support all major audio data interface formats, and the individual devices differ only in the supported interface format.

The ET4344 family is based on a fourth order multi-bit delta-sigma modulator with a linear analog low-pass filter. This family also includes auto-speed mode detection using both sample rate and master clock ratioas a method of auto-selecting sampling rates between 2kHz and 200kHz.

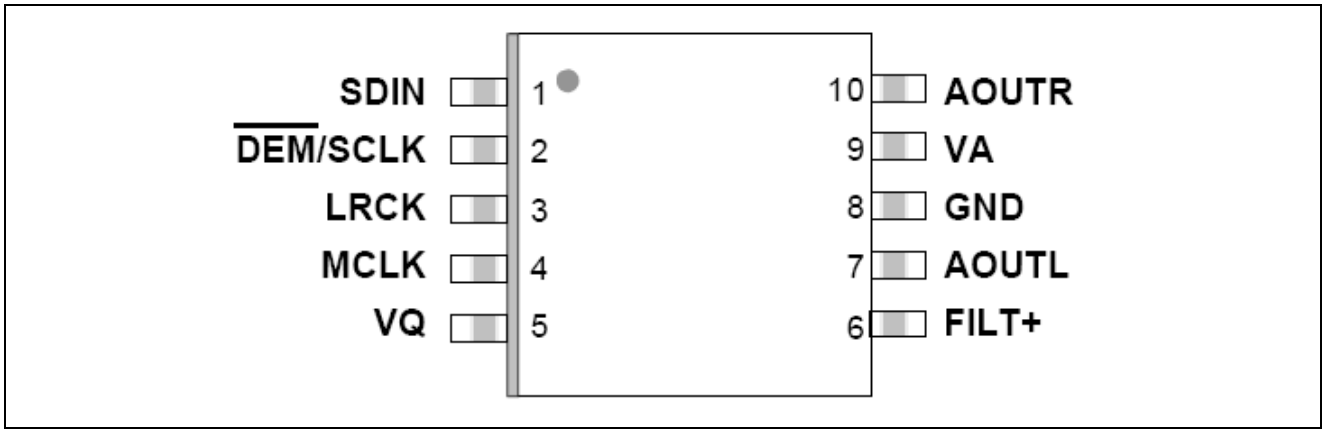
The ET4344 family contains on-chip digital de-emphasis, operates from a single +3.3V or +5V power supply, and requires minimal support circuitry. These features are ideal for DVD players & recorders, digital televisions, home theater and set top box products, and automotive audio systems.

The ET4344 family is available in a 10-pin MSOP package in both Commercial (-10 to +85 °C) and Automotive grades (-40 to +85 °C).

Features

- Multi-bit Delta-Sigma Modulator
- 24-bit Conversion
- Automatically Detects Sample Rates up to 192kHz.
- 105 dB Dynamic Range
- -90 dB THD+N
- Low Clock-Jitter Sensitivity
- Single +3.3V or +5V Power Supply
- Filtered Line-Level Outputs
- On-chip Digital De-emphasis
- Popguard™ Technology
- Package：MSOP10（ET4344U）

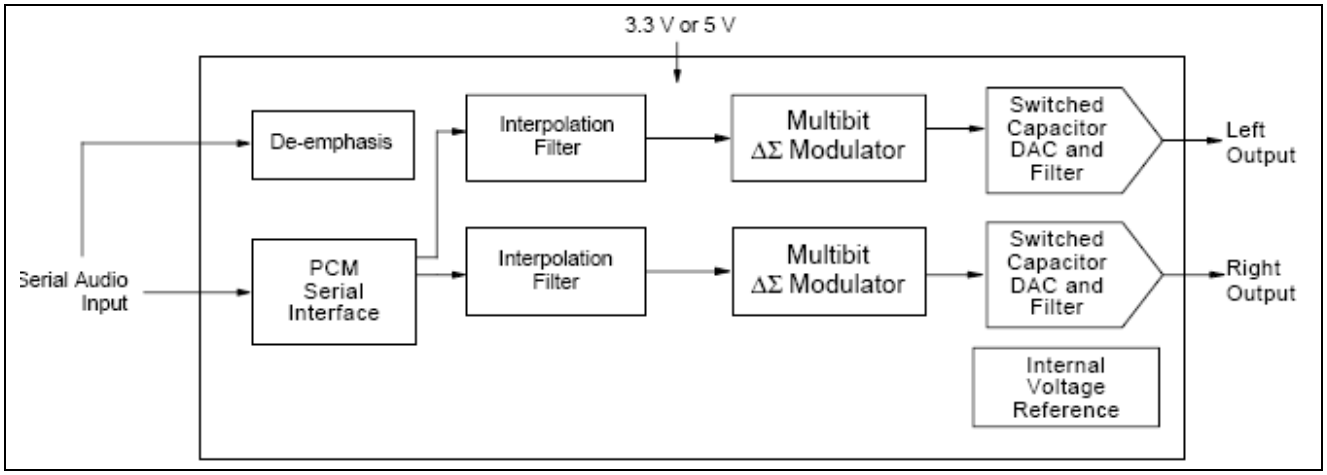
Pin Configuration



Pin Function

Pin No.	Pin Name	Pin Description
1	SDIN	Serial Audio Data Input (Input) - Input for two's complement serial audio data.
2	$\overline{\text{DEM}}$/SCLK	De-Emphasis/External Serial Clock Input (Input) - used for de-emphasis filter control or external serial clock input.
3	LRCK	Left Right Clock (Input) - Determines which channel, Left or Right, is currently active on the serial audio data line.
4	MCLK	Master Clock (Input) - Clock source for the delta-sigma modulator and digital filters.
5	VQ	Quiescent Voltage (Output) - Filter connection for internal quiescent voltage.
6	FILT+	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits.
7	AOUTL	Left Channel Analog Output (Output) - The full scale analog output level is specified in the Analog Characteristics specification table.
8	GND	Ground (Input) - ground reference.
9	VA	Analog Power (Input) - Positive power for the analog and digital sections.
10	AOUTR	Right Channel Analog Output (Output) - The full scale analog output level is specified in the Analog Characteristics specification table.

Block Diagram



Functional Description

The ET4344 family accepts data at standard audio sample rates including 48, 44.1 and 32kHz in SSM, 96, 88.2and 64kHz in DSM, and 192, 176.4 and 128kHz in QSM. Audio data is input via the serial data input pin (SDIN).The Left/Right Clock (LRCK) determines which channel is currently being input on SDIN, and the optional Serial Clock (SCLK) clocks audio data into the input data buffer. The ET4344/5/6/8 differ in serial data formats as shown in Figures1-4.

Master Clock

MCLK/LRCK must be an integer ratio as shown in Table1. The LRCK frequency is equal to Fs, the frequency at which words for each channel are input to the device. The MCLK-to-LRCK frequency ratio and speed mode is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period and by detecting the absolute speed of MCLK. Internal dividers are set to generate the proper clocks. Table1 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies. Please note there is no required phase relationship, but MCLK, LRCK and SCLK must be synchronous.

LRCK	**MCLK (MHz)**									
(kHz)	**64x**	**96x**	**128x**	**192x**	**256x**	**384x**	**512x**	**768x**	**1024x**	**1152x**
32	-	-	-	-	8.1920	12.2880	-	-	32.7680	36.8640
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8680	45.1580	-
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-
64	-	-	8.1920	12.2880	-	-	32.7680	49.1520	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8680	-	-	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	-	-	-	-
128	8.1920	12.2880	-	-	32.7680	49.1520	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8680	-	-	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	-	-	-	-	-	-
Mode	**QSM**				**DSM**		**SSM**			

Table 1. Common Clock Frequencies

Serial Clock

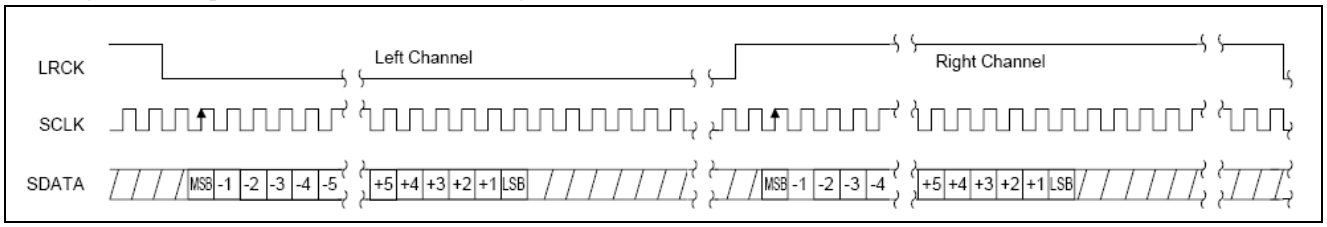
The serial clock controls the shifting of data into the input data buffers. The ET4344 family supports both external and internal serial clock generation modes. Refer to Figures1-4 for data formats.

External Serial Clock Mode

The ET4344 family will enter the External Serial Clock Mode when 16 low to high transitions are detected on the DEM/SCLK pin during any phase of the LRCK period. When this mode is enabled, the Internal Serial Clock Mode and de-emphasis filter cannot be accessed. The ET4344 family will switch to Internal Serial Clock Mode if no low to high transitions are detected on the DEM/SCLK pin for 2 consecutive frames of LRCK. Refer to Figure 6.

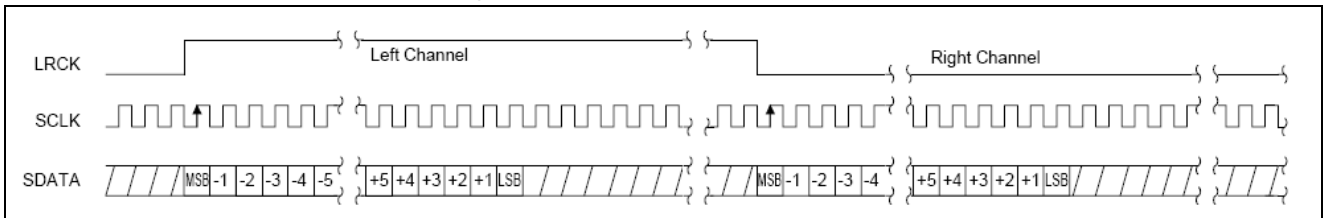
Internal Serial Clock Mode

In the Internal Serial Clock Mode, the serial clock is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK frequency ratio is either 32, 48, 64, or 72 depending upon data format. Operation in this mode is identical to operation with an external serial clock synchronized with LRCK. This mode allows access to the digital de-emphasis function. Refer to Figures1 - 6 for details.



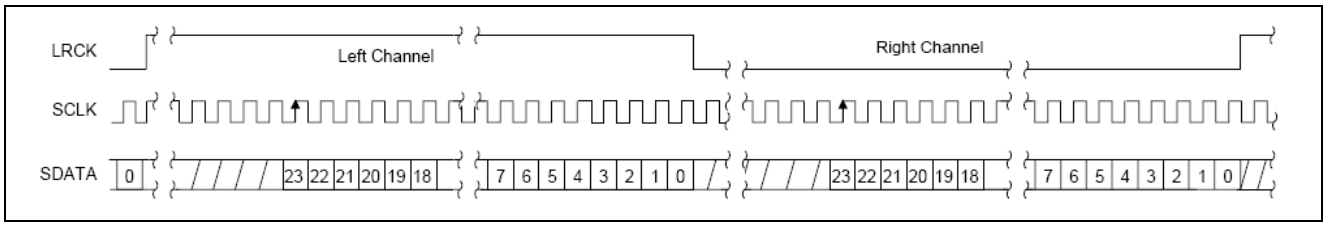
Internal SCLK Mode	External SCLK Mode
I²S, 16-Bit data and INT SCLK = 32 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64	I²S, up to 24-Bit Data Data Valid on Rising Edge of SCLK
I²S, Up to 24-Bit data and INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96	
I²S, Up to 24-Bit data and INT SCLK = 72 Fs if MCLK/LRCK = 1152	

Figure 1. ET4344 Data Format (I^2S)



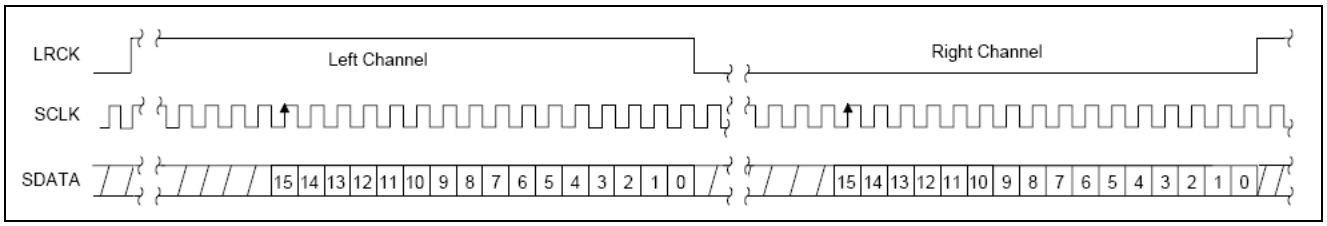
Internal SCLK Mode	External SCLK Mode
Left-Justified, up to 24-Bit Data	Left-Justified, up to 24-Bit Data Data Valid on Rising Edge of SCLK
INT SCLK = 64 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64	
INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96	
INT SCLK = 72 Fs if MCLK/LRCK = 1152	

Figure 2. ET4345 Data Format (Left Justified)



Internal SCLK Mode	External SCLK Mode
Right Justified, 24-Bit Data	Right Justified, 24-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 48 Cycles per LRCK Period
INT SCLK = 64 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64	
INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96	
INT SCLK = 72 Fs if MCLK/LRCK = 1152	

Figure 3. ET4346 Data Format (Right Justified 24)



Internal SCLK Mode	External SCLK Mode
Right Justified, 16-Bit Data	Right Justified, 16-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 32 Cycles per LRCK Period
INT SCLK = 32 Fs if MCLK/LRCK = 1024, 512, 256, 128, or 64	
INT SCLK = 48 Fs if MCLK/LRCK = 768, 384, 192, or 96	
INT SCLK = 72 Fs if MCLK/LRCK = 1152	

Figure 4. ET4348 Data Format (Right Justified 16)

De-Emphasis

The ET4344 family includes on-chip digital de-emphasis. Figure 5 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

The de-emphasis filter is active (inactive) if the $\overline{\text{DEM}}$/SCLK pin is low (high) for 5 consecutive falling edges of LRCK. This function is available only in the internal serial clock mode

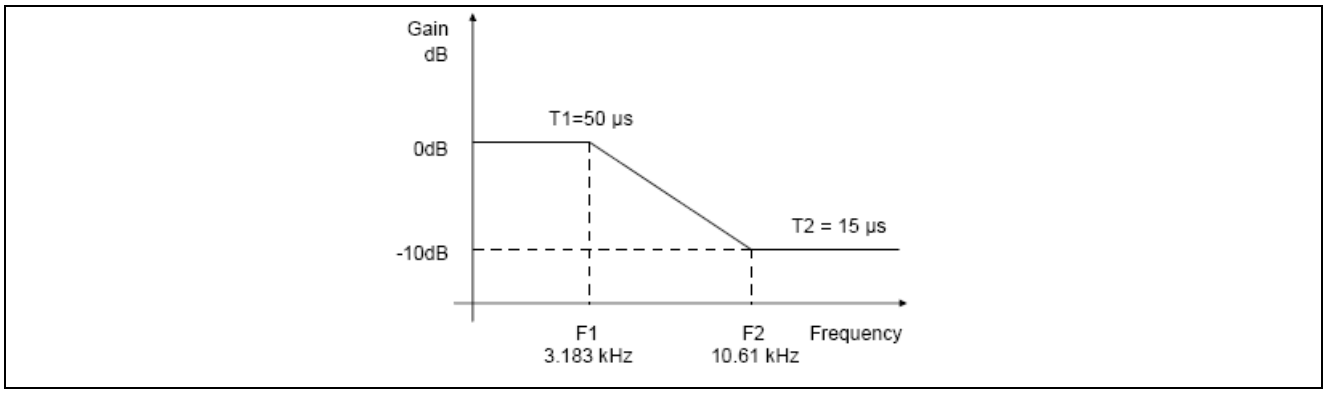


Figure 5. De-Emphasis Curve (Fs = 44.1kHz)

Initialization and Power-Down

The Initialization and Power-down sequence flow chart is shown in Figure 6. The ET4344 family enters the Power-Down State upon initial power-up. The interpolation filters and delta-sigma modulators are reset, and the internal voltage reference, multi-bit digital-to-analog converters and switched-capacitor low-pass filters are powered down. The device will remain in the Power-down mode until MCLK and LRCK are present. Once MCLK and LRCK are detected, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio. Power is then applied to the internal voltage reference. Finally, power is applied to the D/A converters and switched-capacitor filters, and the analog outputs will ramp to the quiescent voltage, VQ.

Output Transient Control

The ET4344 family uses Popguard™ technology to minimize the effects of output transients during power-up and power-down. This technique eliminates the audio transients commonly produced by single-ended single-supply converters when it is implemented with external DC-blocking capacitors connected in series with the audio outputs. To make best use of this feature, it is necessary to understand its operation.

Power-Up

When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to VQ which is initially low. After MCLK is applied the outputs begin to ramp with VQ towards the nominal quiescent voltage. This ramp takes approximately 250ms with a 3.3 µF cap connected to VQ (420ms with a 10µFconnected to VQ) to complete. The gradual voltage ramping allows time for the external DC-blocking capacitors to charge to VQ, effectively blocking the quiescent DC voltage. Once valid LRCK and SDIN are supplied (and SCLK if used) approximately 2000 sample periods later audio output begins.

Power-Down

To prevent audio transients at power-down the DC-blocking capacitors must fully discharge before turning off the power. In order to do this MCLK should be stopped for a period of about 250ms for a 3.3µF cap connected to VQ (420ms for a 10µF cap connected to VQ) before removing power. During this time voltage on VQ and the audio outputs discharge gradually to GND. If power is removed before this time period has passed a transient will occur when the VA supply drops below that of VQ. There is no minimum time for a power cycle, power may be re-applied at any time.

When changing clock ratio or sample rate it is recommended that zero data (or near zero data) be present on SDIN for at least 10 LRCK samples before the change is made. During the clocking change the DAC outputs will always be in a zero data state. If no zero audio is present at the time of switching, a slight click or pop may be heard as the DAC output automatically goes to it's zero data state.

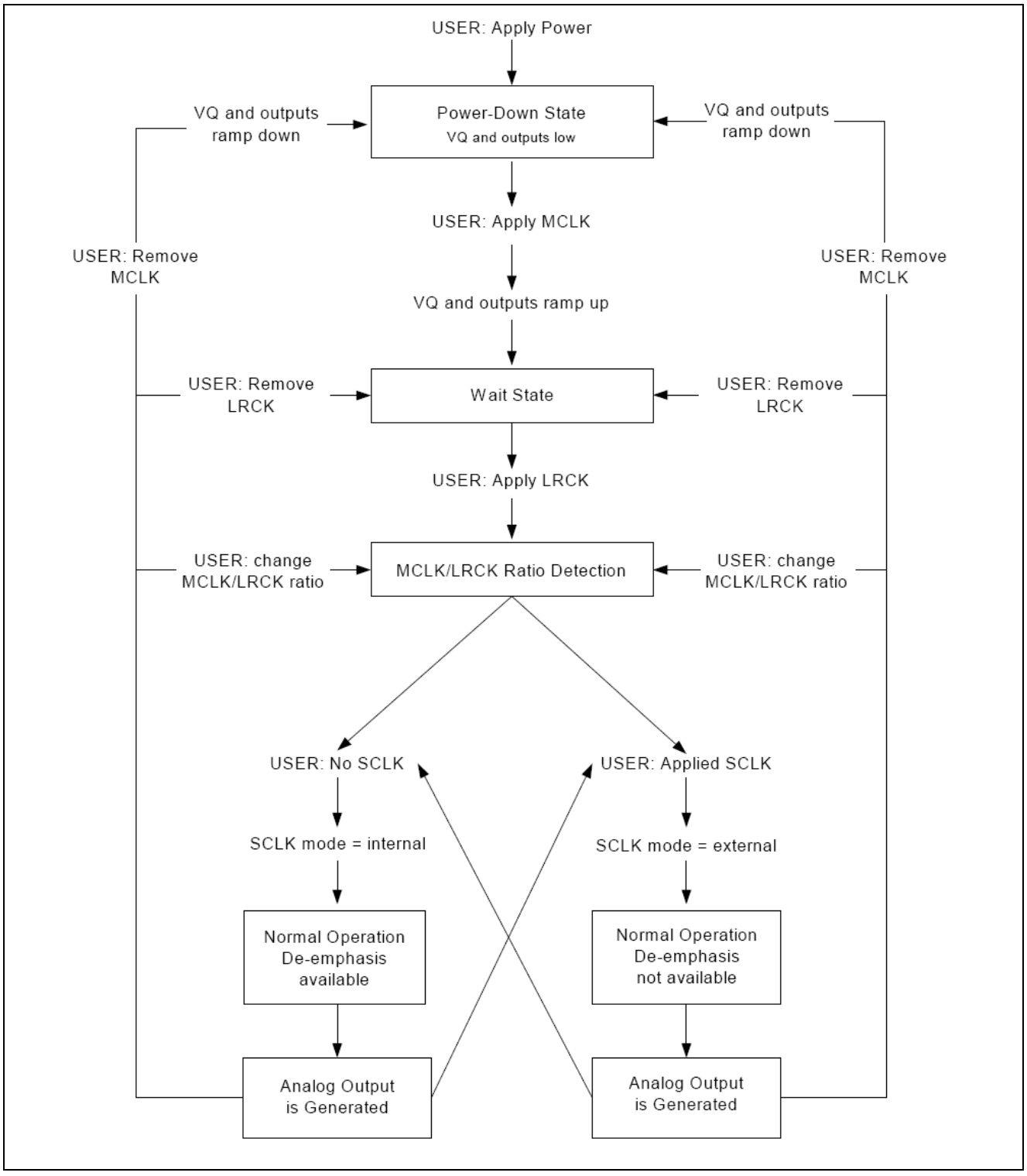


Figure 6. ET4344/5/6/8 Initialization and Power-down Sequence

Grounding and Power Supply Decoupling

As with any high resolution converter, the ET4344 family requires careful attention to power supply and grounding arrangements to optimize performance. Figure 24 shows the recommended power arrangement with VA connected to a clean +3.3V or +5V supply. For best performance, decoupling and filter capacitors should be located as close to the device package as possible with the smallest capacitors closest.

Analog Output and Filtering

The analog filter present in the ET4344 family is a switched-capacitor filter followed by a continuous time low pass filter. Its response, combined with that of the digital interpolator, is given in Figures7-14. There commended external analog circuitry is shown in the "Typical Connection Diagram" on page 16.

FILTER PLOTS

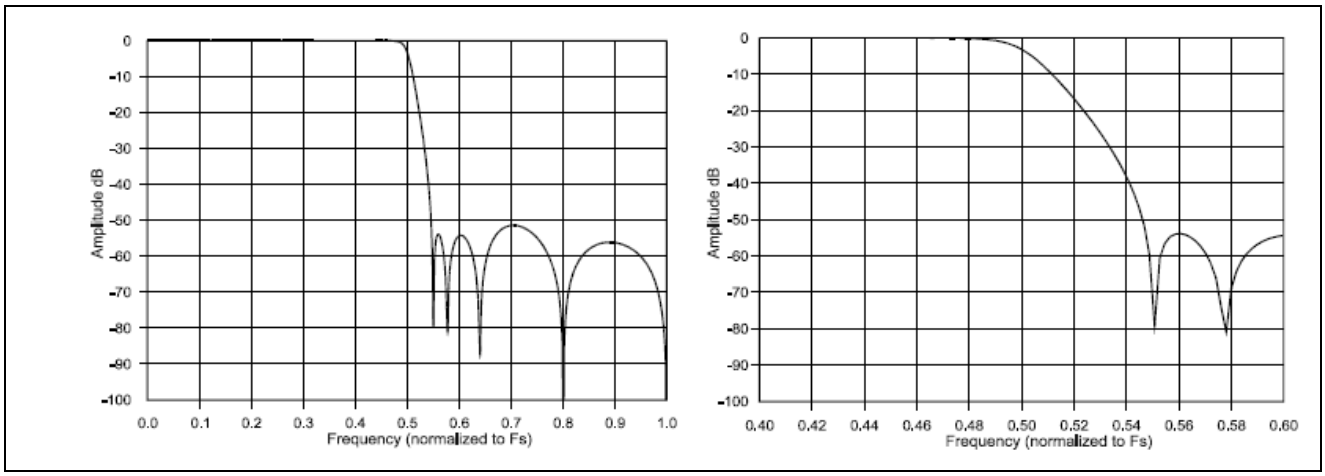


Figure 7. Single-Speed Stopband Rejection

Figure 8. Single-Speed Transition Band

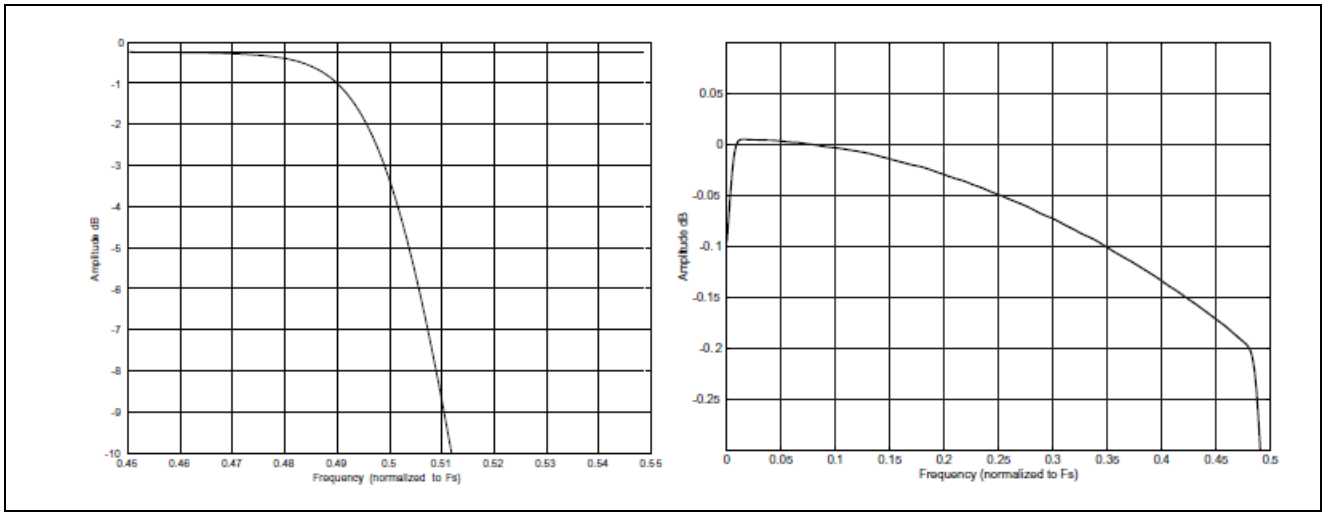


Figure 9. Single-Speed Transition Band

Figure 10. Single-Speed Passband Ripple

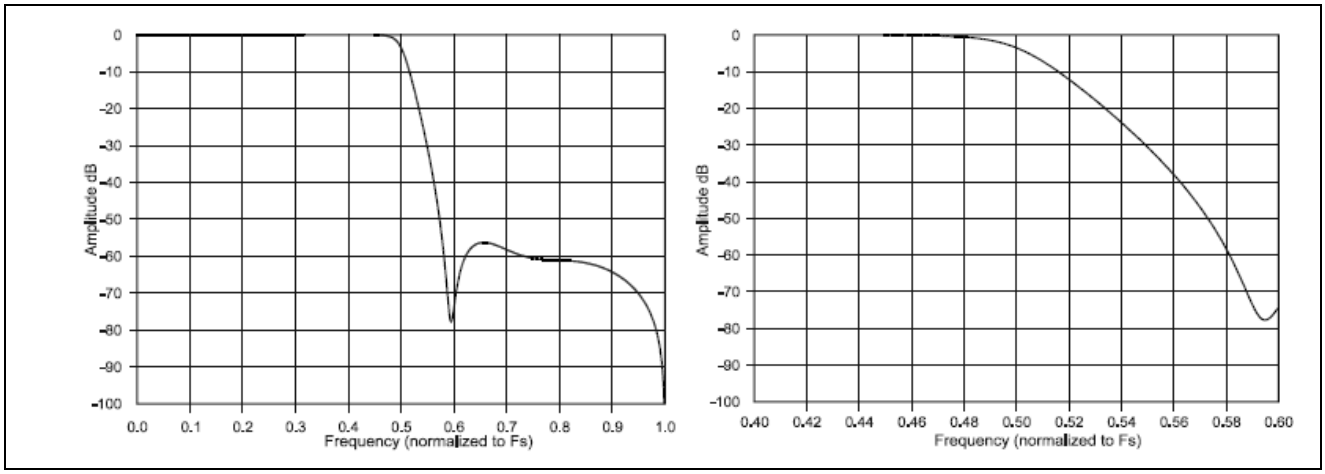


Figure 11. Double-Speed Stopband Rejection

Figure 12. Double-Speed Transition Band

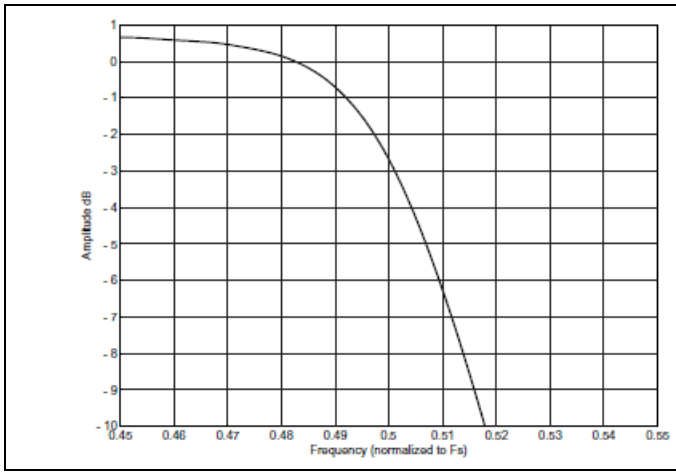


Figure 13. Double-Speed Transition Band

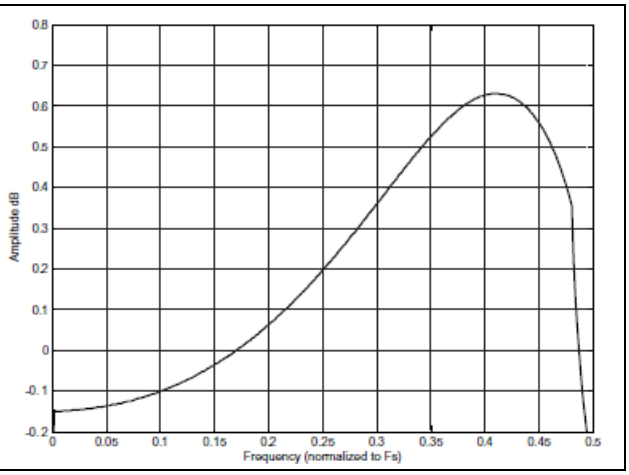


Figure 14. Double-Speed Passband Ripple

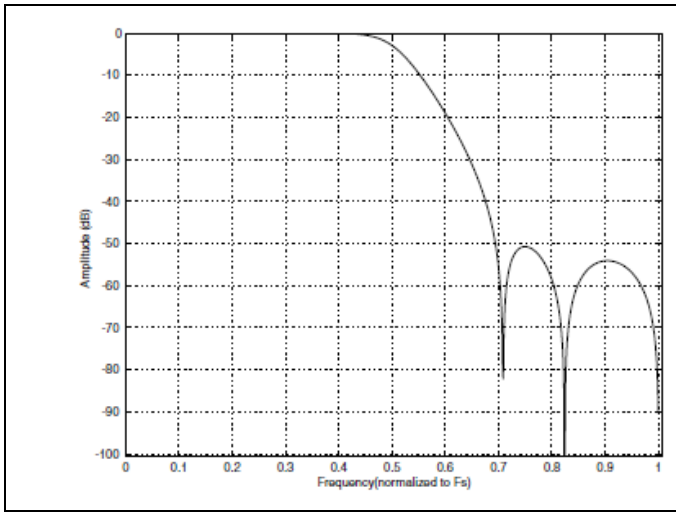


Figure 15. Quad-Speed Stopband Rejection

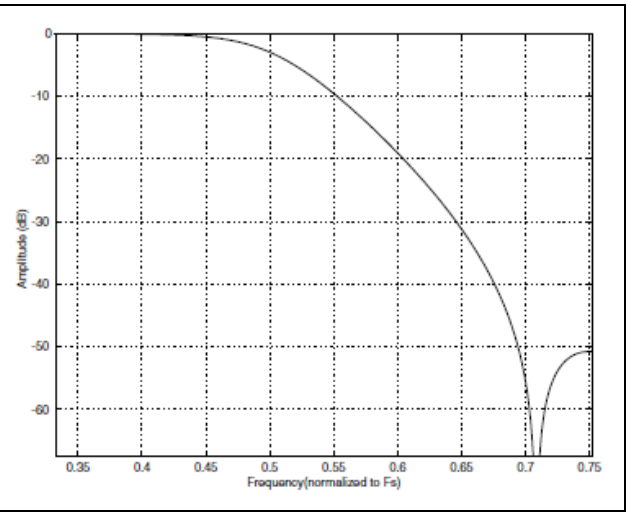


Figure 16. Quad-Speed Transition Band

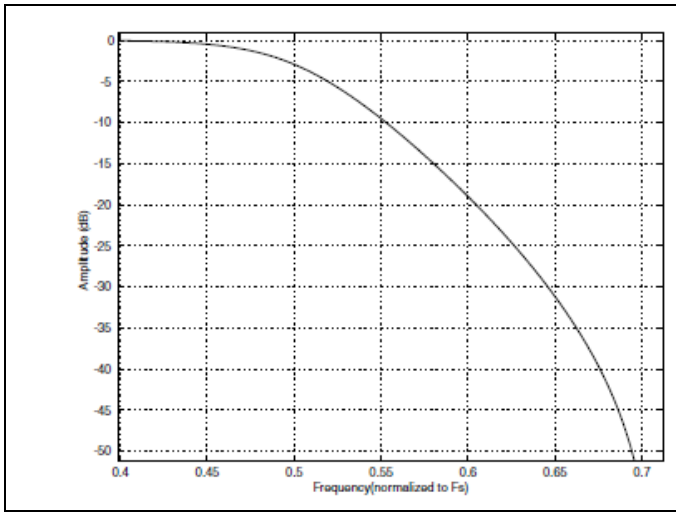


Figure 17. Quad-Speed Transition Band

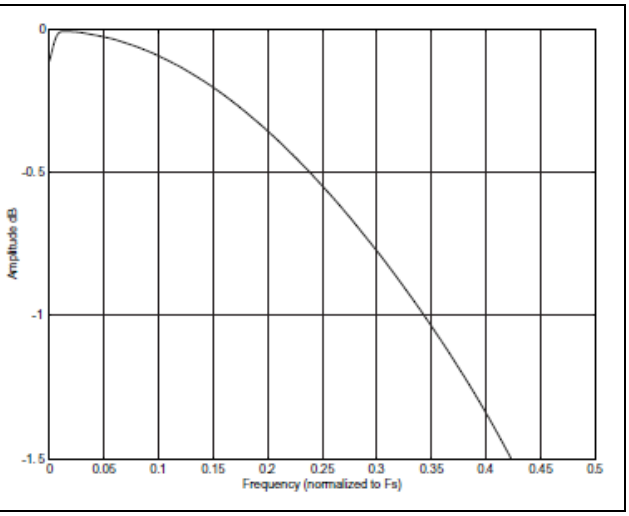


Figure 18. Quad-Speed Passband Ripple

CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltage and T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS（AGND = 0V; all voltages with respect to ground.）

Parameters		Symbol	Min	Tpy	Max	Units
DC Power Supply		VA	4.75	5.0	5.25	V
			3.00	3.3	3.47	V
Specified Temperature Range	-CZZ	T_A	-10	-	+70	℃
	-DZZ		-10	-	+85	℃

Absolute Maximum Ratings

（AGND = 0V; all voltages with respect to ground.）

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA	-0.3	6.0	V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)	T_{op}	-55	125	℃
Storage Temperature	T_{stg}	-65	150	℃

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

DAC ANALOG CHARACTERISTICS

(Full-Scale Output Sine Wave, 997Hz (Note 1), Fs=48/96/192kHz; Test load RL = 3kΩ, CL = 10pF (Figure 19). Measurement Bandwidth 10 Hz to 20kHz, unless otherwise specified.)

Parameter			5V Nom			3.3V Nom			Unit
			Min	Typ	Max	Min	Typ	Max	
Dynamic Performance for ET4344-CZZ (-10 to 70°C)									
Dynamic Range	18 to 24-Bit	A-weighted	99	105	-	97	103	-	dB
		unweighted	96	102	-	94	100	-	dB
	16-Bit	A-weighted	90	96	-	90	96	-	dB
		unweighted	87	93	-	87	93	-	dB
Total Harmonic Distortion + Noise									
	18 to 24-Bit	0 dB	-	-90	-85	-	-90	-85	dB
		-20 dB	-	-82	-76	-	-80	-74	dB
		-60 dB	-	-42	-36	-	-40	-34	dB
	16-Bit	0 dB	-	-90	-84	-	-90	-84	dB
		-20 dB	-	-73	-67	-	-73	-67	dB
		-60 dB	-	-33	-27	-	-33	-27	dB
Dynamic Performance for ET4344-DZZ (-40 to 85°C)									
Dynamic Range	18 to 24-Bit	A-weighted	95	105	-	93	103	-	dB
		unweighted	92	102	-	90	100	-	dB
	16-Bit	A-weighted	86	96	-	86	96	-	dB
		unweighted	83	93	-	83	93	-	dB
Total Harmonic Distortion + Noise									
	18 to 24-Bit	0 dB	-	-90	-82	-	-90	-82	dB

		-20 dB	-	-82	-72	-	-80	-70	dB
		-60 dB	-	-42	-32	-	-40	-30	dB
	16-Bit	0 dB	-	-90	-82	-	-90	-82	dB
		-20 dB	-	-73	-63	-	-73	-63	dB
		-60 dB	-	-33	-23	-	-33	-23	dB

Notes: 1.One-half LSB of triangular PDF dither added to data.

DAC ANALOG CHARACTERISTICS - ALL MODES

Parameter	Symbol	Min	Typ	Max	Unit
Interchannel Isolation (1 kHz)		-	100	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	0.25	dB
Gain Drift		-	100	-	ppm/°C
Analog Output					
Full Scale Output Voltage		0.60•VA	0.65•VA	0.70•VA	Vpp
Quiescent Voltage	V_Q	-	0.5•VA	-	VDC
Max DC Current draw from an AOUT pin	I_{OUTmax}	-	10	-	µA
Max Current draw from VQ	I_{Qmax}	-	100	-	µA
Max AC-Load Resistance(see Figure 20)	R_L	-	3	-	kΩ
Max Load Capacitance(see Figure 20)	C_L	-	100	-	pF
Output Impedance	Z_{OUT}	-	100	-	Ω

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.) See (Note 6)

Parameter	Symbol	Min	Typ	Max	Unit
Combined Digital and On-chip Analog Filter ResponseSingle-Speed Mode					
Passband (Note 2) to -0.1 dB corner		0	-	.35	Fs
to -3 dB corner		0	-	.4992	Fs
Frequency Response 10 Hz to 20 kHz		-.175	-	+.01	dB
StopBand		.5465	-	-	Fs
StopBand Attenuation(Note 3)		50	-	-	dB
Group Delay	tgd	-	10/Fs	-	s
De-emphasis Error (Note 5) Fs = 32 kHz		-	-	+1.5/+0	dB
Fs = 44.1 kHz		-	-	+.05/-.25	dB
Fs = 48 kHz		-	-	-.2/-.4	dB
Combined Digital and On-chip Analog Filter ResponseDouble-Speed Mode					
Passband (Note 2) to +0.1 dB corner		0	-	.22	Fs
to -3 dB corner		0	-	.501	Fs
Frequency Response 10 Hz to 20 kHz		-.15	-	+.15	dB
StopBand		.5770	-	-	Fs
StopBand Attenuation (Note 3)		55	-	-	dB
Group Delay	tgd	-	5/Fs	-	s

Combined Digital and On-chip Analog Filter ResponseQuad-Speed Mode					
Passband (Note 2) to -0.1 dB corner		0	-	0.110	Fs
to -3 dB corner		0	-	0.469	Fs
Frequency Response 10 Hz to 20 kHz		-.12	-	+0	dB
StopBand		0.7	-	-	Fs
StopBand Attenuation (Note 3)		51	-	-	dB
Group Delay	tgd	-	2.5/Fs	-	s

Notes:

2. Response is clock dependent and will scale with Fs.
3. For Single-Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
   For Double-Speed Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.
   For Quad-Speed Mode, the Measurement Bandwidth is 0.7 Fs to 1 Fs.
4. Refer to Figure 20.
5. De-emphasis is available only in Single-Speed Mode.
6. Amplitude vs. Frequency plots of this data are available in "Filter Plots" on page 8.

DIGITAL INPUT CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage(% of VA)	V_{IH}	60%			V
Low-Level Input Voltage(% of VA)	V_{IL}			30%	V
Input Leakage Current(Note 7)	I_{in}			±10	μA
Input Capacitance			8		pF

7.I_{in} for LRCK is ±20μA max.

Electrical Characteristics

Parameters	Symbol	5V Nom			3.3V Nom			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supplies								
Power Supply Currentnormal operation	I_A	-	22	30	-	16	21	mA
(Note 8)power-down state (Note 9)	I_A	-	220	-	-	100	-	μA
Power Dissipationnormal operation	-	-	110	150	-	53	69	mW
power-down state(Note 9)	-	-	1.1	-	-	0.33	-	mW
Package Thermal Resistance	θ_{JA}	-	95	-	-	95	-	℃/Watt
Power Supply Rejection Ratio (Note 8)(1kHz)	PSRR	-	50	-	-	50	-	dB
(60Hz)	-	-	40	-	-	40	-	dB

8.Current consumption increases with increasing FS and increasing MCLK. Typ and Max values arebased on highest FS and highest MCLK. Variance between speed modes is small.

9.Power down mode is defined when all clock and data lines are held static.

10.Valid with the recommended capacitor values on VQ and FILT+ as shown in the typical connection di-agram.

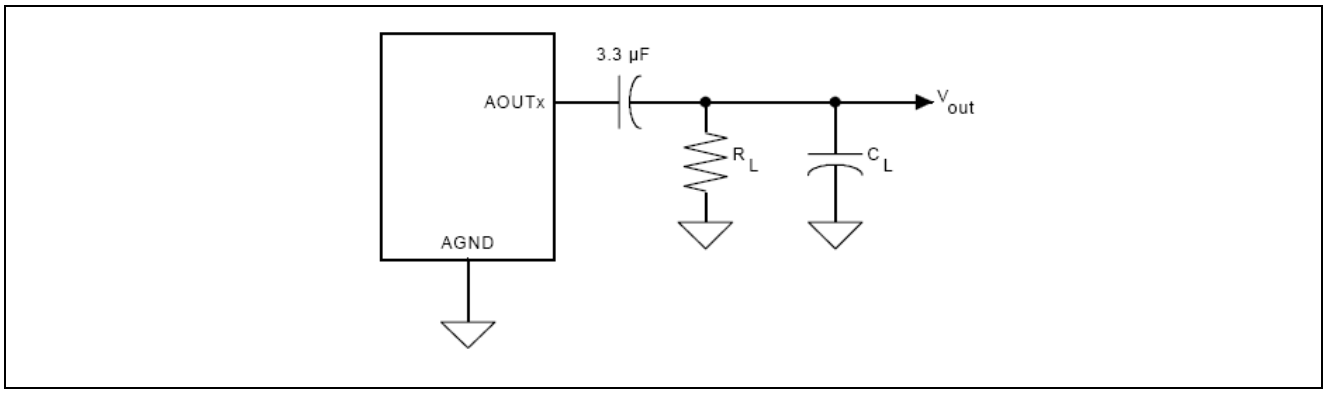


Figure 19. Output Test Load

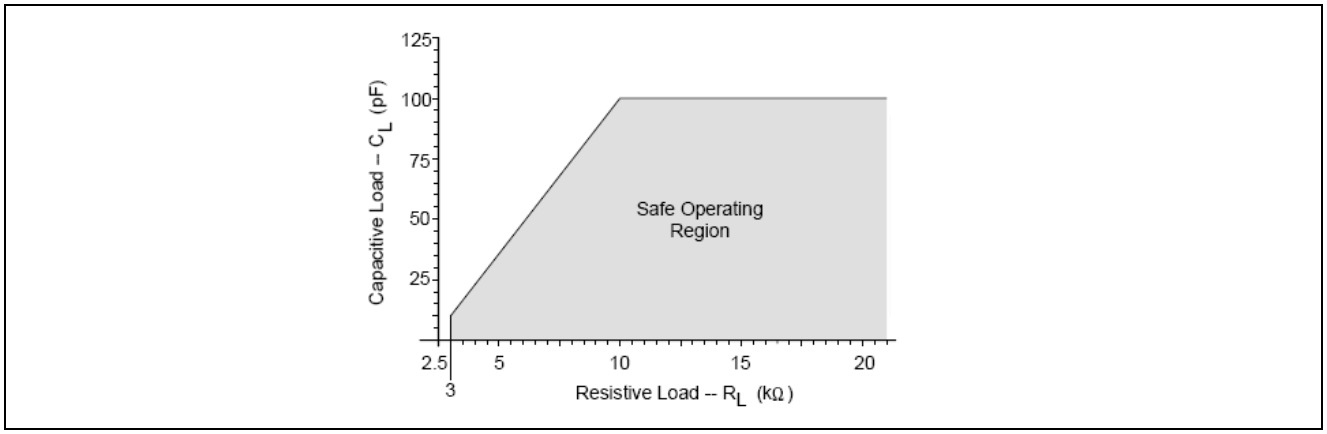


Figure 20. Maximum Loading

SWITCHING CHARACTERISTICS-SERIAL AUDIO INTERFACE

Parameters	Symbol	Min	Typ	Max	Units
MCLK Frequency		0.512	-	50	MHz
MCLK Duty Cycle		45	-	55	%
Input Sample Rate All MCLK/LRCK ratios combined	Fs	2		200	kHz
(Note 11)256x, 384x, 1024x		2		50	kHz
256x, 384x		84		134	kHz
512x, 768x		42		67	kHz
1152x		30		34	kHz
128x, 192x		50		100	kHz
64x, 96x		100		200	kHz
128x, 192x		168		200	kHz
External SCLK Mode					
LRCK Duty Cycle (External SCLK only)		45	50	55	%
SCLK Pulse Width Low	t_{sclkl}	20	-	-	ns
SCLK Pulse Width High	t_{sclkh}	20	-	-	ns
SCLK Duty Cycle		45	50	55	%
SCLK rising to LRCK edge delay	t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time	t_{slrs}	20	-	-	ns

SDIN valid to SCLK rising setup time	t_{sdlrs}	20	-	-	ns
SCLK rising to SDIN hold time	t_{sdh}	20	-	-	ns
Internal SCLK Mode					
LRCK Duty Cycle (Internal SCLK only) (Note 12)		-	50	-	
SCLK Period(Note 13)	t_{sclkw}	10^9/SCLK	-	-	ns
SCLK rising to LRCK edge	t_{sclkr}	-	tsclkw/2	-	µs
SDIN valid to SCLK rising setup time	t_{sdlrs}	10^9/(512)Fs+10	-	-	ns
SCLK rising to SDIN hold timeMCLK / LRCK =1152, 1024, 512, 256, 128, or 64	t_{sdh}	10^9/(512)Fs+15	-	-	ns
SCLK rising to SDIN hold timeMCLK / LRCK = 768, 384, 192, or 96	t_{sdh}	10^9/(384)Fs+15	-	-	ns

11.Not all sample rates are supported for all clock ratios. See Table1, “Common Clock Frequencies,” on page12 for supported ratio’s and frequencies.

12.In Internal SCLK Mode, the Duty Cycle must be 50% +/− 1/2 MCLK Period.

13.The SCLK / LRCK ratio may be either 32, 48, 64, or 72. This ratio depends on part type andMCLK/LRCK ratio. (See Figures1-3)

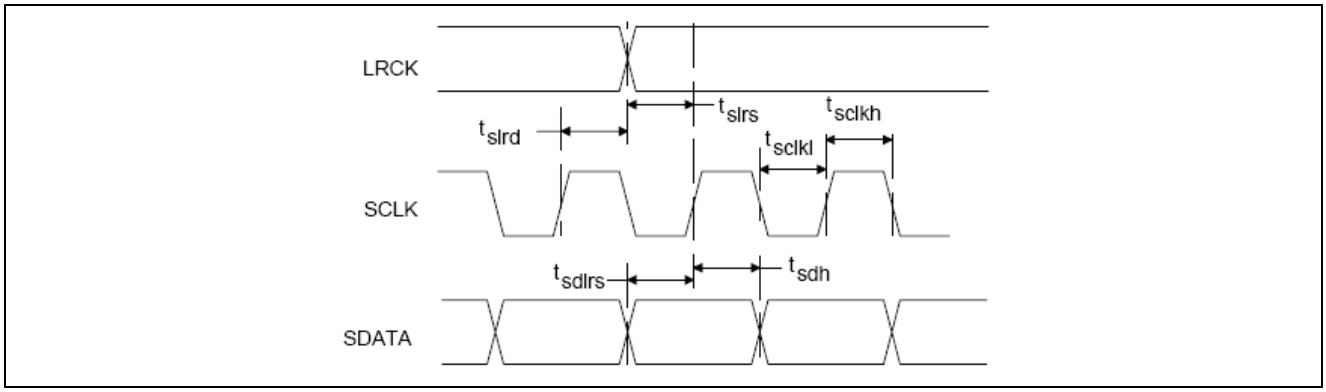
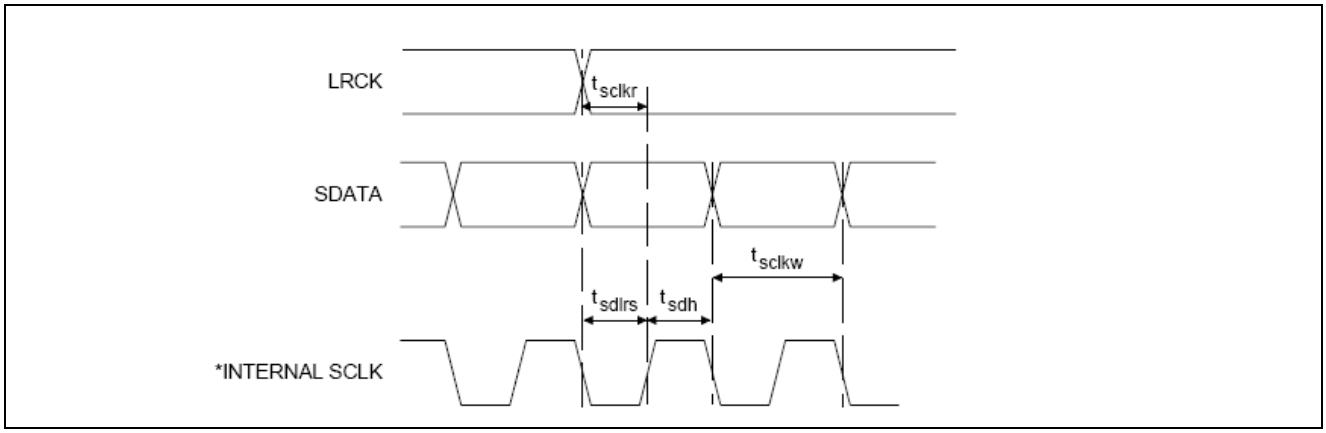
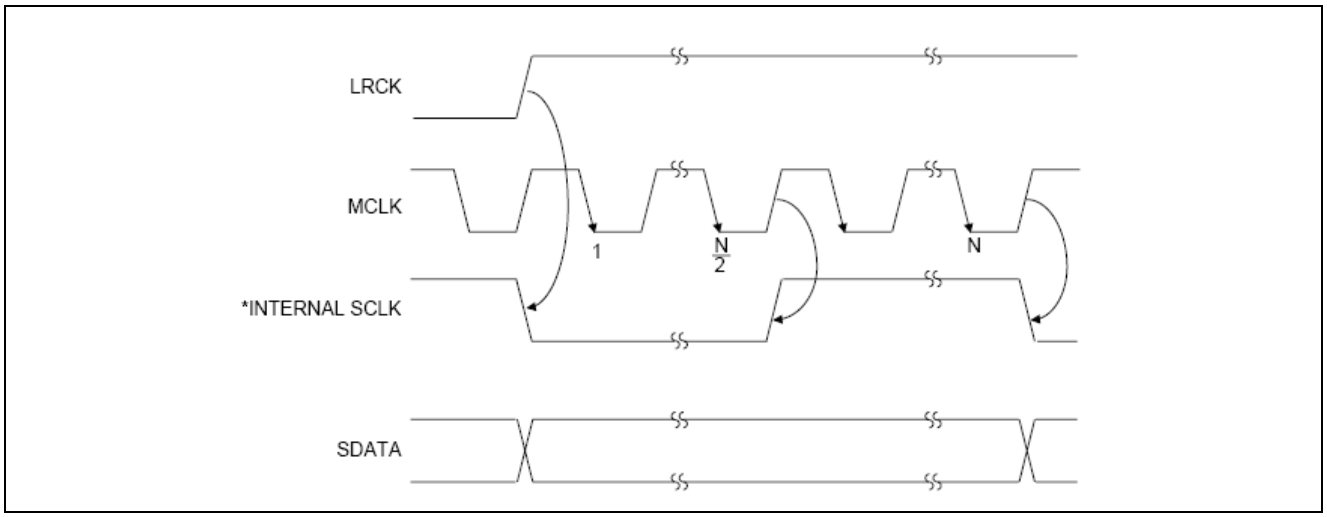


Figure 21. External Serial Mode Input Timing



The SCLK pulses shown are internal to the ET4344/5/6/8.

Figure 22. Internal Serial Mode Input Timing



The SCLK pulses shown are internal to the ET4344/5/6/8.

N equals MCLK divided by SCLK

Figure 23. Internal Serial Clock Generation

Application Circuits

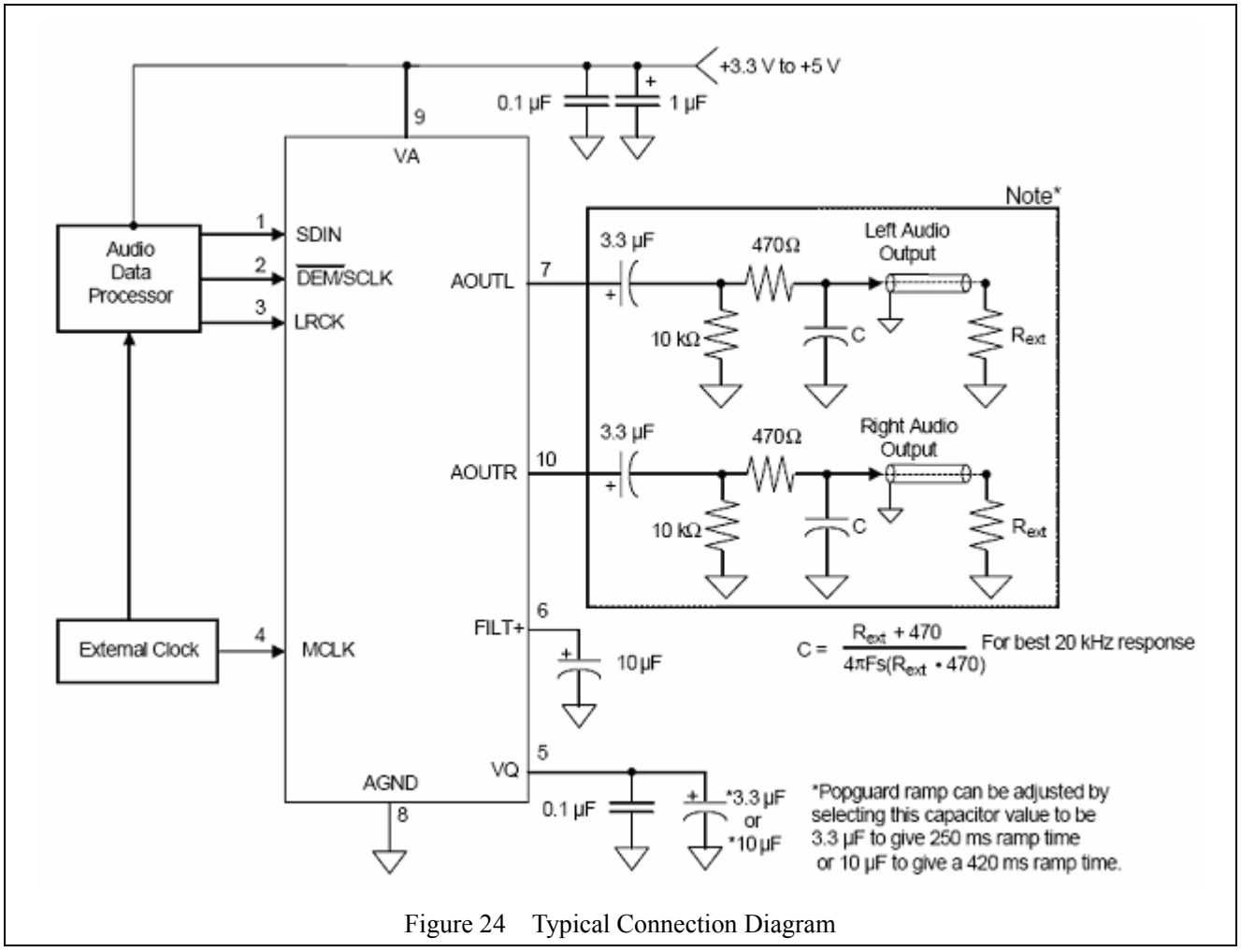


Figure 24 Typical Connection Diagram

Package Dimension

MSOP10