T-42-11-13

February 1990
Edition 1.1

FUJITSU

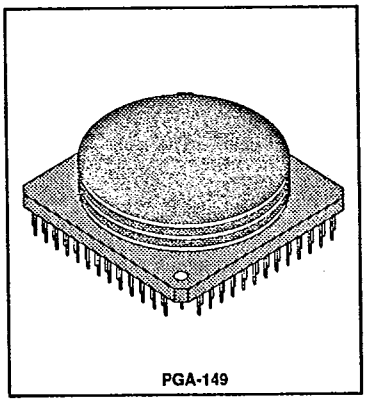
DATA SHEET

ET750, ET1500, ET3000, ET4500
ECL Series Gate Arrays

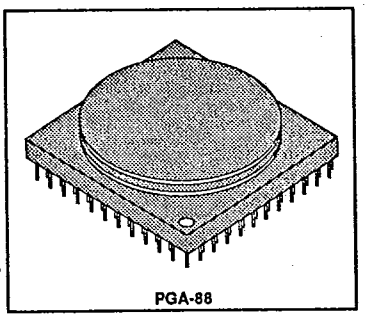
DESCRIPTION

The Fujitsu ET series gate array family is a group of high-speed gate arrays with flexible I/O access. Designed to provide fast ECL internal cells with TTL, ECL, or mixed TTL/ECL input/output buffers, these gate arrays are ideal choices for LSI and VLSI applications that require up to 6160 gates, with high speed internal macrocells and a choice of I/O access.

Used in conjunction with Fujitsu's proprietary integrated design system software on popular CAE workstations, the Fujitsu ECL Series Gate Arrays family of devices lets you define the logical functions to be implemented in the array, and gives you the convenience of TTL with the fast computational power of ECL. You get 100 percent place and route with 90 percent utilization guaranteed.



PGA-149



PGA-88

GENERAL FEATURES

- High speed series gated ECL internal cells
- Mixed ECL/TTL input/output buffers
- 100K series supported upon request
- tpd = 0.22 ns/gate[1]
- tpd = 0.50 ns/gate[2]
- 5.0 ns/pair of TTL I/O buffers

ET750 FEATURES

- Up to 1056 equivalent gates[3]
- 48 fixed-pin ECL output buffers
- 64 TTL input buffers
- 48 non-fixed pin TTL output buffers
- Typical 2 to 3W power dissipation
- 88-pin ceramic pin grid array package

ET1500 FEATURES

- Up to 2112 equivalent gates[3]
- 64 fixed-pin ECL output buffers
- 88 TTL input buffers
- 64 non-fixed pin TTL output buffers
- Typical 3 to 4.5 W power dissipation
- 88-pin ceramic pin grid array package
- 121-pin ceramic pin grid array package

ET3000 FEATURES

- Up to 4224 equivalent gates[3]
- 72 fixed pin ECL output buffers
- 120 TTL input buffers
- 72 non-fixed pin TTL output buffers
- Typical 6 to 7 W power dissipation
- 149-pin ceramic pin grid array package

ET4500 FEATURES

- Up to 6160 equivalent gates[3]
- 84 fixed pin ECL output buffers
- 120 TTL input buffers
- 84 non-fixed pin TTL output buffers
- Typical 9 to 10.2 W power dissipation
- 149-pin ceramic pin grid array package
- 164-pin flat package

[1]Unloaded (F/I = F/O = 1, L = 0 mm)
[2]Typical load (F/I = F/O = 3, L = 3 mm)
[3]Configured as full adders: 1 full adder = 2 basic cells = 11 optimal gates

ELECTRICAL CHARACTERISTICS

FLEXIBLE I/O

I/O Buffer	Power Supply			I/O Buffer	Power Supply		
TTL Level (Pseudo-ECL supported upon request)	+5 V	0 V	—	Mixed ECL/TTL Level	+5 V	0 V	−5.2 V
				ECL Level	—	0 V	−5.2 V

ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Supply Voltage	TTL	V_{CC}	7.0	V
	ECL	V_{EE}	−7.0	
Input Voltage	TTL	V_I	−0.5 to +5.5	V
	ECL		0 to V_{EE}	
Output Voltage	TTL	V_O	−0.5 to +5.5	V
Output Current	ECL 50Ω	I_O	−30	mA
Storage Temperature		T_{STG}	−55 to +150	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition
Supply Voltage	TTL	V_{CC}	+5.0 V ± 5%
	ECL	V_{EE}	−5.2 V ± 5%
Terminating Voltage	ECL	V_T	−2.0 V
Output High Current	TTL	I_{OH}	−2.6 mA max
Output Low Current	TTL	I_{OL}	8.0 mA max
Ambient Temperature		T_A	0 to 70°C
Air Flow		V	5 m/s

ELECTRICAL CHARACTERISTICS (Continued)

ECL DC CHARACTERISTICS (10KH Level)

Recommended operating conditions unless otherwise specified

Parameter		Symbol	Condition	T_A	Value Minimum	Value Maximum	Unit
Output High Voltage		V_{OH}	V_{IH} = −0.9V, V_{IL} = −1.7V	0°C	−1.000	−0.840	V
				25°C	−0.960	−0.810	
				70°C	−0.900	−0.740	
			V_{IH} = −0.9V, V_{IL} = −1.7V[1]	0°C	−1.060	−0.840	
				25°C	−1.020	−0.810	
				70°C	−0.960	−0.740	
Output Low Voltage		V_{OL}	V_{IH} = −0.9V, V_{IL} = −1.7V	0°C	−1.950	−1.650	V
				25°C	−1.950	−1.650	
				70°C	−1.950	−1.620	
			V_{IH} = −0.9V, V_{IL} = −1.7V[1]	0°C	−2.020	−1.950	
				25°C			
				70°C			
Input High Current	Normal Input	I_{IH}	V_{IH} = −0.9V, V_{IL} = −1.8V[2]			40 x N[3]	µA
	Clock Buffer					200	
Input Low Current	Upper Level Input of Series Gate	I_{IL}	V_{IH} = −0.9V, V_{IL} = −1.8V[2]			−10	µA
	Lower Level Input of Series Gate					40 x N[3]	
Input Voltage		I_{IH}		0°C		−0.840	V
				25°C		−0.810	
				70°C		−0.730	
		I_{IL}		0°C	−1.950		
				25°C	−1.950		
				70°C	−1.950		
		V_{ITH}		0°C	−1.170		
				25°C	−1.130		
				70°C	−1.070		
		V_{ITL}		0°C		−1.480	
				25°C		−1.480	
				70°C		−1.475	

Notes: [1]Cut-off mode output buffer
[2]Levels of V_{IH} = 0.9V, V_{IL} = 1.7V are allowable for non-measured pins
[3]N = total number of input loading factor of gates connected to input pins

ELECTRICAL CHARACTERISTICS (Continued)

TTL DC CHARACTERISTICS[1]

Recommended operating conditions unless otherwise specified

Parameter		Symbol	Condition	V_{CC}	Value			Unit
					Minimum	Typ.	Maximum	
Input Low Voltage		V_{IL}	—	—	—	—	0.8	V
Input High Voltage		V_{IH}	—	—	2.0	—	—	V
Output Low Voltage		V_{OL}	I_{OL} = 8 mA	4.75	—	—	0.5	V
Output High Voltage		V_{OH}	I_{OH} = 2.6 mA	4.75	2.4	—	—	V
Input Low Current	Normal	I_{IL1}	V_I = 0.5 V	5.25	—	—	–400	µA
	with Pull-up Resistor	I_{IL2}			—	—	–600	
Input High Current	Normal	I_{IH1}	V_I = 2.4 V	5.25	—	—	20	µA
	Normal and Pull-up	I_{IH2}	V_I = 5.5 V		—	—	200	
Output Short Current		I_{OS}	V_O = 0.5 [2]	5.25	–10	—	–90	mA
Input Clamp Voltage		V_{IC}	I_C = –18 mA	4.75	–0.1	—	–1.5	V
Power Supply Current		I_{CC}	—	5.25	—	•	+50%	mA
Output Hi-Z Leakage Current (3-state output)		I_{OZ}[1]	V_O = 0.5 V, 2.4 V	5.25	–100	—	–100	µA
Output Hi-Z Leakage Current (bidirectional)		I_{OZ}[2]	V_O = 0.5 V, 2.4 V		–500	—	–120	

Notes: [1]Typical value at Vcc = –5.2V, TA = 25_C
[2]Only one output may be shorted at a time for more than one second
• Circuitry dependent

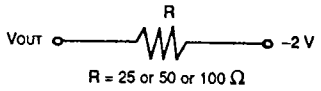
ECL AC CHARACTERISTICS

Recommended operating conditions unless otherwise specified

Parameter	Symbol	Condition	Value in ns
Propagation Delay Time	t_{PLH}	V_{CC} = 5 V V_{EE} = –5.2 V V_A = 0 to 70_C	Maximum: t_{pd} (Typ) x 1.7 + 2 Minimum: t_{pd} (Typ) x 0.3 – 2
	t_{PHL}		

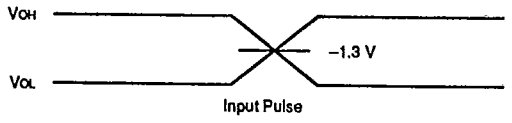
ECL LOAD CIRCUIT MEASUREMENT CONDITIONS

Load Circuit
ECLConfiguration



R = 25 or 50 or 100 Ω

AC Characteristics Measurement Waveform
ECL Configuration



Input Pulse

$t_r = t_f$ = 1.0 ns (20 to 80%)
V_{IN} = –0.9 V, V_{IL} = –1.7 V

ELECTRICAL CHARACTERISTICS (Continued)

TTL AC CHARACTERISTICS

Recommended operating conditions unless otherwise specified

Parameter	Symbol	Condition	Value in ns
Propagation Delay Time	t_{pLH}	V_{CC} = 5 V T_A = 0 to 70°C	Maximum: t_{pd} (Typ) x 1.7 + 2 Minimum: t_{pd} (Typ) x 0.3 – 2
	t_{pHL}		
Enable Time	t_{pZL}		
	t_{pZH}		
Disable Time	t_{pLZ}		
	t_{pHZ}		

TTL LOAD CIRCUIT MEASUREMENT CONDITIONS

Parameter	Output Type	Symbol	CL(pF)	RI(kΩ)	RL(kΩ)	SW1	SW2
Propagation Delay Time	Totem Pole 3-state Bidirectional	t_{pLH}	50	—	1.0	OFF	ON
		t_{pHL}					
	Open Collector	t_{pLH}		0.5	—	ON	OFF
		t_{pHL}					
Disable Time	3-state Bidirectional	t_{pLZ}	5	0.5	1.0	ON	ON
		t_{pHZ}				OFF	ON
Enable Time	3-state Bidirectional	t_{pZL}	50	0.5	1.0	ON	ON
		t_{pZH}		0.5	1.0	OFF	ON

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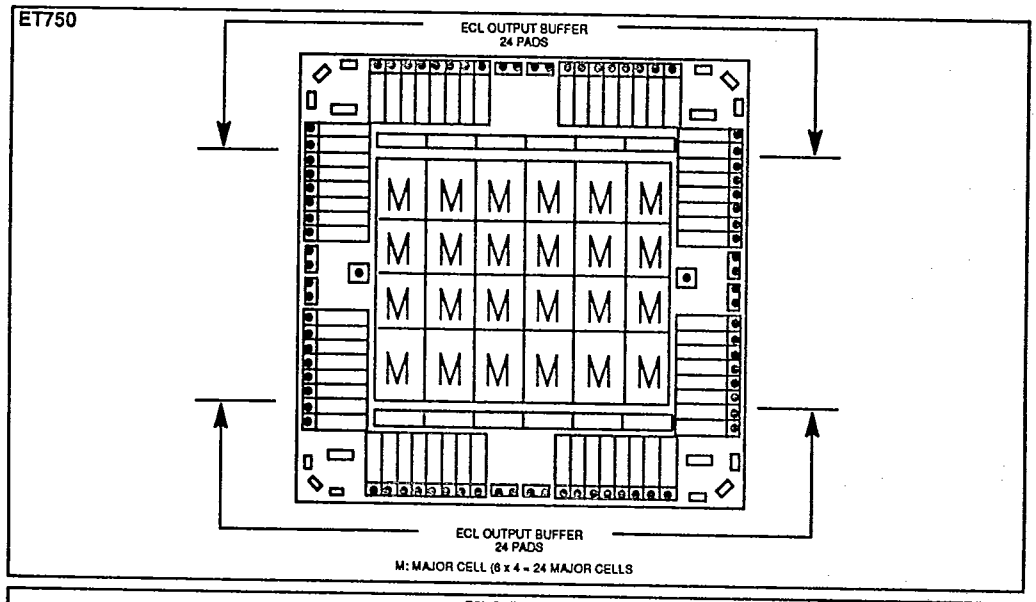
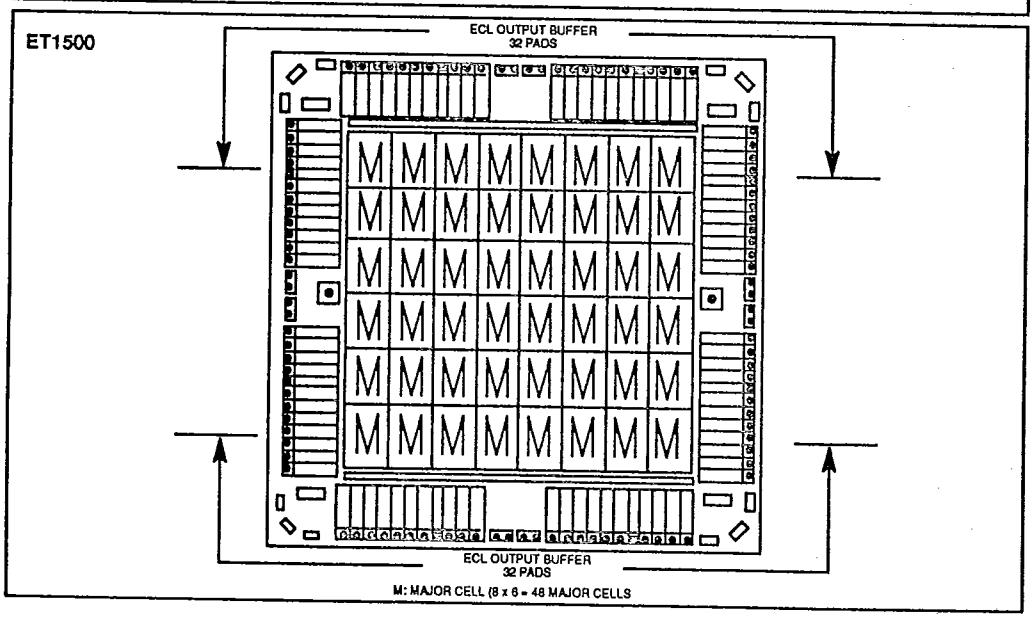
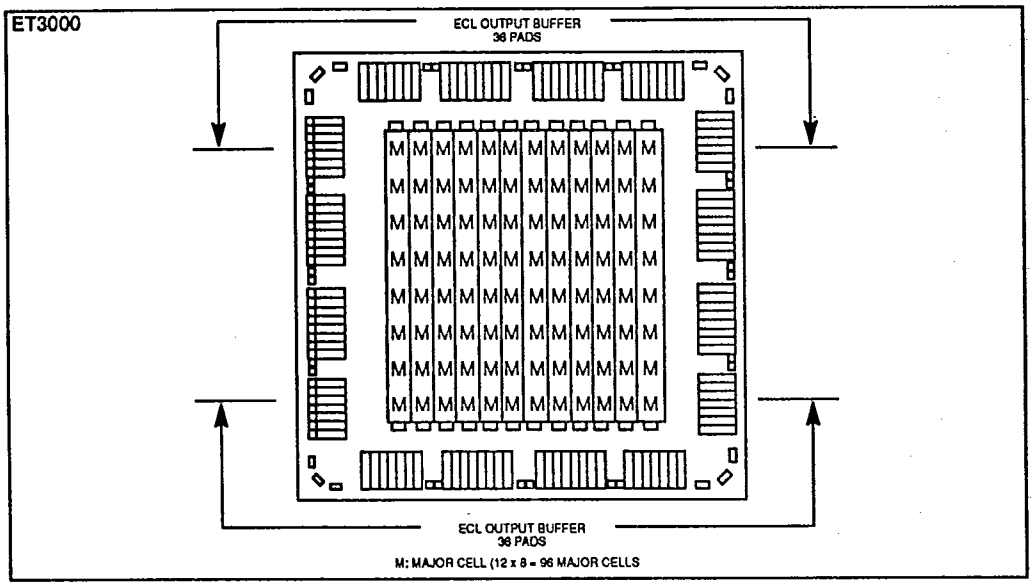
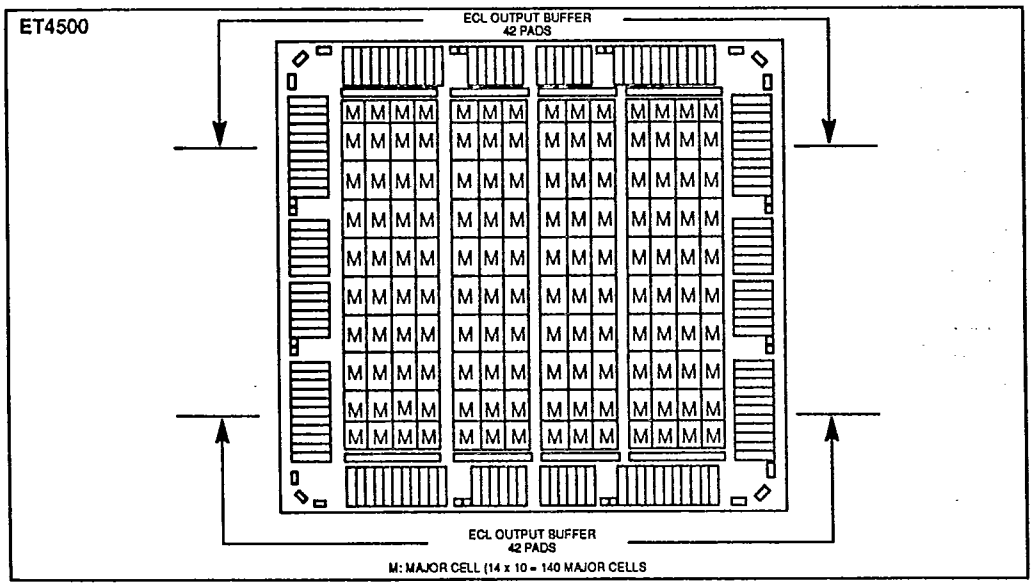
ET750 AND ET1500 Gate Array Chip Layout And I/O Buffer Organization





ET3000 AND ET4500 Gate Array Chip Layout And I/O Buffer Organization





MACROCELL LIBRARY

EXTERNAL BUFFERS

TTL Input Buffers		
Name	**Function**	**I/O Cells**
IN1	Inverting Input Buffer	1
IN1P	Inverting Input Buffer with Input Pull-up	1
IC1	Complementary 1-input Input Buffer	1
IC1P	Complementary 1-input Input Buffer with Input Pull-up	1
INK2	Inverting Input Clock Buffer (F/O=50)	1
IAK2	Non-inverting Input Clock Buffer (F/O=50)	1
TTL Output Buffers		
Name	**Function**	**I/O Cells**
ON1	Inverting Output Buffer	1
OA1	Non-inverting Output Buffer	1
ON1D	Inverting Output Buffer (Driver)	1
OA1D	Non-inverting Output Buffer (Driver)	1
ON1O	Inverting Output Buffer (O/C Type)	1
OA1O	Non-inverting Output Buffer (O/C Type)	1
ON1OD	Inverting Output Buffer (O/C Type, Driver)	1
OA1OD	Non-inverting Output Buffer (O/C Type, Driver)	1
ON1T	Inverting Output Buffer (3-state Output) (Differential Enable)	1
OA1T	Non-inverting Output Buffer (3-state Output) (Differential Enable)	1
OD1T	Differential Input Output Buffer (3-state High Enable)	1
OD2T	Differential Input Output Buffer (3-state Low Enable)	1
ON1TD	Inverting Output Buffer (3-state Output, Driver) (Differential Enable)	1
OA1TD	Non-inverting Output Buffer (3-state Output, Driver) (Differential Enable)	1
OD1TD	Differential Input Output Buffer (3-state, High Enable, Driver)	1
OD2TD	Differential Input Output Buffer (3-state, Low Enable, Driver)	1
TTL Bidirectional Buffer		
Name	**Function**	**I/O Cells**
BN1N	Bidirectional Buffer, Output: Inverting, Input: Inverting	1
BA1N	Bidirectional Buffer, Output: Non-inverting, Input: Inverting	1
BD1N	Bidirectional Buffer, Output: Differential Input, Input: Inverting (High Enable)	1
BD2N	Bidirectional Buffer, Output: Differential Input, Input: Inverting (Low Enable)	1

MACROCELL LIBRARY (Continued)

EXTERNAL BUFFERS

TTL Input Buffers

Name	Function	I/O Cells
IT1	Non-inverting TTL Input Buffer	1
IR1P	Non-inverting TTL Input Buffer with Input Pull-up	1

TTL Output Buffers

Name	Function	I/O Cells
OTR1	Non-inverting TTL Output Buffer	1
OTR2	2-input OR TTL Output Buffer	1
OTR3	3-input OR TTL Output Buffer	1
OTN1	Inverting TTL Output Buffer	1
OTN2	2-input NOR TTL Output Buffer	1
OTN3	3-input NOR TTL Output Buffer	1
OTR1O	Non-inverting TTL Output Buffer (O/C Type)	1
OTR2O	2-input OR TTL Output Buffer (O/C Type)	1
OTR3O	3-input OR TTL Output Buffer (O/C Type)	1
OTN1O	Inverting TTL Output Buffer (O/C Type)	1
OTN2O	2-input NOR TTL Output Buffer (O/C Type)	1
OTN3O	3-input NOR TTL Output Buffer (O/C Type)	1
OTR1D	Non-inverting TTL Output Buffer (Driver)	1
OTR2D	2-input OR TTL Output Buffer (Driver)	1
OTR3D	3-input OR TTL Output Buffer (Driver)	1
OTN1D	Inverting TTL Output Buffer (Driver)	1
OTN2D	2-input NOR TTL Output Buffer (Driver)	1
OTN3D	3-input NOR TTL Output Buffer (Driver)	1
OTR1OD	Non-inverting TTL Output Buffer (O/C Type, Driver)	1
OTR2OD	2-input OR TTL Output Buffer (O/C Type, Driver)	1
OTR3OD	3-input OR TTL Output Buffer (O/C Type, Driver)	1
OTN1OD	Inverting TTL Output Buffer (O/C Type, Driver)	1
OTN2OD	2-input NOR TTL Output Buffer (O/C Type, Driver)	1
OTN3OD	3-input NOR TTL Output Buffer (O/C Type, Driver)	1
OTR1T	Non-inverting TTL Output Buffer (3-state)	1
OTR2T	2-input OR TTL Output Buffer (3-state)	1
OTN1T	Inverting TTL Output Buffer (3-state)	1
OTN2T	2-input NOR TTL Output Buffer (3-state)	1

TTL Bidirectional Buffers

Name	Function	I/O Cells
BTR2A	Bidirectional Buffer, Output: 2-input OR Input: Non-inverting	1
BTN2A	Bidirectional Buffer, Output: 2-input NOR Input: Non-inverting	1

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MACROCELL LIBRARY (Continued)

EXTERNAL BUFFERS

ECL Input Buffers		
Name	**Function**	**I/O Cells**
IE1	ECL Dummy Buffer	1
IED	ECL Dummy Buffer for Differential Macro	1
IEDX	ECL Dummy Buffer for Differential Macro	1

ECL Clock Input Buffers		
Name	**Function**	**I/O Cells**
IENK2	ECL Input Clock Buffer	1
IEAK2	ECL Input Clock Buffer	1
IEDCK2	Differential Input Clock Receiver	1
IEDAK2	Differential Input Clock Receiver	1
IEDNK2	Differential Input Clock Receiver	1

ECL Output Buffers, 100Ω Termination		
Name	**Function**	**I/O Cells**
OER1X	Non-inverting ECL Output Buffer	1
OER2X	2-input OR ECL Output Buffer	1
OER3X	3-2input OR ECL Output Buffer	1
OEN1X	Inverting ECL Output Buffer	1
OEN2X	2-input NOR ECL Output Buffer	1
OEN3X	3-input NOR ECL Output Buffer	1
OER1YD	Non-inverting ECL Output Buffer 50Ω Cutoff Driver	1
OER2YD	2-input OR ECL Output Buffer 50Ω Cutoff Driver	1
OER3YD	3-input OR ECL Output Buffer 50Ω Cutoff Driver	1

ECL Output Buffers, 50Ω Termination		
Name	**Function**	**I/O Cells**
OER1Y	Non-inverting ECL Output Buffer	1
OER2Y	2-input OR ECL Output Buffer	1
OER3Y	3-input OR ECL Output Buffer	1
OEN1Y	Inverting ECL Output Buffer	1
OEN2Y	2-input NOR ECL Output Buffer	1
OEN3Y	3-input NOR ECL Output Buffer	1
OER1ZD	Non-inverting ECL Output Buffer	1
OER2ZD	2-input OR ECL Output Buffer	1
OER3ZD	3-input OR ECL Output Buffer	1

MACROCELL LIBRARY (Continued)

EXTERNAL BUFFERS

ECL Bidirectional Buffers, 100Ω Termination

Name	Function	I/O Cells
BER1YD	Bidirectional ECL Buffer, Output: Non-inverting; Input: Non-inverting, 50Ω Cutoff Driver	1
BER2YD	Bidirectional ECL Buffer, Output: 2-input OR; Input: Inverting, 50Ω Cutoff Driver	1
BER3YD	Bidirectional ECL Buffer, Output: 3-input OR; Input: Inverting, 50Ω Cutoff Driver	1

ECL Bidirectional Buffers, 50Ω Termination

Name	Function	I/O Cells
BER1ZD	Bidirectional ECL Buffer Output: Non-inverting; Input: Non-inverting, 25Ω Cutoff Driver	1
BER2ZD	Bidirectional ECL Buffer Output: 2-input OR; Input: Inverting, 25Ω Cutoff Driver	1
BER3ZD	Bidirectional ECL Buffer Output: 3-input OR; Input: Inverting, 25Ω Cutoff Driver	1

ECL Re-entry Buffers, 100Ω Termination

Name	Function	I/O Cells
RER1X	Re-entry ECL Buffer, Output: Non-inverting; Input: Non-inverting	1
RER2X	Re-entry ECL Buffer, Output: 2-input OR; Input: Inverting	1
RER3X	Re-entry ECL Buffer, Output: 3-input OR; Input: Inverting	1
REN1X	Re-entry ECL Buffer, Output: Inverting; Input: Non-inverting	1
REN2X	Re-entry ECL Buffer, Output: 2-input NOR; Input: Non-inverting	1
REN3X	Re-entry ECL Buffer, Output: 3-input NOR; Input: Non-inverting	1

ECL Re-entry Buffers, 50Ω Termination

Name	Function	I/O Cells
RER1X	Re-entry ECL Buffer Output: Non-inverting; Input: Non-inverting	1
RER2X	Re-entry ECL Buffer Output: 2-input OR; Input: Inverting	1
RER3X	Re-entry ECL Buffer Output: 3-input OR; Input: Inverting	1
REN1Y	Re-entry ECL Buffer Output: Non-inverting; Input: Non-inverting	1
REN2Y	Re-entry ECL Buffer Output: 2-input OR; Input: Inverting	1
REN3Y	Re-entry ECL Buffer Output: 3-input OR; Input: Inverting	1

ECL Complementary Output Buffers, 50Ω Termination

Name	Function	I/O Cells
OEDCY	50Ω Complementary Output Driver	1
OEC1Y	50Ω Complementary Output Driver	1

MACROCELL LIBRARY (Continued)

INTERNAL GATES

OR/NOR Family

Name	Function	Basic Cells
RO1	Inverting/Non-inverting Gate	1
RO2	2-input OR/NOR	1
RO3	3-input OR/NOR	1
RO4	4-input OR/NOR	1
RO5	5-input OR/NOR	1
RO6	6-input OR/NOR	1
RO8	8-input OR/NOR	2
R12	12-input OR/NOR	2
DNR2	Dual 2-input NOR	1
DOR2	Dual 2-input OR	1
DNR3	Dual 3-input NOR	1
DOR3	Dual 3-input OR	1
NR42	4-input NOR + 2-input NOR	1
OR42	4-input OR + 2-input OR	1
RO1T	Inverting/Non-inverting Gate with Twin Outputs	1
RO2T	2-input OR/NOR with Twin Outputs	1
RO3T	3-input OR/NOR with Twin Outputs	1
RO4T	4-input OR/NOR with Twin Outputs	1
RO8T	8-input OR/NOR with Twin Outputs	2
DNR2T	Dual 2-input NOR with Twin Outputs	1
DOR2T	Dual 2-input OR with Twin Outputs	1
DNR3T	Dual 3-input NOR with Twin Outputs	1
DOR3T	Dual 3-input OR with Twin Outputs	1

OR-AND/NAND Family

Name	Function	Basic Cells
RA22	2-2 OR-AND/NAND	1
RA32	3-3 OR-AND/NAND	2
RA42	4-4 OR-AND/NAND	2
RA23	2-2-2 OR-AND/NAND	2
RA33	3-3-3 OR-AND/NAND	2
RA83	4-4-3 OR-AND/NAND	2
RAA3	5-3-2 OR-AND/NAND	2
RA24	2-2-2-2 OR-AND/NAND	4
RA34	3-3-3-3 OR-AND/NAND	4
RA44	4-4-4-4 OR-AND/NAND	4
RAD4	4-3-3-3 OR-AND/NAND	4
RAE4	5-4-3-2 OR-AND/NAND	4

MACROCELL LIBRARY (Continued)

INTERNAL GATES

OR-AND/NAND Family (Continued)

Name	Function	Basic Cells
RA45	4-4-4-4-4 OR-AND/NAND	4
RAF5	5-4-3-2-1 OR-AND/NAND	4
RA48	4-4-4-4-4-4-4-4 OR-AND/NAND	6
RA22T	2-2 OR-AND/NAND with Twin Outputs	1
RA32T	3-3 OR-AND/NAND with Twin Outputs	2
RA34T	3-3-3-3 OR-AND/NAND with Twin Outputs	4
RAD4T	4-3-3-3 OR-AND/NAND with Twin Outputs	4
RAE4T	5-4-3-2 OR-AND/NAND with Twin Outputs	4

Exclusive OR Family

Name	Function	Basic Cells
ER2	2-input EOR/ENOR	1
EOR3	3-input EOR	2
ENR3	3-input ENOR	2
EOR4	4-input EOR	2
ENR4	4-input ENOR	2
ER21	2-1 AND-EOR/ENOR (NOR)	1
ER22	2-2 OR-EOR/ENOR (NOR)	1
EOR4T	4-input EOR with Twin Outputs	2
ENR4T	4-input ENOR with Twin Outputs	2
ER21T	2-1 AND-EOR/ENOR with Twin Outputs	1
ER22T	2-2 OR-EOR/ENOR with Twin Outputs	1

Multiplexer Family

Name	Function	Basic Cells
M21	2-to-1 Multiplexer	1
M21E	2-to-1 Multiplexer with Enable (Low)	1
M21G	2-to-1 Multiplexer with Gated Inputs	1
M21D	Dual 2-to-1 Multiplexer with Com Select	2
M21Q	Quad 2-to-1 Multiplexer	4
M41	4-to-1 Multiplexer	4
M41B	4-to-1 Multiplexer with Enable (Low)	4
M41A	4-to-1 Multiplexer with Enable (High)	4
M21GT	2-to-1 Multiplexer with Gated Inputs	1
M21ET	2-to-1 Multiplexer with Enable (Low)	1
M21QT	Quad 2-to-1 Multiplexer with Twin Outputs	4
M41BT	4-to-1 Multiplexer with Enable (Low)	4

MACROCELL LIBRARY (Continued)

INTERNAL GATES

Decoder Family

Name	Function	Basic Cells
D14A	1-to-4 Decoder (High) with Enable (High)	4
D14B	1-to-4 Decoder (High) with Enable (Low)	4
D14D	1-to-4 Decoder (Low) with Enable (Low)	2
D14C	1-to-4 Decoder (Low) with Enable (High)	2
D18B	1-to-4 Decoder (High) with Enable (Low)	8

Adder Family

Name	Function	Basic Cells
ADH2	Half Adder with Gated Inputs	1
ADF2	Full Adder with Gated Inputs	2
ADF	Full Adder	2
AD2C	2-bit Look-Ahead-Carry	4
AD3S	3-bit Adder (Sum)	2
AD3C	3-bit Adder (Carry)	2
ADFT	Full Adder	2
ADH2T	Full Adder with Gated Inputs	1

Latch/Flip-Flop Fmily

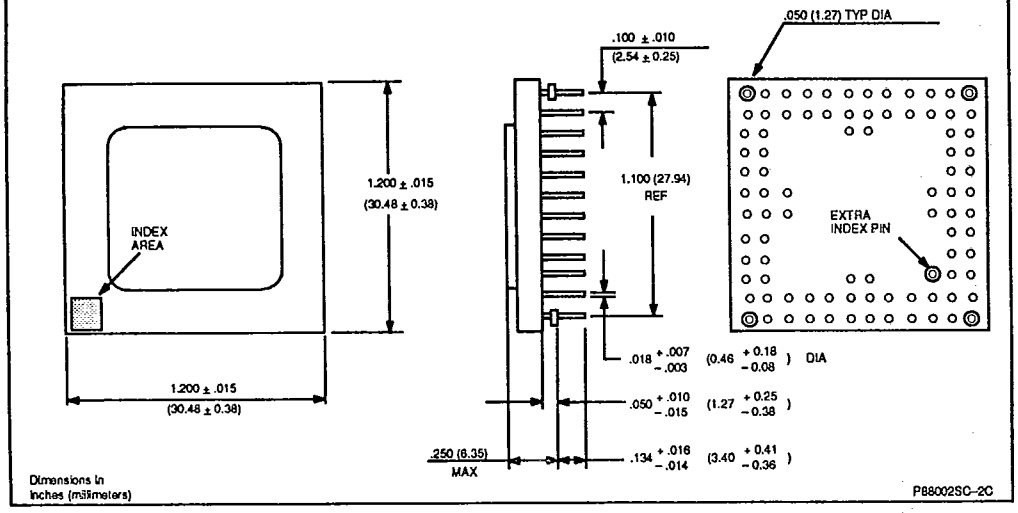
Name	Function	Basic Cells
LD1	D Latch with Reset	1
LD1B	D Latch with Clock Enable (Low)	1
LD1A	D Latch with Clock Enable (High)	1
LD2	D Latch with Multiplexer	2
LD1D	Dual D Latch with Reset	2
FD1	D Flip-Flop with Reset	2
FD2	D Flip-Flop with Multiplexer	4
FD4	D Flip-Flop with Reset	2
FD1D	Dual D Latch with Reset	4
FD3A	Scan D Flip-Flop	4
FD1A	D Flip-Flop with Reset	2

Differential Receiver Family

Name	Function	Basic Cells
DRM1	2-to-1 Multiplexer with Differential Inputs	1
DRM2	2-to-1 Multiplexer with Differential Inputs and Differential Multiplexer Control	1
DRF1	D Flip-Flop with Differential Clock and Data	1

PACKAGE DIMENSIONS

88–LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE



149–LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE WITH 6-FIN HEATSINK