Inductive Cell Balancer IC with Balancing Current Up to 2A

DESCRIPTION

ETA3003 is an inductive cell balancer. Unlike conventional passive balancing technique, ETA3003 utilizes a control scheme with an inductor to shuffle currents between two cells until the cells are balanced. Due to the switching nature, the heat and power dissipation generated in conventional linear balance technique are greatly reduced. The balance time is also significantly reduced due to higher balancing current not being limited by package thermal dissipation. ETA3003 consumes only 2μA ultra-low current from batteries in standby mode, extending the battery shelf time. The final balanced voltages of both cells are also highly accurate which enhances the performance and lifetime for the batteries connected in series. ETA3003 can also be used in multiple cells stacking with even number of cells. ETA3003 includes protection features similar to precondition in battery charging, that is when one cell's voltage is grossly lower than the other, the balancing current is reduced to a safe level until the lower voltage cell is charged up.

ETA3003 is available in ESOP-8 package.

FEATURES

- Inductive, switching control scheme
- Up to 90% charger transfer efficiency
- Accurate balanced voltages down to 30mV
- Auto detect unbalance and auto balance
- Low sleeping supply current, 2μA
- Programmable balancing current up to 2A
- Precondition balancing current
- Battery over voltage protection
- Support small size inductor

APPLICATIONS

- Multi-cells System
- Battery Pack
- Portable Equipment and Instrumentation
- Battery Backup Systems
- E-Cigarette

TYPICAL APPLICATION

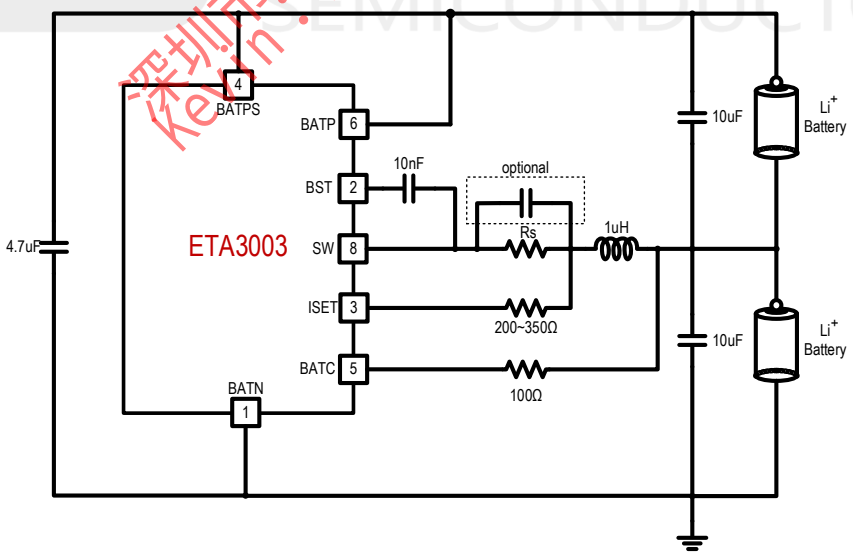


Figure 1: Typical Application Circuit

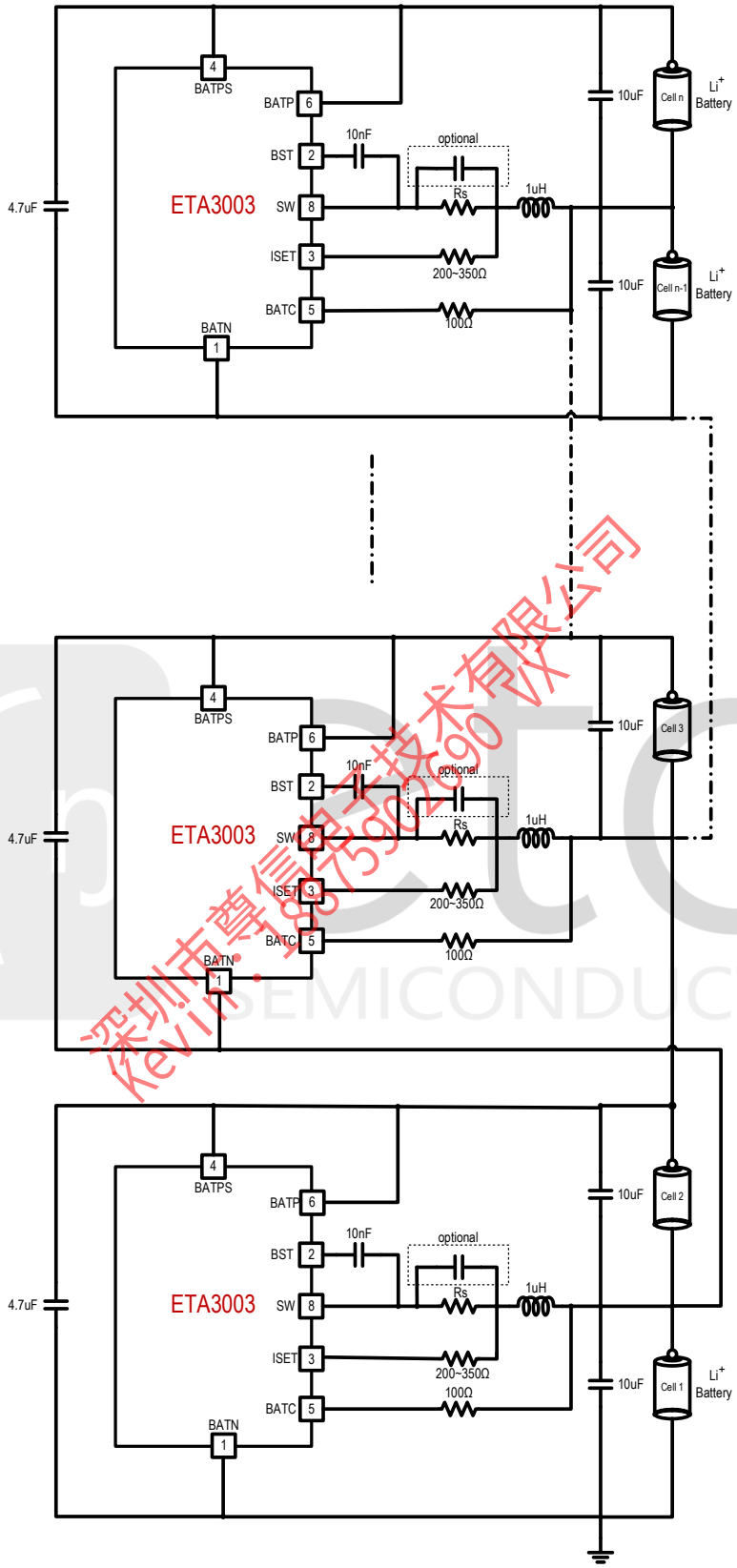
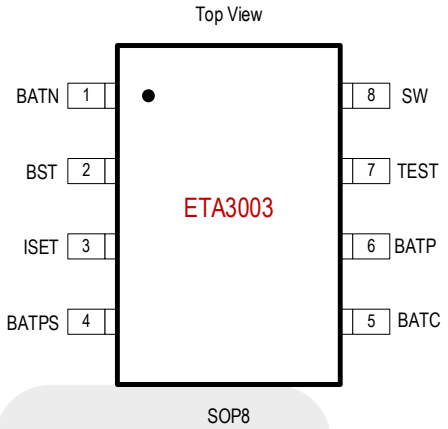


Figure 2: Multi-Cells Balancing Solution

ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA3003S8A	SOP8	ETA3003 YWWXL	4000

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

SW, ISET Voltage to BATN.....-0.3V to 12V
BST to SW Voltage.....-0.3V to 6V
BATC to BATN Voltage.....-0.3V to 6V
BATP to BATN Voltage.....-0.3V to 12V
SW, BATC, BATP to BATN current....Internally limited
Operating Temperature Range..... -40°C to 85°C
Storage Temperature Range.....-55°C to 150°C
Thermal Resistance θ_{JC} θ_{JA}
SOP8.....45.....90..... °C/W
Lead Temperature (Soldering, 10sec).....260°C
ESD CDM (Charged Device Mode).....1KV

ELECTRICAL CHARACTERISTICS

(T_A=25 °C, L = 1μH, C_{BOT}=C_{TOP}=10μF if not specified)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{SUPPLY}	Quiescent current	V_{BATP}=8V, V_{BATP}-V_{BATC}=V_{BATC}-V_{BATN}		2		μA
	Operating supply current	V_{BATP}=8V, in balancing mode, No Switching		900		μA
V_{BATP}	VBATP operating voltage				10	V
V_{BATC}	VBATC operating voltage				5	V
UVLO	Under lock-out voltage threshold	V_{BATP} Rising		3.75		V
UVLO_HYS	UVLD hysteresis			200		mV
DETECTION						
T_{SLEEP}	Detection interval timer	Part sleeps during T_{SLEEP}		2		S
T_{ALLOW}	Unbalance detection acknowledgment time	Unbalance status is accepted after T_{ALLOW} when enter CHECK state.		3.85		mS
T_{CHECK}	Maximum unbalance checking timer	IC get back to sleeping mode if don't detect unbalance after T_{CHECK}		7.68		mS

T_{DONE}	Finishing Timer	Maximum switching skip before enter sleep mode	62	mS
V_{KICK}	Unbalance detection threshold	Balancing only work if OVP>V_{BATP}>UVLO and V_{KICK} Detected between 2 cells	100	mV
V_{ERROR}	Balancing Accuracy	Error voltage between 2 cells after balancing finish	-70 70	mV
BALANCE CONTROLLER				
FREQ	Switching Frequency	PWM Clock	1	MHz
$I_{AVERAGE}$	Average Inductor current Regulation	R_S = 50mΩ	1	A
$I_{PRECOND}$	Precondition current Regulation	R_S = 50mΩ	100	mA
R_{DS_ON}	High side switch on Resistance	$I_{AVERAGE}$ =2A	40	mΩ
	Low side switch on Resistance	$I_{AVERAGE}$ =2A	40	mΩ
BATTERY PROTECTION				
TOP_OVP	Top Cell over voltage protection threshold	$V_{(BATP-BATC)}$ Rising	5	V
TOP_OVP_HYST	TOP_OVP hysteresis	$V_{(BATP-BATC)}$ Falling	350	mV
BOT_OVP	Bottom Cell over voltage protection threshold	$V_{(BATC-BATN)}$ Rising	5	V
BOT_OVP_HYST	BATC_OVP hysteresis	$V_{(BATC-BATN)}$ Falling	350	mV
TOP_PRECOND	Top battery precondition threshold	$V_{(BATP-BATC)}$ Rising	2.8	V
TOP_PREC_HYST	TOP_PRECOND hysteresis	$V_{(BATP-BATC)}$ Falling	150	mV
BOT_PRECOND	Bottom battery precondition threshold	$V_{(BATC-BATN)}$ Rising	2.8	V
BOT_PREC_HYST	BOT_PRECOND hysteresis	$V_{(BATC-BATN)}$ Falling	150	mV
BALANCE PROTECTION				
TOP_ILIM	Top cell drive current limit	DOWN direction: $V_{(BATP-BATC)}$> $V_{(BATC-BATN)}$	4.5	A
BOT_ILIM	Lower cell drive current limit	UP direction: $V_{(BATP-BATC)}$< $V_{(BATC-BATN)}$	4.5	A
THERMAL SHUTDOWN				
TSD	Thermal shutdown		160	°C
TSD_HYST	TSD Hysteresis		30	°C

PIN DESCRIPTION

PIN#	NAME	DESCRIPTION
1	BATN	Negative terminal sense voltage input and common Ground pin.
2	BST	Bootstrap pin. Connect a 10nF capacitor from BST to SW.
3	ISET	Balancing current setting pin. Connect a resistor from SW to an inductor to program the balancing current. Under an extremely high noise environment, a 1nF capacitor between ISET pin and SW pin can improve the ISET voltage stability, so a capacitor position reservation here is recommended.
4	BATPS	Sense voltage input for top cell.
5	BATC	Sense voltage input for bottom cell. Connect a 10μF capacitor between BATC and BATN.
6	BATP	Power input from top cell. Connect a 10μF capacitor between BATP and BATC.
7	TEST	Factory Use Only. Float this Pin.
8	SW	Switching node. Connected to an inductor.

FUNCTIONAL BLOCK DIAGRAM

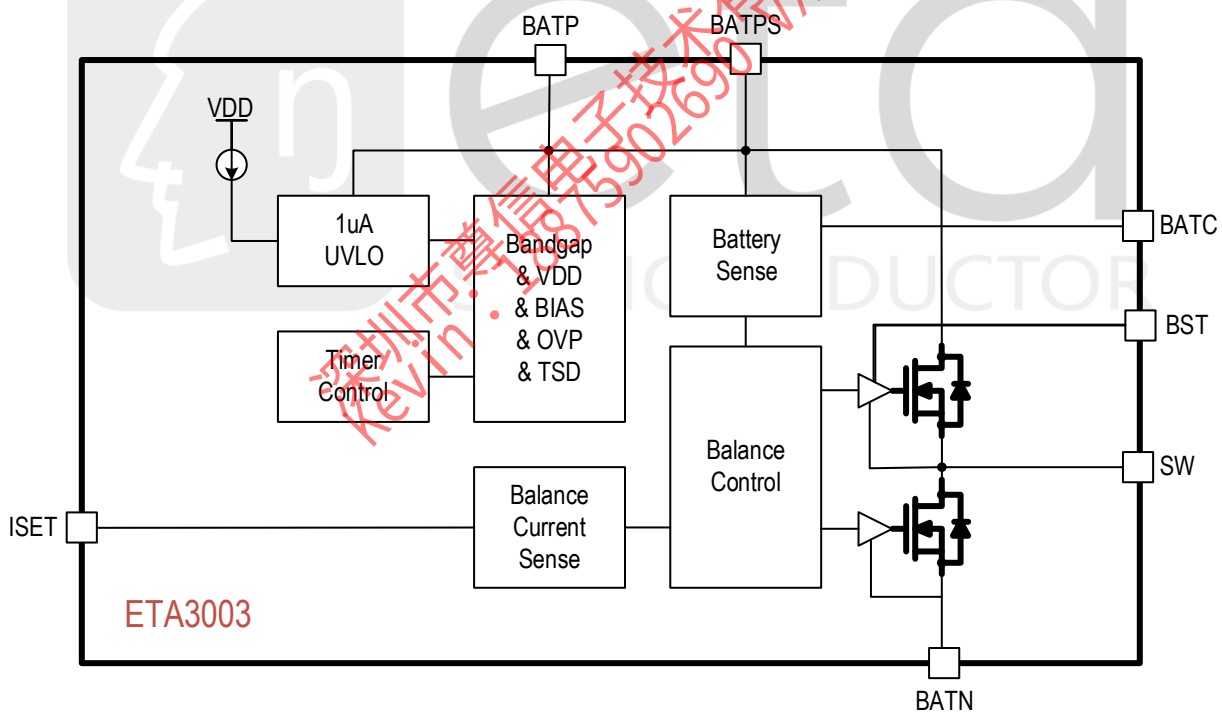
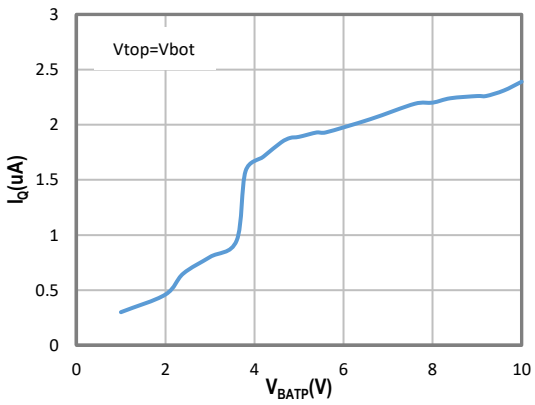


Figure 3: Functional Block Diagram

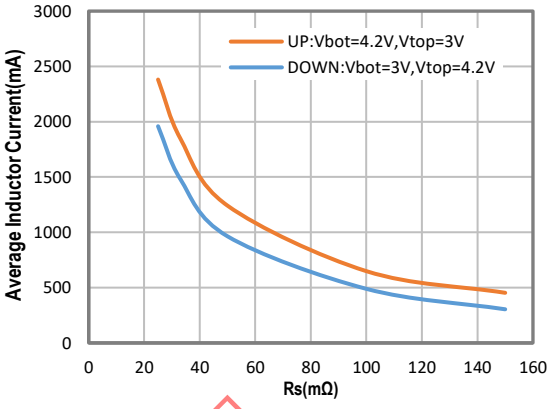
TYPICAL PERFORMANCE CHARACTERISTICS

(TA=25°C, unless otherwise specified)

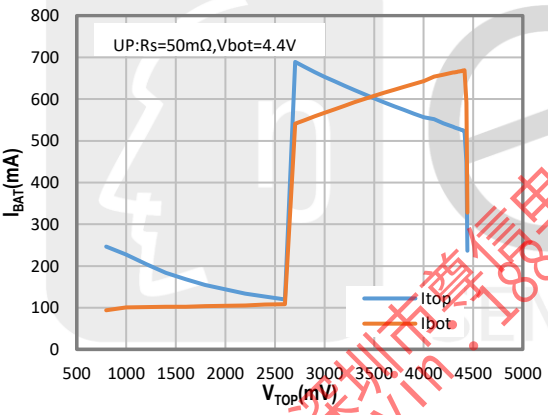
I_Q Vs. V_{BATP}



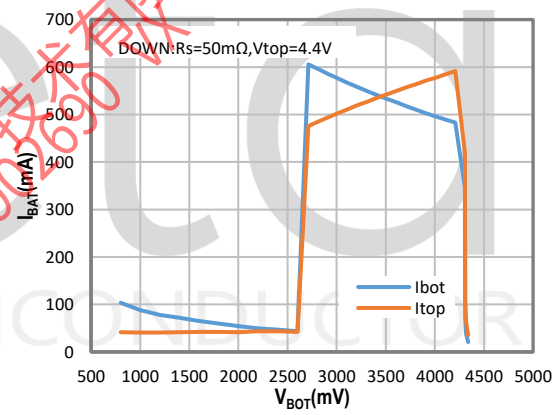
Average Inductor Current Vs. Rs



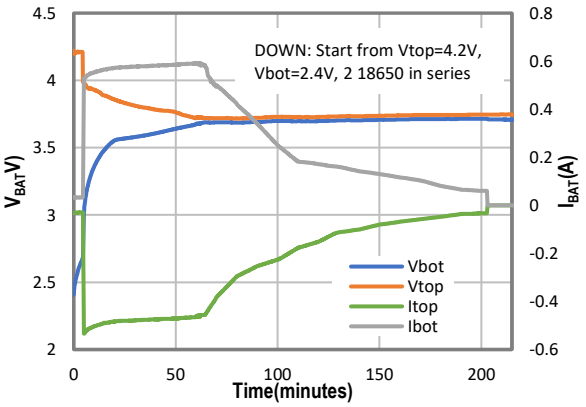
I_{BAT} Vs. V_{TOP}



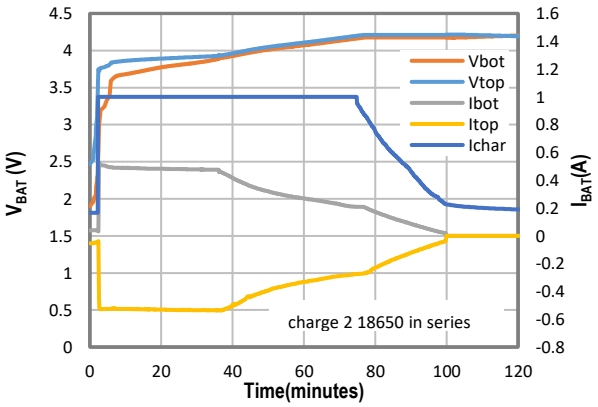
I_{BAT} Vs. V_{BOT}



Balancing Without Charger



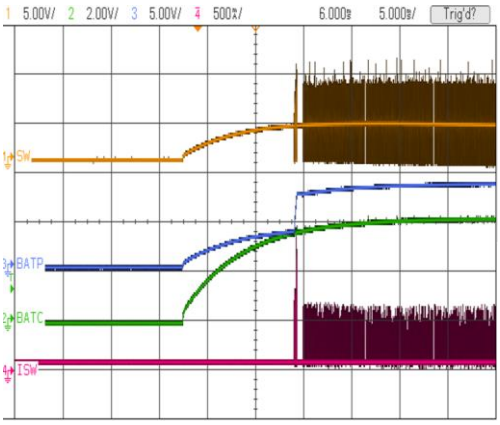
Balancing in Charging



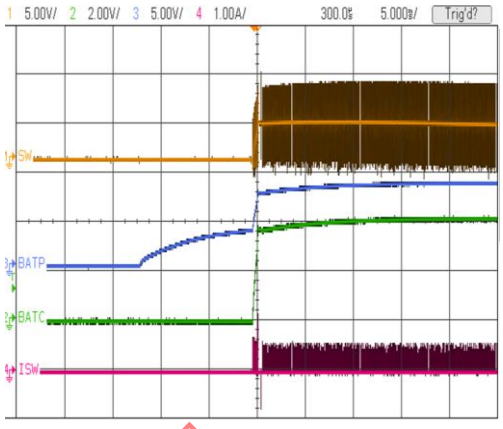
TYPICAL PERFORMANCE CHARACTERISTICS Cont'd

(TA=25°C, unless otherwise specified)

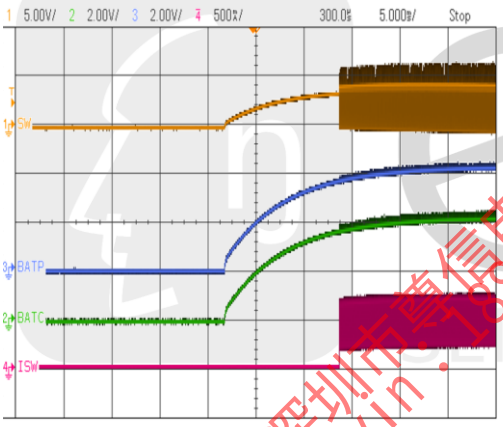
V_{BOT} plug-in Start-Up, V_{TOP} = Floating, R_S = 50mΩ, V_{BOT} = 4.3V



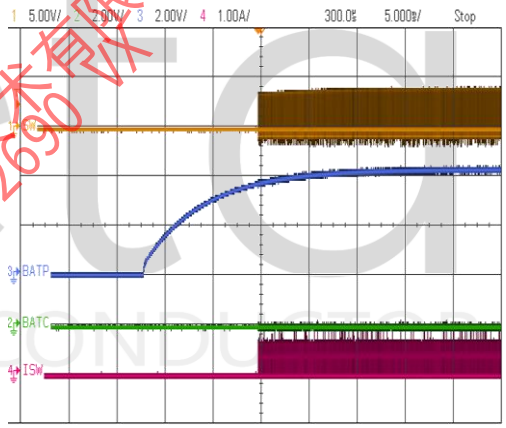
V_{TOP} plug-in Start-Up, V_{BOT} = Floating, R_S = 50mΩ, V_{TOP} = 4.3V



V_{BOT} plug-in Start-Up , V_{TOP} = Shorted , R_S = 50mΩ, V_{BOT} = 4.3V

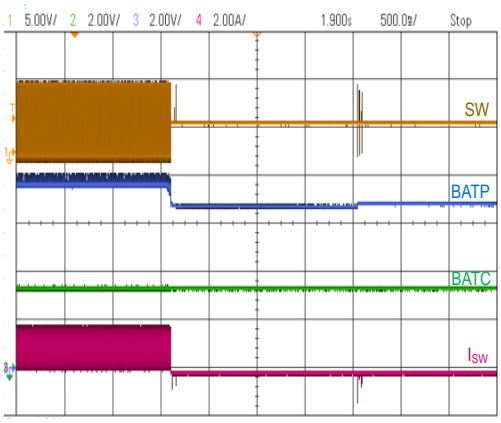


V_{TOP} plug-in Start-Up , V_{BOT} = Shorted , R_S = 50mΩ, V_{TOP} = 4.3V



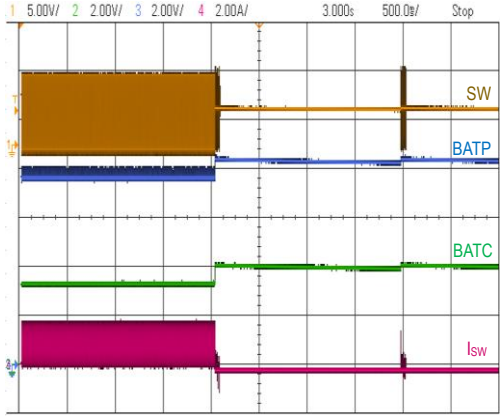
V_{TOP} plug-out, DOWN Condition, R_S = 50mΩ,

V_{TOP} = 4.3V, V_{BOT} = 3.5V



V_{BOT} plug-out, DOWN Condition, R_S = 50mΩ,

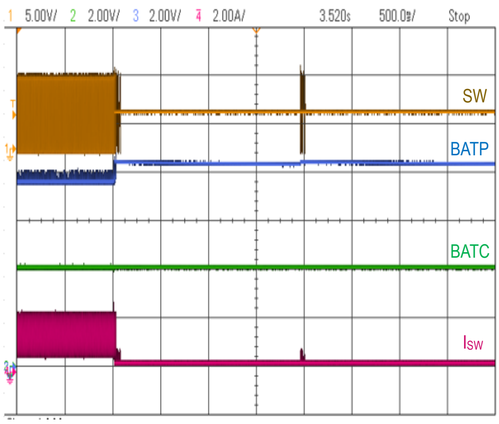
V_{TOP} = 4.3V, V_{BOT} = 3.5V



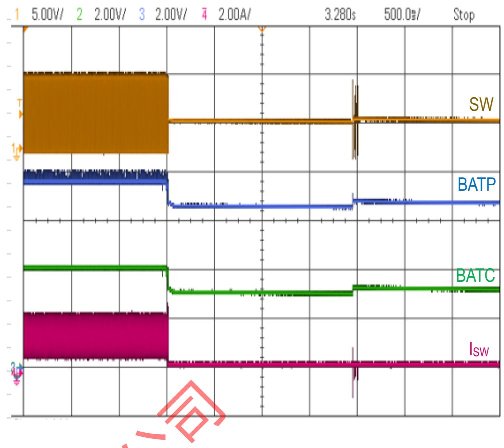
TYPICAL PERFORMANCE CHARACTERISTICS Cont'd

(TA=25°C, unless otherwise specified)

V_{TOP} plug-out, UP Condition, R_S = 50mΩ, V_{BOT} = 4.3V, V_{TOP} = 3.5V



V_{BOT} plug-out, UP Condition, R_S = 50mΩ, V_{BOT} = 4.3V, V_{TOP} = 3.5V



FEATURE DESCRIPTION

The ETA3003 is a battery cell balancer with lossless inductive architecture based on ETA's proprietary technology. The technology is developed by ETA Solutions and any copy without ETA's agreement will be forbidden.

During operation, ETA3003 detects the difference between 2 cells then start balancing if the difference exceeds V_{KICK}. Once detected V_{KICK}, ETA3003 will discharge the higher voltage cell, store that discharging energy in the inductor then charge that energy to the lower voltage cell. ETA3003 keeps balancing until there is no difference between 2 cells.

ETA3003 technology allows balancing in either charge or discharge phases of the battery with minimized loss. Without unbalanced condition, ETA3003 operates in sleep mode with low supply current. This is an advantage to extend battery pack life time.

STATE MACHINE

The ETA3003 provides a completed state machine that controls whole operation intelligently. With this state machine, ETA3003 is equipped with self-protection from any accident during balancing. It also keeps the part stay asleep as much as possible until unbalance detected.

ETA3003 always starts from CHECK state when battery is plugged in.

Any fault always forces ETA3003 back to SLEEP State where ETA3003 burns only 2μA (typically) from BATP.

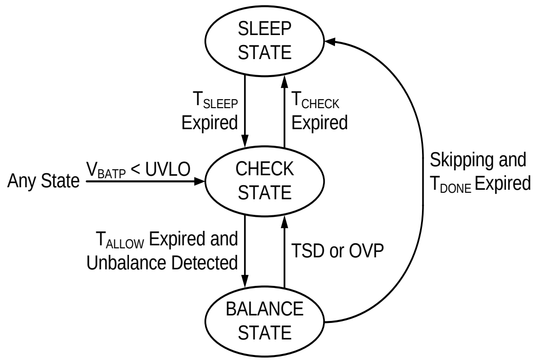


Figure 4: State Machine Diagram

The ETA3003 timing diagram for state machine is shown in following figure.

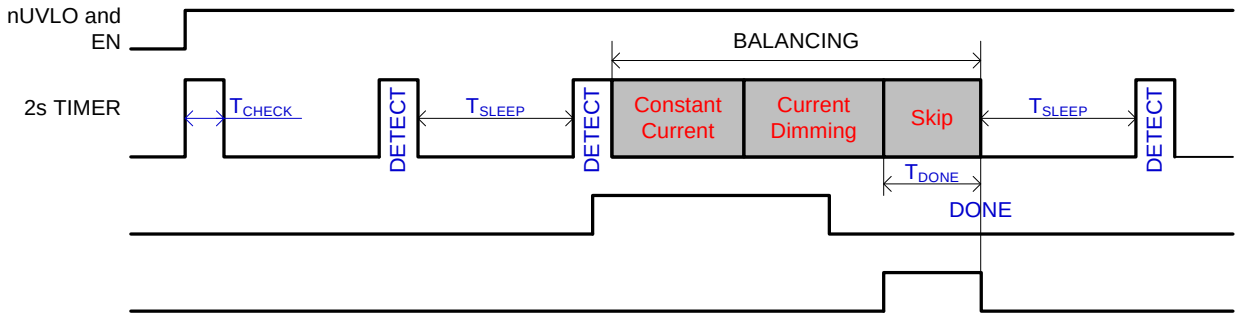


Figure 5: Timing Profile

UNBALANCE DETECTION

When state is in CHECK State, ETA3003 detects V_{KICK} difference between 2 cells to enter BALANCE State. If the top cell voltage is higher, balancing will be "DOWN", meaning discharge the top cell to charge to bottom cell. And if the bottom cell voltage is higher, balancing will be "UP", meaning discharge the bottom cell to charge to top cell.

BALANCING PROFILE

ETA3003 balancing always starts with "Constant Current Regulation" phase since it is always with high voltage difference. Constant current is set by R_{ISET}.

When the detected difference at IC pin is almost zero, but due to battery equivalent series resistance, real difference is not zero, then current is not immediately zero but reduced slowly depend on battery capacitance. This condition is called "Current Dimming" phase.

When two cell voltages are equal, balancing current becomes almost zero, when this persists for a time period of T_{DONE}, the balancing finishes one cycle, and ETA3003 goes back to SLEEP State.

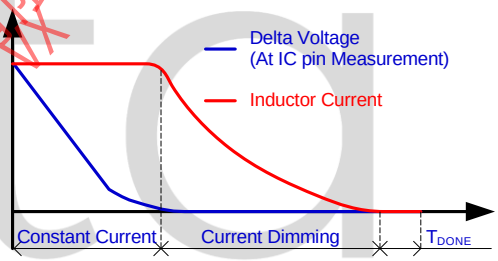


Figure 6: Balancing Profile

PROTECTION

ETA3003 provides full protection to batteries that extend the life time of the batteries:

- Short and Low Voltage Protection: When either of the cell voltage below $V_{PRECOND}$, maximum balancing current will be re-defined to 10% of the level set by ISET pin resistor.
- Open and Over Voltage Protection: When either of the cell voltage is greater than V_{OVP}, ETA3003 will stop balancing, and go back to SLEEPING. Part will wake up after T_{SLEEP}.
- Thermal Shutdown: When part gets hotter than 160°C, ETA3003 will stop balancing, and go back to SLEEPING. Part will wake up after T_{SLEEP}.
- Current Limit Protection: Maximum of the peak of inductor current is allowed to 5.5A.

APPLICATION INFORMATION

BALANCING CURRENT SETTING

Balancing current is defined as the average inductance current. Average inductance current is regulated following ISET resistor configuration.

AVERAGE INDUCTION CURRENT	RECOMMENDED COMPONENT			
	ISET RESSITOR	ISET CAPACITOR	INDUCTOR	BATTERY CAPACITOR
500mA	100mΩ	0pF – 10nF	0.47-1μH	4.7μF – 10μF
625mA	80mΩ	0pF – 10nF	0.68-1μH	4.7μF – 10μF
800mA	62.5mΩ	0pF – 10nF	0.68-1μH	4.7μF – 10μF
1000mA	50mΩ	0pF – 10nF	0.68-1μH	4.7μF – 10μF
1250mA	40mΩ	0pF – 10nF	0.68-1μH	10μF
1515mA	33mΩ	0pF – 10nF	0.68-1μH	10μF
1667mA	30mΩ	0pF – 10nF	1μH	10μF
2000mA	25mΩ	0pF – 10nF	1-2μH	10μF

RESTRICTED CONDITIONS

ETA3003 does not allow following restricted conditions:

- Short SW to ISET
- Exceed the absolute maximum rating of each IC pin

MULTI-CELLS BALANCING SOLUTION

It is also possible to use several ETA3003 ICs in application to balance multi-cell series battery, such as shown in the Figure 2 (n cells).

Each ETA3003 manages balancing of 2 neighbor cells. Each ETA3003 operates independently.

PCB DESIGN GUIDELINE

In an UP case that bottom cell voltage is greater than top cell voltage, bottom cell becomes input and top cell becomes output of the switching regulation. In a DOWN case that top cell voltage is greater than bottom cell voltage, top cell becomes input and bottom cell becomes output. These mean parallel battery capacitors are always output capacitor or input capacitor for regulator. So please require to locate as close as possible to IC pins to minimize series resistance.

Please try to get the order of battery pins are BATP – BATC – BATN to make an easy battery connection.

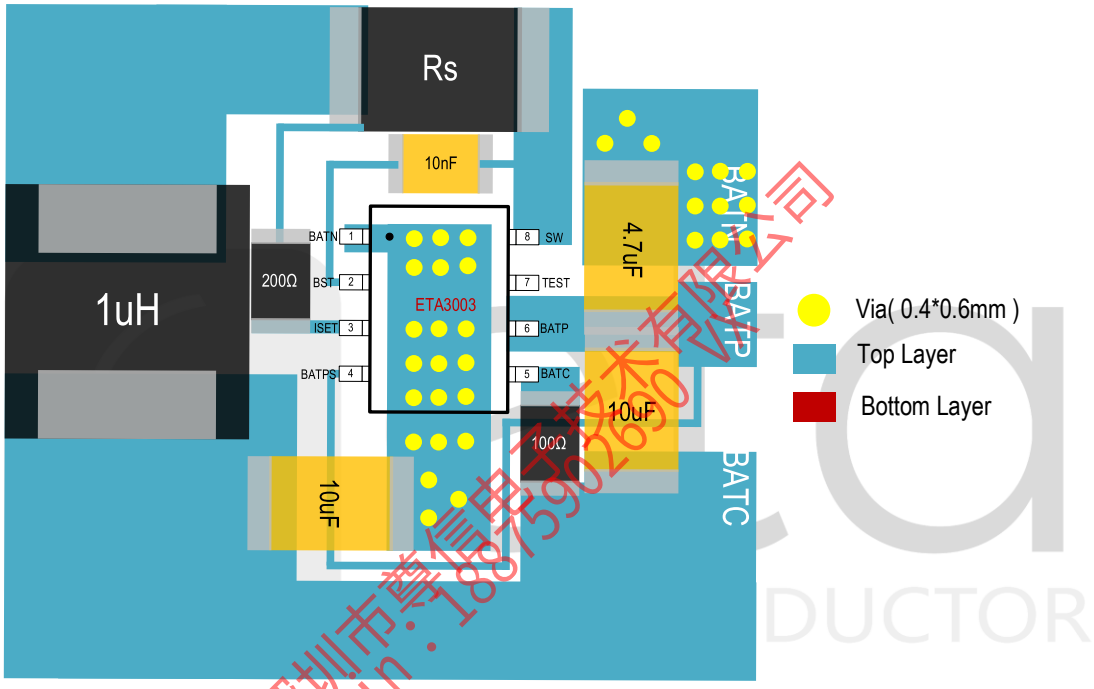
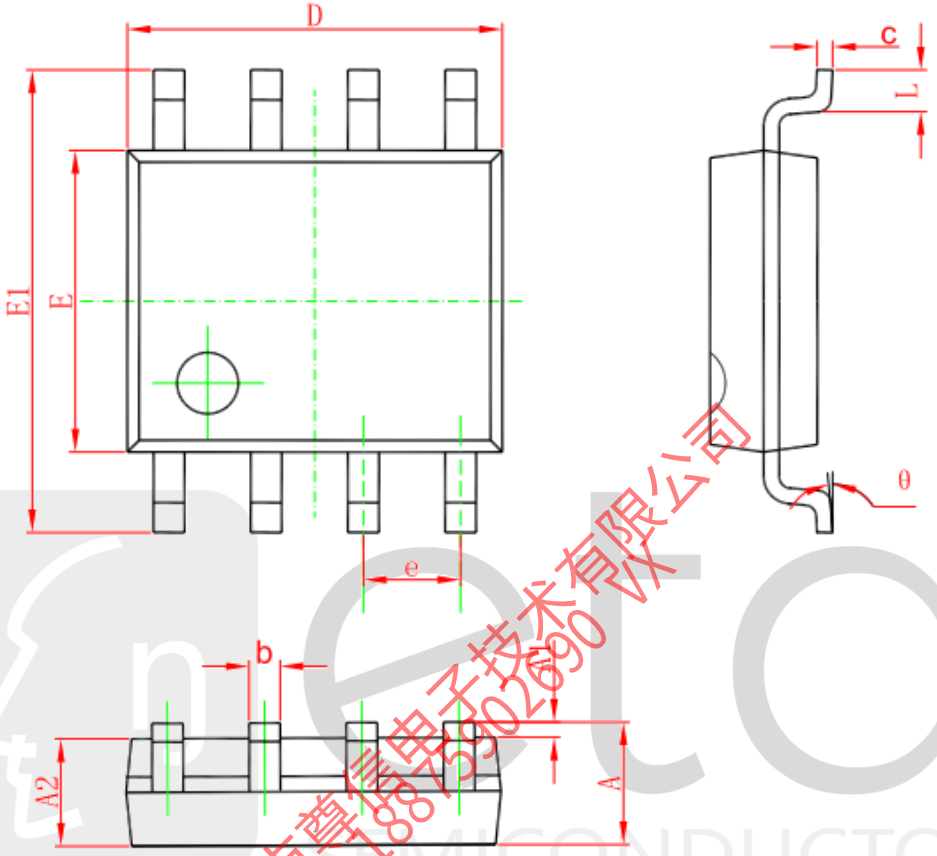


Figure 7: PCB Layout Guideline

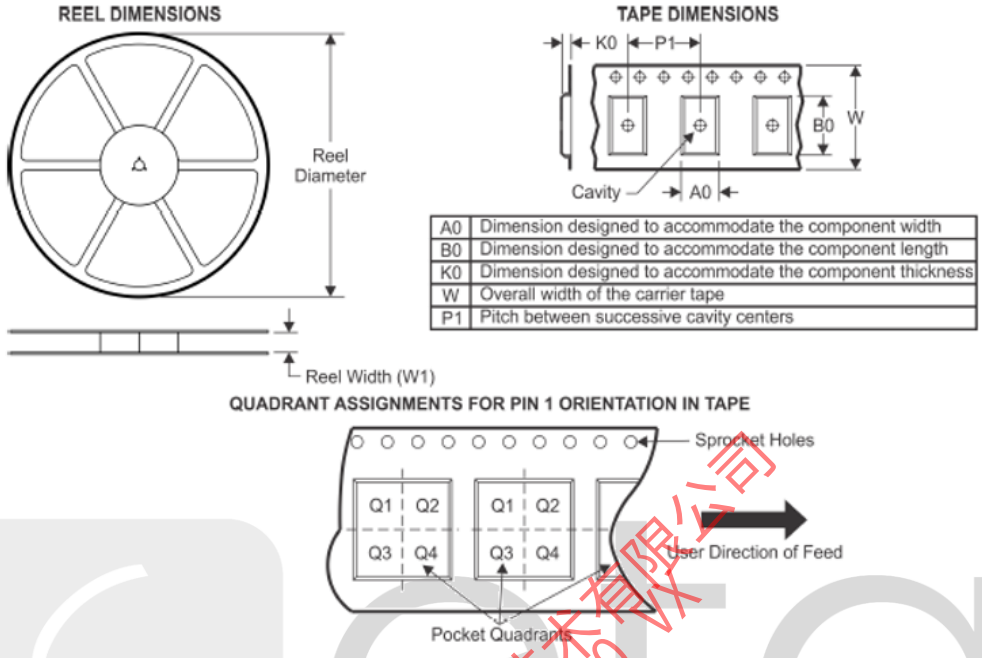
PACKAGE OUTLINE

Package: SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA3003S8A	SOP8	8	4000	330	12.7	6.6	5.4	2.05	8	12	Q1