5A, 2MHz I²C Controlled Output Synchronous Step-Down Converter

DESCRIPTION

The ETA3555 is a high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 5A of pulse load. It integrates an I²C interface that dynamically scales the output voltages on demand. The DCDC control block belongs to a new breed of high frequency synchronous Step-Down converter that combines the advantages of voltage mode control and Constant-On-Time control. Its adaptive Constant-On-Time control dynamically changes switch on time to achieve a constant switching frequency. It does not have the minimum on-time constrain normally a fixed-frequency current mode Step-down requires, allowing it to go down to very low duty ratio without affecting loop stability. The voltage mode nature also provides a more superior load transient response and a seamless transition from PFM to PWM modes. Cycle-by-cycle current limit provides output short-circuit protection and an input OVP function guards ETA3555 against possible input voltage surge. ETA3555 is housed in a 2mm x 1.6mm CSP-20 Package.

FEATURES

- I²C Dynamic Output Control
- Synchronous High Efficiency up to 95%
- Fast load transient response
- Capable of Delivering 5A
- Input OVP at 6.2V
- No External Schottky Diode Needed
- Thermal shutdown and UVLO
- CSP-20 (4x5) package

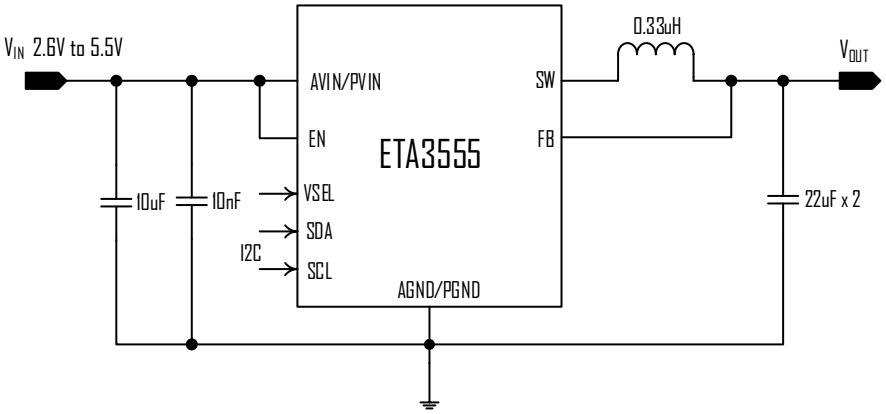
APPLICATIONS

- ARM based CPUs
- Smart Phone
- Tablet, MID
- Smart Set-Top Box, OTT

ORDERING INFORMATION

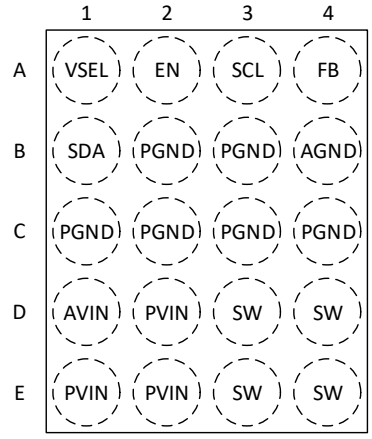
PART	PACKAGE PIN	TOP MARK
ETA3555CSU	CSP-20 (4x5)	3555 YWWL (Date Code)

TYPICAL APPLICATION



Typical Application Circuit

PIN CONFIGURATION



Top View

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VIN Voltage .....–0.3V to 6.0V
All Other Pin Voltage .....VIN–0.3V to VIN+0.3
SW to ground current.....Internally limited
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–55°C to 150°C
Thermal Resistance θ_{JA}
CSP-20.....35 ..... °C/W

ELECTRICAL CHACRACTERISTICS

(V_{IN} = 3.6V, unless otherwise specified. Typical values are at TA = 25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		2.5		5.5	V
Input UVLO	Rising, Hysteresis=250mV		2.35		V
Input OVP	Rising, Hysteresis=200mV		6.15		V
Input Supply Current	I_{OUT}=0, PFM Mode, Device Not Switching		55		μA
Input Shutdown Current	EN=GND		0.1	10	μA
Thermal Shutdown	Rising, Hysteresis =20°C		155		°C
DC/DC converter					
Default Output Voltage	VSEL=0, default bit	1.0	1.02	1.04	V
	VSEL=1, default bit	1.12	1.15	1.18	V
Load Regulation			0.5		%/A
Line Regulation	V_{IN} =3V to 4V		0.04		%/V
Switching Frequency			2		MHz
Maximum Duty Cycle			100		%
PMOS Switch On Resistance	I_{SW} =500mA		40		mΩ
NMOS Switch On Resistance	I_{SW} =500mA		15		mΩ
High Side PMOS Switch Current Limit	IPEAK Bit = 00		4		A
	IPEAK Bit = 01		6.5		A
	IPEAK Bit = 10		8		A
	IPEAK Bit = 11		10		A
Maximum Output Current Limit	IPEAK Bit = 01		6		A
Short Circuit Hiccup mode off time	EN=5V		20		ms

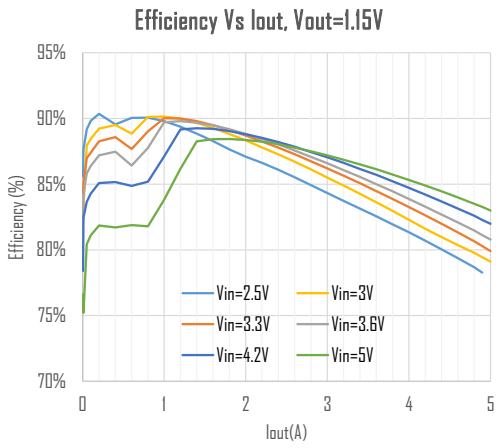
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Discharge Pull-down			1000		Ω
EN, VSEL					
Input Low Voltage				0.4	V
Input High Voltage		1.2			V
Input Current				1	μA
I²C Control					
SCL Clock Frequency			400		KHz
SDA Setup Time			100		ns
SDA hold time			50		ns
Input Low Voltage				0.4	V
Input High Voltage		1.2			V

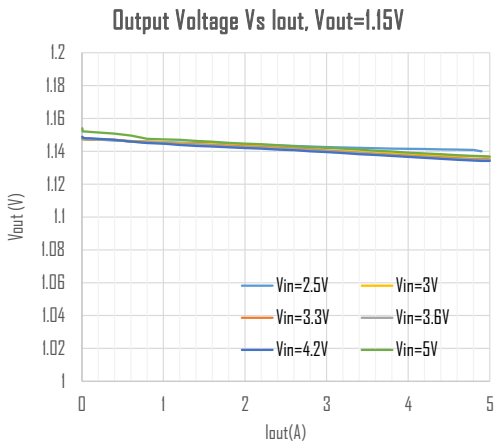
PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
A1	VSEL	Output voltage and mode selection pin
A2	EN	Chip enable control pin, pull high to turn the chip on
A3	SCL	Clock pin for I²C interface
A4	FB	Feedback Input pin, connect to the output capacitor thru a trace.
B1	SDA	Data IO pin for I²C interface
B2, B3, C1, C2, C3, C4	PGND	Power ground for large switching current
B4	AGND	Analog ground, for internal control circuit
D1	AVIN	Analog supply for internal control circuit
D2, E1, E2	PVIN	Power supply for large switching current
D3, D4, E3, E4	SW	Switching node, to connect a 0.33-0.47uH inductor

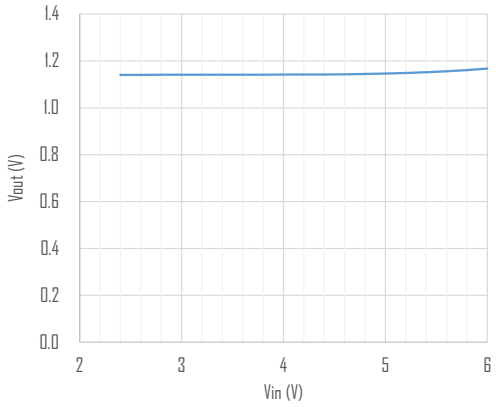
TYPICAL CHARACTERISTICS

(Typical values are at T_A = 25°C unless otherwise specified.)

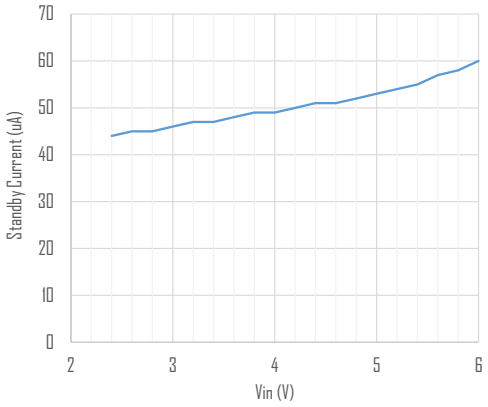




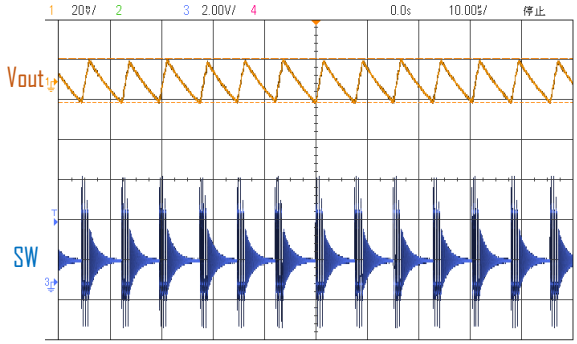
Vout Vs Vin, Iout=0.1A



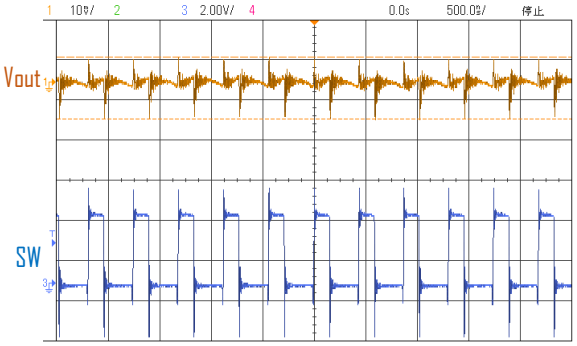
Vin Stanby Current at Iout=0A



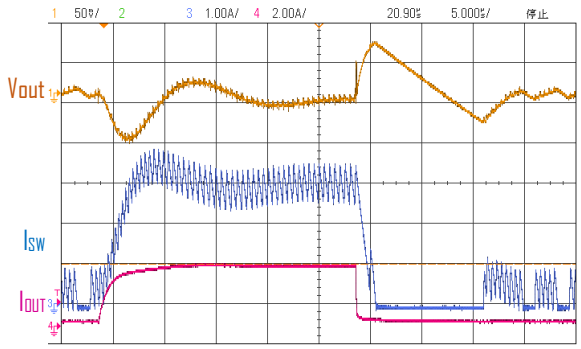
Switching Waveform: V_{IN}=3.6V, Vout=1.15V, I_{OUT}=100mA



Switching Waveform: V_{IN}=3.6V, Vout=1.15V, I_{OUT}= 3A



Load Transient Respond: Vin=3.6V, Vout=1.15V, I_{OUT}=0.3 – 3A



FUNCTIONAL DECRIPTIONS

The ETA3555 is a high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 5A of pulse load. It integrates an I^2C interface that dynamically scales the output voltages on demand. The I^2C interface can also program the ramp rate output voltage changes and enable or disable the regulator.

DCDC Control scheme

ETA3555 uses an adaptive Constant-On-Time control scheme that the ON time is dynamically adjusted according to VIN and VOUT so to achieve a nearly constant switching frequency. This control scheme provides simpler compensation and superior transient response

over traditional constant frequency current mode control, while still maintaining the advantage of switching at a constant frequency at about 2MHz. It also provides a seamless transition from PFM to PWM that normally a constant frequency current mode control scheme is hard to achieve. Further mode, because it is a COT control scheme, the system can achieve high step-down ratio at ease, because lower constrain on the minimum on- time requirement existing in constant frequency scheme.

Current Limit and Short-Circuit protection

ETA3555 employs a cycle-by-cycle peak current limit and it also has a hiccup mode that protects the circuit during dead-short condition. When the dead-short condition is removed, the IC goes back to normal operation.

Soft-start

ETA3555 has an internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the I soft-start circuitry slowly ramps up current available at SW.

UVLO and Thermal Shutdown

If IN drops below UVLO threshold, the UVLO circuit inhibits switching. Once IN rises above ULVO threshold, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J= +155°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

Register Description

ETA3555 DEVICE ADDRESS: C0

ETA3555 REGISTER TABLE

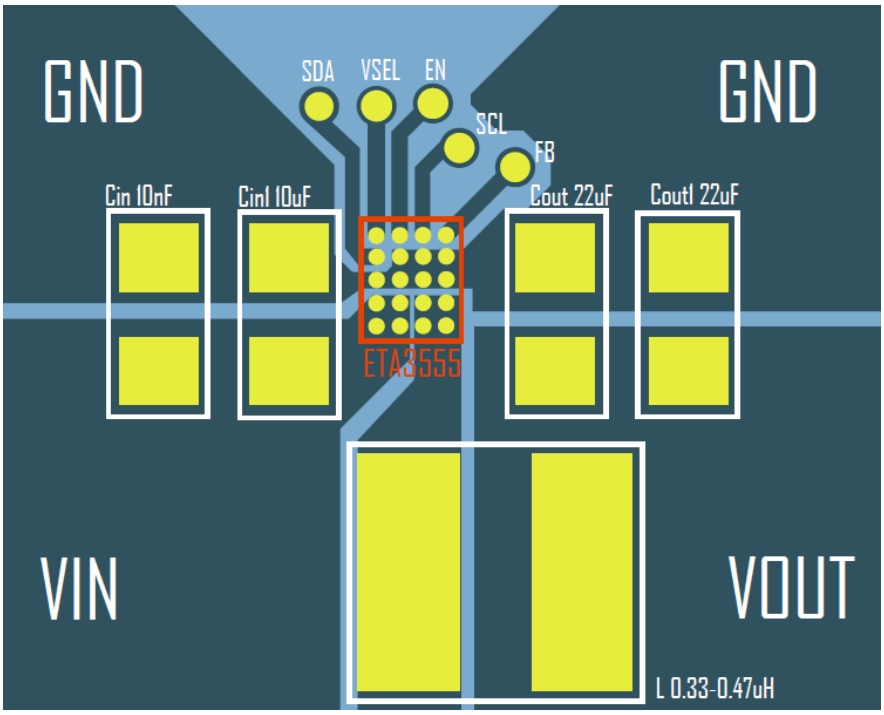
Address		B7	B6	B5	B4	B3	B2	B1	B0
00h	Name	BUCK_EN0	MODE0	VSEL0<5>	VSEL0<4>	VSEL0<3>	VSEL0<2>	VSEL0<1>	VSEL0<0>
	Default	1	0	1	0	1	0	1	0
	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
01h	Name	BUCK_EN1	MODE1	VSEL1<5>	VSEL1<4>	VSEL1<3>	VSEL1<2>	VSEL1<1>	VSEL1<0>
	Default	1	0	1	1	0	1	1	1
	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
02h	Name	Out_dis	SLEW<2>	SLEW<1>	SLEW<0>	DVSMODE	SWRST	IPEAK_1	IPEAK_0
	Default	0	0	0	0	0	0	0	1
	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
03h	Name	VENDOR<2>	VENDOR<1>	VENDOR<0>	PGOOD	DIE_ID<3>	DIE_ID<2>	DIE_ID<1>	DIE_ID<0>
	Default	1	0	0	1	1	0	0	0
	Access	R	R	R	R	R	R	R	R

Output Voltage Setting

Vout=0.6V+10mV*B<5:0>(Addr 00h/01h)

PCB GUIDELINE

A recommended PCB layout is shown below. The input capacitor has to be placed as close to the ETA3555 as possible.



PACKAGE OUTLINE

Package: CSP-20 (4x5)