80dB PSRR, Low Noise, RF, 300mA LDO in SOT23-6

DESCRIPTION

ETA5052 is a low-dropout (LDO) low-power linear voltage regulator features high power-supply rejection ratio (PSRR), ultralow-noise, fast start-up, and excellent line and load transient responses. Its PSRR can be as high as 80dB and its noise level can be as low as 30μVRMS of output voltage noise at 2.8V output with a 0.1μF bypass capacitor. Therefore, ETA5052 is an ideal power supply for noise-sensitive applications such as RF transmissions, cellphones, CMOS sensors and audios etc.

ETA5052's output voltage is adjustable through external feedback resistors and is housed in SOT23-6 package.

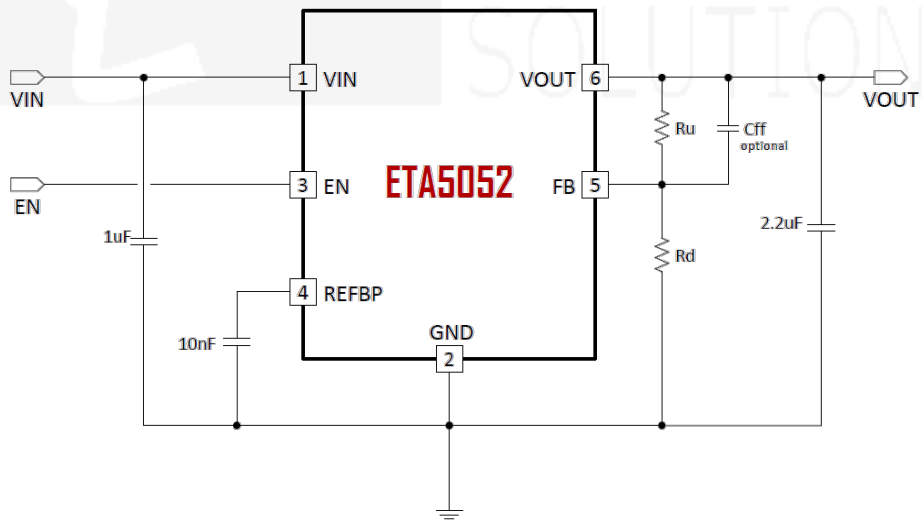
FEATURES

- High PSRR, 80 dB at 10Hz,70dB at 10Kz
- Low Noise, 30μVRMS
- Stable With a Wide Range of Ceramic Capacitor larger than 1μF
- Excellent Load and Line Transient Response
- Very Low Dropout Voltage
- 300mA output current

APPLICATIONS

- RF power
- Sensors
- Audio

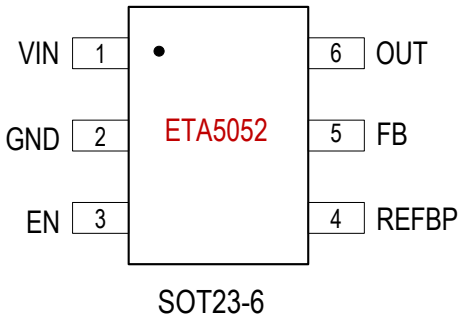
TYPICAL APPLICATION



ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA5052V0S2G	SOT23-6	DCYW	3000

PIN CONFIGURATION



SOT23-6

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VIN, EN, VOUT, FB, REFBP Voltage .....–0.3V to 6V
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–55°C to 150°C

Thermal Resistance	θ_{JA}	θ_{JC}	
SOT23-6	180	90	°C/W

Lead Temperature (Soldering 10sec) .....260°C
ESD HBM (Human Body Mode).....2KV
ESD CDM (Charged Device Mode).....1KV

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.8V, V_{OUT} = 2.8V, unless otherwise specified. Typical values are at TA = 25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range (1)		2.7		5.5	V
Under Input Voltage Lock Out	Rising, Hysteresis=100mV		2.6		V
Ground Current	0μA ≤ IOUT ≤ 200mA		170		μA
Shutdown Current	VEN = 0V, 2.7V ≤ VIN ≤ 5.5V			1	μA
Dropout Voltage (2)	IOUT = 200mA		135		mV
Continuous Output Current				300	mA
Output Current Limit	VOUT = 95%	350	600		mA
Output Foldback Current Limit	VOUT = 0V		300		mA
Line Regulation	VOUT + 1V ≤ VIN ≤ 5.5V			0.12	%/V
Load Regulation	0μA ≤ IOUT ≤ 200mA		0		mV
FB Feedback Voltage		1.178	1.200	1.222	V
FB Pin Current	VFB = 1.8V			1	μA
REFBP Voltage		1.188	1.200	1.212	V
Power Supply Rejection Ratio	Freq = 100Hz, IOUT = 10mA		80		dB
	Freq = 1KHz, IOUT = 100mA		80		
	Freq = 10kHz, IOUT = 100mA		70		
	Freq = 100kHz, IOUT = 100mA		60		
Output Noise Voltage			30		μVRMS
Start-up time,	Floating REFBP, Iout=0		95		μs
	C_{REFBP} = 4.7nF, Iout=0		105		
	C_{REFBP} = 10nF, Iout=0		110		
	C_{REFBP} = 33nF, Iout=0		128		
EN pin input Logic Low	2.7V ≤ VIN ≤ 5.5V			0.5	V
EN pin input Logic High	2.7V ≤ VIN ≤ 5.5V	1.2			V
Thermal Shutdown	Rising, Hysteresis =30°C		150		°C

(1): Minimum V_{IN} is 2.7 V or V_{OUT} + $V_{DROPOUT}$, whichever is greater.

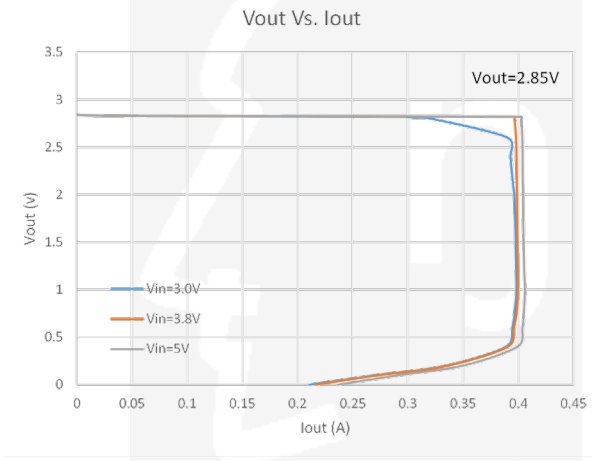
(2): Only measure for options of VOUT higher than 2.7V because minimum of VIN be 2.7V.

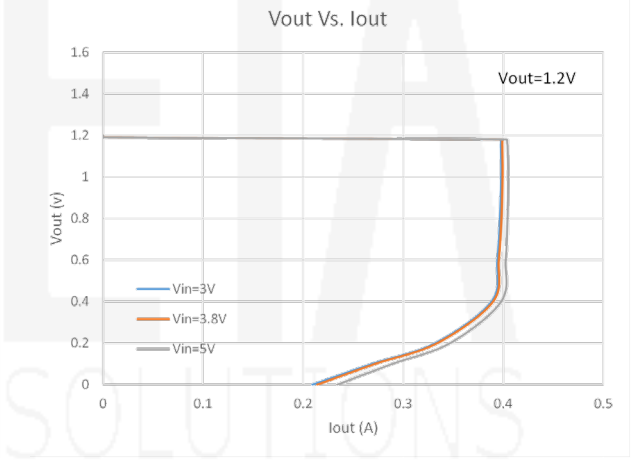
PIN DESCRIPTION

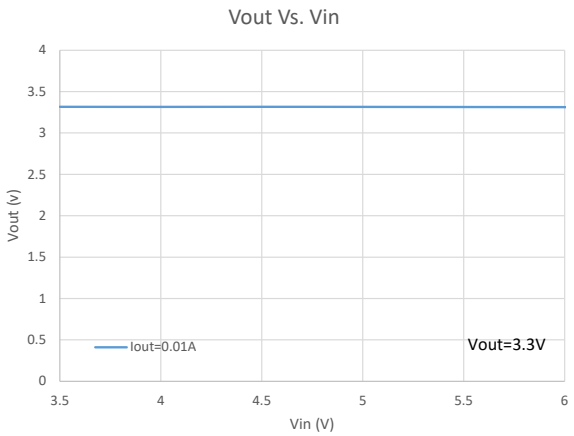
PIN #	NAME	DESCRIPTION
1	VIN	Input Supply Pin
2	GND	Ground Pin
3	EN	Enable Pin. Drive it high to enable IC, drive it low to disable. EN can be connected to IN if not used.
4	REFBP	Reference Voltage Bypass pin. Bypass this pin to GND by an external capacitor to improve PSRR performance at high frequency.
5	FB	Feedback pin for setting up output voltage.
6	VOUT	Output of regulator

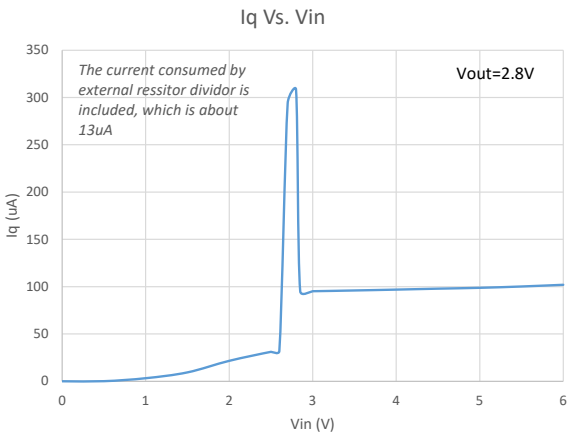
TYPICAL CHARACTERISTICS

(Typical values are at T_A = 25°C unless otherwise specified.)





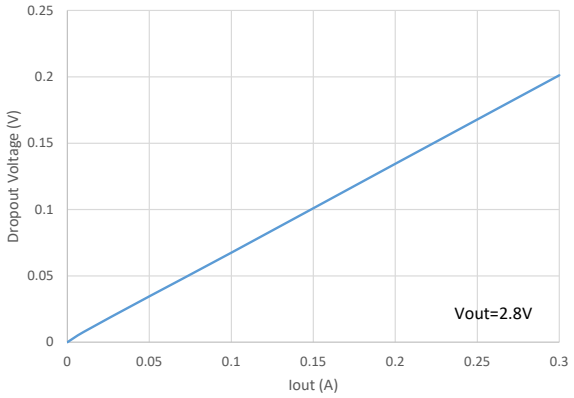




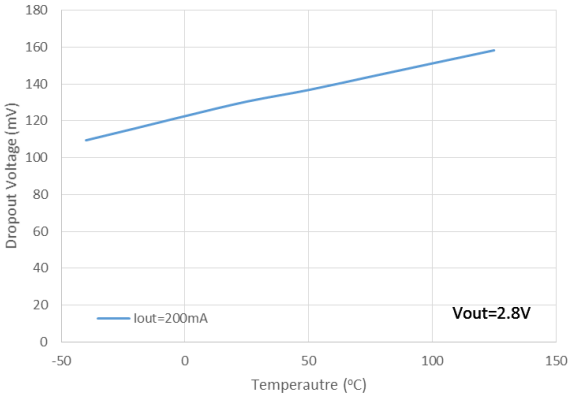
TYPICAL CHARACTERISTICS Cont'

(Typical values are at T_A = 25°C unless otherwise specified.)

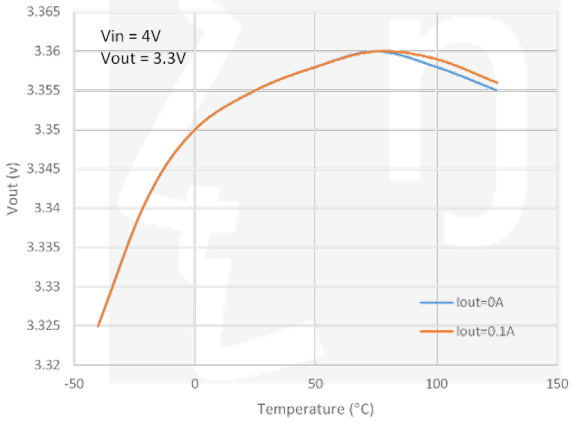
Dropout Voltage Vs. Iout



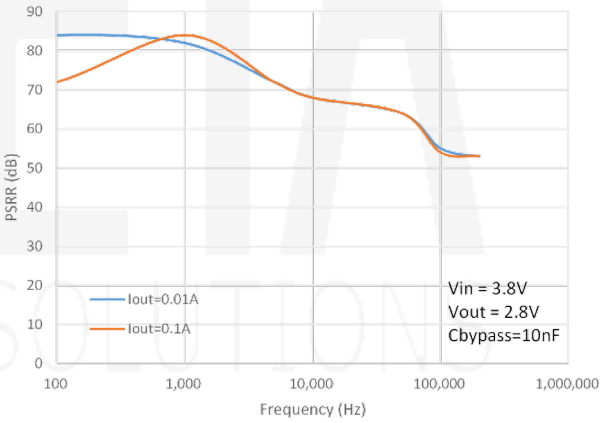
Dropout Voltage Vs. Temperature



Vout Vs. Temp

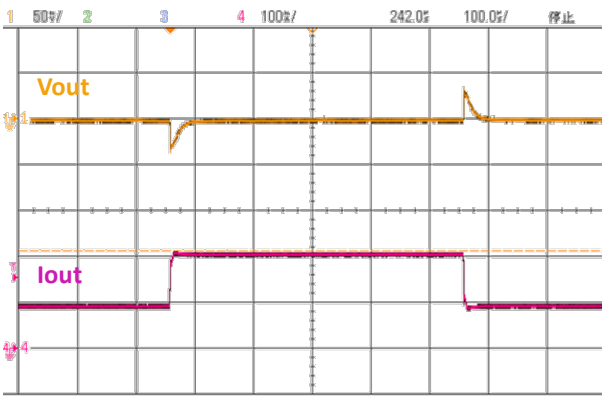


PSRR



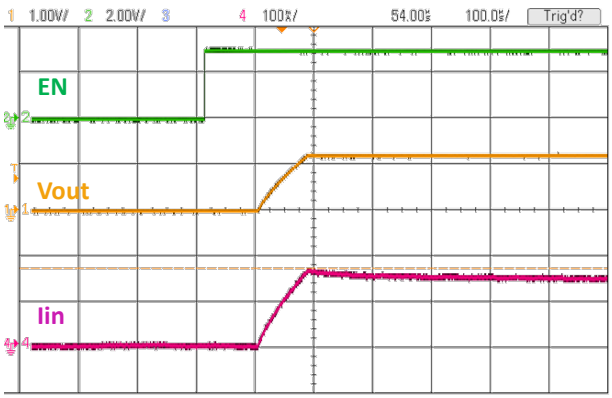
Load Transient Response

Vin=5V, Vout=3.3V, Iout=0.1-0.2A

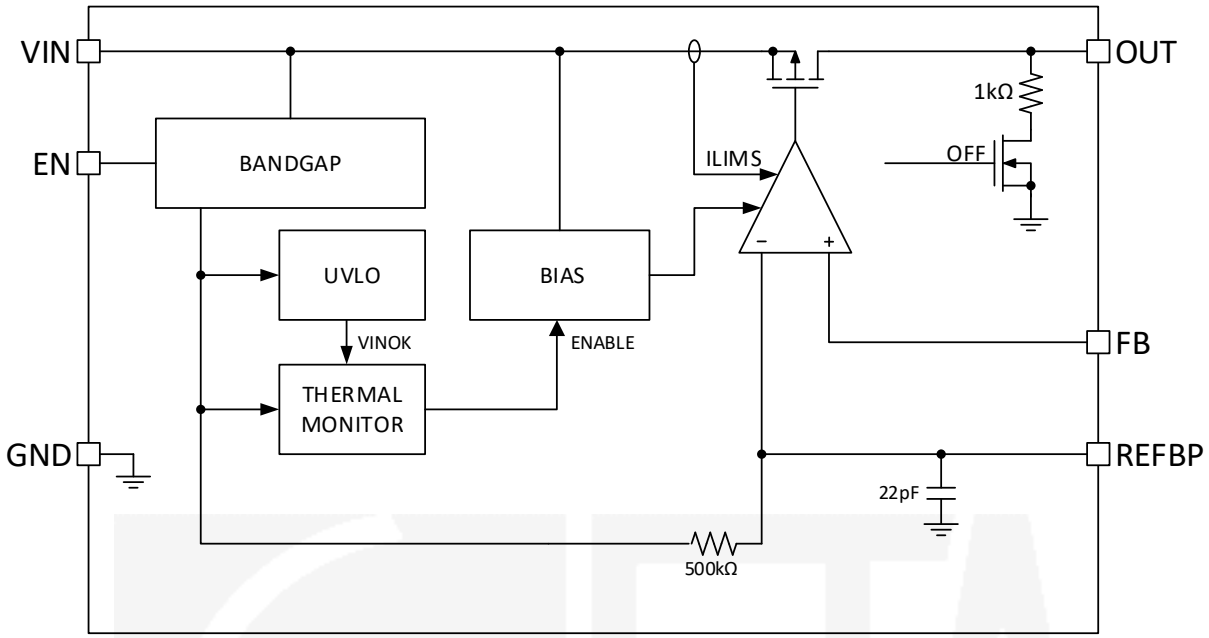


Startup Waveforms

Vin=3.6V, Vout=1.2V, Iout=150mA, No C_{bypass}



FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The ETA5052 family of LDO regulators has been optimized for application in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current, and enable-input to reduce supply currents to less than 1μA when the regulator is turned off.

Enable Sequence

ETA5052 is enabled when all below conditions happen. Otherwise, ETA5052 is in standby mode.

- EN pin voltage above Logic High level
- VIN is higher than Under-Voltage-Lock-Out Level.
- Junction Temperature is not at Over-Temperature Protection level.

Once all above conditions happen, ETA5052 first enable BANDGAP, and Pre-charge REFBP before enable internal 2.64V regulator and BIAS. Finally, when internal bias ready, ETA5052 enable LDO core.

ETA5052 is completed forced in shutdown mode when EN pin is at below LOGIC_LOW that supply current is less than 1μA. Otherwise, part only shutdown the VOUT while other circuit still in operation. Once ETA5052 is in shutdown conditions, Output is discharged by 1kΩ resistor.

Output Current Limit and Foldback Current Limit

ETA5052 family features an internal current limit. In normal operation, the ETA5052 limits output current to approximately 600mA. When current limiting engages, the output voltage scales back linearly until the over current condition ends.

In case output is in hard short conditions, ETA5052 also features an internal foldback limit that reduces the output current limit to a lower level, 300mA, then reduce power dissipation ratings of the package.

Reference Bypass

ETA5052 provides a pin that bypass internal reference voltage with an external capacitor. This improves PSRR at high frequency and also help reduces output noise.

Over-Temperature Protection

Thermal protection disables the output when the junction temperature rises to approximately 150°C, allowing the device to cool down. When the junction temperature cools to approximately 120°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

APPLICATION INFORMATION

External Output Voltage Setting

In external Output Voltage Setting Version selected, the ETA5052regulator is programmed using an external resistor divider. The output voltage is calculated using below equation.

$$V_{OUT} = V_{REF} \ x \ (1 + \frac{R_u}{R_d})$$

Where VREF = 1.200V typically (the internal reference voltage)

Resistors Ru and Rd should be chosen for approximately 40μA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistors values can cause accuracy issues. The recommended design procedure is to choose R2 = 30kΩ to set the divider current at 40μA, then R1 is calculated using below equation.

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) x \ R_2$$

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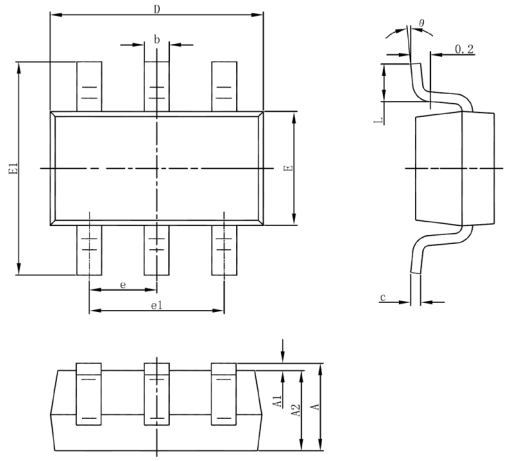
PACKAGE OUTLINE

Package: SOT23-6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°