PMU with 24V Current Limit Switch and 200mA Linear Regulator

DESCRIPTION

ETA5196 is a power management unit(PMU) consisting of a 24V current limit switch and a 200mA LDO linear regulator. The input operating voltage can be as high as 24V and input standoff voltage is up to 32V.

The LDO is capable of delivering up to 200mA current with a linear foldback current limit.

ETA5196 is available in SOT23-6 and SOP8 package.

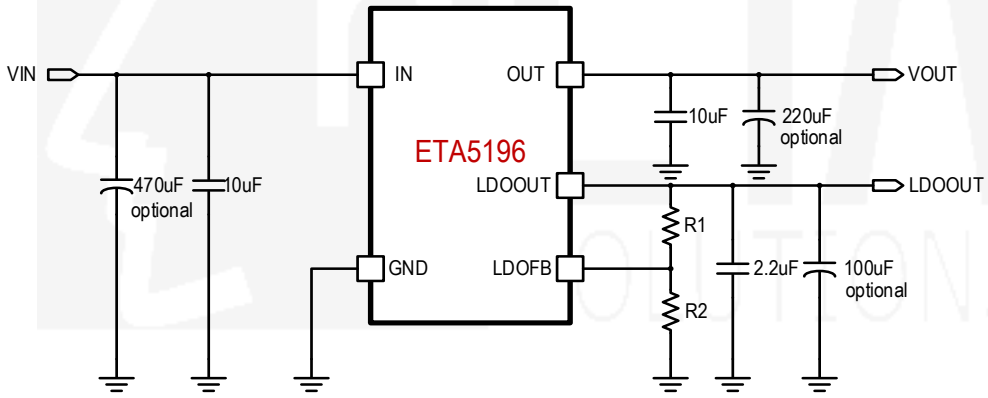
FEATURES

- Stable with Wide Range of Output Capacitor
- Wide Input Voltage Range: 3.8V-24V
- Wide Output Voltage Range of LDO: 1.1V-12V
- 32V Input Standoff Voltage
- Dual Thermal Shutdown
- SOT23-6 and SOP8 package
- RoHS Compliant

APPLICATIONS

- Power Meter
- Power Meter Module

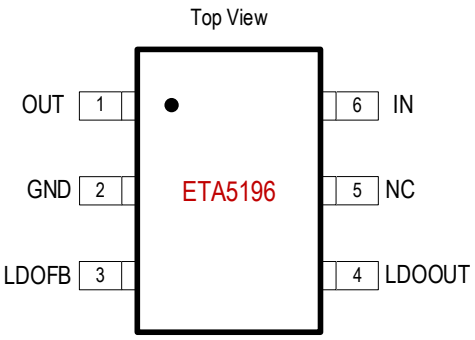
TYPICAL APPLICATION



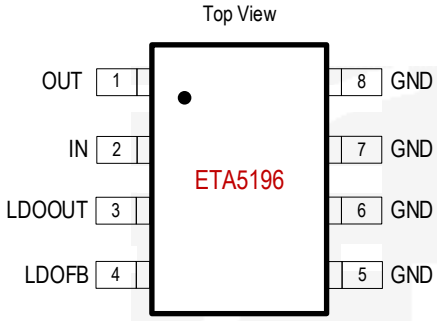
ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA5196V030S2G	SOT23-6	I2YW	3000
ETA5196V070S2G	SOT23-6	IdYW	3000
ETA5196V100S2G	SOT23-6	IC|YW	3000
ETA5196V066S8A	SOP8	ETA5196 00066 YWWXL	4000

PIN CONFIGURATION



SOT23-6



SOP8

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

IN, OUT, LDOOUT Voltage……–0.3V to 32V
LDOFB Voltage…….. –0.3V to 6.5V
OUT, LDOOUT to GND current……Internally limited
Operating Temperature Range……–40°C to 85°C
Storage Temperature Range……–55°C to 150°C

Thermal Resistance	θ_{JC}	θ_{JA}
SOT23-6	90	180 °C/W
SOP8		80 °C/W

Lead Temperature (Soldering, 10sec)…… 260°C
ESD HBM (Human Body Mode) ……2KV
ESD CDM (Charged Device Mode)……1KV

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{LDOOUT}=5V, unless otherwise specified. Typical values are at T_A = 25°C.)

PARAMETER	SYMBOL	TESTCONDITIONS	MIN	TYP	MAX	UNIT
Input Standoff Voltage	VIN_MAX		32			V
Input Voltage Range	VIN_RANGE		3.8		24	V
Input UVLO for System	SYS_UVLO	Rising, Hysteresis=200mV	3.4	3.5	3.65	V
Input Supply Current	IQ	V_{IN} = 7V		100		μA
		V_{IN} = 12V		180		μA
		V_{IN} = 24V		200		μA
Thermal Shutdown for System	SYS_TSD	Rising, Hys=15°C		155		°C
CURRENT LIMIT SWITCH						
Input UVLO For Current Limit Switch	SW_UVLO	Rising, Hysteresis=500mV	7.5	8.0	8.5	V
Thermal Shutdown for Switch	SW_TSD	Rising, Hys=15°C		135		°C
Power Switch On Resistance	RON	I_{SW} = 500mA, -40°C≤T_J≤120°C		500	900	mΩ

Current Limit Threshold	SW_ILIM_030		255	300	345	mA
	SW_ILIM_066		560	660	759	
	SW_ILIM_070		595	700	805	
	SW_ILIM_100		850	1000	1150	
Foldback Current Limit Reduction Ratio	SW_IFLDBCK	I_{OUT_CC} / (V_{IN}– SW_VFLDBCK –V_{OUT})		10		%ILIM/ V
Current Limit Foldback Start Threshold	SW_VFLDBCK	V_{IN}-V_{OUT}		2.5		V
LOW DROP-OUT REGULATOR LDO						
Dropout Voltage	$V_{DROPOUT}$	I_{LDOOUT}=100mA		1.5		V
LDOFB Threshold	V_{REF}	-40°C≤T_J≤120°C	1.067	1.1	1.133	V
LDOFB Input Leakage	I_{FB}				0.01	μA
Maximum Continuous Output Current	I_{OUT}				200	mA
LDO Current Limit	LDO_ILIM	V_{LDOFB} = 1.05V	300		400	mA
LDO Current Limit at Foldback	LDO_IFLDBCK	V_{LDOOUT} < 0.25V	70	90		mA
LDO Current Limit Foldback Start threshold	LDO_VFLDBCK	LDOFB pin Voltage		0.9		V

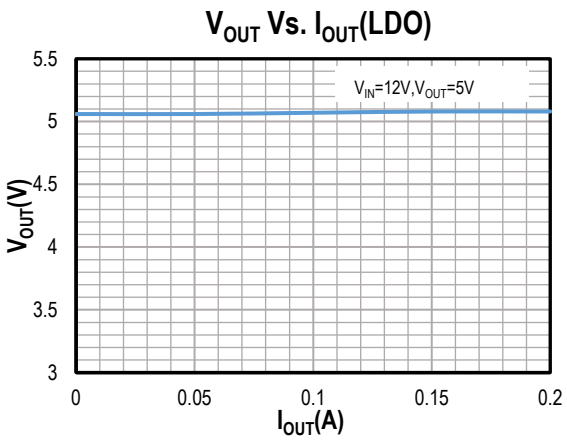
PIN DESCRIPTION

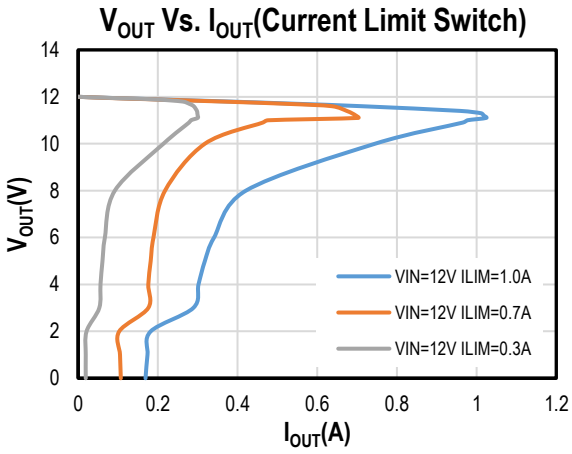
SOT23-6 PIN #	NAME	DESCRIPTION
1	OUT	Output pin of the current limit switch. Bypass with a 10uF capacitor to GND. A 220uF or larger electrolytic capacitor can be also placed at the output.
2	GND	Ground
3	LDOFB	Feedback pin of the LDO
4	LDOOUT	Output pin of the LDO. Bypass with a 2.2uF capacitor to GND. A 100uF or larger electrolytic capacitor can be also placed at the output.
5	NC	Not connected
6	IN	Input pin. Bypass with a 10uF capacitor to GND. A 470uF or larger electrolytic capacitor can be also placed at the input.

SOP8 PIN #	NAME	DESCRIPTION
1	OUT	Output pin of the current limit switch. Bypass with a 10uF capacitor to GND. A 220uF or larger electrolytic capacitor can be also placed at the output.
2	IN	Input pin. Bypass with a 10uF capacitor to GND. A 470uF or larger electrolytic capacitor can be also placed at the input.
3	LDOOUT	Output pin of the LDO. Bypass with a 2.2uF capacitor to GND. A 100uF or larger electrolytic capacitor can be also placed at the output.
4	LDOFB	Feedback pin of the LDO
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground

TYPICAL CHARACTERISTICS

(V_{IN} = 12V, TA=25°C, unless otherwise specified)





FUNCTION DESCRIPTION

Enable and Disable

LDO is enabled if all of following conditions occur:

- V_{IN} is greater than UVLO
- Junction temperature of IC does not exceed SYS_TSD

LDO is disable if one of above conditions do not occur.

Current Limit Switch is enabled if all of following conditions occur:

- V_{IN} is greater than SW_UVLO
- Junction temperature of IC does not exceed SW_TSD

Current Limit Switch is disable if one of above conditions do not occur.

Current Limit Switch

The current limit ensures that the current through the switch does not exceed the maximum.

Low Dropout (LDO) Regulator

The ETA5196 is equipped with a low dropout regulator which can configure the output voltage from 1.1V to 12V. The LDO can provide up to 200mA current for the output device.

To inhibit the heat generation of LDO, ETA5196 reduces the LDO current limit. In the foldback condition, the current is reduced linearly when LDO_FB pin voltage falls below 0.9V and get the minimum of 90mA when LDO_FB pin voltage reach 0.2V.

Thermal Shutdown

ETA5196 is integrated with dual independent thermal shutdown activities. When the temperature of IC exceeds SW_TSD (135°C typically), the part shutdowns Current Limit Switch. LDO is still maintained as long as the IC temperature is still under SYS_TSD (155°C typically).

APPLICATION INFORMATION

LDO Output Voltage Setting

The output voltage of the ETA5196 LDO regulator can be programmed by using an external resistor divider. The output voltage is calculated by the equation below.

$$V_{LDOOUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right)$$

Where: V_{REF} =1.1V typically (the internal reference voltage)

To minimize feedback resistor current which is determined by V_{REF} and R_1, R_1 has to be from 22kΩ to 220kΩ and thus R_2 is calculated by the following equation:

$$R_2 = \left(\frac{V_{LDOOUT}}{V_{REF}} - 1 \right) \times R_1$$

LDO output voltage configuration is recommended in following table:

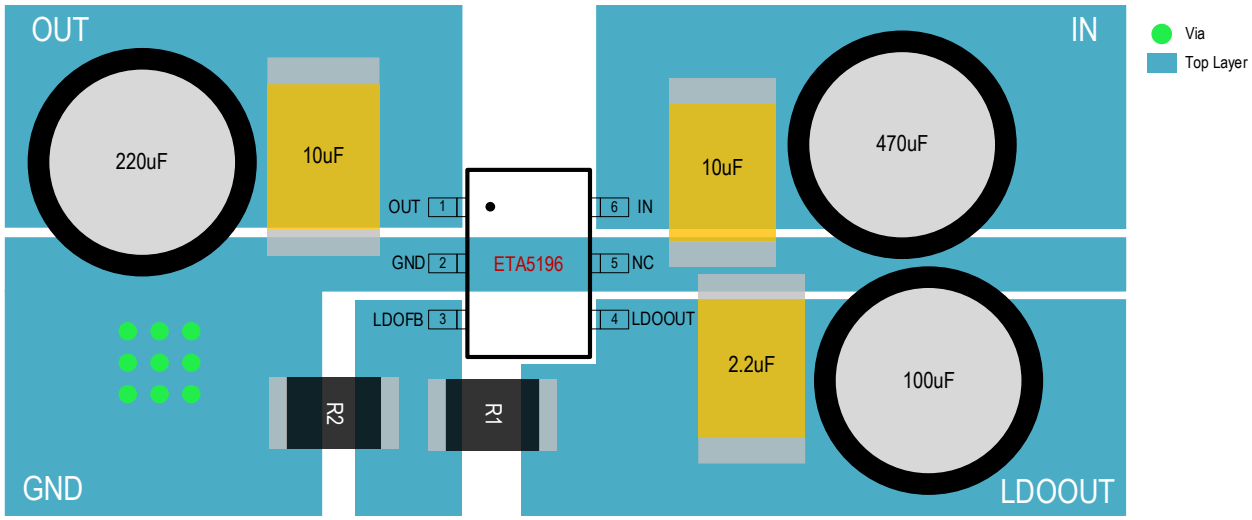
R_1 = 22kΩ (I_{FB} = 50μA)		R_1 = 33kΩ (I_{FB} = 33μA)		R_1 = 44kΩ (I_{FB} = 25μA)		R_1 = 66kΩ (I_{FB} = 16.67μA)	
R_2 (kΩ)	V_{OUT} (V)	R_2 (kΩ)	V_{OUT} (V)	R_2 (kΩ)	V_{OUT} (V)	R_2 (kΩ)	V_{OUT} (V)
11	1.2	3	1.2	4	1.2	6	1.2
14	1.8	21	1.8	28	1.8	42	1.8
28	2.5	42	2.5	56	2.5	84	2.5
44	3.3	66	3.3	88	3.3	132	3.3
58	4	87	4	116	4	174	4
78	5	117	5	156	5	234	5
98	6	147	6	196	6	294	6
118	7	177	7	236	7	354	7
138	8	207	8	276	8	414	8
158	9	237	9	316	9	474	9
178	10	267	10	356	10	534	10
2	1.2	3	1.2	4	1.2	6	1.2
14	1.8	21	1.8	28	1.8	42	1.8
28	2.5	42	2.5	56	2.5	84	2.5

LDO Output Capacitor Selection

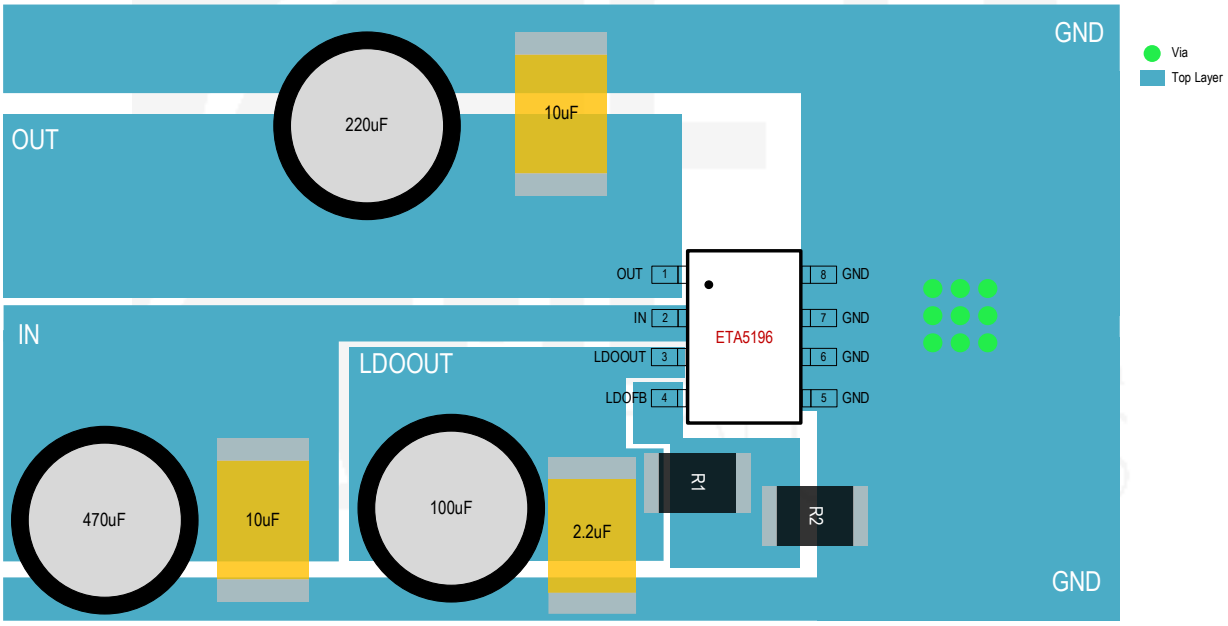
By using ETA Solutions architecture, LDO output can be stable with any capacitor type ranging from 1μF to 100μF. To maximize LDO performance, it is strong recommended to select output capacitor with some below tips:

- If need to use huge capacitor, It will be no problem to use a 1μF ceramic capacitor in parallel with a huge electrolytic capacitor. Or it can even be a single electrolytic capacitor.
- Use the capacitor bigger than 2.2uF for the setting of LDOOUT lower than 1.5V for better transient.

PCB GUIDELINES



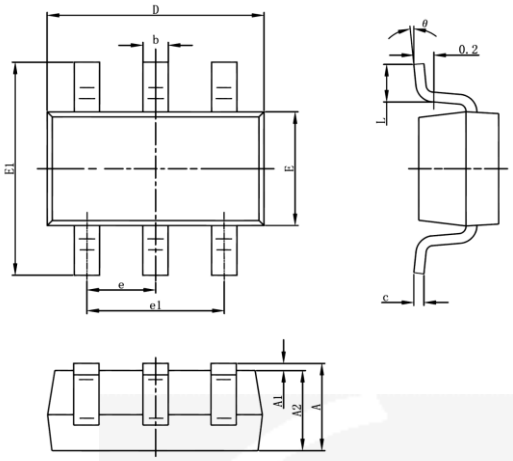
SOT23-6 package

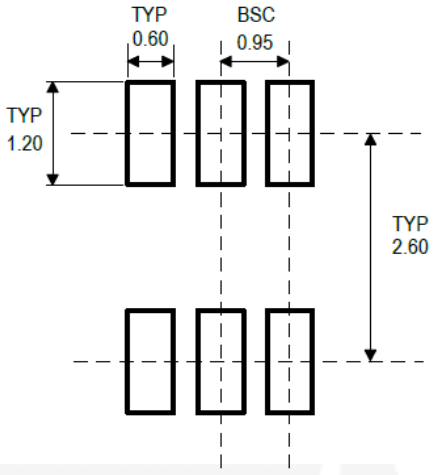


SOP8 package

PACKAGE OUTLINE

Package: SOT23-6

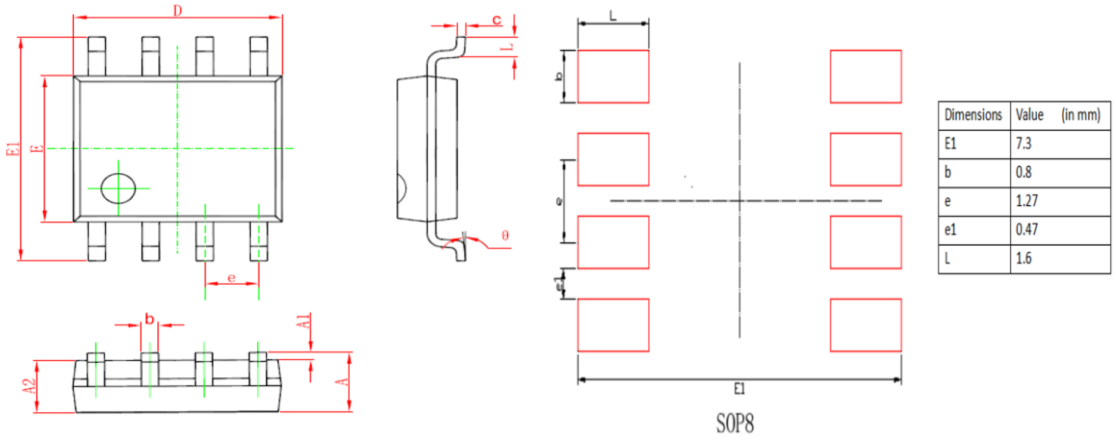




RECOMMENDED LAND PATTERN

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Package: SOP8

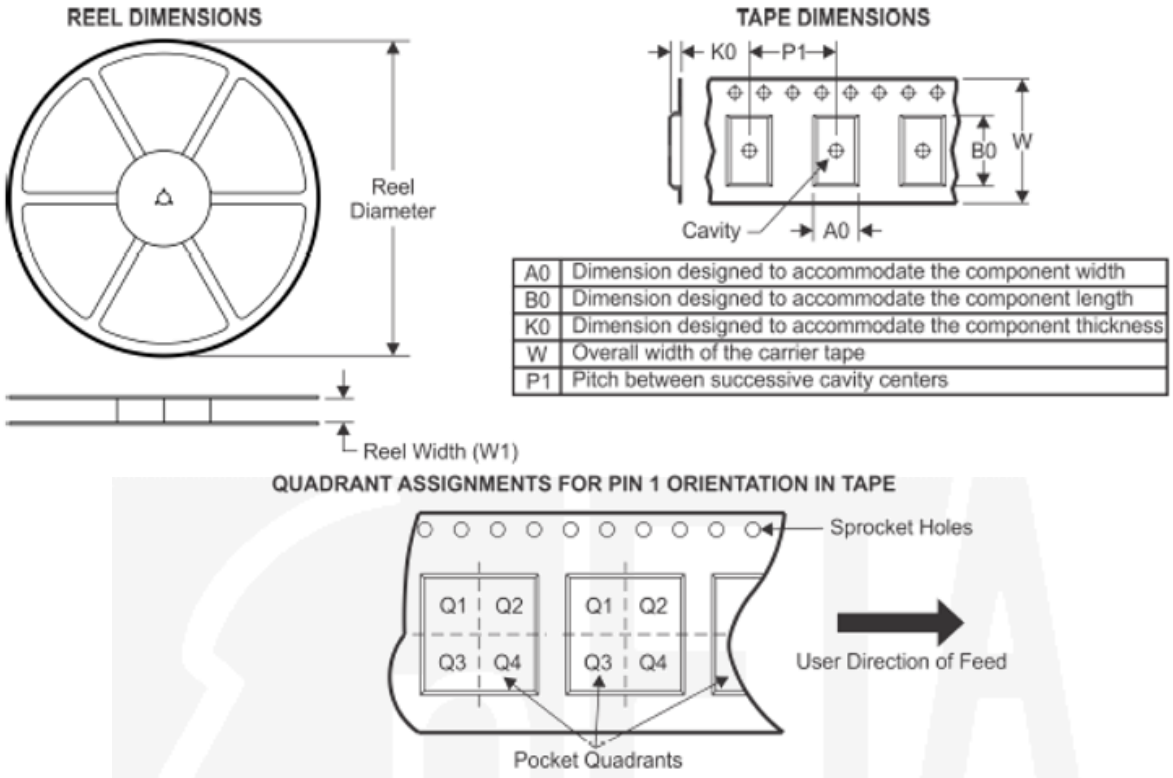


SOP8

Dimensions	Value (in mm)
E1	7.3
b	0.8
e	1.27
e1	0.47
L	1.6

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA5196V030S2G	SOT23-6	6	3000	180	9.5	3.17	3.23	1.37	4	8	Q3
ETA5196V070S2G	SOT23-6	6	3000	180	9.5	3.17	3.23	1.37	4	8	Q3
ETA5196V100S2G	SOT23-6	6	3000	180	9.5	3.17	3.23	1.37	4	8	Q3
ETA5196V066S8A	SOP8	8	4000	330	12.7	6.6	5.4	2.05	8	12	Q1