13.5V/3A, 1-Cell Battery Charger with Power Path Management

DESCRIPTION

ETA6964 is a highly-integrated 3A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. It features fast charging with high input voltage support for a wide range of smart phones, tablets and portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. Its input voltage and current regulation deliver maximum charging power to battery. The solution is highly integrated with input reverse-blocking FET (Q1), high-side switching FET (Q2), low-side switching FET (Q3), and battery FET (Q4) between system and battery. It also integrates the bootstrap diode for the high-side gate drive for simplified system design. The device supports a wide range of input sources: standard USB host port, USB charging port, and USB compliant high voltage adapter. To support fast charging using high voltage adapter. The device is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. The device also meets USB On-the-Go (OTG) operation power rating specification by supplying 5.15 V on BUS with constant current limit up to 1.2A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.5 V minimum system voltage. With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This Supplement Mode prevents overloading the input source.

ETA6964 also integrates an input OVP controller to protect itself from an input voltage surge as high as 40V.

ETA6964 is available in a QFN4x4-24 package.

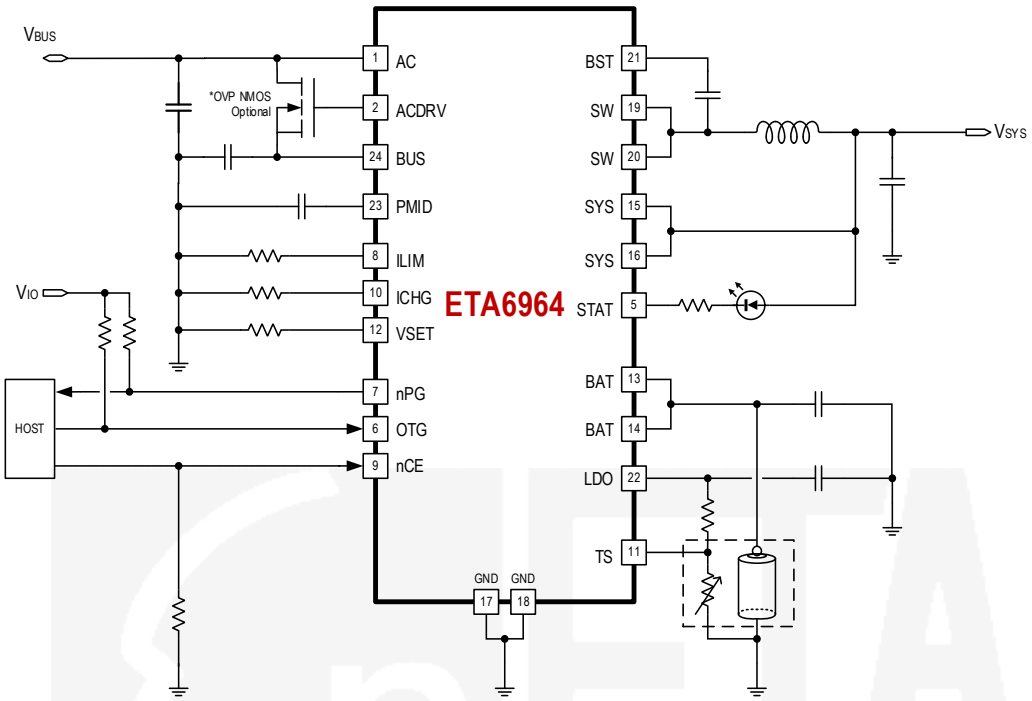
FEATURES

- High-Efficiency, 1.5MHz Synchronous Switching Buck Charger
  - 91% Charge Efficiency at 2A from 5V Input
  - Programmable PFM Mode for Light Load Conditions
- Supports USB On-The-Go (OTG)
  - Boost Converter with Up to 1.2A Output
  - 91% Boost Efficiency at 1A Output
  - Output Short Circuit Protection
- Wide Range Single Input to Support both USB Input and High Voltage Adapters
  - Support 3.9V to 13.5V Input Voltage Range with 22V Absolute Maximum Input Voltage Rating
  - Maximum Power Tracking by Input Voltage Limit Up to 4.5V (V_{INDPM})
  - Auto Detect USB BC1.2, SDP, CDP, DCP and Non-Standard Adaptors
- High Battery Discharge Efficiency with 27mΩ Battery Discharge MOSFET
- Fast Turn-Off of Operational External OVPFET, Standing Input Voltage Up to 40V
- Narrow VDC (NVDC) Power Path Management
- High Integration Includes All MOSFETs, Current Sensing and Loop Compensation
- Safety
  - Battery Temperature Sensing for Charge and Boost Mode
  - Thermal Regulation and Thermal Shutdown
- Input UVLO and Overvoltage Protection
- Available in a QFN4x4-24 package

APPLICATIONS

- Tablet PC, Smart Phone, Internet Devices
- Portable Audio Speaker
- Handheld Computers, PDA, POS

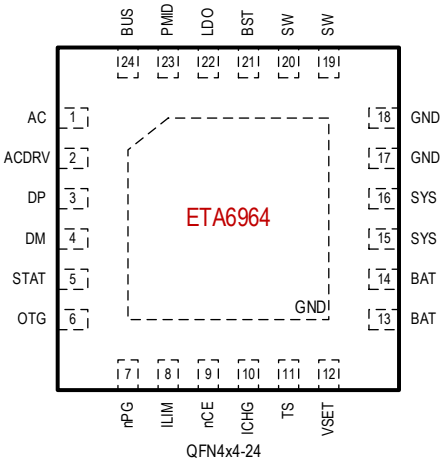
TYPICAL APPLICATION



ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA6964Q4Y	QFN4x4-24	ETA6964 YWW2L	5000

PIN CONFIGURATION



ABSOLUTEMAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

AC to GND Voltage .....–2V to 40V
ACDRV to GND Voltage .....–0.3V to 40V
BUS to GND Voltage .....–2V to 22V
PMID, SW to GND Voltage.....–0.3V to 22V
SYS, BAT to GND Voltage.....–0.3V to 6V
BST to SW Voltage .....–0.3V to 6V
All Other Pin to GND Voltage.....–0.3V to 6V
SW, BUS, BAT, SYS to PGND Current.....Internally limited
Operating Temperature Range.....–40°C to 85°C
Storage Temperature Range.....–55°C to 150°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN4x4-24	35	10	°C/W

Lead Temperature (Soldering 10sec) .....260°C

ELECTRICAL CHARACTERISTICS

(V_{BAT}= 3.6V, unless otherwise specified. Typical values are at T_A = 25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS					
Battery discharge current (BAT, SW, SYS) in buck mode	V_{BAT} = 4.5V, V_{BUS} < $V_{BUS-UVLOZ}$,leakage between V_{BAT} and V_{BUS}, T_J< 85°C			5	μA
Battery discharge current (BAT, SW, SYS)	V_{BAT}=4.5V,No V_{BUS},T_J < 85°C		80	160	μA
Input supply current (V_{BUS}) in buck mode	V_{BUS} > V_{BUS_UVLO}, V_{BUS} > V_{BAT}, converter switching, V_{BAT} = 3.8V, I_{SYS} = 0A		5		mA
Battery Discharge Current in boost mode	V_{BAT} = 4.2V, boost mode, I_{BUS} = 0A, converter switching		2		mA
BUS, AC AND BAT PIN POWER-UP					
V_{AC} operating range	V_{AC} rising	3.9		13.5	V
OVPFET turn on threshold	V_{AC} rising		3.65	3.9	V
	V_{AC} falling		500		mV
Sleep mode falling threshold(V_{BUS} – V_{BAT})	$V_{BUS\_MIN\_FALL}$ ≤ V_{BAT} ≤ V_{REG}, V_{BUS} falling	15	60	110	mV
Sleep mode rising threshold(V_{BUS}– V_{BAT})	$V_{BUS\_MIN\_FALL}$ ≤ V_{BAT}≤ V_{REG}, V_{BUS} rising	110	220	330	mV
V_{AC} Overvoltage rising threshold	V_{AC} rising,	13	14	15	V
V_{AC} Overvoltage hysteresis	V_{AC} falling		500		mV
Battery Depletion Threshold	V_{BAT} falling	2.2	2.4	2.6	V
Battery Depletion Threshold	V_{BAT} rising	2.35	2.58	2.8	V
Battery Depletion rising hysteresis	V_{BAT} rising		180		mV
Bad adapter detection falling threshold	V_{BUS} falling	3.7	3.9	4.1	V
Bad adapter detection hysteresis			80		mV
Bad adapter detection current source	Sink current from BUS to GND		30		mA
POWER-PATH					
System regulation voltage	V_{BAT} < 3.5V		3.68		V
System Regulation Voltage	I_{SYS} = 0A, V_{BAT} = 4.4V		V_{BAT}+ 70mV		
Top reverse blocking MOSFET on-resistance between BUS and PMID - Q1	-40°C≤ T_A ≤ 125°C	20	40	60	mΩ
Top switching MOSFET on-resistance between PMID and SW - Q2	V_{LDO} = 5V , -40°C≤ T_A ≤ 125°C	35	70	105	mΩ
Bottom switching MOSFET on-resistance between SW and GND - Q3	V_{LDO} = 5V, -40°C≤ T_A ≤ 125°C	21	43	65	mΩ
SYS-BAT MOSFET on-resistance – Q4	Measured from BAT to SYS, V_{BAT} = 4.2V, T_J = –40°C~125°C	13	27	40	mΩ
BATFET forward voltage in supplement mode			30		mV
BATTERY CHARGER					

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Charge voltage setting	R_{VSET} > 50kΩ, –40 °C≤ T_J ≤ 85°C	4.179	4.200	4.221	V
	R_{VSET} < 500Ω, –40°C ≤ T_J ≤ 85°C	4.323	4.344	4.365	V
	R_{VSET} = 10kΩ, –40 °C≤ T_J ≤ 85°C	4.378	4.4	4.422	V
Charge voltage setting accuracy	–40°C ≤T_J ≤ 85°C	-0.5		+0.5	%
Charge current regulation range		0		3000	mA
Charge current regulation setting	R_{ICHG} = 4KΩ, V_{BAT} = 3.8V	1.8	2.0	2.2	A
Charge current regulation accuracy	I_{CHG} = 240 mA, V_{BAT} = 3.8V	-10		+10	%
Charge current regulation setting ratio	R_{ICHG} = 4KΩ, V_{BAT} = 3.8V		8000		AxΩ
Battery LOWV falling threshold	Fast charge to Pre-charge	2.6	2.8	3	V
Battery LOWV rising threshold	Pre-charge to fast charge	2.9	3.1	3.3	V
Pre-charge current regulation	V_{BAT} = 2.6V	90	180	270	mA
Termination current regulation	V_{BAT} = 4.208V	90	180	270	mA
Battery short voltage	V_{BAT} falling	1.8	2	2.2	V
Battery short voltage	V_{BAT} rising	2.05	2.25	2.45	V
Battery short current	V_{BAT} = 1V		145		mA
Recharge Threshold below V_{BAT_REG}	V_{BAT} falling	70	120	170	mV
INPUT VOLTAGE AND CURRENT REGULATION					
Input voltage regulation limit		4.32	4.5	4.68	V
Input voltage regulation accuracy		-4		4	%
Input current regulation limit	V_{AC} = 5V, R_{ILIM} = 1.35KΩ, –40°C≤ T_J ≤ 85°C	1.8	2	2.2	A
Input current regulation limit accuracy	V_{AC} = 5V, R_{ILIM} = 1.35KΩ, –40°C ≤ T_J ≤ 85°C	-10		10	%
Input current setting ratio, I_{ILIM} = K_{ILIM} /R_{ILIM}	V_{AC} = 5V, R_{ILIM} = 1.35KΩ, –40°C ≤ T_J ≤ 85°C		2700		AxΩ
Input current limit during system start-up sequence			200		mA
BAT PIN OVERVOLTAGE PROTECTION					
Battery overvoltage threshold	V_{BAT} rising, as percentage of V_{BAT_REG}		108		%
Battery overvoltage threshold Hysteresis	V_{BAT} falling, as percentage of V_{BAT_REG}		103		%
THERMAL REGULATION AND THERMAL SHUTDOWN					
Junction Temperature Regulation Threshold	Temperature Increasing		110		°C
Thermal Shutdown Rising Temperature			160		°C
Thermal Shutdown Hysteresis			30		°C
JEITA Thermistor Comparator (BUCK MODE)					
T1 (0°C) threshold, Charge suspended T1 below this temperature.	Charger suspends charge. As Percentage to V_{LDO}		73.3		%
Falling	As Percentage to V_{LDO}		71.5		%

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T2 (10°C) threshold, Charge back to I_{CHG}/5 and 4.2 V below this temperature	As Percentage to V_{LDO}		68		%
Falling	As Percentage to V_{LDO}		66.8		%
T3 (45°C) threshold, charge back to I_{CHG} above this temperature.	Charger suspends charge. As Percentage to V_{LDO}		44.7		%
Falling	As Percentage to V_{LDO}		45.7		
T5 (60°C) threshold, charge suspended above this temperature.	As Percentage to V_{LDO}		34.2		%
Falling	As Percentage to V_{LDO}		35.3		%
COLD OR HOT THERMISTER COMPARATOR (BOOST MODE)					
Cold Temperature Threshold, TS pin Voltage Rising Threshold	As Percentage to V_{LDO} (Approx. -20°C w/ 103AT), TJ = –20°C~125°C	78	80.0	82	%
Falling	T_J = –20°C - 125°C	77	79.0	81	%
Hot Temperature Threshold, TS pin Voltage falling Threshold	As Percentage to V_{LDO} (Approx. 60°C w/ 103AT), T_J = –20°C~125°C	29.2	31.2	33.2	%
Rising	T_J = –20°C ~125°C	32.4	34.4	36.4	%
CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)					
HSFET cycle-by-cycle over-current threshold		4.8	5.8	7.5	A
System over load threshold		4.7	5.2	5.7	A
CHARGE UNDER-CURRENT COMPARATOR (CYCLE-BY-CYCLE)					
LSFET under-current falling threshold	From sync mode to non-sync mode		250		mA
PWM					
PWM switching frequency	Oscillator frequency		1500		kHz
Maximum PWM duty cycle			97		%
BOOST MODE OPERATION					
Boost mode regulation voltage	V_{BAT} = 3.8 V, I_{PMID} = 0 A	5	5.15	5.3	V
Boost mode regulation voltage accuracy	V_{BAT} = 3.8 V, I_{PMID} = 0 A	-3		3	%
Battery voltage exiting boost mode	V_{BAT} falling	2.6	2.8	3.0	V
	V_{BAT} rising	2.8	3	3.2	V
OTG mode output current		1.2	1.4		A
OTG overvoltage threshold	Rising threshold	5.6	6	6.4	V
HSFET under current falling threshold			100		mA
V_{LDO} REGULATION					
LDO output voltage	V_{BUS} = 9V, I_{LDO} = 40mA		5		V
LDO output current limit	V_{BUS} = 9V, V_{LDO} = 4V		80		mA
LOGIC I/O PIN CHARACTERISTICS (nCE, OTG)					
Input low threshold				0.4	V
Input high threshold		1.3			V
High-level leakage current	Pull up rail 1.8 V			1	μA

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC I/O PIN CHARACTERISTICS (nPG, STAT)					
Low-level output voltage				0.4	V
V_{BUS}/V_{BAT} POWER UP					
Bad adapter detection duration			30		ms
BATTERY CHARGER					
Deglitch time for charge Termination			7		s
Deglitch time for recharge			32		ms
System over-current deglitch time to turn off Q4			1		ms
Battery over-voltage deglitch time to disable charge			10		μs
Typical Charge Safety Timer Range			10		Hr
DP/DM DETECTION					
$V_{DP/DM\_600MVSRC}$	Voltage source (600 mV)		600		mV
R_{DM_19K}			19		kΩ
V_{DP/DM_0P325}			0.325		V
V_{2P7_VTH}	DP/DM Threshold for non-standard adapter	2.55	2.7	2.85	V
V_{2P0_VTH}	DP/DM Threshold for non-standard adapter	1.85	2.0	2.15	V
V_{1P2_VTH}	DP/DM Threshold for non-standard adapter	1.05	1.2	1.35	V

PIN DESCRIPTION

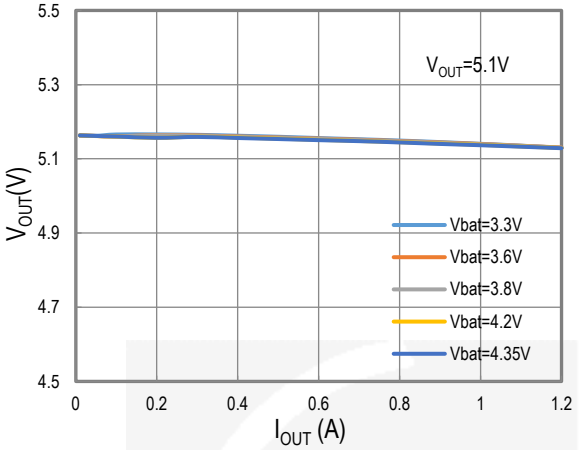
PIN NAME	PIN #	DESCRIPTION
AC	1	Input voltage sensing. When V_{AC} is below OVP threshold and above UVLO, external OVPFET turns on. If external OVP is not used, this pin must be shorted to BUS pin.
BUS	24	Charger input voltage. Bypass it with a 10μF ceramic capacitor from BUS to PGND. The capacitor should be close to BUS pin.
ACDRV	2	Charge pump output to drive external N-channel MOSFET (OVPFET). ACDRV voltage is 7.5 V above V_{BUS} when V_{AC} voltage is below OVP threshold and above UVLO threshold. If external OVP is not used, leave this pin floating.
DP	3	Positive line of the USB data line pair. DP/DM based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and non-standard adaptors
DM	4	Negative line of the USB data line pair. DP/DM based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors
STAT	5	Open-drain charge status output. Connect the STAT pin to a logic rail via 10kΩ resistor. The STAT pin indicates charger status. Connect a current limit resistor and a LED from a rail to this pin. Charge in progress: LOW Charge complete or charger in SLEEP mode: HIGH Charge suspend (fault response)or No bat: 1Hz, 50% duty cycle Pulses
OTG	6	Boost mode enable pin. When this pin is pulled HIGH, OTG is enabled. OTG cannot be floating.
nPG	7	Open drain active low power good indicator. Connect to the pull up rail through 10kΩ resistor. LOW indicates a good input source if the input voltage is between UVLO and OVP threshold, above SLEEP mode threshold, and current limit is above 30 mA.
ILIM	8	ILIM sets the input current limit. A resistor is connected from ILIM pin to ground to set the input current limit as $I_{INDPM}= K_{ILIM} /R_{ILIM}$. The acceptable range for ILIM current is 500 mA - 3200 mA. The resistor based input current limit is effective only when the input adapter is detected as unknown. Otherwise, the input current limit is determined by D+/D– detection outcome.
nCE	9	Charge disable control pin. nCE=0, charge is enabled. nCE=1, charge is disabled.
ICHG	10	ICHG pin sets the charge current limit. A resistor is connected from ICHG pin to ground to set charge current limit as $ICHG = K_{ICHG} /R_{ICHG}$. The acceptable range for charge current is 300 mA – 3000 mA.
TS	11	Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from LDO to TS to GND. Charge suspends when either TS pin is out of range. When TS pin is not used, connect a 10kΩ resistor from LDO to TS and connect a 10kΩ resistor from TS to GND. It is recommended to use a 103AT-2 thermistor.

PIN NAME	PIN #	DESCRIPTION
VSET	12	VSET pin sets default battery charge voltage in ETA6964. Program battery regulation voltage with a resistor pull-down from VSET to GND. R_{PD} > 50kΩ (float pin) = 4.208 V, R_{PD} < 500Ω (short to GND) = 4.352 V, 5kΩ < R_{PD} < 25kΩ = 4.400 V
BAT	13, 14	Positive battery terminal. The internal BATFET and current sensing is connected between SYS and BAT. Connect a 10μF close to the BAT pin.
SYS	15, 16	Converter output connection point. The internal current sensing network is connected between SYS and BAT. Connect a 20μF close to the SYS pin.
GND	17, 18	Power Ground
SW	19, 20	Switching node output. Connected to output inductor. Connect the 10nF bootstrap capacitor from SW to BST
BST	21	Bootstrap capacitor connection for the high-side FET gate driver. Connect a 10nF ceramic capacitor from BST pin to SW pin.
LDO	22	LDO Output Voltage. Bypass the pin with 4.7μF capacitor from LDO to GND. The capacitor should be closed to the pin
PMID	23	Connection point between reverse blocking FET and high-side switching FET. Bypass it with a minimum of 10μF capacitor from PMID to PGND. This capacitor should be close to the PMID pin.
EP	EP	Thermal pad and ground reference. This pad is ground reference for the device and it is also the thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane through PCB vias under the pad.

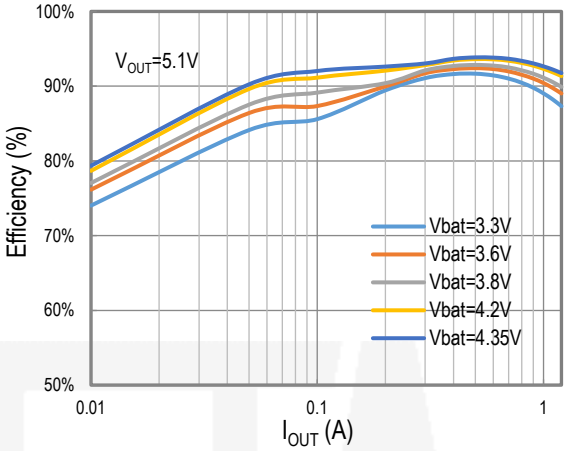
TYPICAL PERFORMANCE CHARACTERISTICS

(Typical values are at T_A = 25°C unless otherwise specified.)

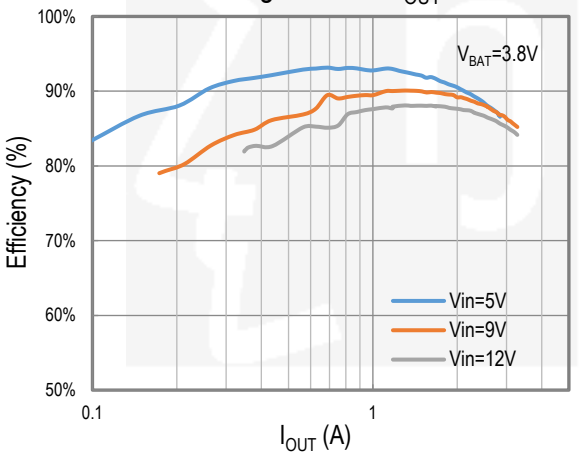
OTG V_{OUT} Vs. I_{OUT}



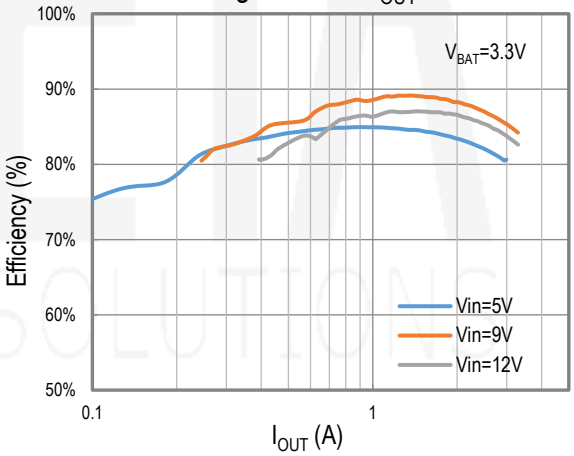
OTG Eff. Vs. I_{OUT}



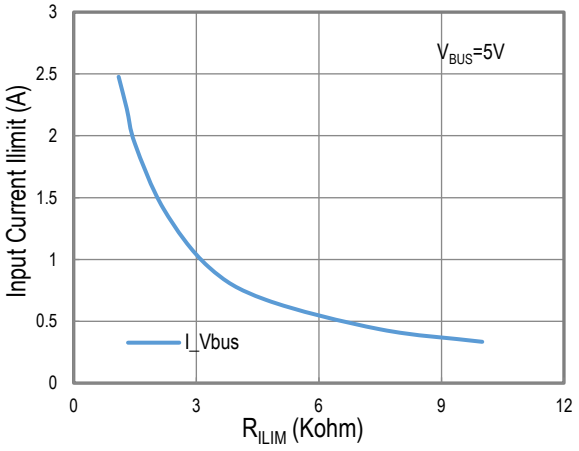
Charger Eff. Vs. I_{OUT}



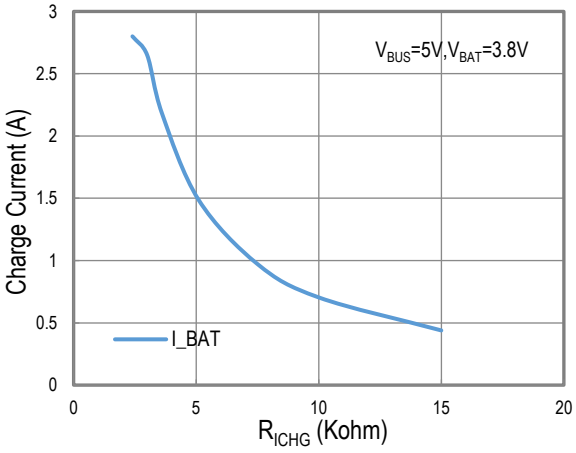
Charger Eff. Vs. I_{OUT}



Input Current limit Vs. R_{ILIM}

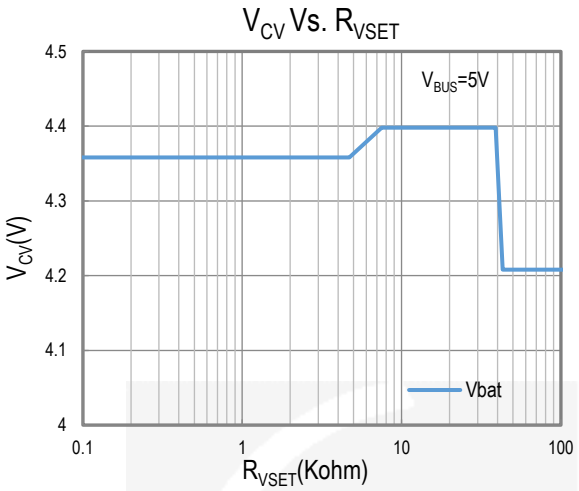


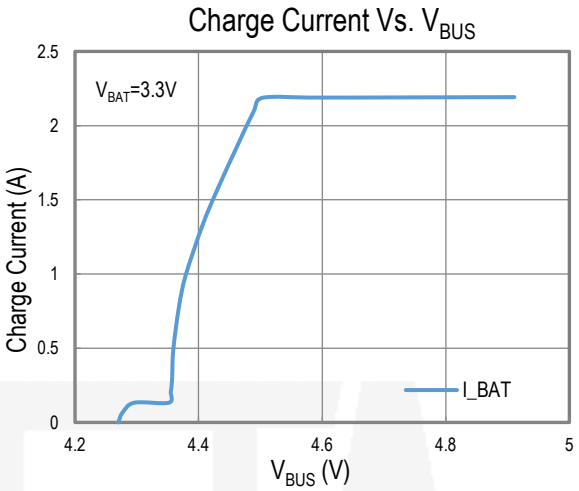
Charge Current Vs. R_{ICHG}

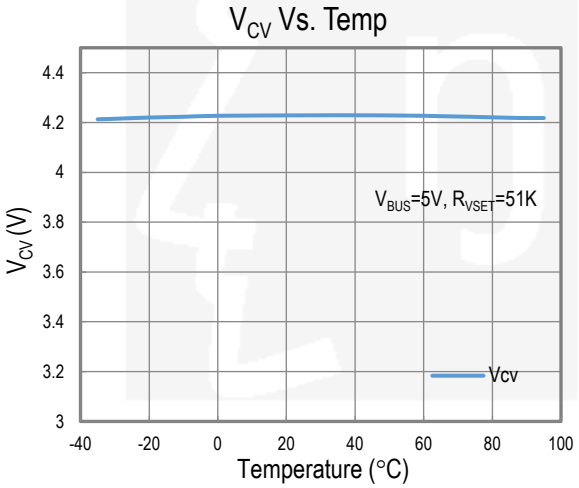


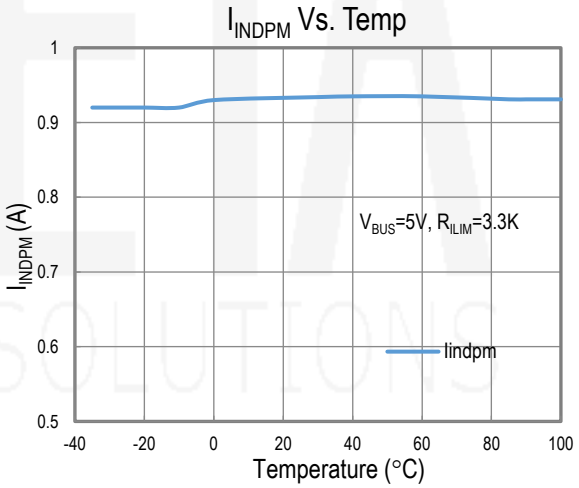
TYPICAL PERFORMANCE CHARACTERISTICS cont'

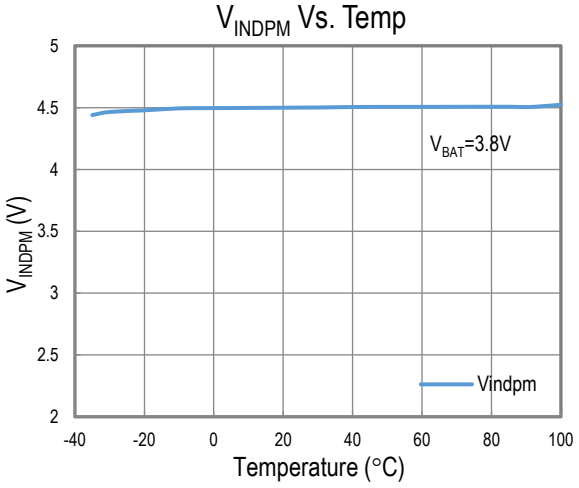
(Typical values are at T_A = 25°C unless otherwise specified.)

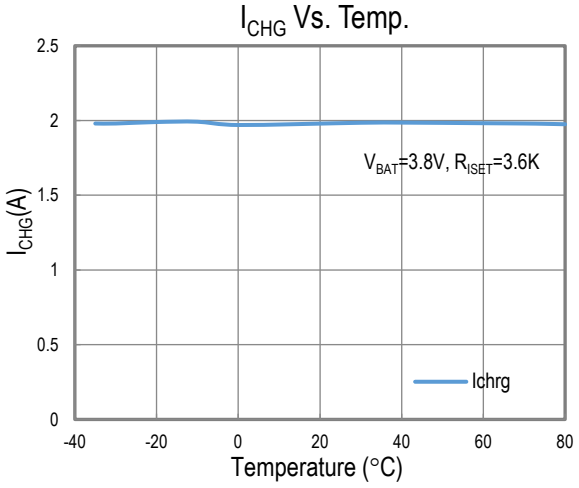












FUNCTION DESCRIPTION

The ETA6964 device is a highly integrated 3A switch-mode battery charger for single cell Li-Ion and Li-polymer battery. It includes the input reverse-blocking FET (Q1), high-side switching FET (Q2), low-side switching FET (Q3), and battery FET (Q4), and bootstrap diode for the high-side gate drive.

POWER UP FROM BATTERY WITHOUT INPUT SOURCE

When a battery is applied without other input, the device checks the battery voltage to turn on BATFET but not V_{LDO} to minimize the supply current, especially for NTC resistor network. All supply will be directly from battery. V_{LDO} is disabled until BOOST is enabled. Anyway, in order to optimize the discharge current from battery at light load, BATFET gate charge pump operates with lower frequency.

POWER UP WITH INPUT SOURCE

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. Power up OVP FET
2. Power up V_{LDO}
3. Poor Source Qualification
4. Input Voltage Limit Threshold Setting (V_{INDPM} threshold)
5. Converter Power-up

OVPFET POWER UP

The external OVPFET provides an additional layer of voltage protection for the device. The external OVPFET is enabled when all the below conditions are valid.

1. V_{AC} above $V_{AC\_PRESENT}$
2. V_{AC} below V_{BAT} + V_{SLEEP} (200mV) in boost mode
3. V_{AC} below V_{AC_OV}
4. After T_{DEB} (15ms nom) delay is completed

If one of the above conditions is not valid, the device is in high impedance state (HIZ) with REGN LDO off. The device draws less current (I_{BUS_HIZ}) from V_{BUS} during a HIZ state. The battery powers the system when the device is in a HIZ state.

LDO POWER UP

LDO is enabled when the below conditions are met:

1. V_{AC} is above 3.65V
2. V_{AC} is above V_{BAT} + V_{SLEEP} (200mV) in Buck mode or V_{AC} below V_{BAT} + V_{SLEEP} in Boost mode

Right after two above conditions are valid, V_{LDO} is powered up right away

POWER SOURCE QUALIFICATION

After LDO powers up, the device checks the current capability of the input source. The input source has to meet the following

requirements in order to start the buck converter.

1. 200mS delay after LDO enable
2. V_{AC} voltage below the V_{AC_OVP} threshold
3. V_{AC} voltage above 3.8V when pulling down 30mA at AC pin

If the device fails the poor source detection in 30ms, it repeats poor source qualification every 2 seconds.

DP/DM DETECTION SETS INPUT CURRENT LIMIT IN ETA6964

The ETA6964 contains a DP/DM based input source detection to set the input current limit at V_{BUS} plug-in. The DP/DM detection includes standard USB BC1.2 and non-standard adapter. When input source is plugged in, the device starts standard USB BC1.2 detections. The USB BC1.2 is capable to identify Standard Downstream Port (SDP), Charging Downstream Port (CDP) and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer expires, the nonstandard adapter detection is applied to set the input current limit. The non-standard detection is used to distinguish vendor specific adapters (Apple and Samsung) based on their unique dividers on the DP/DM pins. Base on DP/DM configuration, the input current limit will be set following the below table:

Table 1: Non-standard Adapter Detection

NON-STANDARD ADAPTER	DP THRESHOLD	DM THRESHOLD	INPUT CURRENT LIMIT (A)
Divider1	V_{DP} within V_{2P7_VTH}	V_{DM} within V_{2P0_VTH}	2.1
Divider2	V_{DP} within V_{1P2_VTH}	V_{DM} within V_{1P2_VTH}	2
Divider3	V_{DP} within V_{2P0_VTH}	V_{DM} within V_{2P7_VTH}	1
Divider4	V_{DP} within V_{2P7_VTH}	V_{DM} within V_{2P7_VTH}	2.4

Table 2: Input Current Limit Setting from D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT (A)
USB SDP	0.5
USB CDP	1.5
USB DCP	2.4
Divider1	2.1
Divider2	2
Divider3	1
Divider4	2.4
Unknown Adapter	0.5

INPUT VOLTATE LIMIT THRESHOLD SETTING (VINDPM)

The device's V_{INDPM} is set at 4.5V. The device supports dynamic V_{INDPM} tracking which tracks the battery voltage. The device's V_{INDPM} tracks battery voltage with 200mV offset such that when V_{BAT} + 200mV is greater than 4.5V, the V_{INDPM} value is automatically adjusted to V_{BAT} + 200mV.

BUCK POWER UP

After the input current is set, the device starts Buck converter and allow HSFET and LSFET switching. ETA6964 provide soft-start time, V_{SYS} short protection to avoid overshoot current. When switching is over the soft-start time, BATFET starts turning on then allows charging progress. The device provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current limit is set to the lower of 200 mA. After the system rises above 2.2 V, the device limits input current to the value of R_{ILIM} setting. As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

In order to improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the voltage ratio of V_{SYS} and V_{BUS}.

BOOST POWER UP

ETA6964 provide boost converter up to 1.2A output current. The boost is enabled when the below conditions are valid:

1. V_{BAT} above the battery voltage exiting boost mode threshold
2. V_{BUS} is less than $V_{BAT}+V_{SLEEP}$ (200mV)
3. OTG pin is high
4. TS pin is within acceptable range ($V_{BHOT}<V_{TS}<V_{BCOLD}$)

During boost mode, V_{BUS} output is 5.15 V by default and 1.5MHz Frequency. The output current can reach up to 1.2 A. The boost output is maintained when BAT is above V_{OTG_BAT} threshold. When OTG is enabled, the device starts up with PFM and later transits to PWM to minimize the overshoot.

AUTONOMOUS BATTERY CHARGER

The device charges 1-cell Li-Ion battery with up to 3A charge current for high capacity tablet battery. The 27mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

With battery charging is enabled (nCE pin is LOW), the device autonomously completes a charging cycle without host involvement A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled (nCE is low)
- No thermistor fault on TS
- No safety timer fault

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and device is not in DPM mode or thermal regulation.

When a full battery voltage is discharged below recharge threshold, the device automatically starts a new charging cycle. After the charge is done, toggle nCE pin can initiate a new charging cycle.

The STAT output indicates the charging status: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking).

BATTERY CHARGER PROFILE

The device charges the battery in five phases: battery short, preconditioning, constant current, constant voltage and

top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. in this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

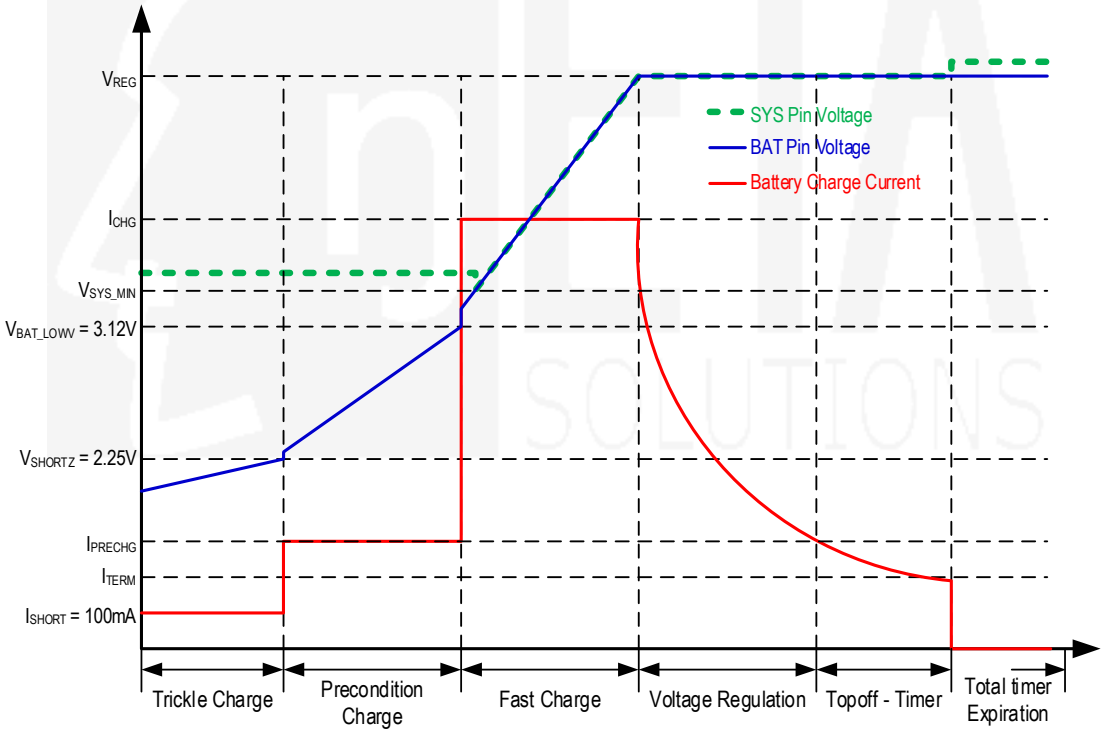


Figure 1: Battery Charger Profile

CHARGE TERMINATION CONFIGURATION

When battery voltage reach regulation level set by VSET pin, the device allow charger enter termination. In this state, when charge current falls below I_{TERM} level, charger will be terminated. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

CHARGE SAFETY TIMER

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below V_{BATLOW} threshold and is 10 hours when the battery below V_{TERM}.

MINIMUM SYS VOLTAGE

Because the rail that provide power to system is SYS voltage, so to make sure the system always has enough voltage even with a fully depleted battery, the system is regulated above the minimum system voltage 3.5V. When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 180 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of BATFET.

When the battery charging is disabled and above minimum system voltage setting 3.5V or charging is terminated, the system is always regulated at typically 70mV above battery voltage.

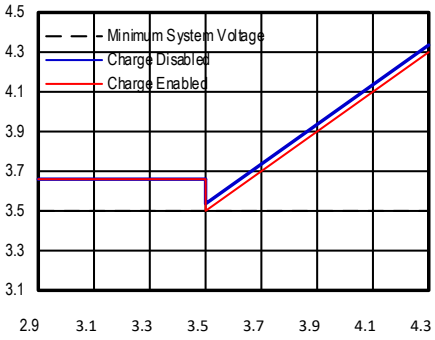


Figure 2: System Voltage vs Battery Voltage

DYNAMIC POWER MANAGEMENT

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (I_{INDPM}) or the voltage falls below the input voltage limit (V_{INDPM}). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

SUPPLEMENT MODE

When the system voltage falls 10 mV ($V_{BAT} > V_{SYS\_MIN}$ when Q4 is full on. In this condition, discharge current is almost 1A) or 20mV ($V_{BAT} < V_{SYS\_MIN}$ when Q4 is in regulation. In this condition, gate of Q4 is regulated at about only threshold voltage of the FET, then discharge current is almost zero) below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET V_{DS} stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce R_{DSON} until the BATFET is in full conduction. At this point onwards, the BATFET V_{DS} linearly increases with discharge current. Following figure shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

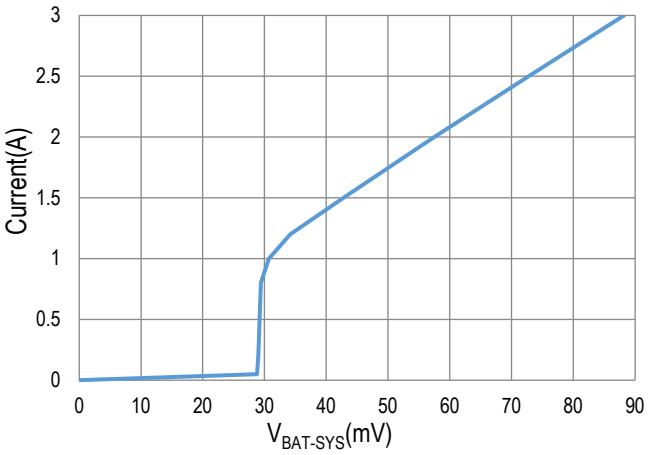


Figure 3: BATFET Current at Entering Supplement Mode

THERMISTOR QUALIFICATION DURING CHARGING MODE

The charger device provides a single thermistor input for battery temperature monitor.

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the V_{T1} to V_{T5} thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

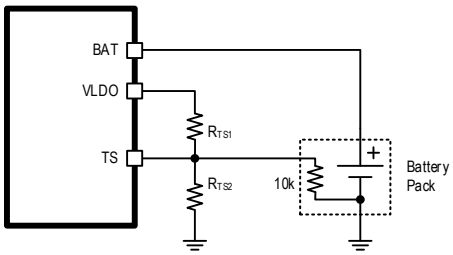


Figure 4: Thermistor Configuration

At cool temperature (T1-T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1V.

The charger provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3-T5) can be VREG . The current setting at cool temperature (T1-T2) can be further reduced to 20% of fast charge current.

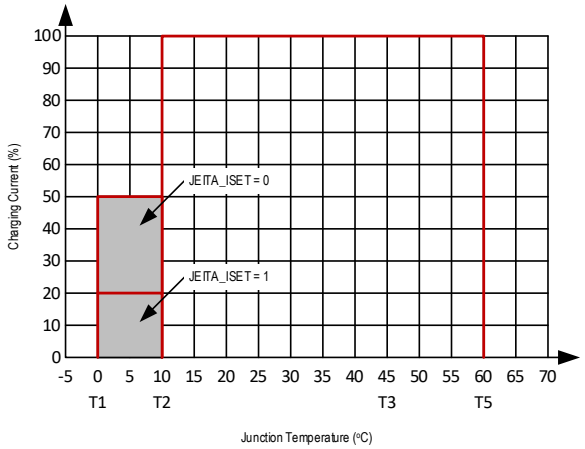


Figure 5: JEITA Profile: Charging Current

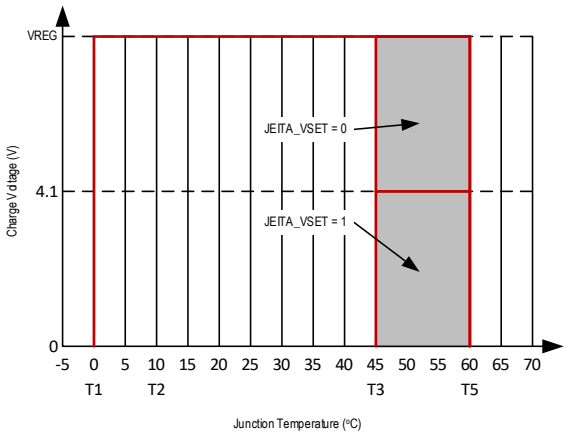


Figure 6: JEITA Profile: Charging Voltage

The resistor bias network has been updated as below.

$$R_{TS1}=\frac{\left(\frac{V_{LDO}}{V_{T1}}-1\right)}{\frac{1}{R_{TS2}}+\frac{1}{R_{THCOLD}}} \qquad RTS2=\frac{V_{LDO}\times R_{THCOLD}\times R_{THHOT}\times\left(\frac{1}{V_{T1}}-\frac{1}{V_{T5}}\right)}{R_{THHOT}\times\left(\frac{V_{LDO}}{V_{T5}}-1\right)-R_{THCOLD}\times\left(\frac{V_{LDO}}{V_{T1}}-1\right)}$$

THERMISTOR QUALIFICATION DURING BATTERY DISCHARGE MODE

For battery protection during boost mode, the device monitors the battery temperature to be within the V_{BCOLD} to V_{BHOT} thresholds. When temperature is outside of the temperature thresholds, the boost mode is suspended.

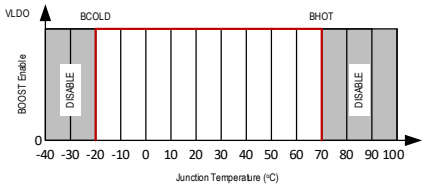


Figure 7: TS Pin Thermistor Sense Threshold in Boost Mode

INDICATION OUTPUT

POWER GOOD INDICATION ON nPG PIN

The nPG pin goes LOW to indicate a good input source when:

- V_{BUS} above V_{BUS_UVLO}
- V_{BUS} above battery (not in sleep)
- V_{BUS} below V_{AC_OV} threshold
- V_{BUS} above V_{BUS_MIN} (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)

CHARGING STATUS INDICATION ON STAT PIN

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED. STAT indication operates as shown as in below table.

Table 2: STAT Indication table

CHARGE STATE	STAT INDICATION
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (input overvoltage, TS fault, timer fault or system overvoltage) Boost Mode suspend (due to TS fault)	Blinking at 1Hz (0.5s LOW / 0.5s HIZ)

INPUT OVERVOLTAGE PROTECTION IN CHARGE MODE (ACOV)

If V_{BUS} exceeds over voltage threshold V_{AC_OV}, the device stops switching immediately. The device will automatically resume normal operation once the input voltage drops back below the OVP threshold.

SYSTEM OVERVOLTAGE PROTOECTION IN CHARGE MODE (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 14% above system regulation voltage. Upon SYSOVP, converter stops

immediately to clamp the overshoot.

V_{BUS} OUTPUT SHORT PROTECTION IN BOOST MODE

The device monitors boost output voltage and other conditions to provide output short circuit and overvoltage protection. The Boost build-in accurate constant current regulation to allow OTG to adaptive to various types of load. If short circuit is detected on BUS, the Boost turns off and retry 7 times. If retries are not successful, OTG is disabled.

V_{BUS} OVERVOLTAGE PROTECTION IN BOOST MODE

When the V_{BUS} rises above regulation target and exceeds the over voltage threshold V_{OTG_OVP}, the device enters overvoltage protection which stops switching.

THERMAL REGULATION IN BUCK MODE

ETA6964 monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC surface temperature at 110°C in buck mode. When the internal junction temperature exceeds thermal regulation limit (110°C), the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate.

THERMAL SHUTDOWN

The device monitors the internal junction temperature to provide thermal shutdown during any mode. When IC surface temperature exceeds T_{SHUT} (160°C) BATFET and Converter are disabled.

When IC temperature is T_{SHUT_HYS} (30°C) below T_{SHUT} (160°C), The BATFET is enabled automatically to restore system.

BATTERY OVER-VOLTAGE PROTECTION

The battery overvoltage limit is clamped at 8% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge.

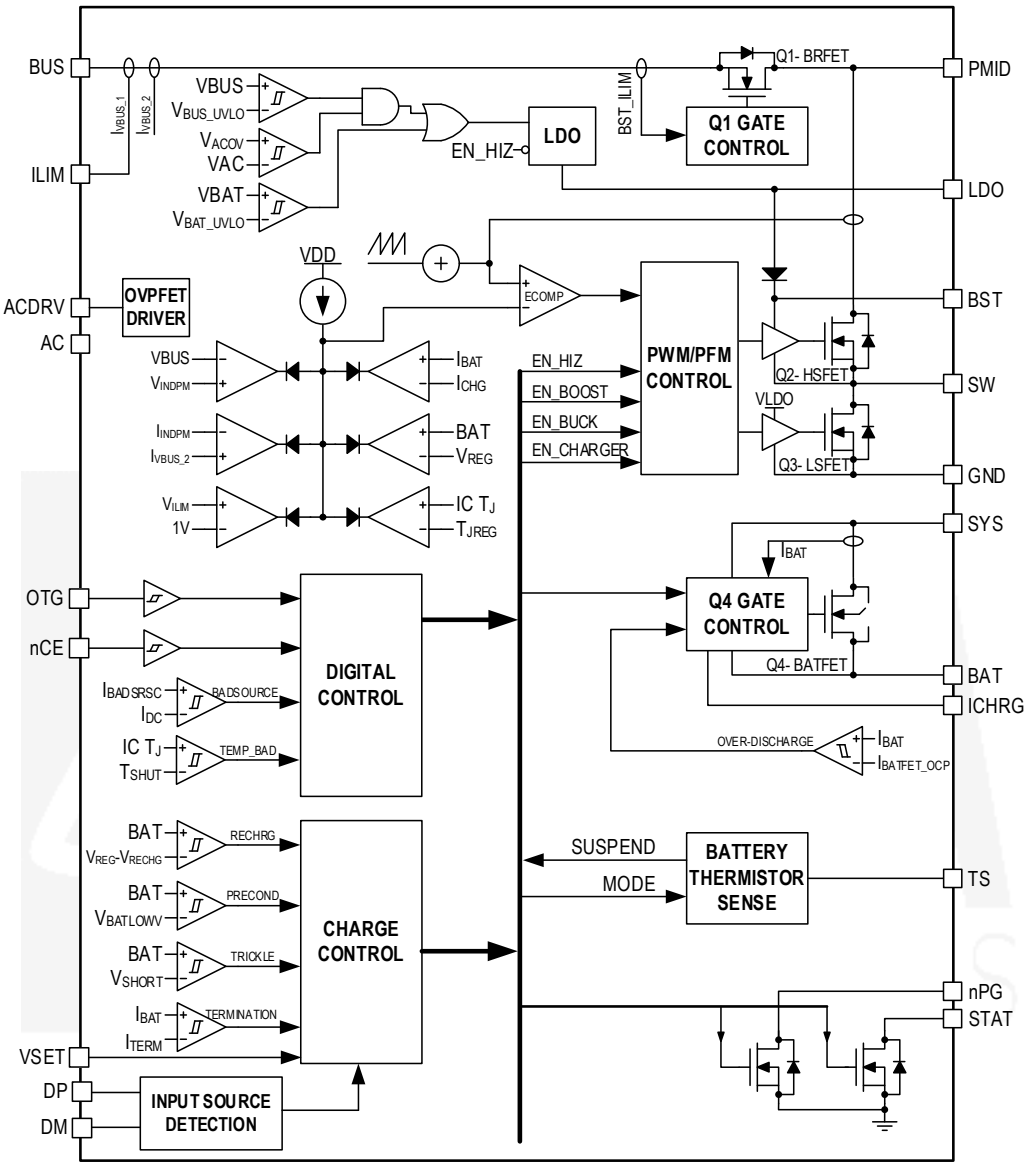
BATTERY OVER-DISCHARGE PROTECTION

When battery is discharged below the battery depletion falling threshold $V_{BAT\_DPL\_FALL}$, the BATFET is turned off to protect battery from over discharge. To recover from over-discharge, an input source is required at BUS pin. When an input source is plugged in, the BATFET turns on. The battery is charged with I_{SHORT} (typically 150 mA) current when the V_{BAT} is smaller than the trickle charge voltage threshold V_{SHORT}, or pre-charge current when the battery voltage is between V_{SHORT} and the pre-charge voltage threshold V_{BAT_LOWV}.

SYSTEM OVER-CURRENT PROTECTION

When the system is shorted or significantly overloaded (I_{BAT} > I_{BATOP}) so that its current exceeds the over-current limit, the device latches off BATFET. To recover from over-discharge latch-off, an input source plug-in is required at BUS.

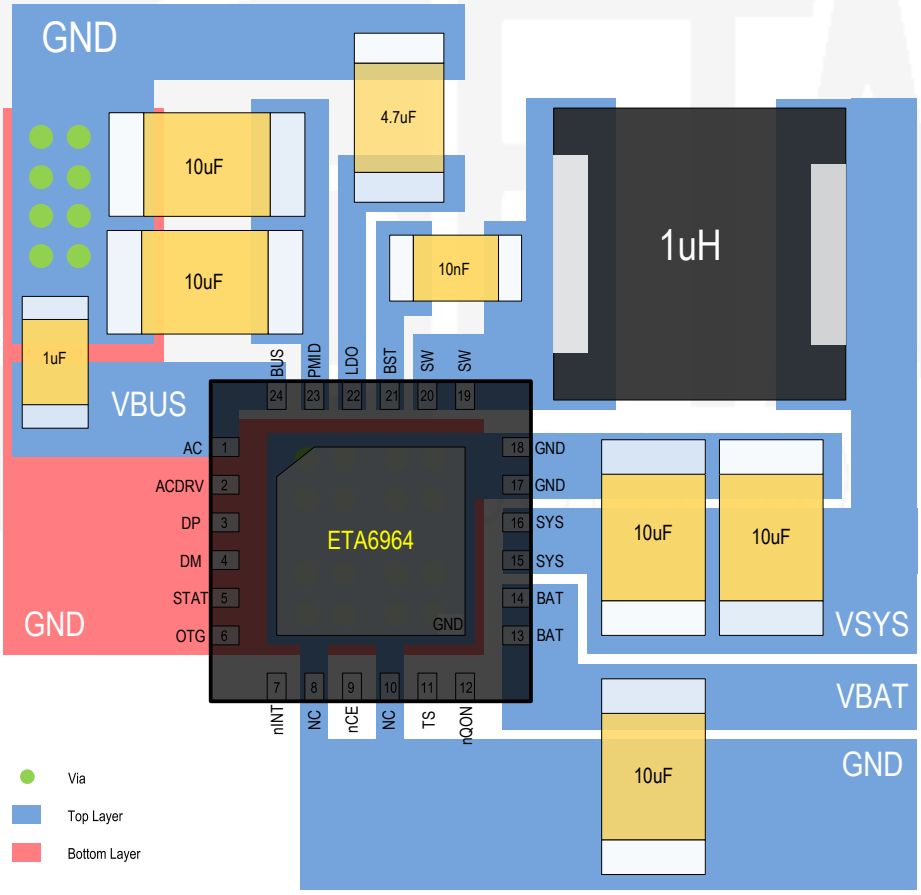
FUNCTION BLOCK DIAGRAM



PCB DESIGN GUIDELINE

In order to have as clean as possible supply for converter, please follow following suggestion:

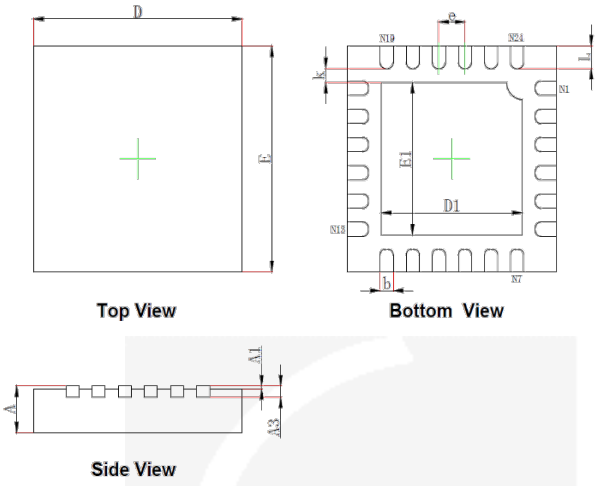
1. Place the BUS, PMID, BAT, SYS, LDO capacitor as close as possible to the pins and wide bottom layer for PGND connections. Also add as much as possible vias for PGND to minimize copper resistance added to PMID capacitor.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Use thermal pad as the single ground connection point.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Ensure that the number and sizes of vias allow enough copper for a given current path.
9. Ensure almost the bottom layer be ground unless bridge connection.



PACKAGE OUTLINE

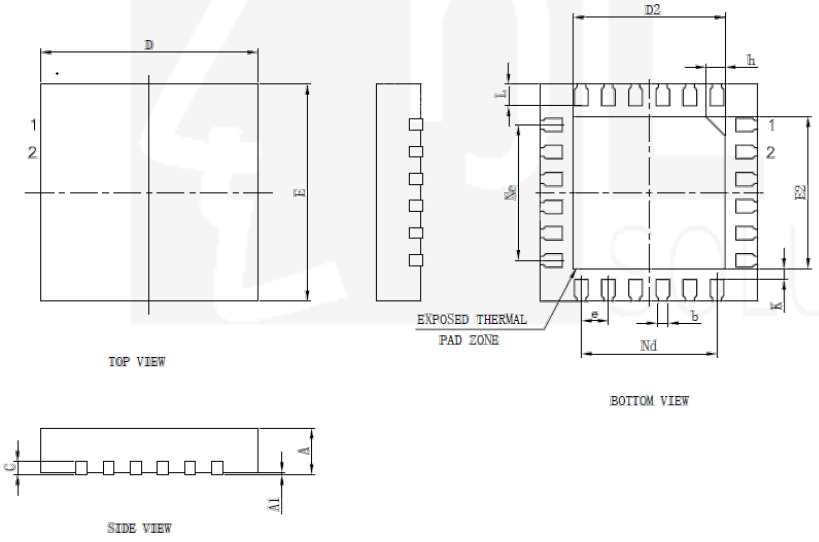
QFN4x4-24

From assembly house 1:



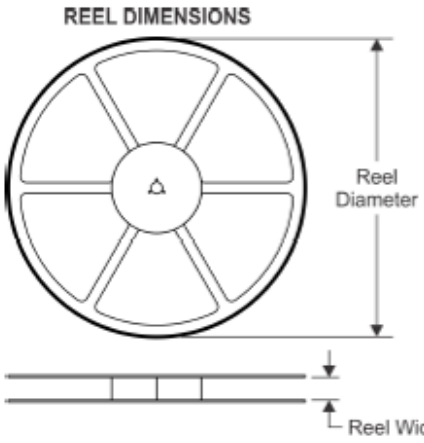
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

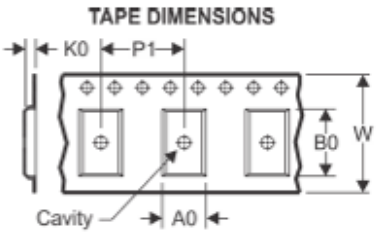
From assembly house 2:



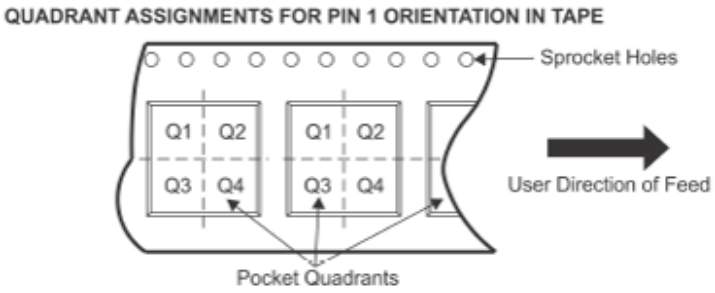
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.85	0.90	0.95
	0.80	0.85	0.90
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.35	0.40	0.45
K	0.15	0.20	0.25
h	0.30	0.35	0.40
L/F载体尺寸	2.9X2.9		

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA6964Q4Y	QFN4*4-24	24	5000	330	12.4	4.3	4.3	1.1	8	12	Q2